



CEPC vertex Detector

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(On behalf of the CEPC physics and detector group)



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Items in meeting with IDRC chair

- Total area and Timeline for ALICE ITS3, should compare with CEPC vertex
 - ALICE ITS3 timeline is about 2~3 years earlier (ITS3 2032 installation)
 - ITS3: 0.06 m^2 , CEPC: 0.15 m^2
- Material budget for normal ladders (especially for carbon fiber)
 - mu3E ladders has $0.1\% X_0$ per layer (we quoted $0.25\% X_0$ per layer)
 - Carbon fiber thickness in CEPC prototyping can reach 0.12mm, same level as mu3E
- Accessibility for 65/55 nm technology in China
 - TowerJazz 65nm CIS can be submitted by TJ agency in China
 - R & D of SMIC 55nm technology is on going
- Serial powering is widely used in ATLAS/CMS upgrade, should look into it
 - Wei Wei's talk will compare DC/DC and Serial powering scheme

Data rate estimation of CEPC VTX

	Data rate@triggerless (old result, 30MW)	Data rate@triggerless (new result, 50MW)
Higgs (240GeV)	0.43 Gbps	>1Gbps

Old

New

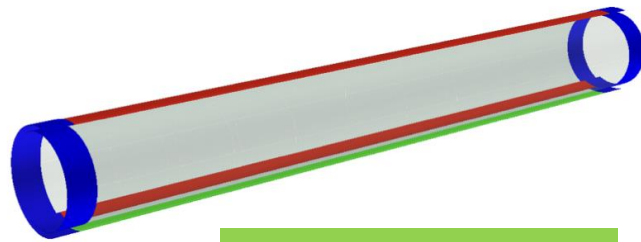
- Bunch structure of ZH runs was not taken into account
 - Bunch structure @ ZH: 50% duty cycle (10ms with collision; 10ms without collision)
 - Old result was average data rate (underestimated)
 - New result will double the data rate
- Old result was using **30MW** , new result is using **50MW**
- In new estimation, Even Higgs run has rate above 1Gbps per chip
- Triggerless scheme may needed to reconsidered

Update in CEPCSW

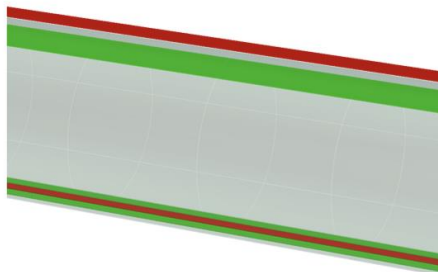
■ Stitching layer layout is implemented in CEPCSW

- Dead area is also considered
- Digitization is OK now, can be used for BG simulation
- Code for reconstruction is still under development

Module -> Layer

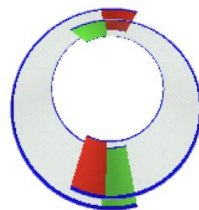


By Chengdong Fu

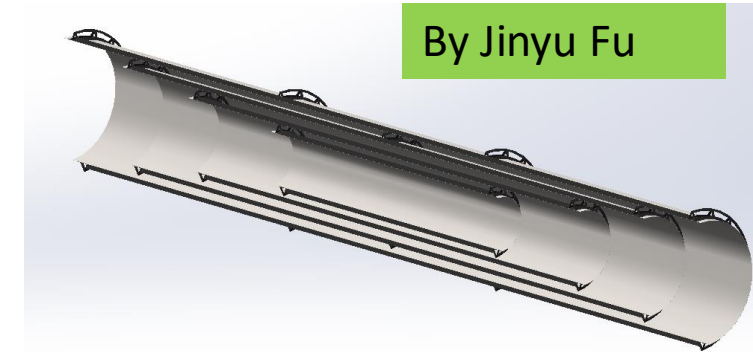


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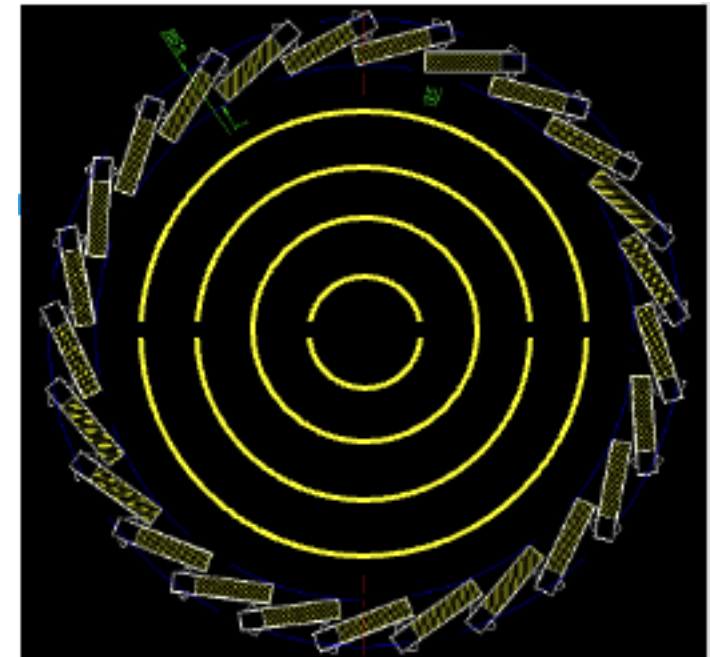
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</module>
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Parameter to confirm



By Jinyu Fu



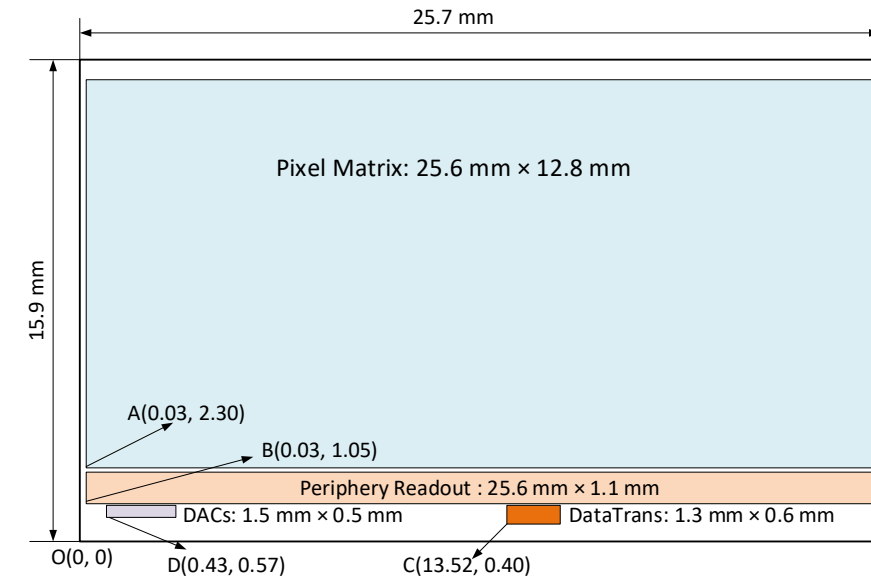
Chip design for ref- TDR and power consumption

■ Power consumption

- **Fast priority digital readout** for 40MHz at Z pole
- 65/55nm CIS technology
- Power consumption can be reduced to $\sim 40\text{mW}/\text{cm}^2$

■ Air cooling feasibility study

- Baseline layout can be cooled down to $\sim 20^\circ\text{C}$
 - Based on 3 m/s air speed, estimated by thermal simulation



	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm ²
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	$\sim 45\text{ mW}/\text{cm}^2$

Update of chip design

■ Got the Design kit for TJ 65nm (p type standard process)

By Ying Zhang

– Can start the pixel layout design

- Pixel size estimation and power consumption estimation

– Two small issue for 65nm design kit from TowerJazz China

- Substrate resistance only up to 0.13kOhm (it was 1k Ohm in TJ 180nm CIS)
- Only support 4 metal layers (ALICE ITS3 was using 7 metal layers)
- Do not support modified process

Feedback from Christine Hu :

- ## ALICE ITS3 proposal on stitching design



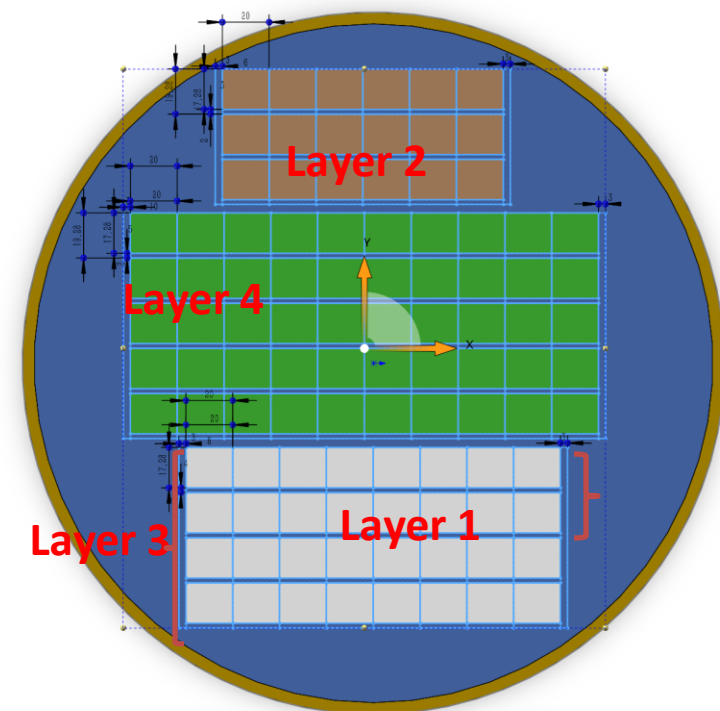
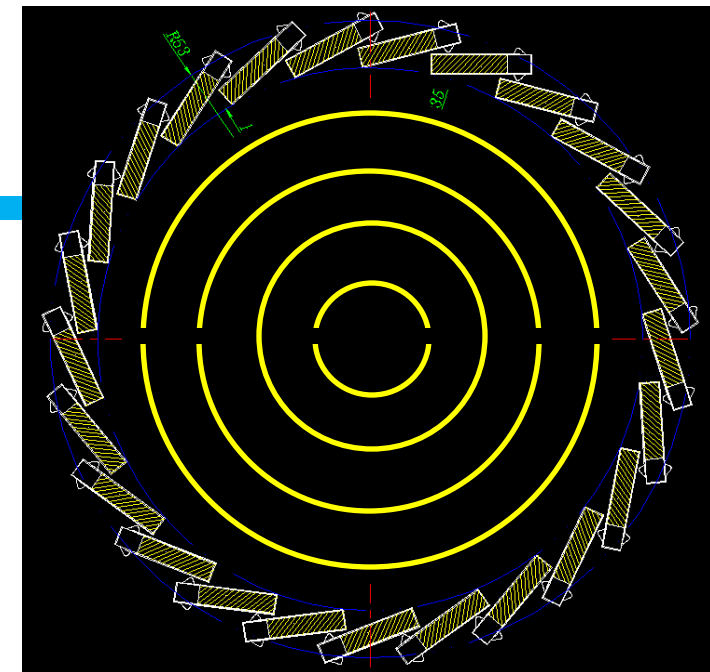
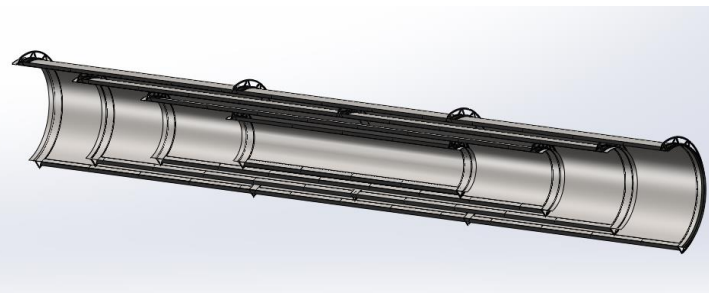
Backup

Vertex baseline: bent MAPS

- 4 single layer of bent MAPS + 1 double layer ladder MAPS
 - Material budget is a factor of 2 lower than alternative option
- Use single bent MAPS for Inner layer
 - Low material budget 0.06%X0 per layer
- Ladder design for outer layer
 - No dead area in ladder design

layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-45mm	0.5% X0
Total		0.74% X0

Long barrel layout (no endcap disk)
to cover $\cos \theta \leq 0.991$



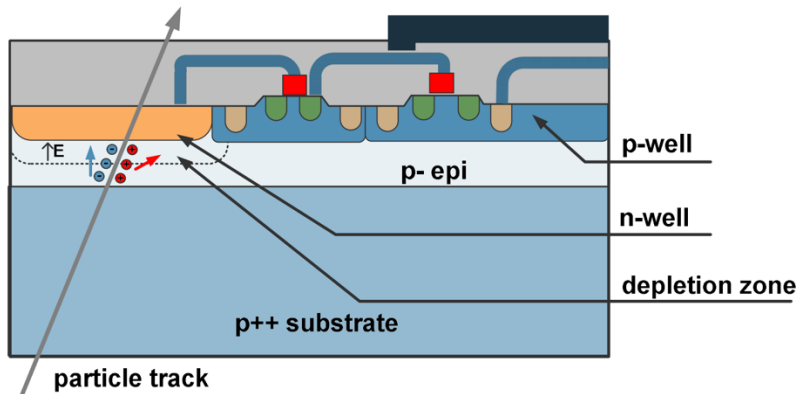
Technology survey and our choices

■ Vertex detector Technology selection

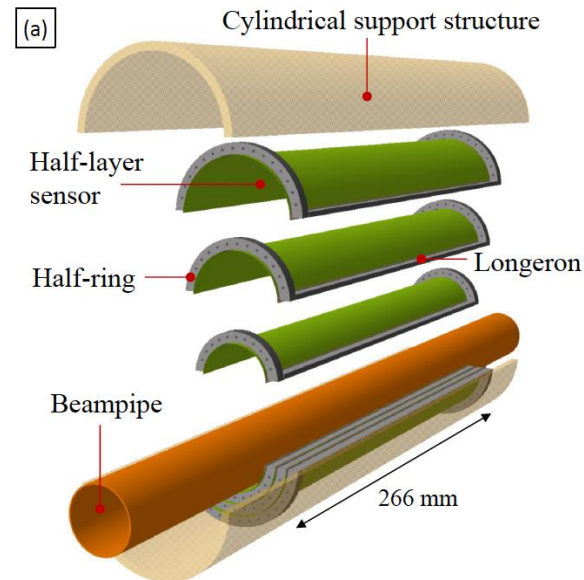
- Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
 - Advantage: 2~3 times smaller material budget compared to alternative (ladder options)
- Alternative: Ladder design based on CMOS MAPS

Monolithic active Pixel CMOS (MAPS)

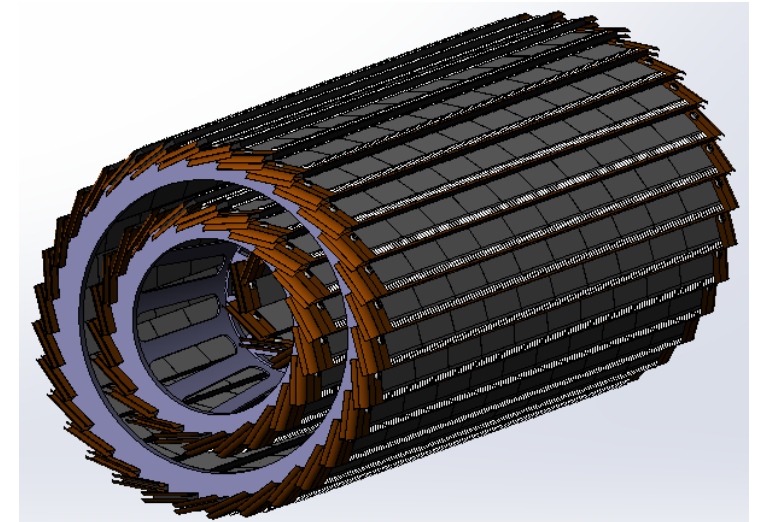
Monolithic Pixels



Baseline: curved MAPS



Alternative: ladder based MAPS



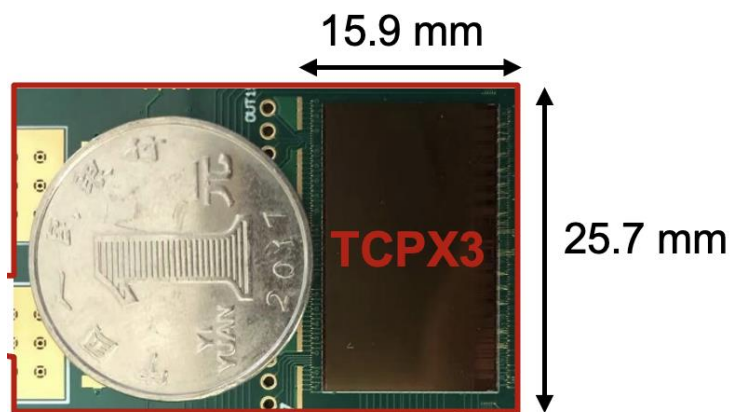
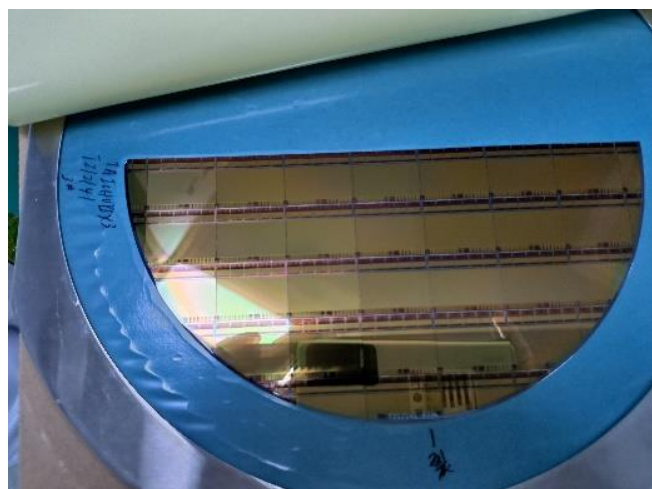
[1] ALICE ITS3 TDR: <https://cds.cern.ch/record/2890181>

R&D status and final goal

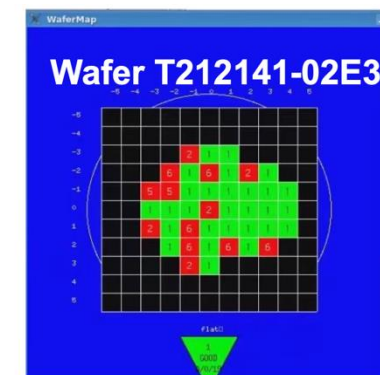
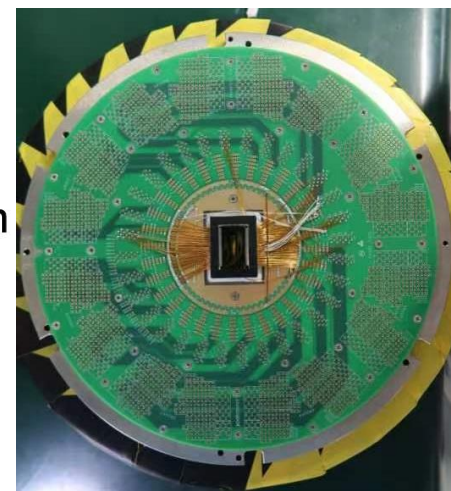
Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11*11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

R&D efforts: Full-size TaichuPix3

- Full size CMOS chip developed, 1st engineering run
 - 1024×512 Pixel array, Chip Size: 15.9×25.7mm
 - 25μm×25μm pixel size with high spatial resolution
 - Process: Towerjazz 180nm CIS process
 - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)



TaichuPix-3 chip vs. coin



An example of wafer test result

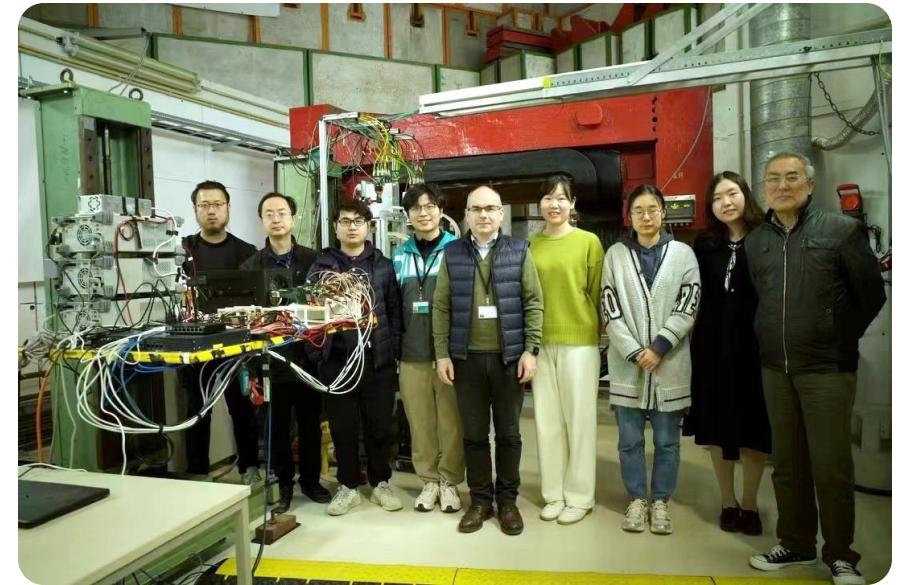
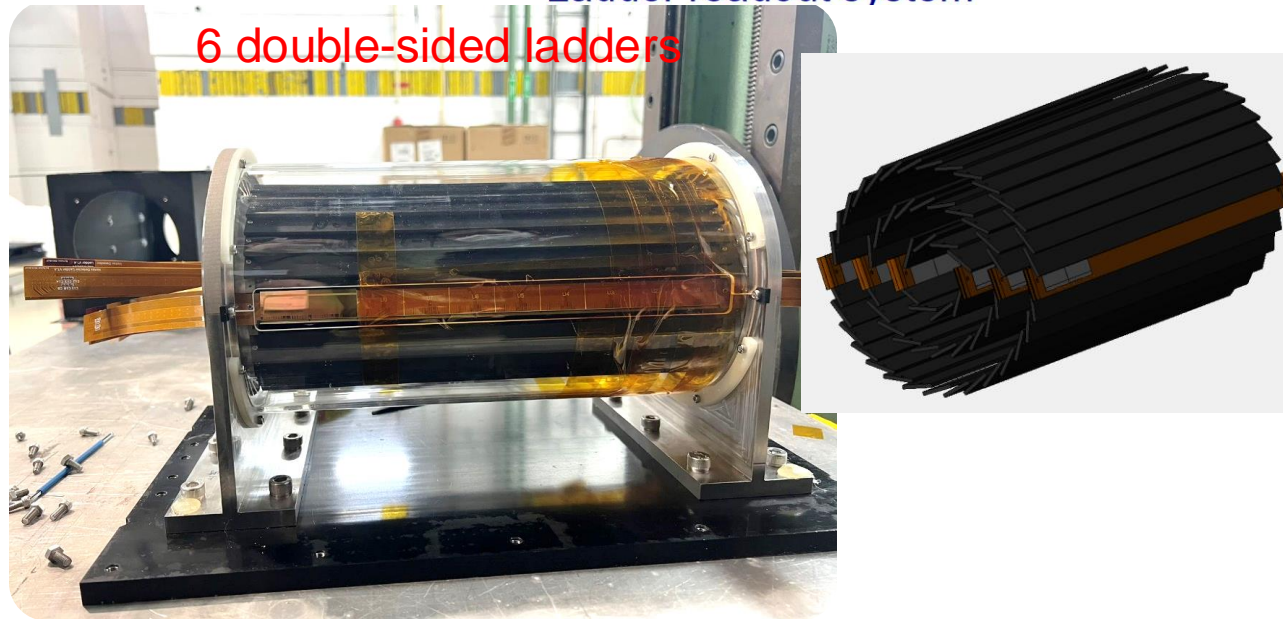
	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

R&D effort: vertex detector prototype



TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution $\sim 4.9 \mu\text{m}$



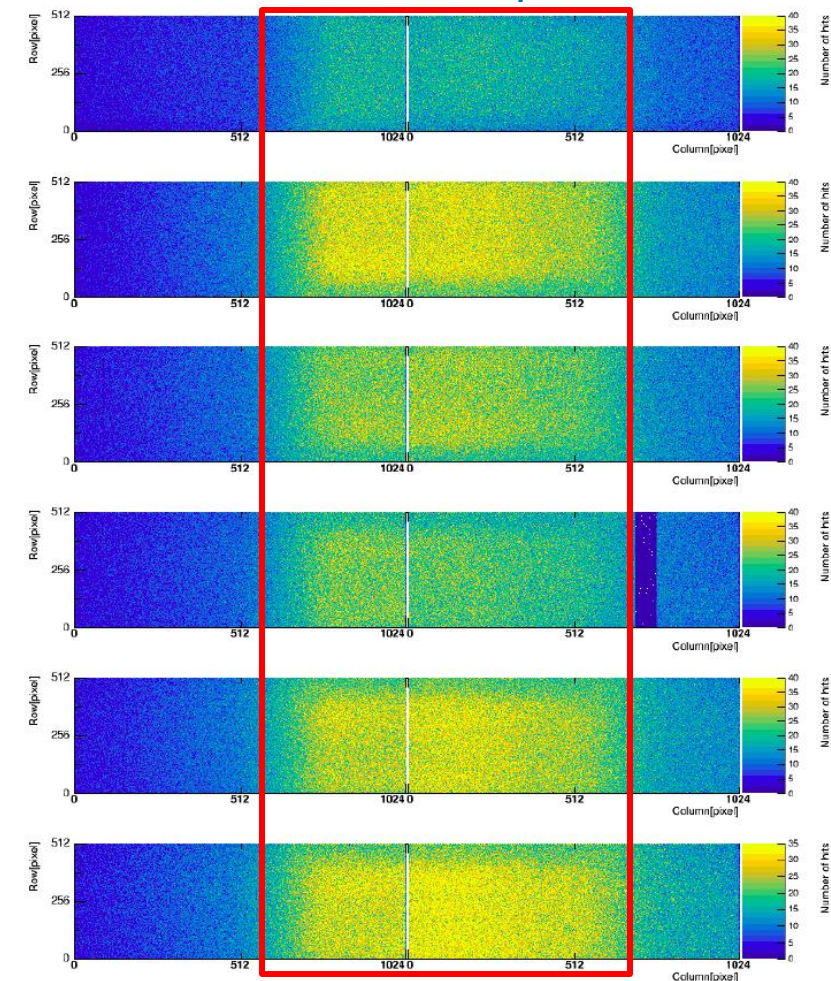
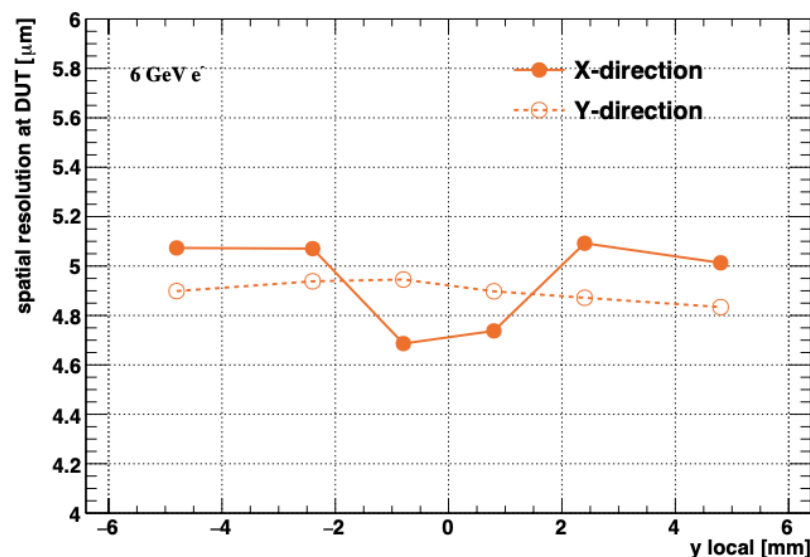
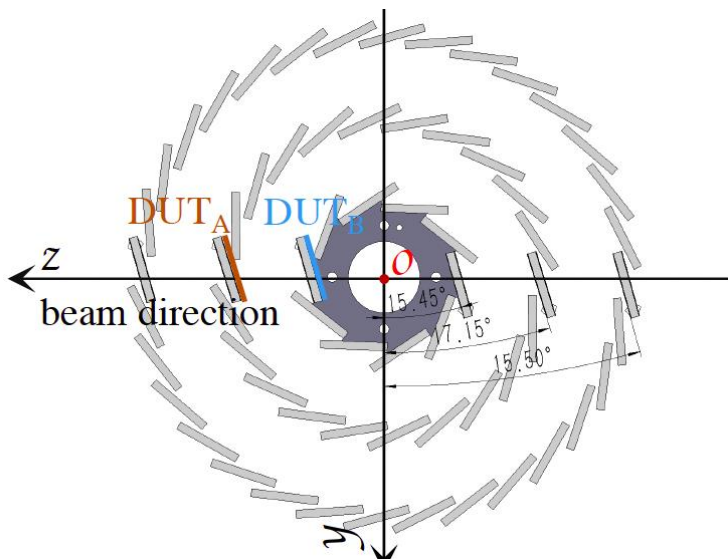
	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts and results: vertex detector prototype beam test

Hit maps of multiple layers of vertex detector

Spatial resolution $\sim 5 \mu\text{m}$

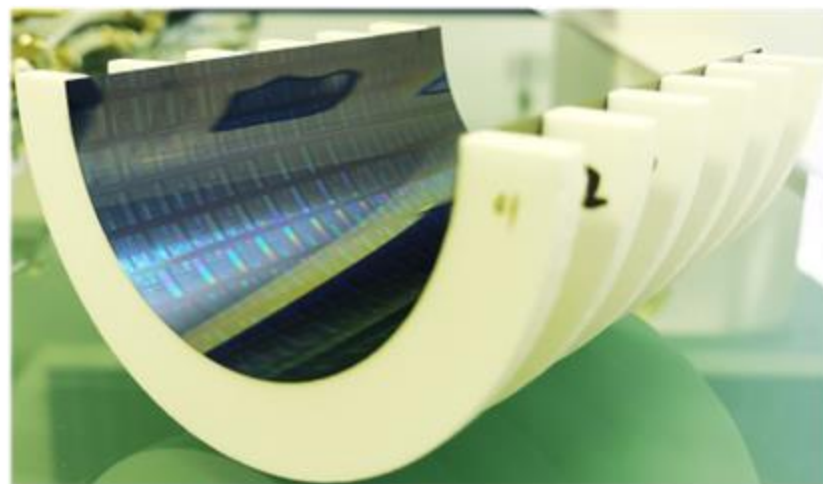
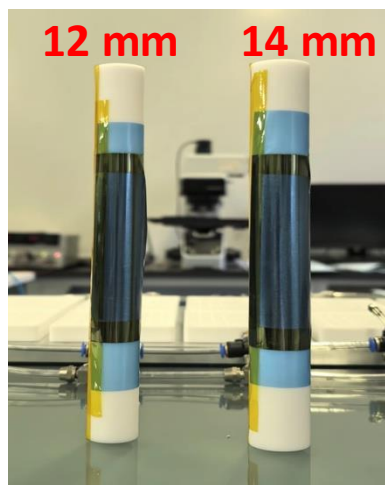
Beam spot



	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility study: Mechanical prototype with dummy wafer can curved to radius ~12mm
 - Thinning silicon wafer to 40um



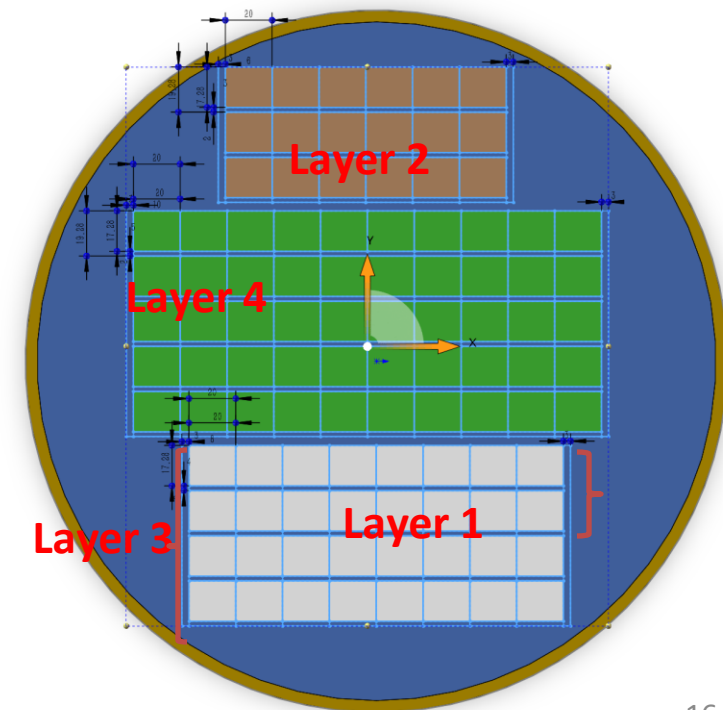
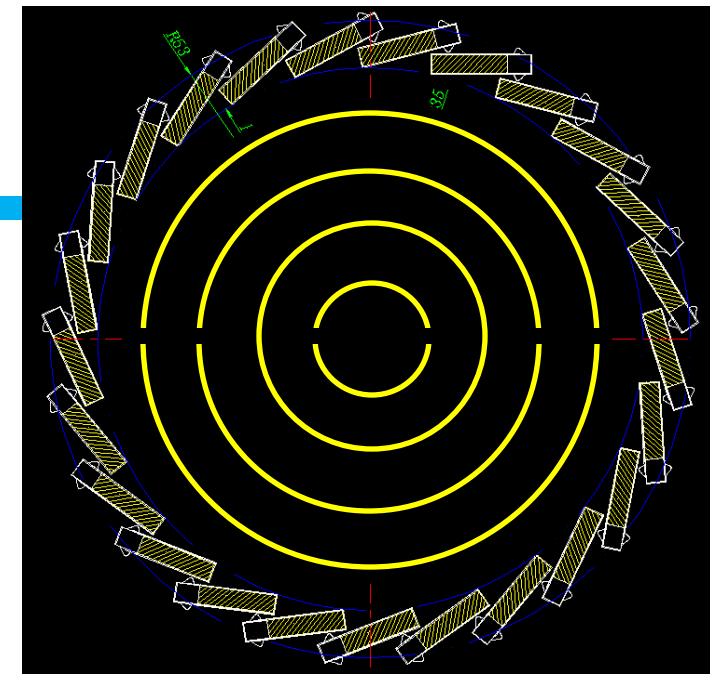
	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

Vertex baseline: bent MAPS

- 4 single layer of bent MAPS + 1 double layer ladder MAPS
 - Material budget is a factor of 2 lower than alternative option
- Use single bent MAPS for Inner layer
 - Low material budget 0.06%X0 per layer
- Ladder design for outer layer
 - No dead area in ladder design

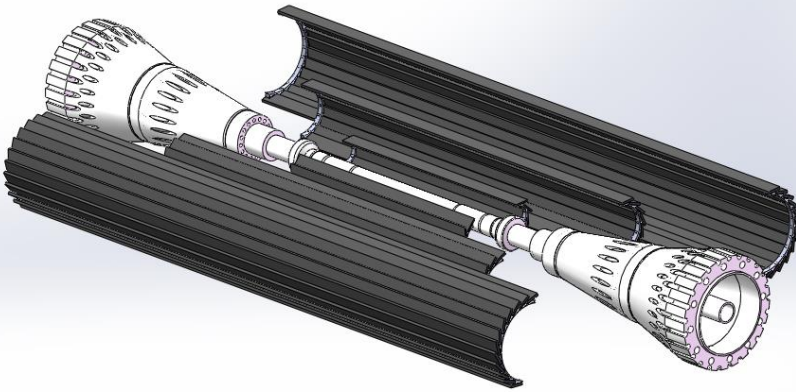
layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-45mm	0.5% X0
Total		0.74% X0

Long barrel layout (no endcap disk)
to cover $\cos \theta \leq 0.991$

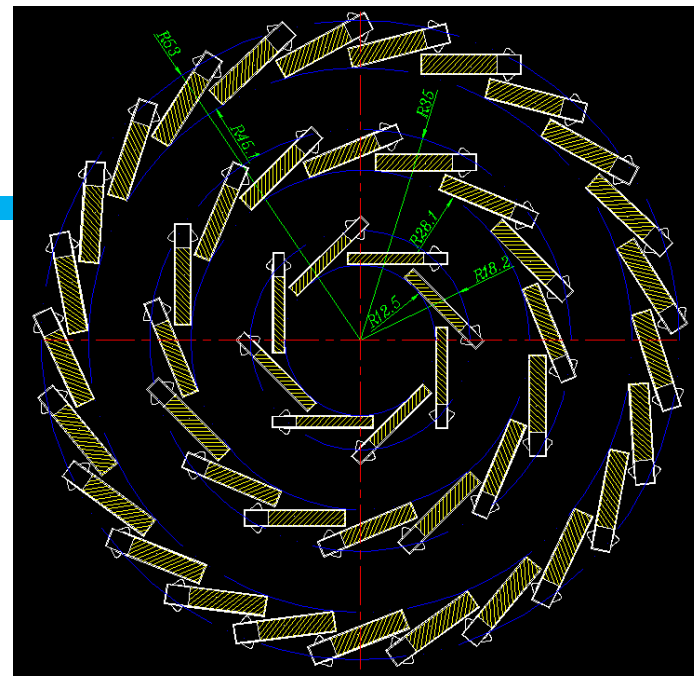


Alternative : CMOS ladder

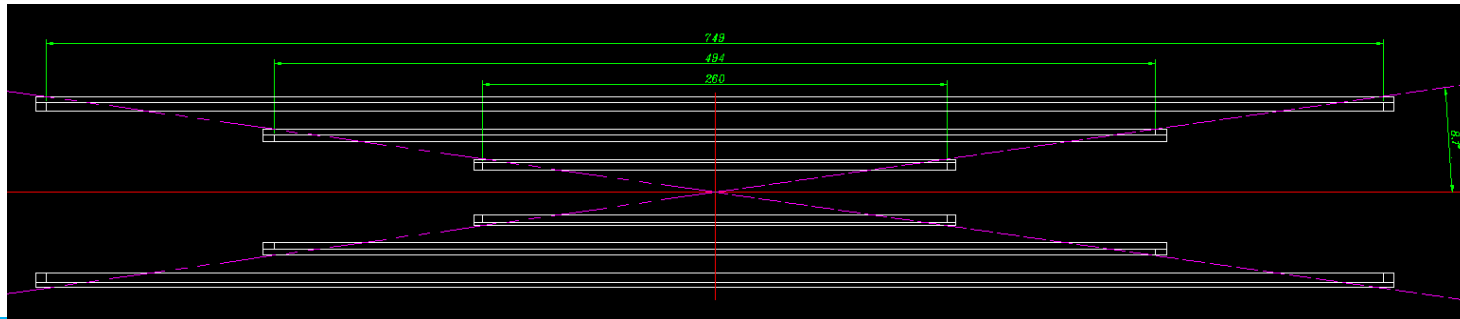
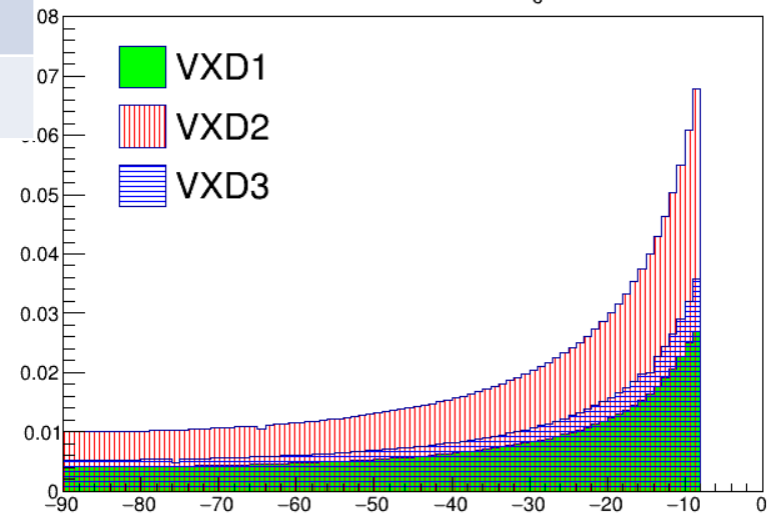
- Alternative: CMOS chip with long ladder layout
 - 3 double-side layer with ladders design
 - 2 times of material compared to baseline layout



layer	Radius	Material
Layer 1/2	12.5 -18 mm	~0.5% X0
Layer 3/4	28 - 35mm	~0.5% X0
Layer 5/6 (Ladders)	45 - 53mm	~0.5% X0
Total		~1.5% X0



Material budget at
 $\Phi = 33$ degree
Material Budget (X_0)

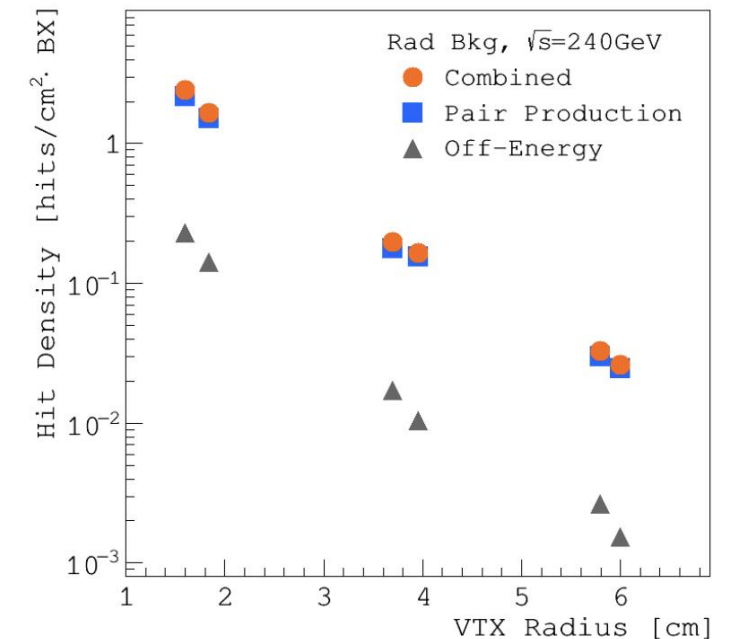


Data rate estimation of CEPC VTX

	Hit density (Hits/cm ² /BX)	Bunch spacing (ns)	Hit rate (M Hits/cm ²)	Data rate@triggerless (Gbps)	Pixel/bunch	Data rate@trigger (Mbps)
Higgs	0.81	591	1.37	0.43	7.96	<10
W	0.81	257	3.16	0.98	7.96	~10
High lumi Z pole	0.45	23	19.6	5.9	4.4	118

Hit density from background (from CDR)

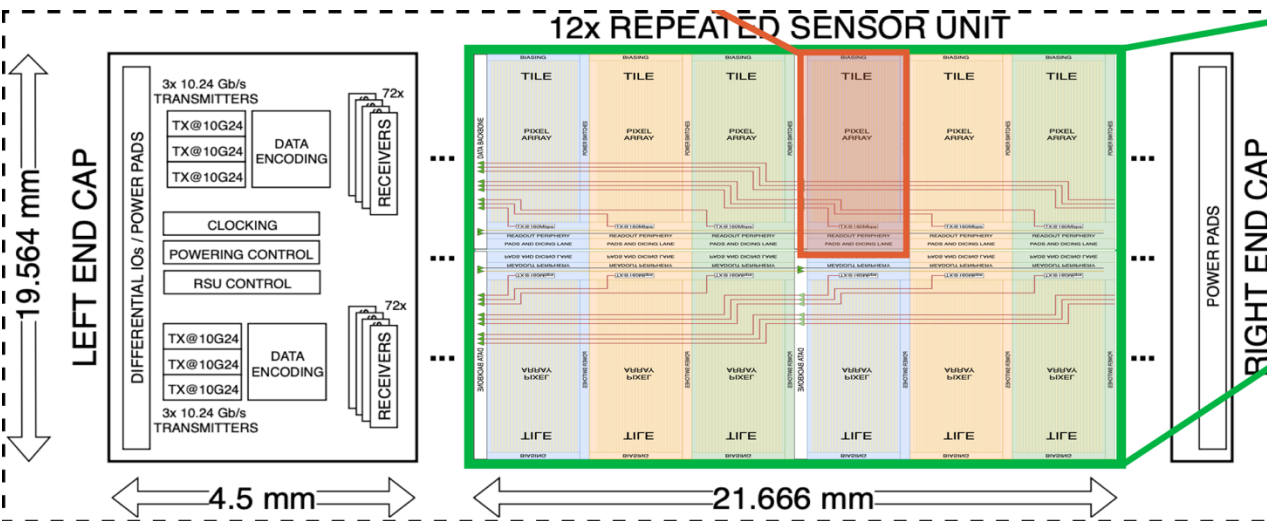
- Data rate is dominated by background from pair production
 - Estimated based on old version of software
 - More details in Haoyu's MDI talk this afternoon
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1Gbps per chip for triggerless readout



Ladder Electronics

- Baseline: stitching and RDL metal layer on wafer to replace PCB
- Alternative: flexible PCB
 - Signal, clock, control, power, ground will be handled by control board through flexible PCB

baseline: ALICE ITS3 like stitching and RDL layer on bent MAPS [1]



Alternative: flexible PCB

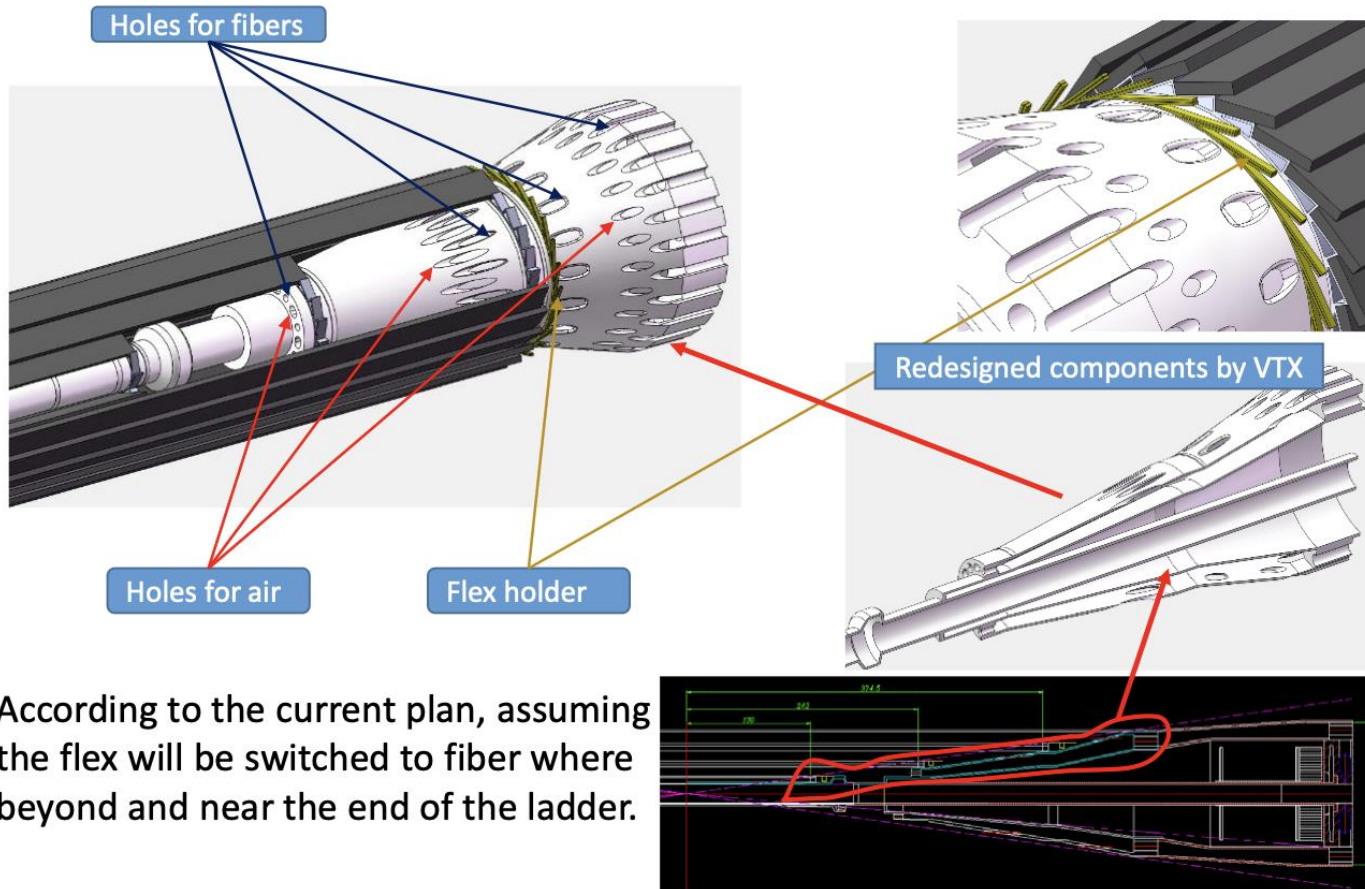


叠层		Stack Up	
Layer 1	12.5 um	Coverlay (yellow)	
	20 um	Coverlay Adhesive	
	24 um	ED Base Copper	12 um + Plated 18 um
	13 um	Polyimide (Adhesiveless)	
Layer 2	12.5 um	Adhesive	
	12 um	ED Base Copper	12 um
	25 um	Polyimide (Adhesiveless)	
Layer 3	12 um	ED Base Copper	12 um
	12.5 um	Adhesive	
	13 um	Polyimide (Adhesiveless)	
Layer 4	24 um	ED Base Copper	12 um + Plated 18 um
	20 um	Coverlay Adhesive	
	12.5 um	Coverlay (yellow)	
FPC厚度: 213 um		Spec: 210 um +/- 50 um	
Created By: HLJ		Date:	

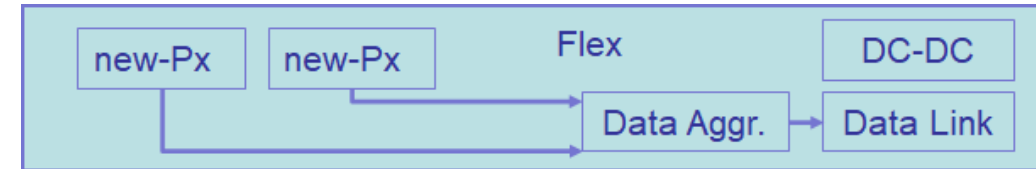
[1] ALICE ITS3 TDR: <https://cds.cern.ch/record/2890181>

Vertex technologies: Cable and service

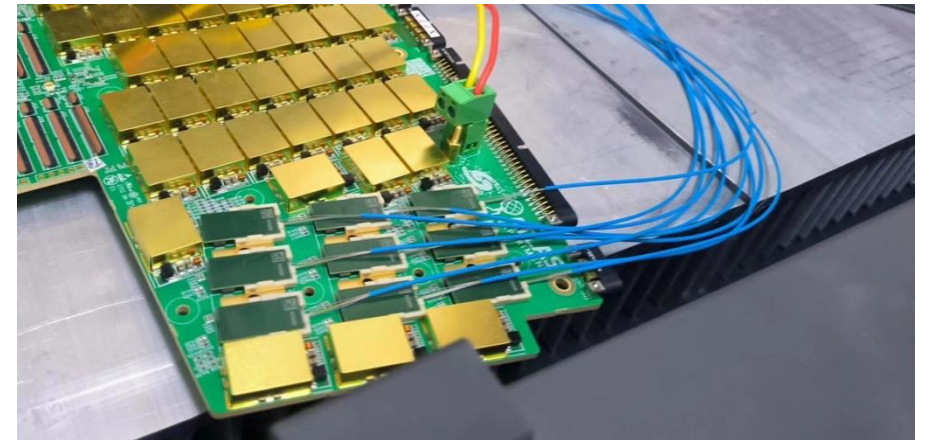
- Limited space in MDI region for cable and service
 - All fast signal transferred into optical fiber in service region



According to the current plan, assuming the flex will be switched to fiber where beyond and near the end of the ladder.



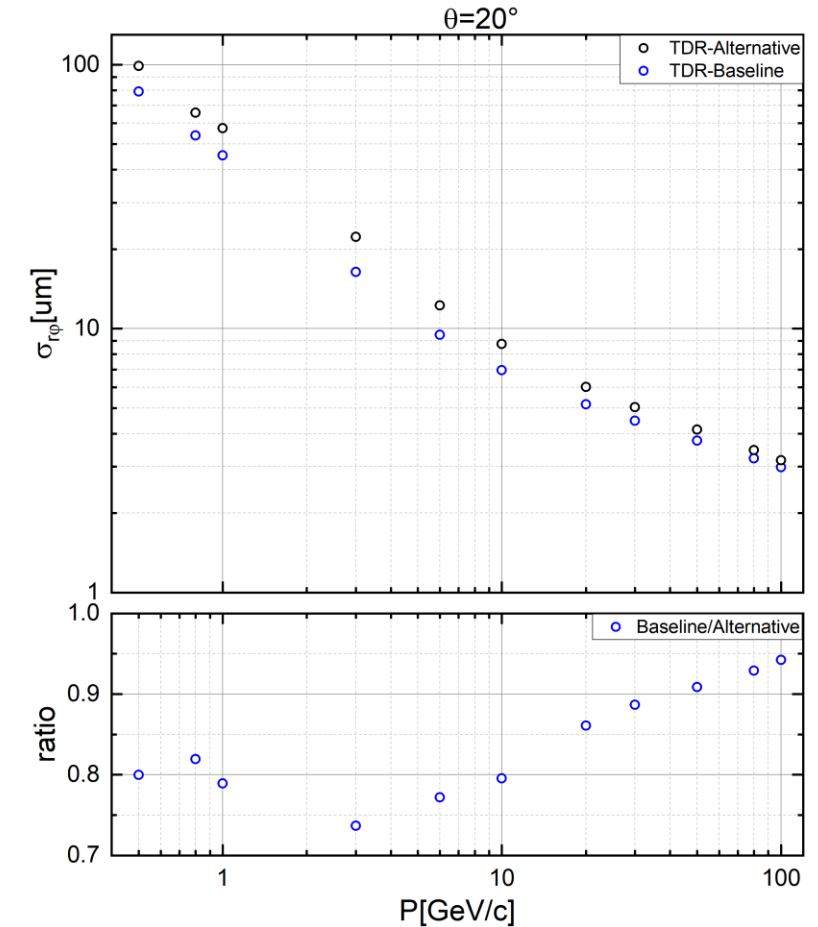
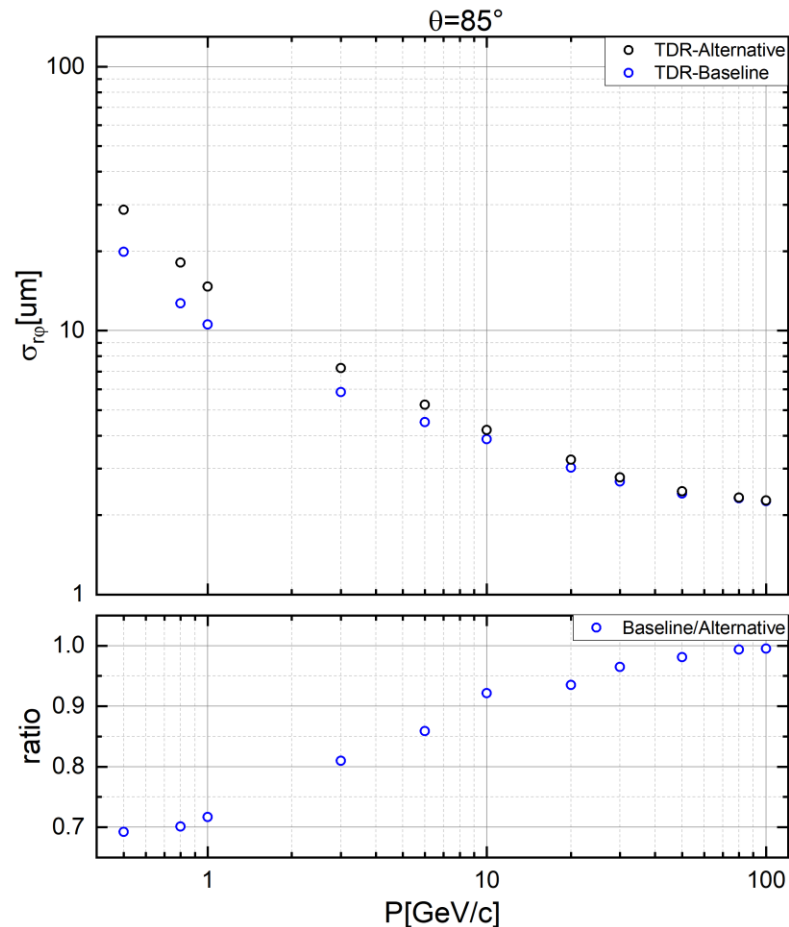
Example from ATLAS HGTD upgrade



Physics Performance: impact parameter resolution

■ Compared to alternative (ladder) option

– baseline layout (Stitching (baseline)) has significant improvement ($\sim 30\%$)



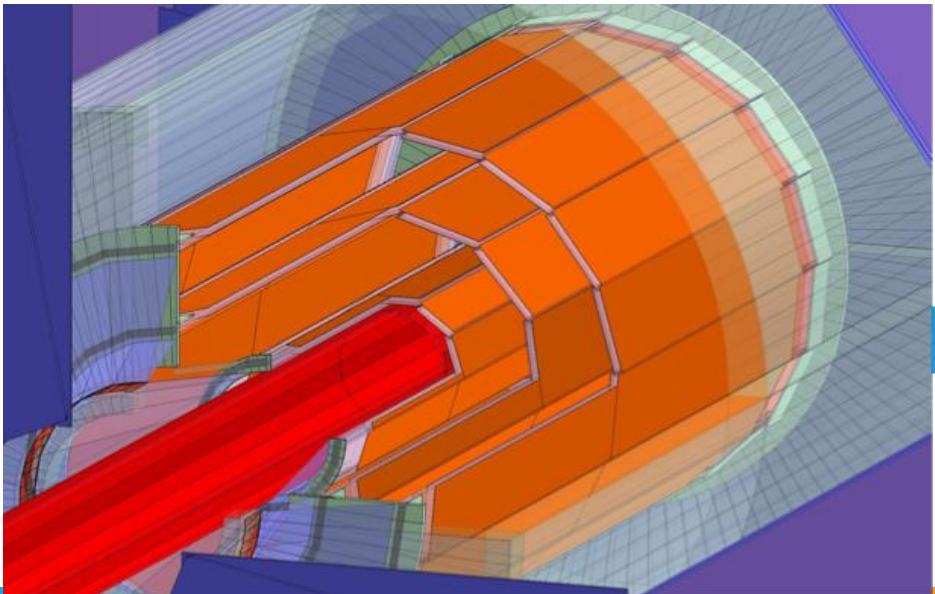
Research team

- IHEP:15 faculty, 5 postdoc, 6 students
 - CEPC vertex prototype, X-ray camera, ATLAS ITK and HGTD upgrade
- IPHC/CNRS: Christine Hu et al (5 faculty)
 - CEPC Jadepix design, ALICE ITS3 pixel upgrade
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty, 1 student)
 - CEPC Taichupix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: chip design, ladder assembly (3 faculty, 1 postdoc, 5 students)
- North West U. : Chip design (5 faculty, 2 postdoc, 5 students)
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing: irradiation study, chip design : (2 faculty, 4 students)
- Total : 36 faculty, 9 postdoc, 26 students

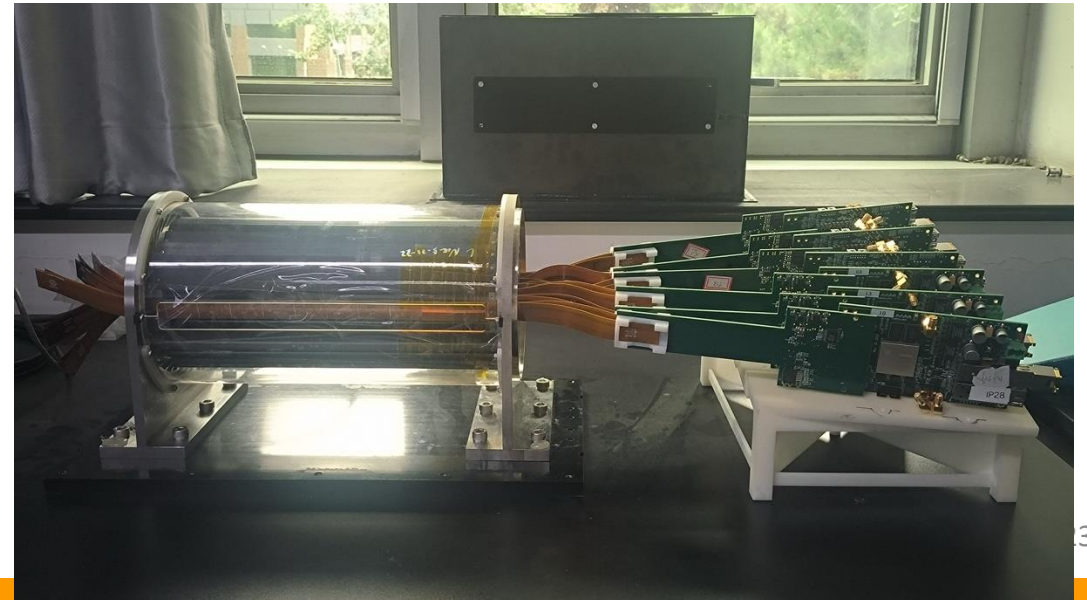
Summary

- 1st full-size Prototype for CEPC vertex detector developed
- Reference detector TDR is in preparation, for 2025 for the proposal of China's 15th 5-year plan.
- We are active expanding international collaboration and explore synergies with other international projects (especially framework of DRD7 (electronics) and DRD8 (mechanics and integration) more than DRD3 (solid state detectors)).

CEPC vertex conceptual design (2016)



CEPC vertex prototype (2023)



Summary: working plan

	Status	CEPC Final goal	Expected date
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS	2027: Full-size 65nm chip
Spatial resolution	4.9 μm	3-5 μm with final chip	2028
Stitching	11*11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor	2029
Bent silicon with small radius	Bent Dummy wafer radius $\sim 12\text{mm}$	Bent final wafer with radius $\sim 11\text{mm}$	2030
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power	2027: thermal mockup
Detector integration	Detector prototype with ladder design	Detector with bent silicon design	2032



Thank you for your attention!

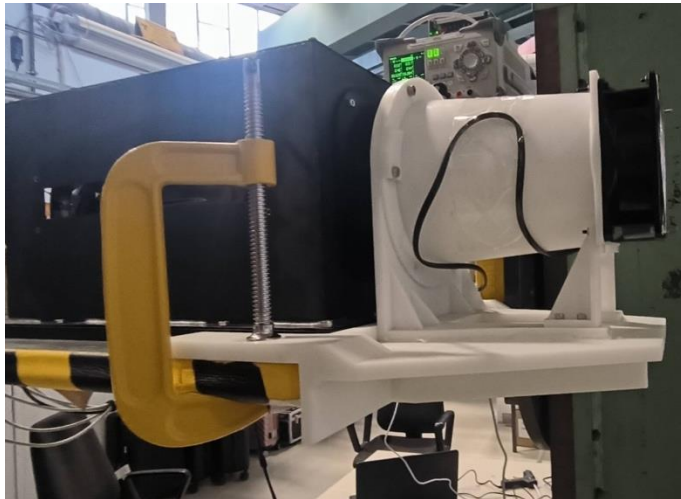


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Institute of High Energy Physics
Chinese Academy of Sciences

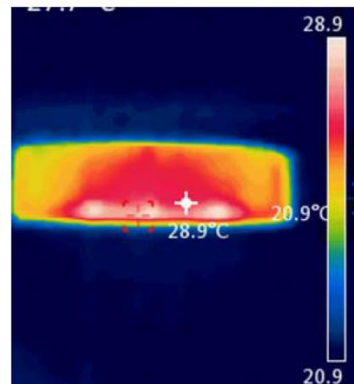
R&D efforts: Air cooling in vertex prototype

Dedicated air cooling channel designed in prototype.

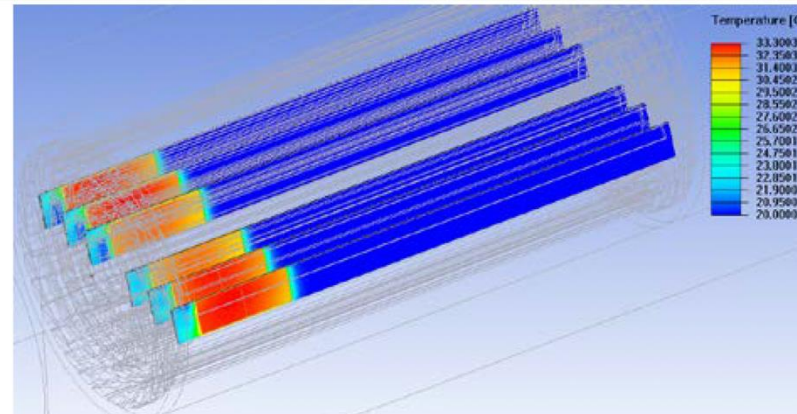
- Measured Power Dissipation of Taichu chip: $\sim 60 \text{ mW/cm}^2$ (17.5 MHz in testbeam)
- Before (after) turning on the cooling, chip temperature 41°C (25°C)
 - In good agreement to our cooling simulation
 - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9°C



Prototype cooling simulation: Max 33.3°C

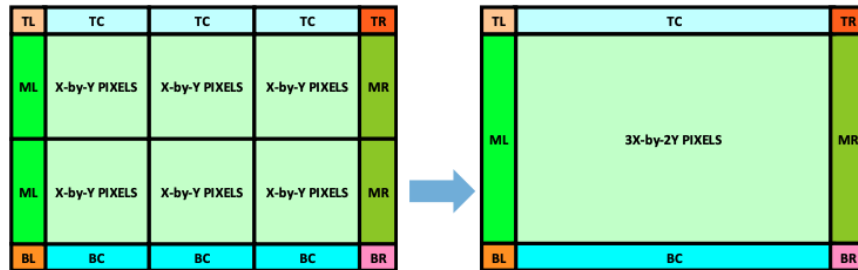


Key technology	Status	CEPC Final goal
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power

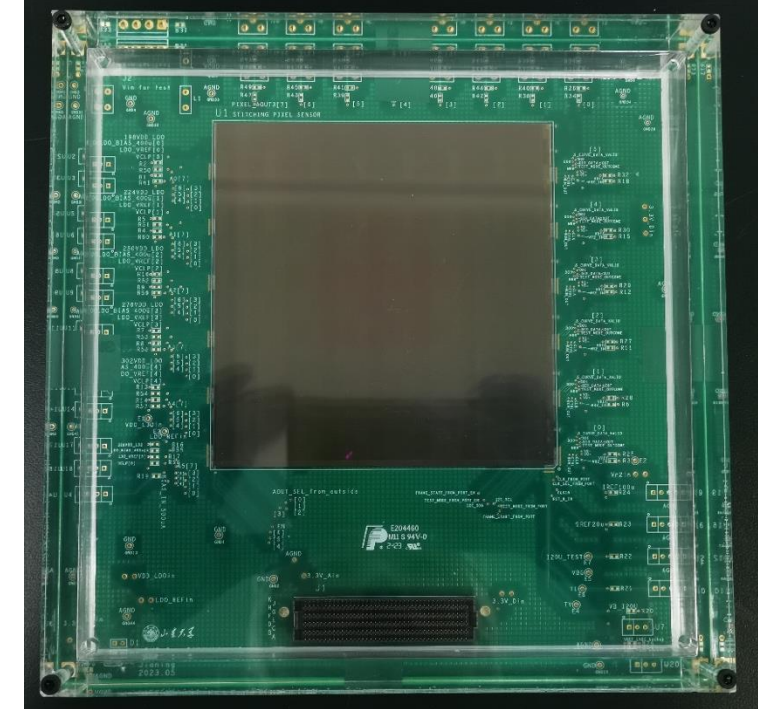
R&D efforts and results: R & D for curved MAPS

■ Stitching chip design (by ShanDong U.)

- 350nm CIS technology Xfabs
- Wafer level size after stitching $\sim 11 \times 11 \text{ cm}^2$
- reticle size $\sim 2 \times 2 \text{ cm}^2$
- 2D stitching
- Engineering run, chip under testing



Stitching chip : $11 \times 11 \text{ cm}^2$



Key technology

Stitching

Status

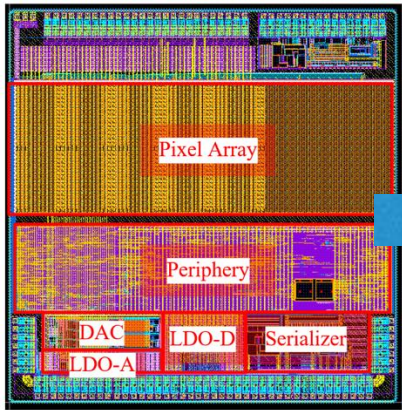
11*11cm stitched chip with Xfab 350nm CIS

CEPC Final goal

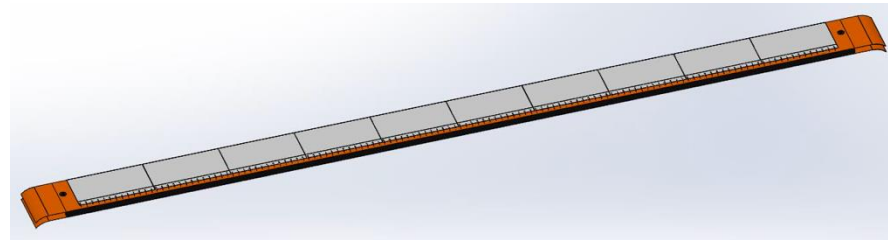
65nm CIS stitched sensor

Overview of CEPC vertex detector prototype R & D

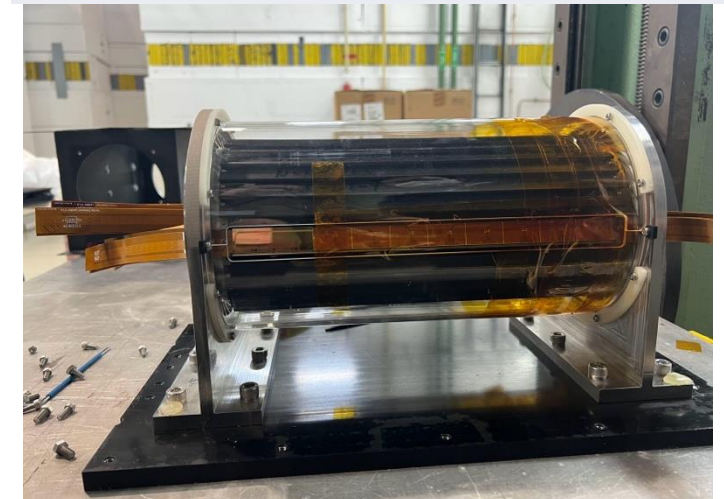
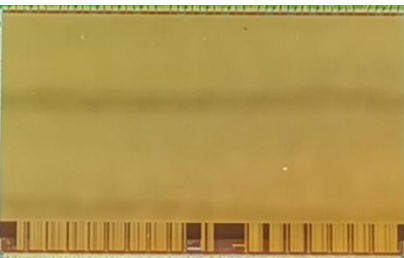
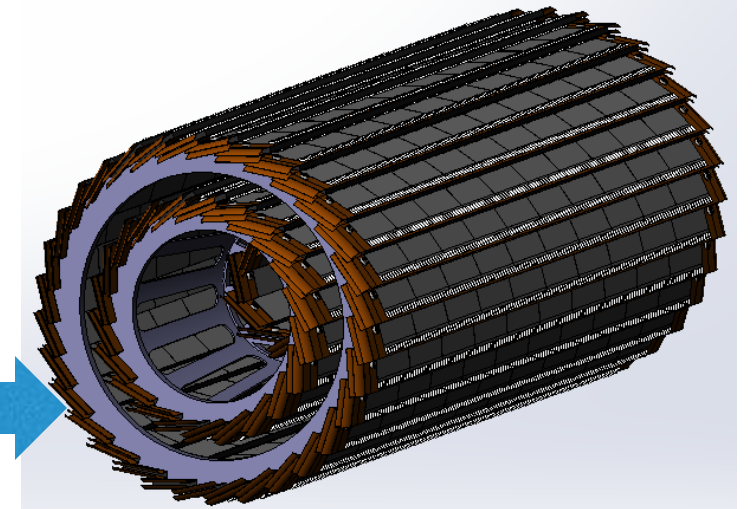
CMOS Sensor chip development



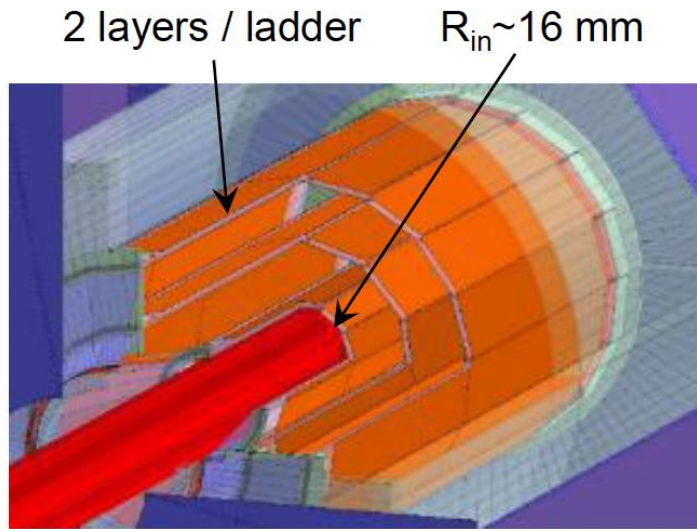
Detector module (Ladder) Prototyping



Vertex detector prototype



Silicon Pixel Chips for Vertex Detector



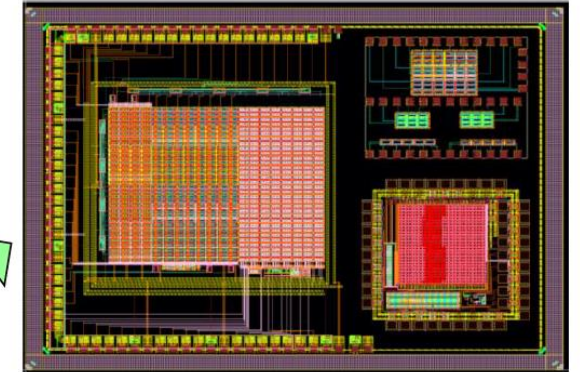
Goal: $\sigma(\text{IP}) \sim 5 \mu\text{m}$ for high P track

CDR design specifications

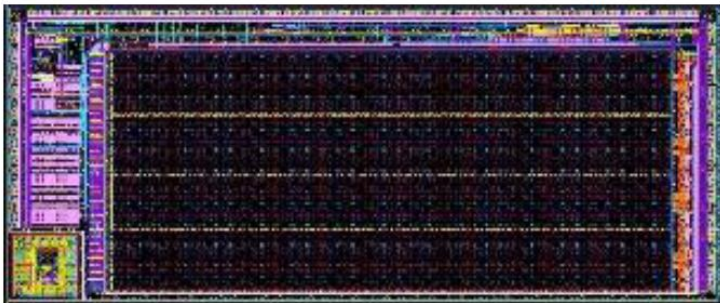
- Single point resolution $\sim 3 \mu\text{m}$
- Low material ($0.15\% X_0$ / layer)
- Low power ($< 50 \text{ mW/cm}^2$)
- Radiation hard (1 Mrad/year)

Silicon pixel sensor develops in 5 series:
JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process



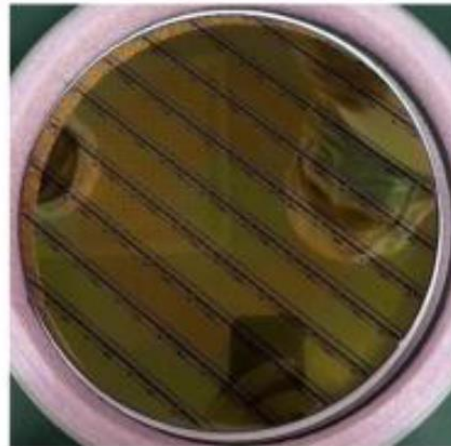
JadePix-3 Pixel size $\sim 16 \times 23 \mu\text{m}^2$



Tower-Jazz 180nm CiS process
Resolution 5 microns, 53 mW/cm^2

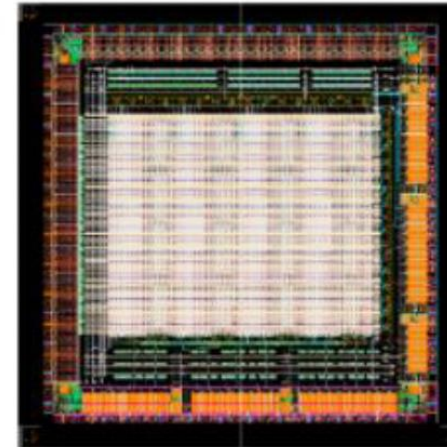
MOST 1

TaichuPix-3, FS $2.5 \times 1.5 \text{ cm}^2$
 $25 \times 25 \mu\text{m}^2$ pixel size

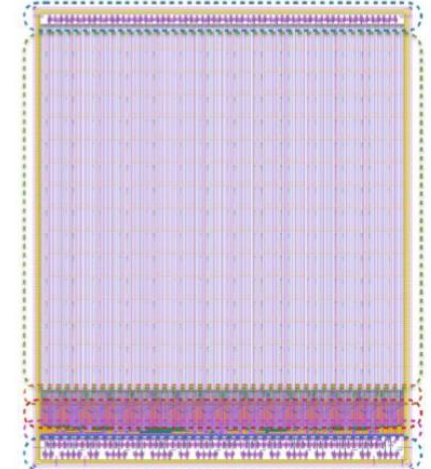


MOST 2

CPV4 (SOI-3D), 64×64 array
 $\sim 21 \times 17 \mu\text{m}^2$ pixel size

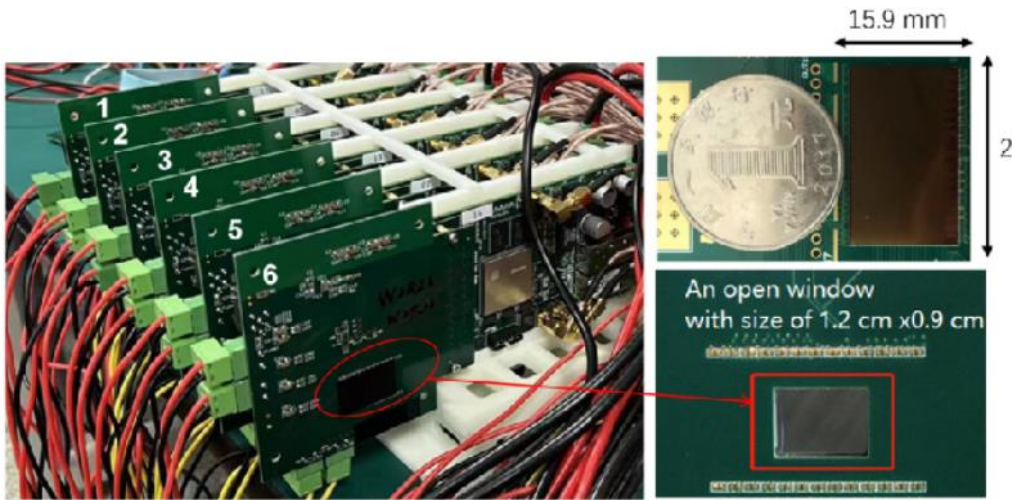


Arcadia by Italian groups
for IDEA vertex detector
LFoundry 110 nm CMOS

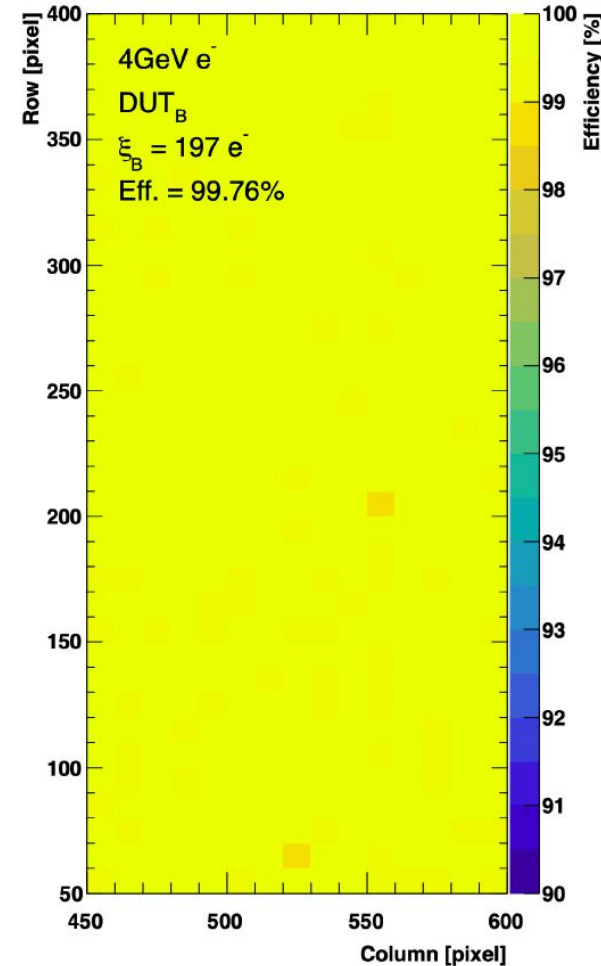


R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY

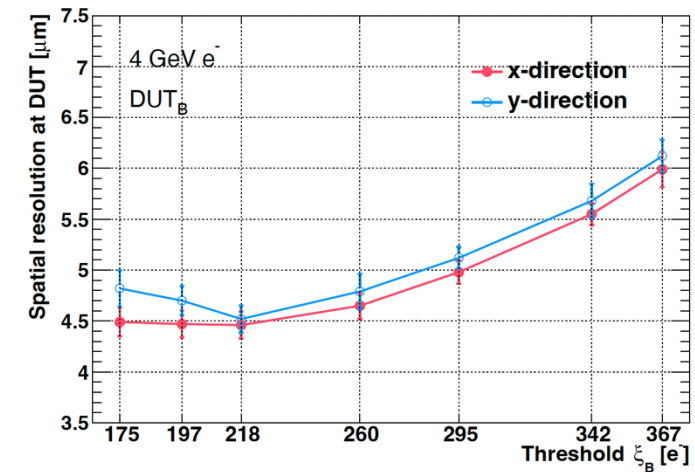
Spatial resolution 4~5 μm , Efficiency >99%



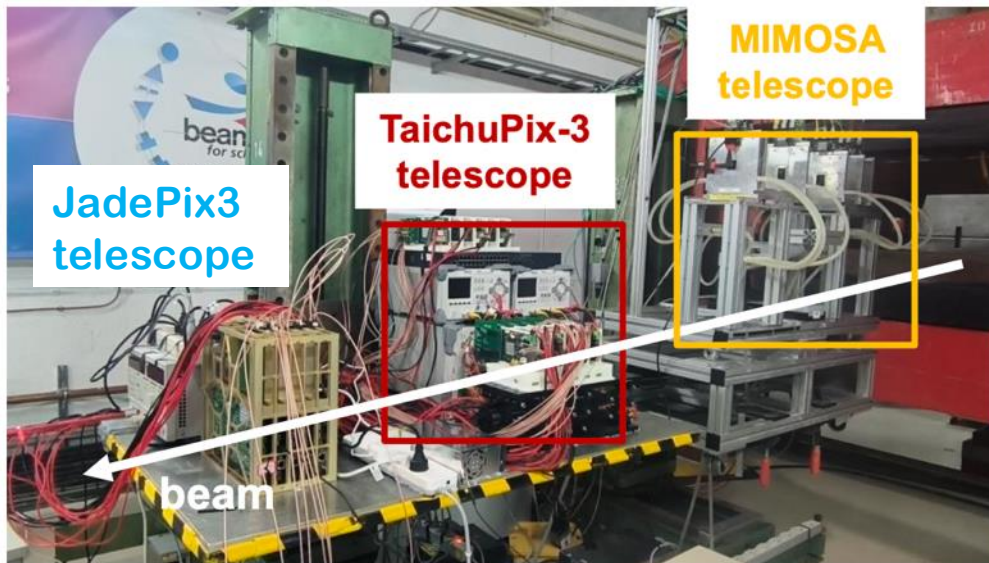
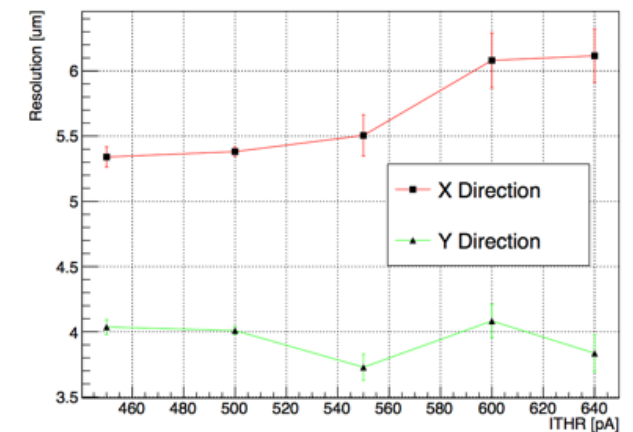
TaichuPix3 efficiency



TaichuPix3 resolution



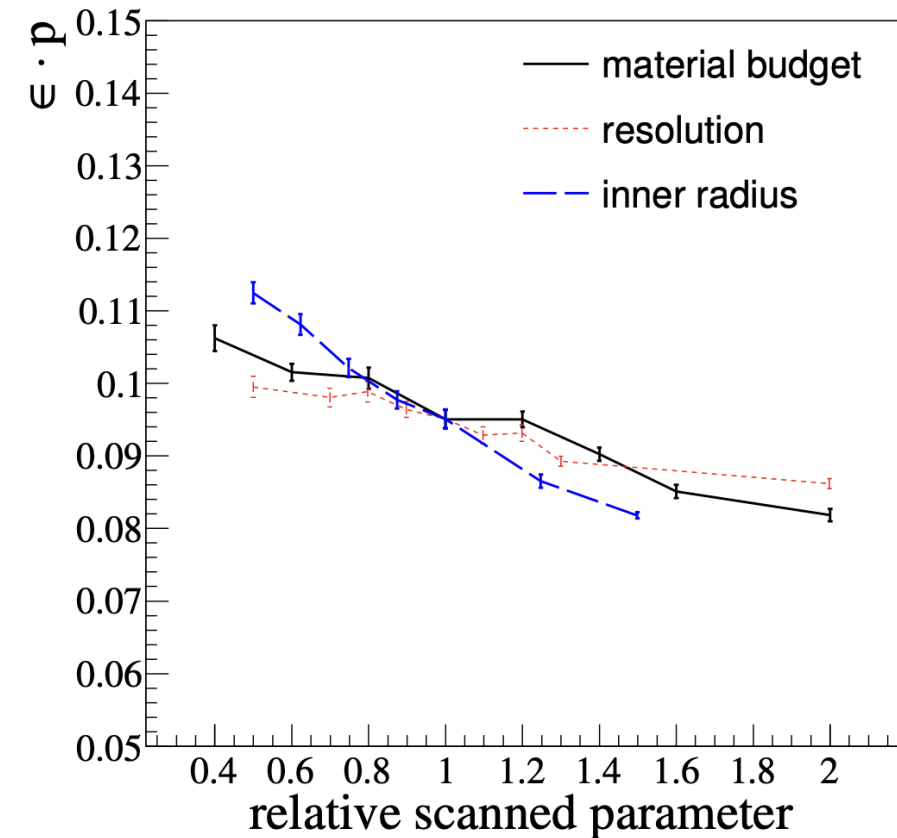
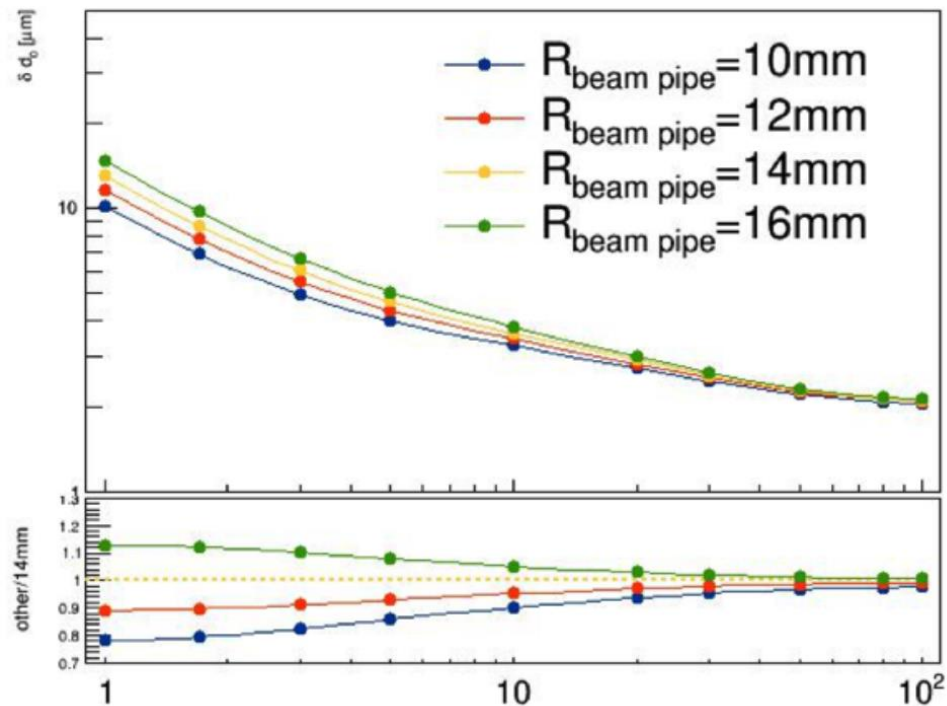
JadePix3 resolution



Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

Vertex Requirement

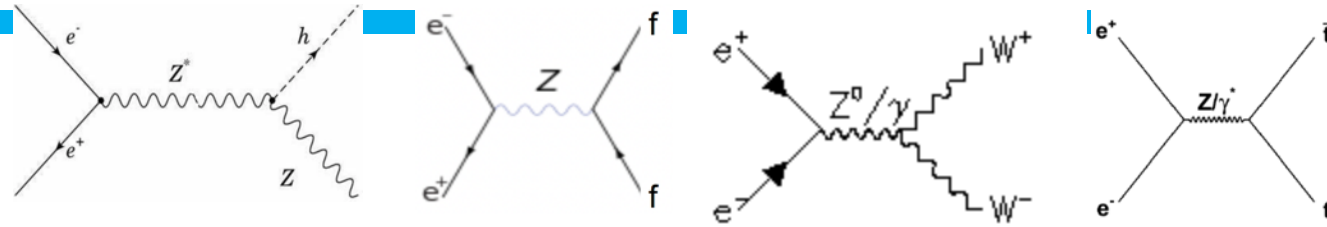
- 1st priority: Small inner radius, close to beam pipe (11mm)
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor: 3~5 μm



CEPC physics program

An extremely versatile machine with a broad spectrum of physics opportunities

→ Far beyond a Higgs factory



Operation mode			ZH	Z	W+W-	$t\bar{t}$
\sqrt{s} [GeV]			~240	~91.2	~160	~360
Run time [years]			10	2	1	5
CDR (30 MW)	$L / \text{IP} [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$		3	32	10	-
	$\int L dt [\text{ab}^{-1}, 2 \text{ IPs}]$		5.6	16	2.6	-
	Event yields [2 IPs]		1×10^6	7×10^{11}	2×10^7	-
Run Time [years]			10	2	1	~5
Latest	30 MW	$L / \text{IP} [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$	5.0	115	16	0.5
	50 MW	$L / \text{IP} [\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}]$	8.3	191.7	26.6	0.8
		$\int L dt [\text{ab}^{-1}, 2 \text{ IPs}]$	20	96	7	1
		Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5

- Huge measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top
- Searching for exotic or rare decays of H, Z, B and τ , and new physics
- CEPC community joined ECFA Phy focus

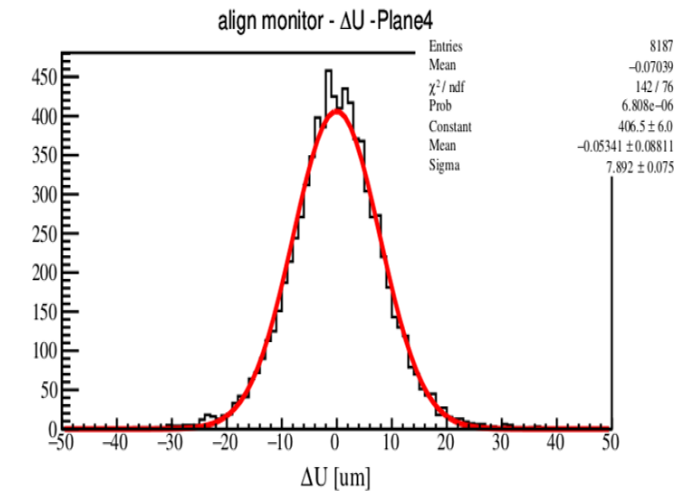
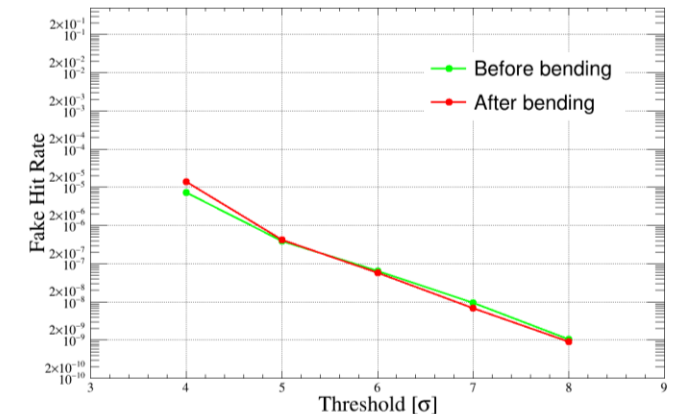
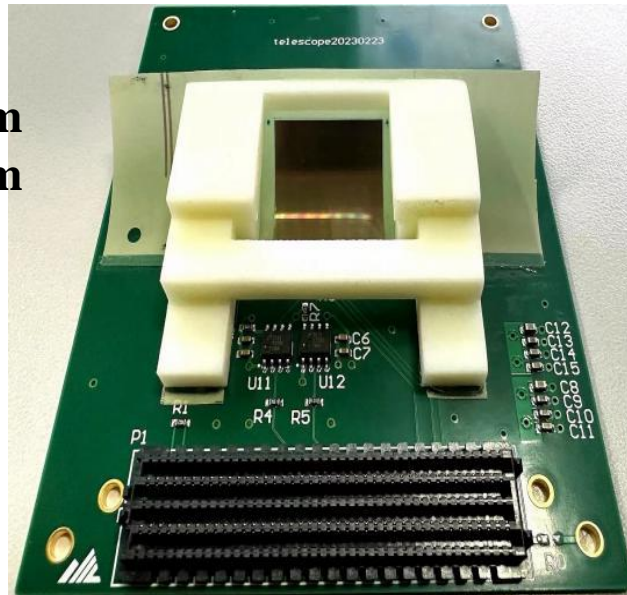
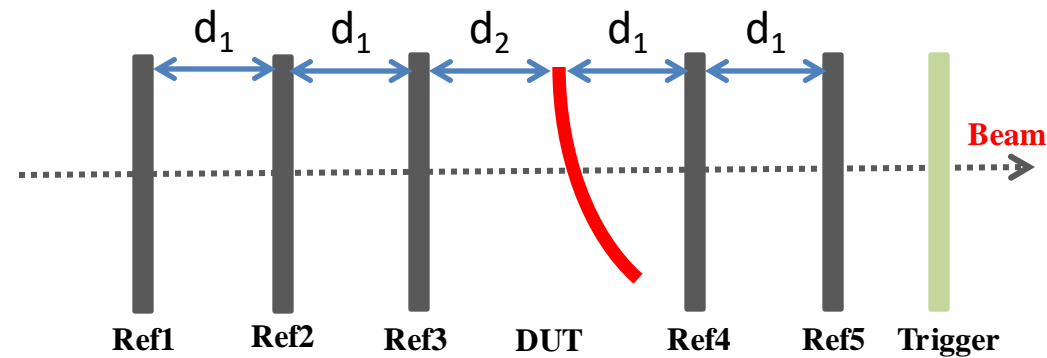
Both 50 MW and $t\bar{t}$ modes are currently considered as CEPC upgrades.

R&D efforts : Curved MAPS testbeam

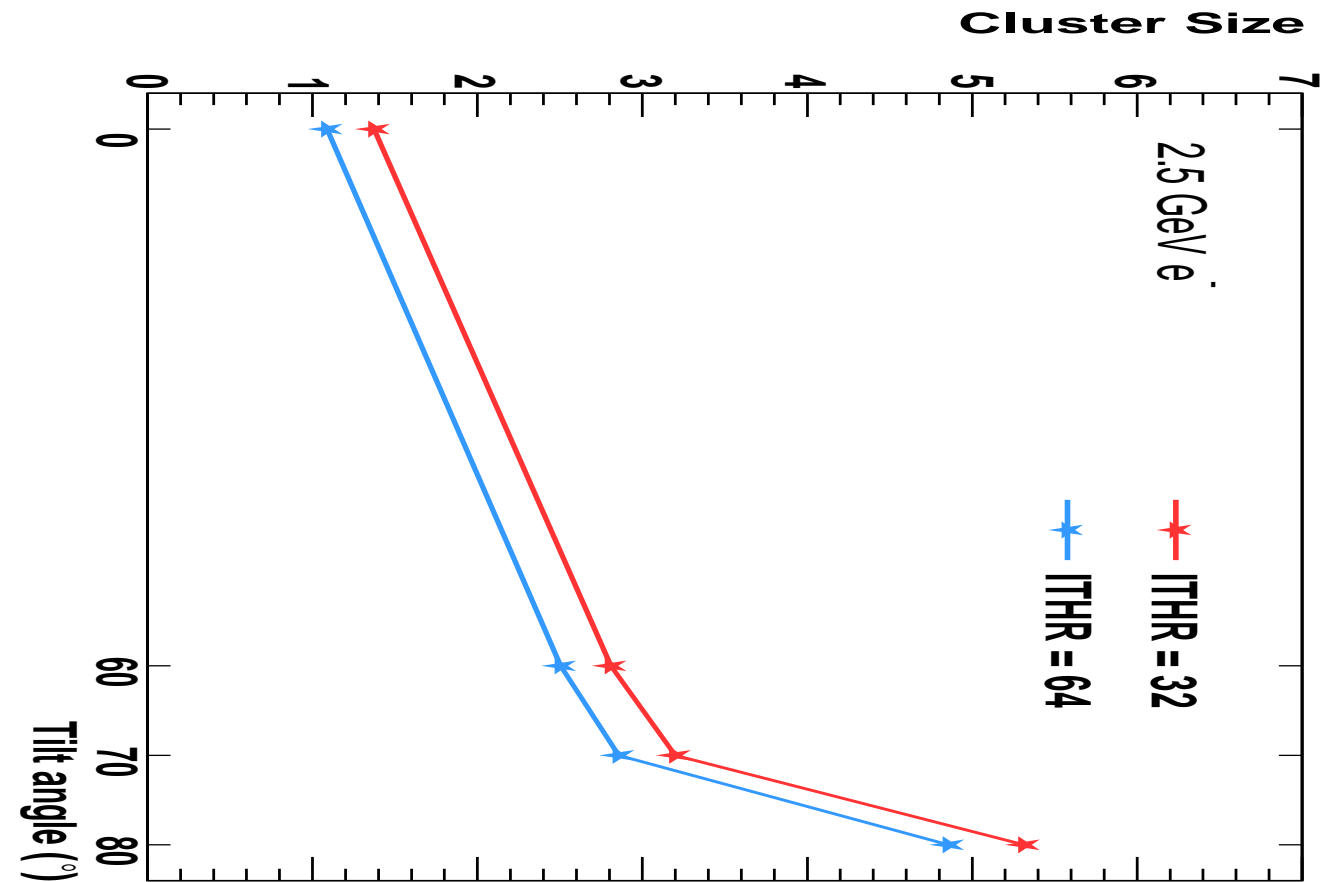
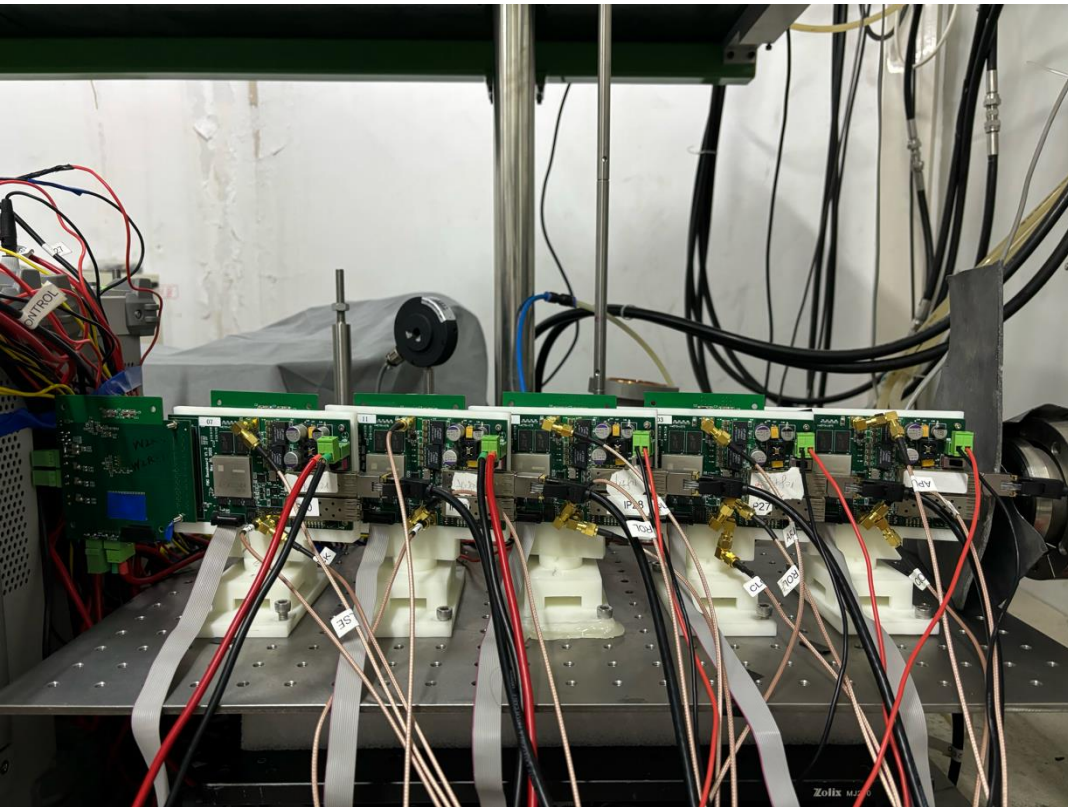
R & D of curved maps with MIMOSA28 chip

- No visible difference in noise level or spatial resolution before/after bending

$d_1 = 25 \text{ mm}$
 $d_2 = 30 \text{ mm}$

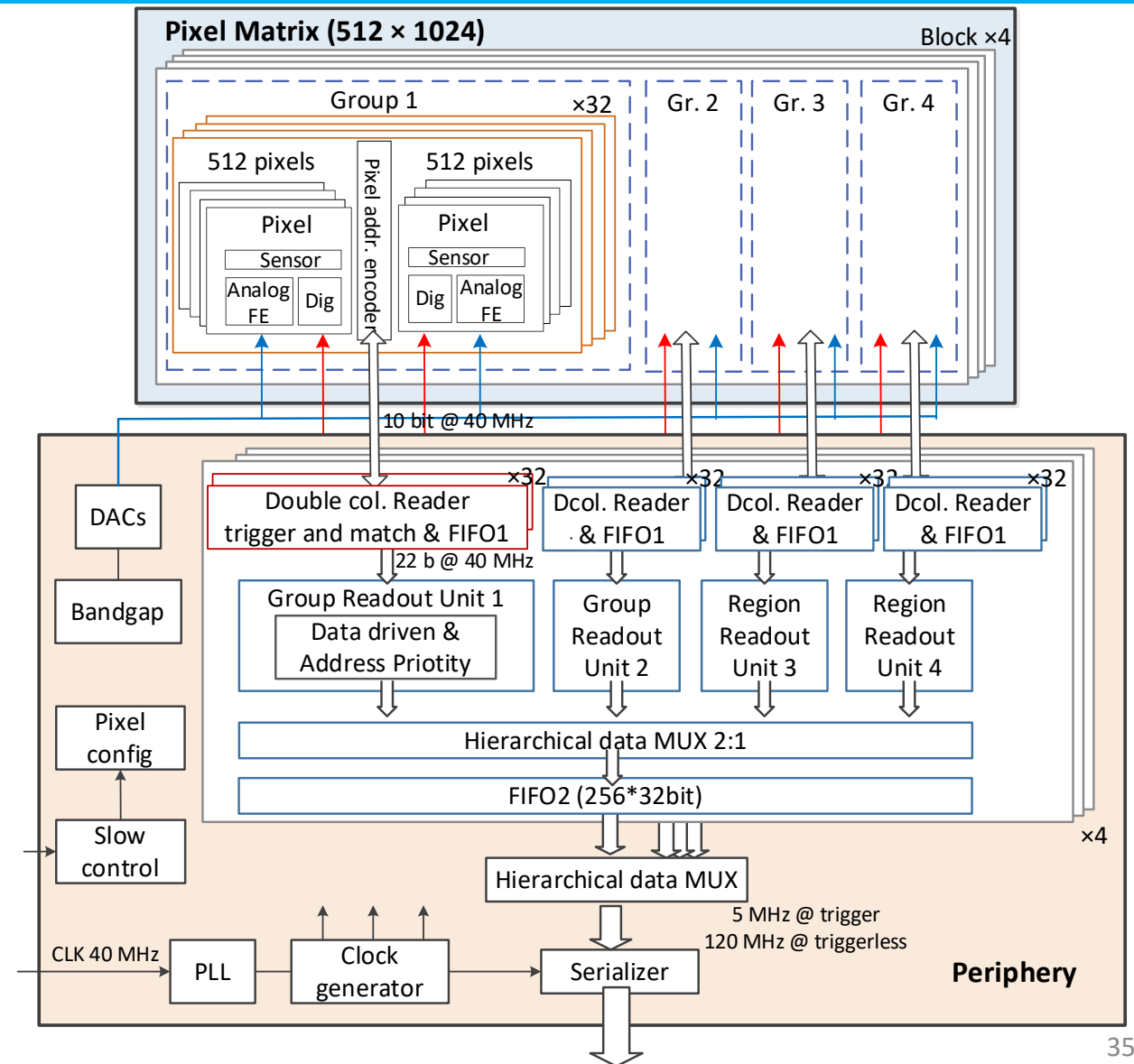


Long barrel : cluster size vs incident angle



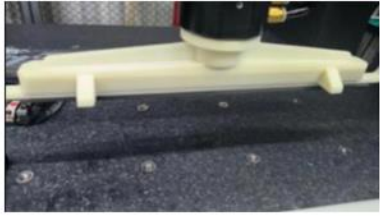
TaichuPix design

- Pixel $25\ \mu\text{m} \times 25\ \mu\text{m}$
 - Continuously active front-end, in-pixel discrimination
 - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
 - Priority based data-driven readout
 - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
 - L1 FIFO: de-randomize the injecting charge
 - L2 FIFO: match the in/out data rate
 - between core and interface
- Trigger-less & Trigger mode compatible
 - Trigger-less: 3.84 Gbps data interface
 - Trigger: data coincidence by time stamp
only matched event will be readout
- Features standalone operation
 - On-chip bias generation, LDO, slow control, etc

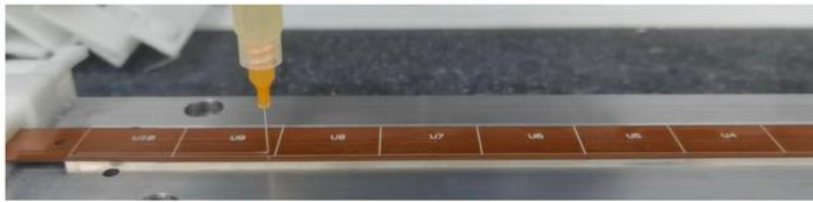


TaichuPix3 vertex detector prototype

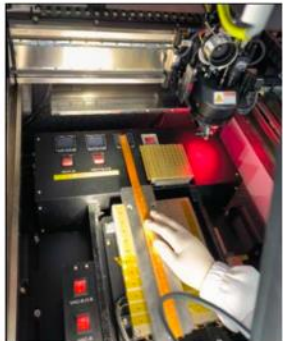
New pickup tools



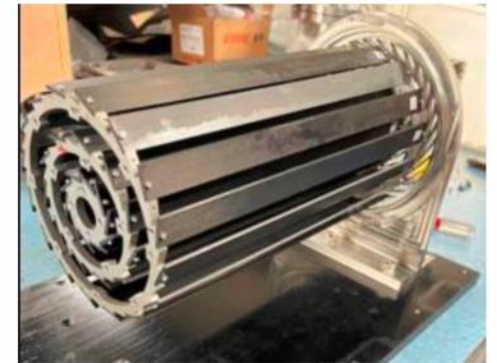
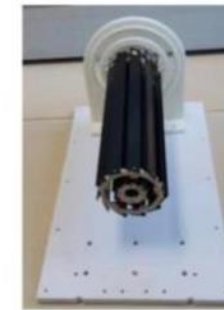
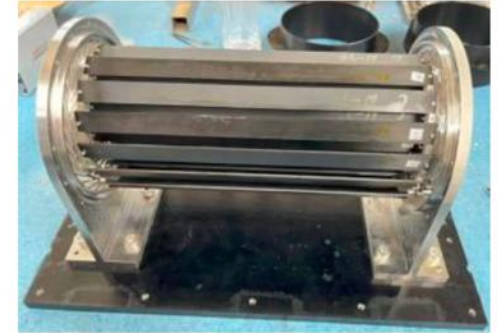
Dummy ladder glue automatic dispensing using gantry



Ladder on wire bonding machine



Dummy Ladder on holder

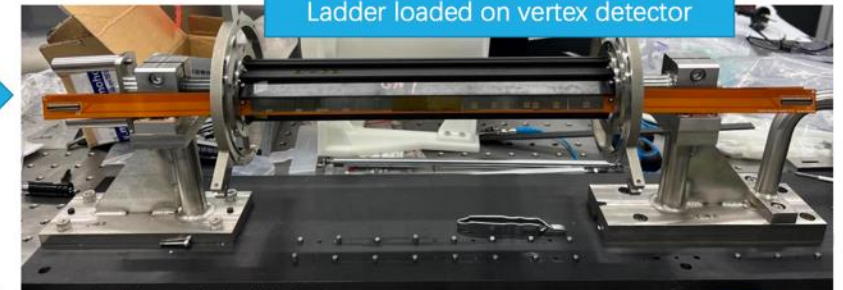


**The first vertex detector
(prototype) ever built in China**

Ladder support tools



Ladder loaded on vertex detector



Research team

- IHEP: overall intergration, chip design, detector assembly, electronics, offline
 - Overall : Joao, Zhijun ,Ouyang Qun
 - Mechanical: Jinyu Fu
 - Electronics: Wei wei, Ying Zhang, Jun Hu, Yunpeng Lu , Yang Zhou, Xiaoting Li
 - DAQ: Hongyu Zhang
 - Detector assembly: Mingyi Dong
 - Physics: Chengdong Fu, linghui Wu, Gang Li
- IFAE: Chip design , Sebastian Grinstein, Raimon Casanova et al
- IPHC/CNRS: chip design , Christine Hu, Yongcai Hu et al
- ShanDong: chip design , Meng Wang, Liang Zhang, Jianing Dong
- CCNU: chip design, ladder assembly, Xiangming Sun, Ping Yang
- North West U. : Chip design Xiaoming Wei, Jia Wang, Yongcai Hu
- Nanchang U. : chip design, Tianya Wu
- Nanjing: irradiation study: Ming Qi , Lei Zhang