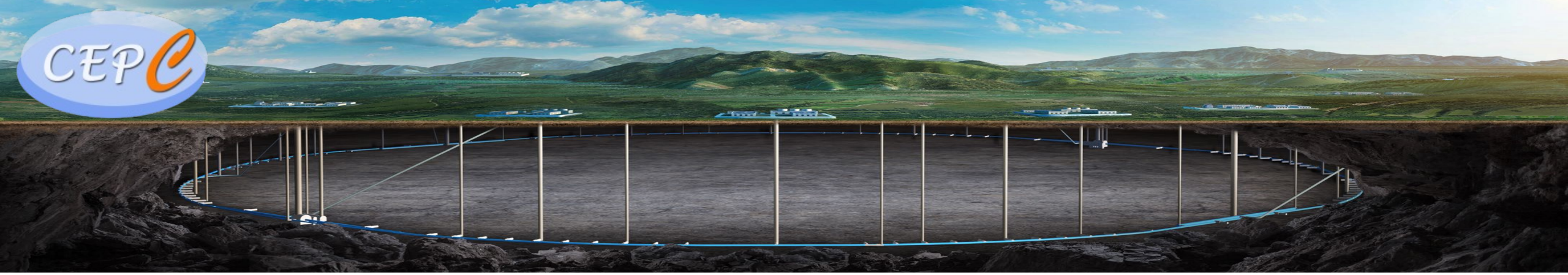

CEPC vertex Detector

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Preliminary outline for Vertex section @ referenece TDR

Chapter 3 Vertex

3.1 Physics Requirements

3.2 Technology survey and our choice

3.3 R&D efforts and results

3.3.1 CMOS Stitching

3.3.2 CMOS normal chip

3.4 Detailed design including electronics, cooling and mechanics

3.4.1 Layout

3.4.2 CMOS sensor design

3.4.3 Cooling and mechanics

3.5 Readout electronics

3.5.1 background estimation

3.5.2 Data rate and readout scheme

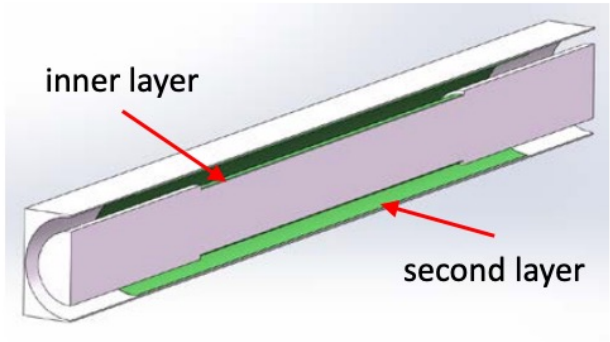
3.6 Performance from simulation (impact parameters)

Cooling update

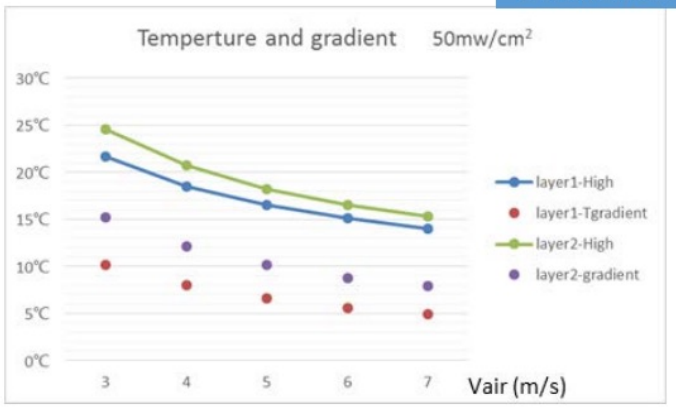
For the innermost layer (R=11mm), it is quite close to the beam pipe(R=10.7mm), the air cooling simulation has been conducted.

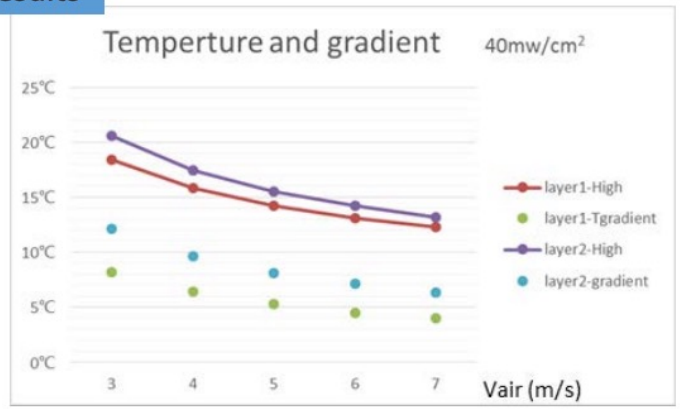
- Power dissipation: 50 mW/cm^2 , 40 mW/cm^2
- Inlet air temperature 5 ℃
- Inlet air velocity varys from 3 m/s to 7 m/s

(Second layer involved, beam pipe temperature ignored)



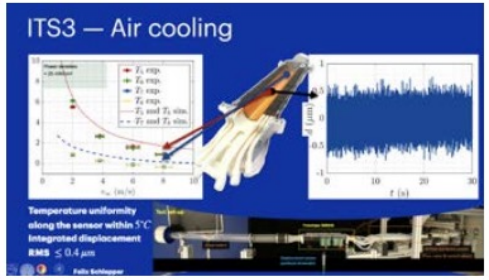
Simulation results





by Jinyu Fu

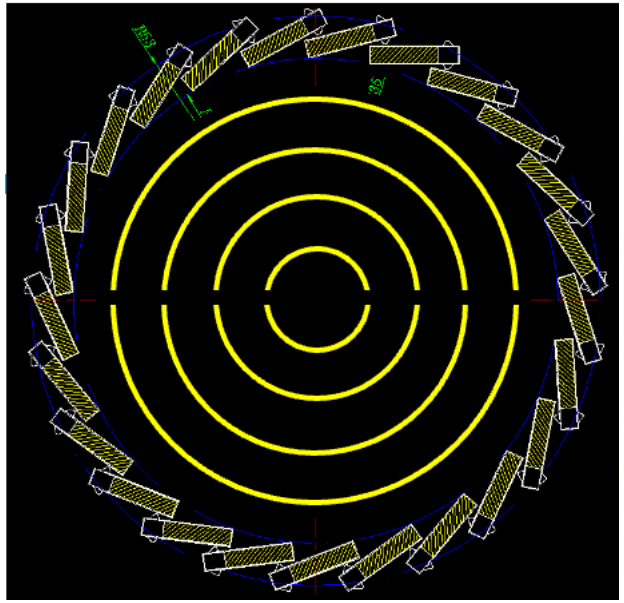
- To air cool the innermost layer detector within 20 ℃ seems feasible. *Temperature gradient should be controlled in a certain level from safety point view?*
- More to be studied !



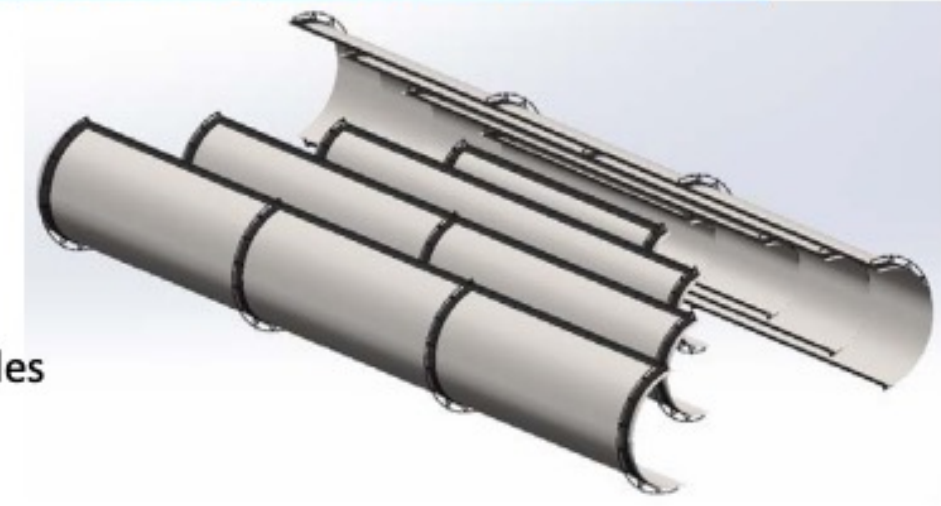
Update on mechanics design

- More update on mechanics design with support ring structure
- Start refining layout layout to reduce dead area
- Alignment and software framework are identified as important issue

by Jinyu Fu



Preliminary structure design of the bent MAPS detector



- one layer has two hemicycles
- low support materials
- more area for ventilation

Beam pipe

- Beam pipe design talk from 洛阳 Mechnics workshop
  - Optimzed for inner beam pipe thickness (<20 C and <100kPa)
  - 0.2mm beam pipe thickness for water cooling ,0.3mm for oil cooling option
  - Significant rate for water corroding the beam pipe (~10um per year)
  - Expect more study on plasma coating for beam pipe protection from water
    - Expect to reduce the rate by two order of magnitude ?

By 何龙岩

冷却通道宽度/mm	外铍管最高温度(油冷)/°C	外铍管最高温度(水冷)/°C
0.1	21.7	17.9
0.15	21.6	17.9
0.2	21.1	17.7
0.25	20.3	17.5
0.3	19.8	17.4
0.35	19.2	17.2

冷却通道宽度/mm	压降(油冷)/KPa	压降(水冷)/KPa
0.1	1254.11	698.03
0.15	363.03	199.28
0.2	167.04	92.83
0.25	94.76	52.67
0.3	55.26	30.88
0.35	36.15	20.34

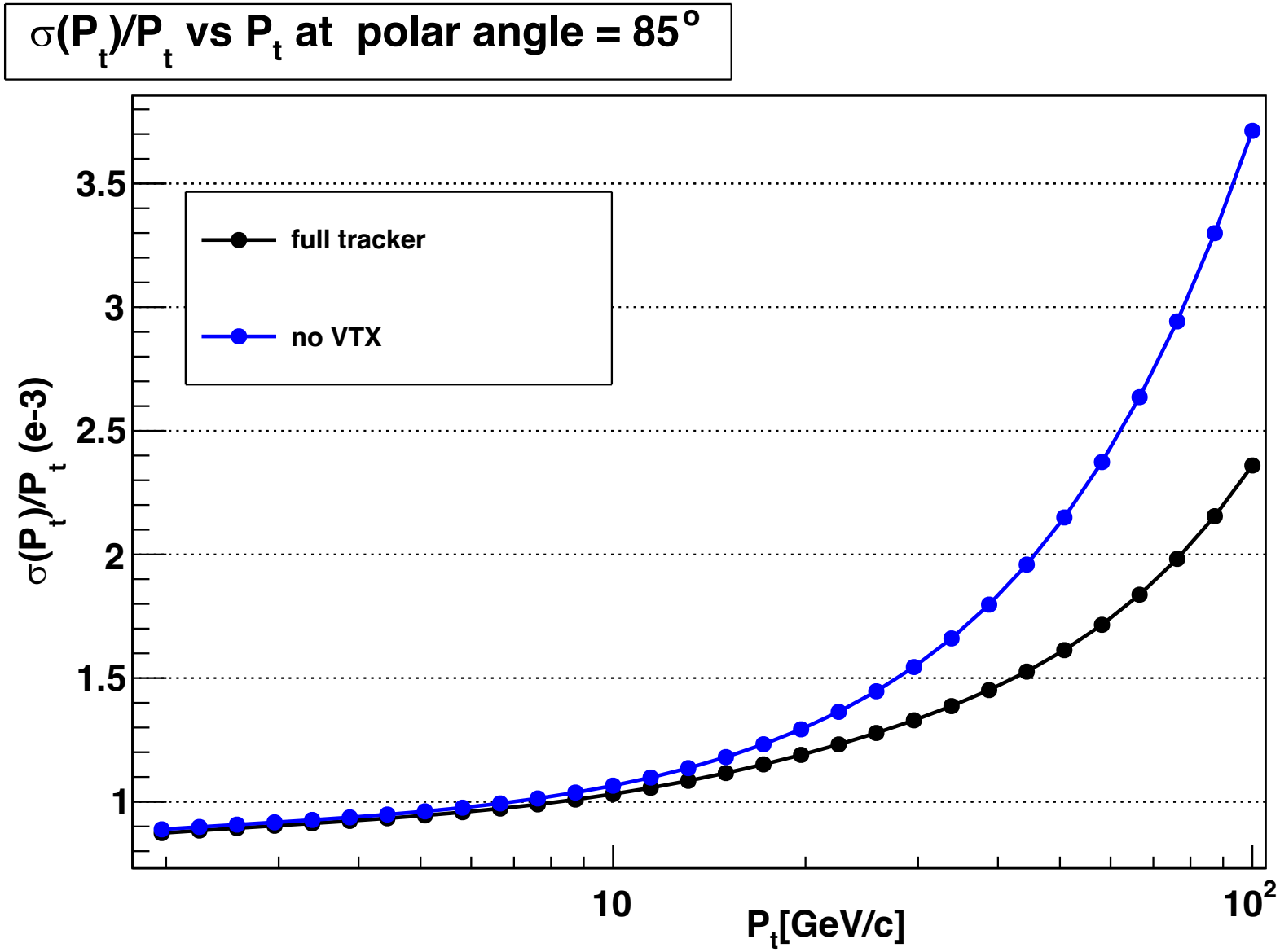
Collider Ring RF Parameters (low lumi Z)

- Bunch spacing for low-lumi-Z (10MW) confirmed to be 69ns (3* 23ns)

30/50 MW SR power per beam for each mode. Higgs/ttbar shared cavities for the two rings. W/Z separate cavities. HL-Z cavities bypass.	ttbar 30/50 MW		Higgs 30/50 MW	W 30/50 MW	Z 10 MW	Z 30/50 MW
	New cavities	Higgs cavities				
Luminosity / IP [10^{34} $cm^{-2}s^{-1}$]	0.5 / 0.8		5 / 8.3	16 / 26.7	38	115 / 192
RF voltage [GV]	10 (6.1 + 3.9)		2.2	0.7	0.12	0.12 / 0.1
Beam current / beam [mA]	3.4 / 5.6		16.7 / 27.8	84 / 140	267	801 / 1345
Bunch charge [nC]	32		21	21.6	22.4	22.4 / 34.2
Bunch length [mm]	2.9		4.1	4.9	8.7	8.7 / 10.6
650 MHz cavity number	192	336	192/336	96 / 168 / ring	48 / ring	30 / 50 / ring
Cell number / cavity	5	2	2	2	2	1
Gradient [MV/m]	27.6	25.2	24.9 / 14.2	15.9 / 9.1	5.4	17.4 / 8.7
Q_0 @ 2 K at operating gradient	3E10	3E10	3E10	3E10	3E10	2E10
HOM power / cavity [kW]	0.4 / 0.66	0.16 / 0.26	0.4 / 0.67	0.93 / 1.54	1.9	2.9 / 6.2
Input power / cavity [kW]	188 / 315	71 / 118	313 / 298	313 / 298	206	1000
Optimal Q_L	1E7 / 6E6	9E6 / 5.4E6	1.6E6 / 9.5E5	8E5 / 2.7E5	1.4E5	1.5E5 / 3.8E4
Optimal detuning [kHz]	0.01 / 0.02	0.02 / 0.03	0.1 / 0.2	0.7 / 2	7	6.7 / 21.7
Cavity number / klystron	4 / 2	2	2	2	2	1
Klystron power [kW]	800	800	800	800	800	1200
Klystron number	48 / 96	168	96 / 168	96 / 168	48	60 / 100
Cavity number / cryomodule	4	6	6	6	6	1
Cryomodule number	48	56	32 / 56	32 / 56	16	60 / 100
Total cavity wall loss @ 2 K [kW]	12.1	7.1	3.9 / 2.3	1.6 / 0.9	0.1	0.45 / 0.2

Ref: Jiyuan Zhai, CEPC workshop-EU 2024

Impact of vertex detector on tracking



Backup

Items in meeting with IDRC chair

- Total area and Timeline for ALICE ITS3, should compare with CEPC vertex
  - ALICE ITS3 timeline is about 2~3 years earlier (ITS3 2032installation)
  - ITS3: 0.06 m^2, CEPC: 0.15 m^2
- Material budget for normal ladders (especially for carbon fiber)
  - mu3E ladders has 0.1% X0 per layer (we quoted 0.25% X0 per layer)
  - Carbon fiber thickness in CEPC prototyping can reach 0.12mm, same level as mu3E
- Accessibility for 65/55 nm technology in China
  - TowerJazz 65nm CIS can be submitted by TJ agency in China
  - R & D of SMIC 55nm technology is on going
- Serial powering is widely used in ATLAS/CMS upgrade, should look into it
  - Wei Wei's talk will compare DC/DC and Serial powering scheme

Data rate estimation of CEPC VTX

	Data rate@triggerless （old result, 30MW)	Data rate@triggerless （new result, 50MW）
Higgs (240GeV)	0.43 Gbps	>1Gbps

Old New

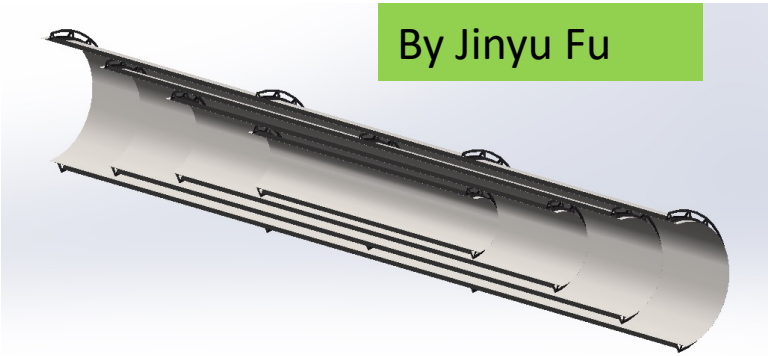
- Bunch structure of ZH runs was not taken into accounted
  - Bunch structure @ ZH: 50% duty cycle (10ms with collision; 10ms without collision)
  - Old result was average data rate (underestimated)
  - New result will double the data rate
- Old result was using 30MW , new result is using 50MW

- In new estimation, Even Higgs run has rate above 1Gbps per chip
- Triggerless scheme may needed to reconsidered

Update in CEPCSW

- Stitching layer layout is implemented in CEPCSW
  - Dead area is also considered
  - Digitization is OK now, can be used for BG simulation
  - Code for reconstruction is still under development

By Jinyu Fu



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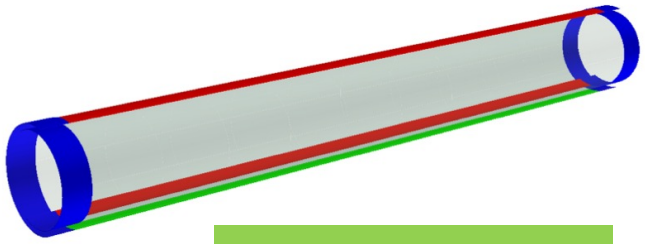
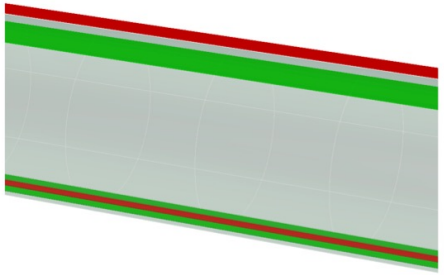


By Chengdong Fu



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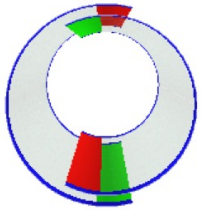
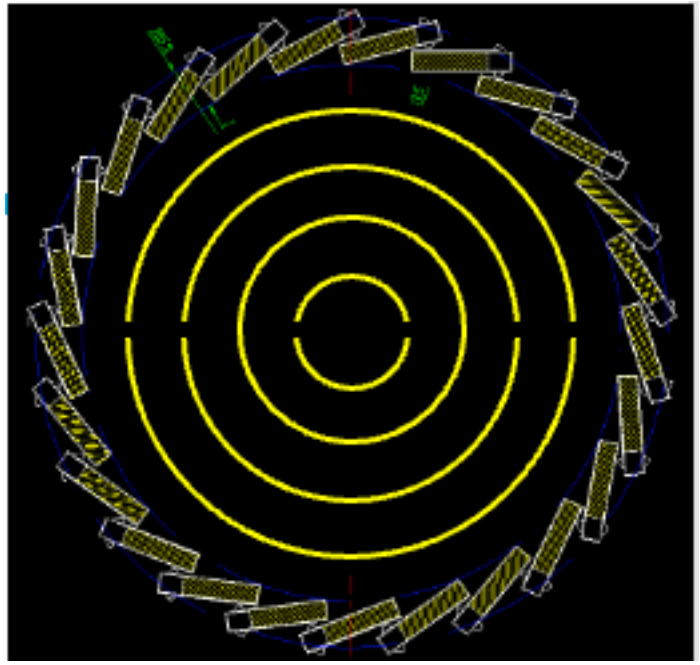
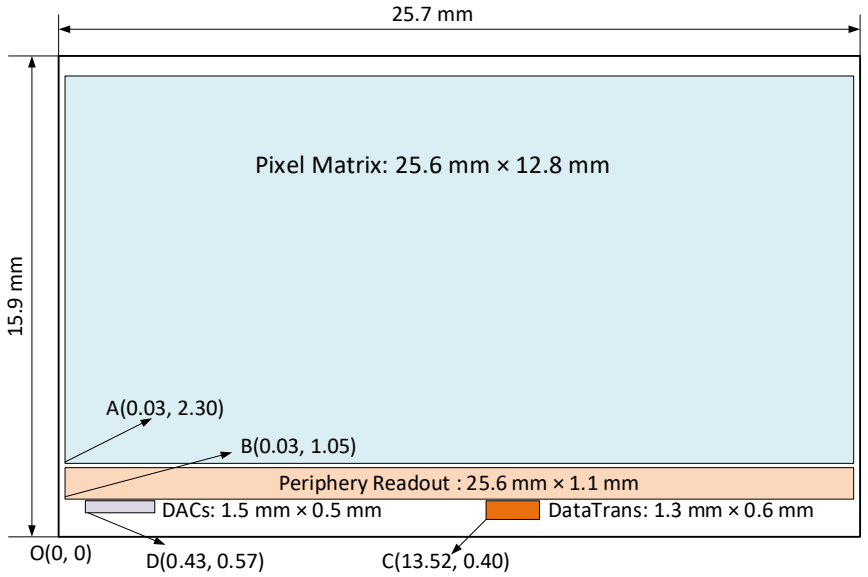


Parameter to confirm



Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation



	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm^2
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~45 mW/cm^2

Update of chip design

- Got the Design kit for TJ 65nm (p type standard process)

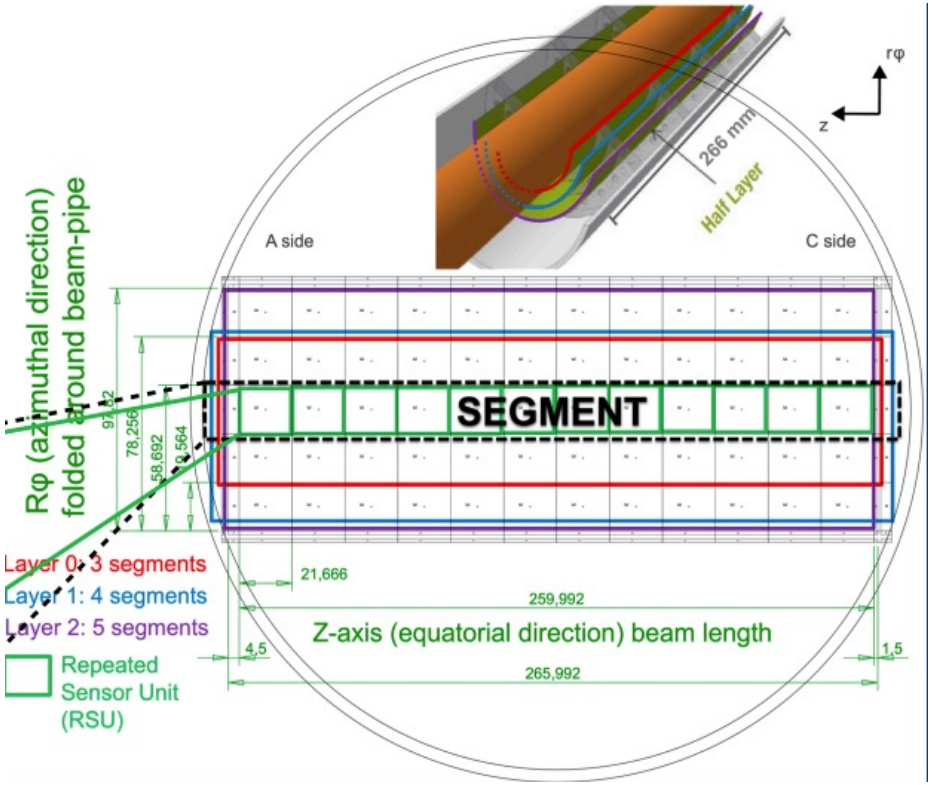
By Ying Zhang

  - Can start the pixel layout design
    - Pixel size estimation and power consumption estimation
  - Two small issue for 65nm design kit from TowerJazz China
    - Substrate resistance only up to 0.13kOhm (it was 1k Ohm in TJ 180nm CIS)
    - Only support 4 metal layers (ALICE ITS3 was using 7 metal layers)
    - Do not support modified process

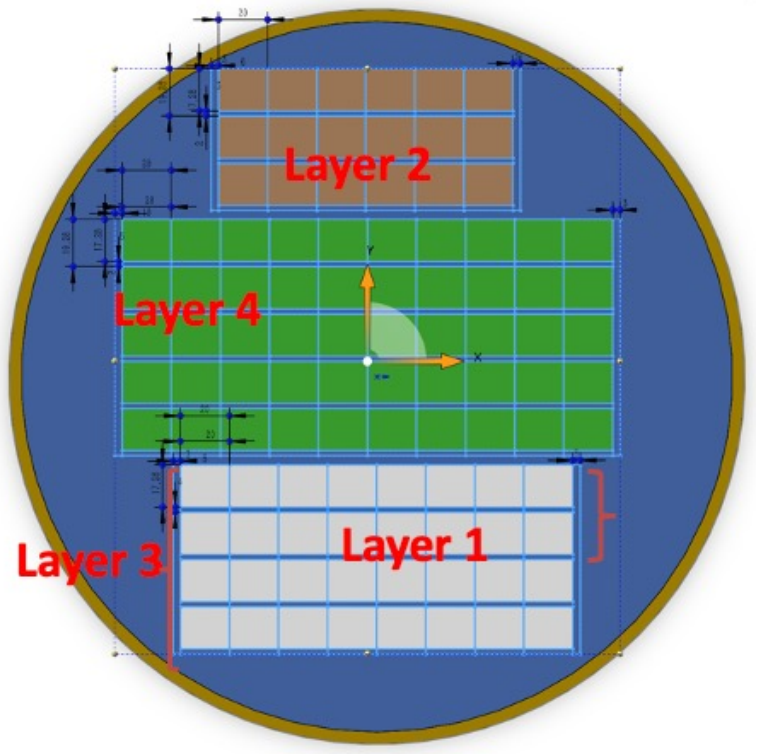
Feedback from Christine Hu

- Feedback from Christine Hu :
  - Needed to careful about the yield in stitching design

ALICE ITS3 proposal on stitching design



Our preliminary proposal on stitching design



Preliminary outline for Vertex section @ referenece TDR

3. Vertex detector (Zhijun & Meng Wang)

- a. Requirements (position and vertex) Zhijun , Manqi
- b. Technology survey and our choices (both baseline & backup options), Zhijun & Meng
- c. R&D efforts and results

  →CMOS Stitching: Meng Wang

  → CMOS normal chip: Zhijun, Wei Wei, Yupeng
- d. Detailed design including electronics, cooling and mechanics

  → Layout: Zhijun & Meng Wang

  → CMOS sensor design: Wei Wei， Ying Zhang, Yunpeng

  →Cooling and mechanics: Jinyu Fu
- e. Readout electronics & BEC

  →Background estimation : Haoyu Shi

  → Data rate and readout scheme: Jun Hu, Wei Wei
- f. Performance from simulation (impact parameters). Chengdong Fu