CEPC CMOS Strip Tracker

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On behalf of CMOS Strip Tracker Team

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Welcome more contributors!

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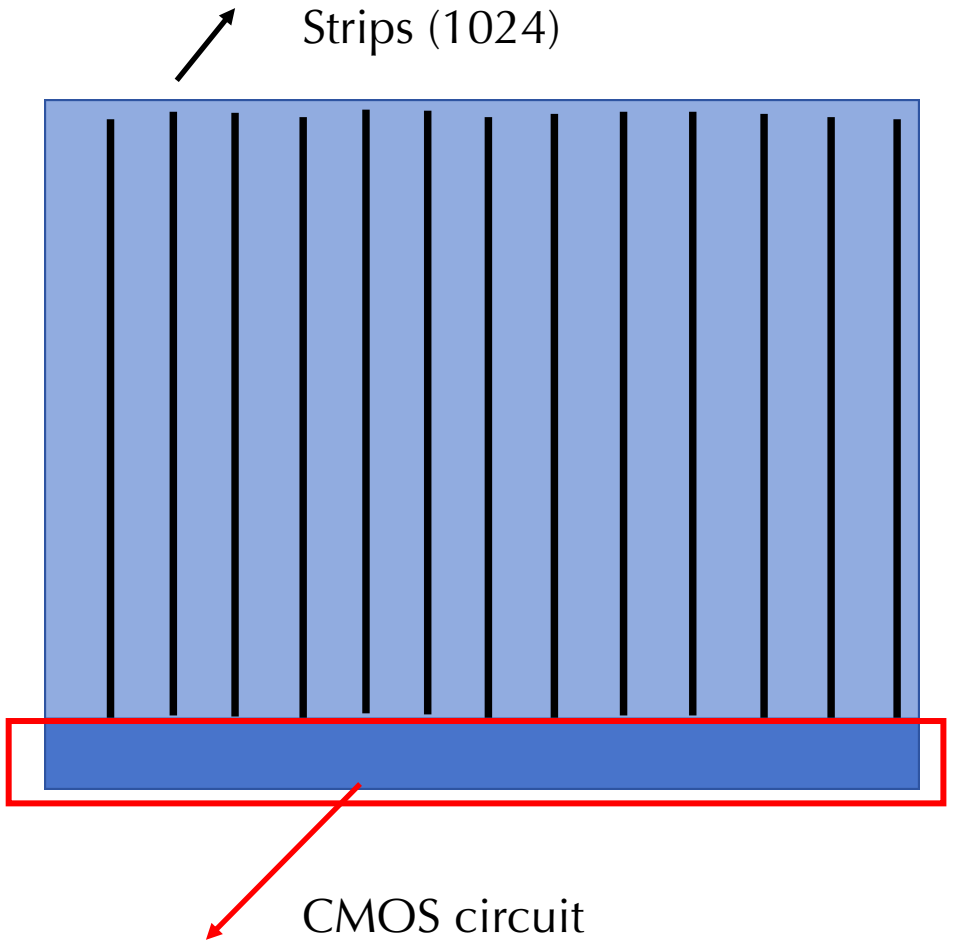
CMOS Strip Chip - CSC

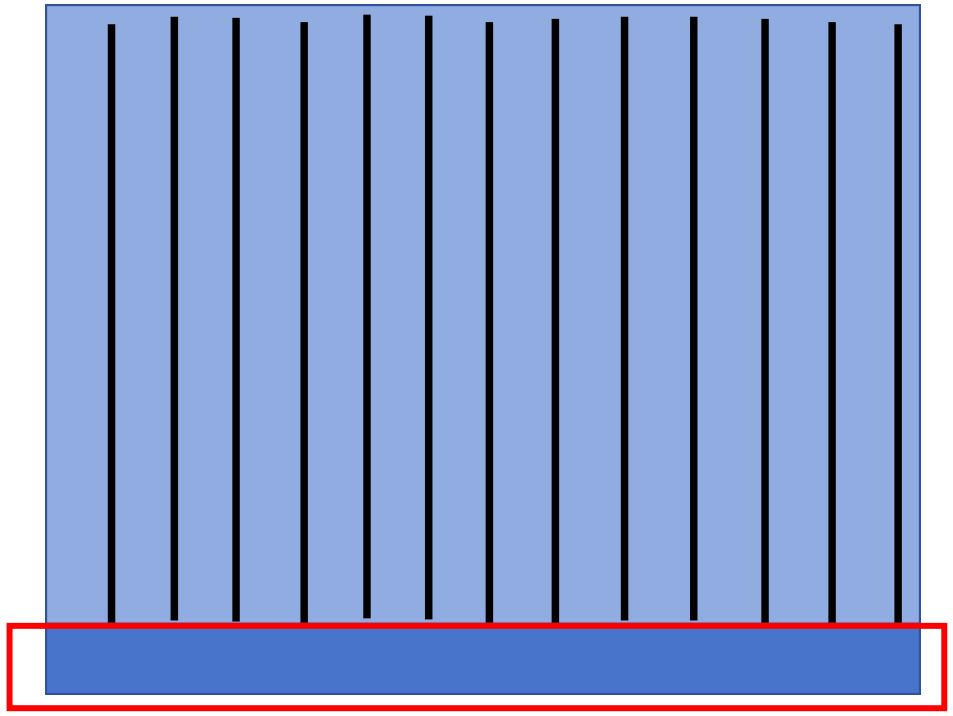
Version 1.1



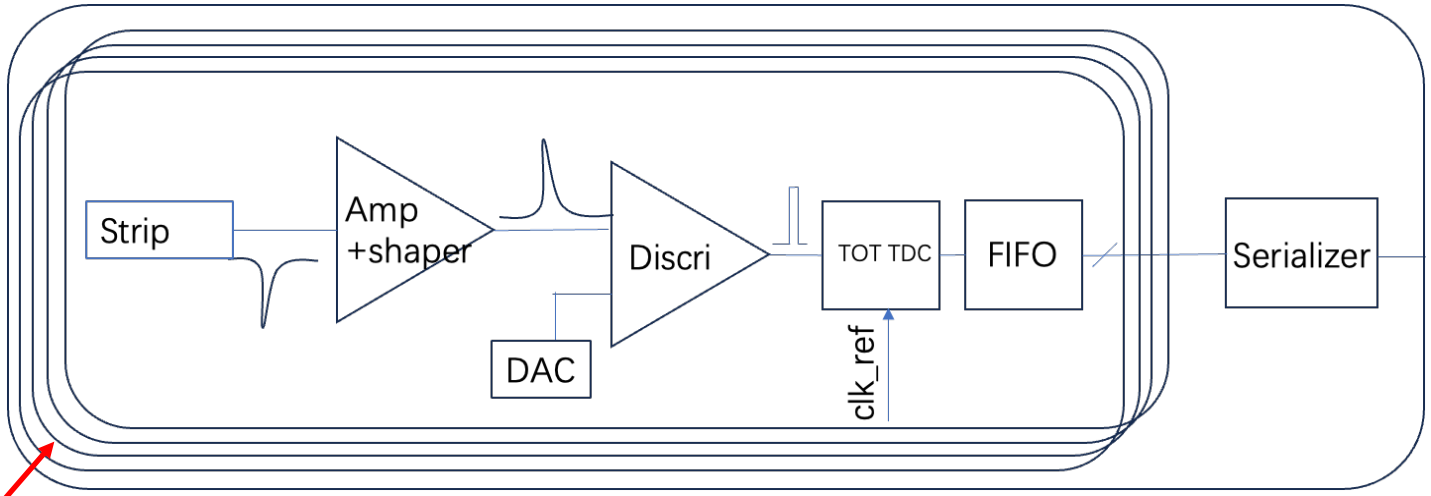
Parameter	Requirement / expectation
Strip width	10μm
Strip pitch	20μm
Strip number / chip	1,024
Chip size	2.1×2.3cm^2 (active area: 2.05x2.05)
Spatial resolution	σ_ϕ~4.2μm, σ_r~21um
Time resolution	< 3ns
Power consumption	~ 80mW/cm^2
Data size per hit	32 bits (10b chn ID + 8b BX + 6b TOT + 5b chip ID)
Event rate / chip	Maximum ~0.25Gbps
LV / HV	1.8V / 200V
Wafer resistivity	2k Ω cm
Technology Node	150 nm

CSC: Front-end electronics

Strips (1024)

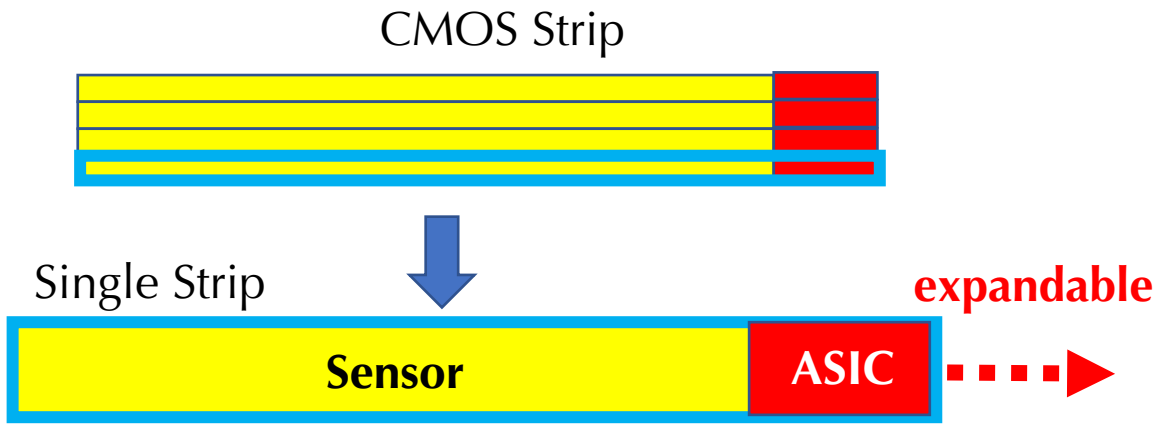


CMOS circuit



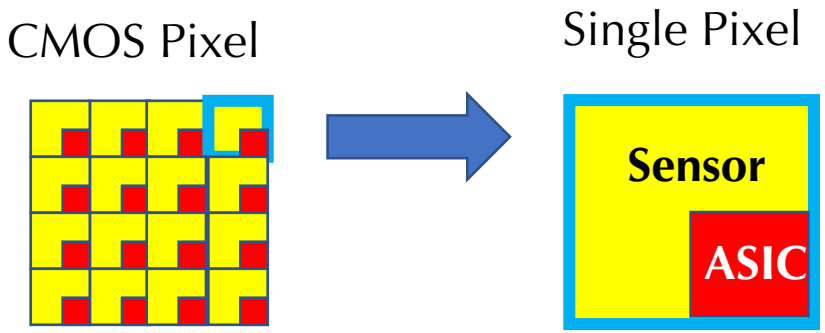
CMOS Strip Chip – Basic Concept

- CMOS **strip** is different than CMOS **pixel**



- Pros: ASIC no constrain from the strip sensor
  more space to integrate more circuit
- Cons: large capacitance of strip sensors
  Special care for amplifier design

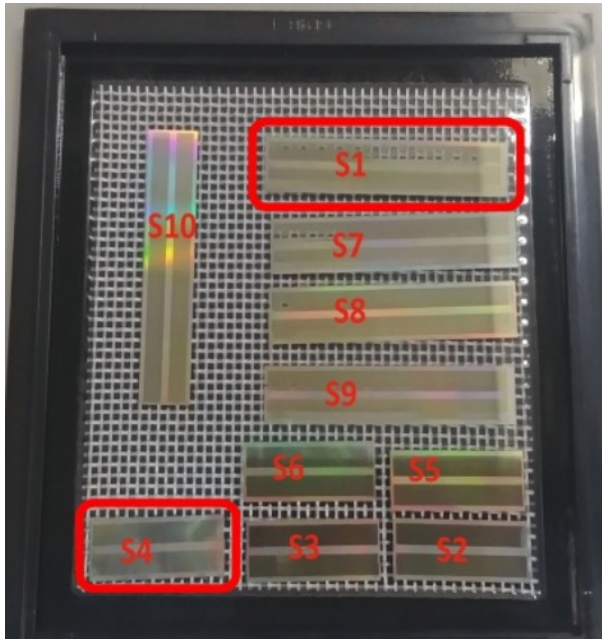
Negligible cross-talk between sensors and ASIC.

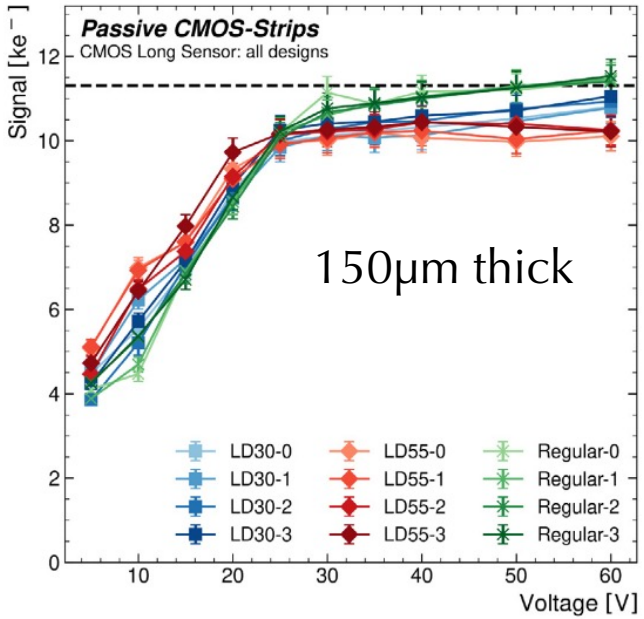


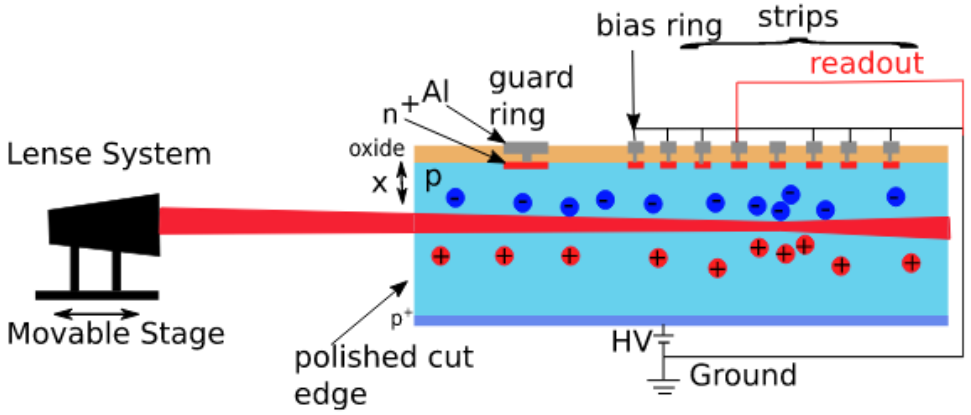
- Pros: small capacitance of sensor area
- Cons: ASICs and sensors share same area
  special care for separation to avoid cross-talk

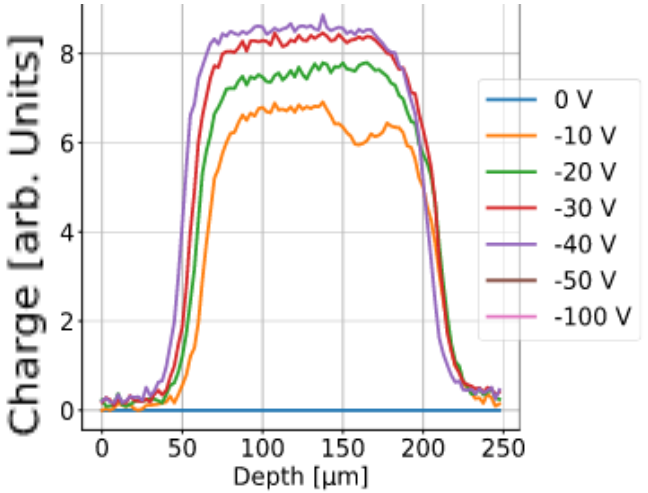
Existing passive CMOS sensor

- First large sized CMOS passive sensor(> 4cm)
  - Main designer : Tianyang Wang
  - Stitching technology on 6-in wafer with LFoundary
- Successfully tested of strip sensor behavior
- Confirmed feasibility of CMOS strip sensor path









https://doi.org/10.1016/j.nima.2022.166671

Available HR wafer from domestic company

- Zhonghuan (天津中环)
- 2kΩ HR wafer
- 8-inch wafer size

No.	Characteristics		
1	生长方法	Growth Metchod	FN
2	型号	Type	P
3	掺杂类型	Dopant	Boron
4	电阻率	Resistivity	>2000Ω.cm
5	晶向	Crystal Orientation	<100>
6	晶向偏离度	Off Orientation	±0.5°
7	直径	Diameter	200±0.2mm
8	V槽位置	Flat Location	<110>±1° 深度：1-1.25mm 角度：89-95°
9	边缘轮廓	Edge Profile	R型 22±2°SEMI
10	厚度	Thickness	725±25μm
11	总厚度变化	Thickness Variation(TTV)	≤10
13	弯曲度	Bow	≤30
14	翘曲度	Warp	≤60
15	颗粒	Particle	0.3＜10
16	正面	Surface Condition	抛光
17	背面	Backside Condition	酸腐
18	碳含量	Carbon Concentration (Cs)	≤2E16
19	氧含量	Oxygen Concentration(NEW ASTM)	≤2E16
20	金属沾污	Surface Metal Contamination(Al、Na、K、Ca、Fe、Ni、Cu、Zn、Cr)	＜5E10

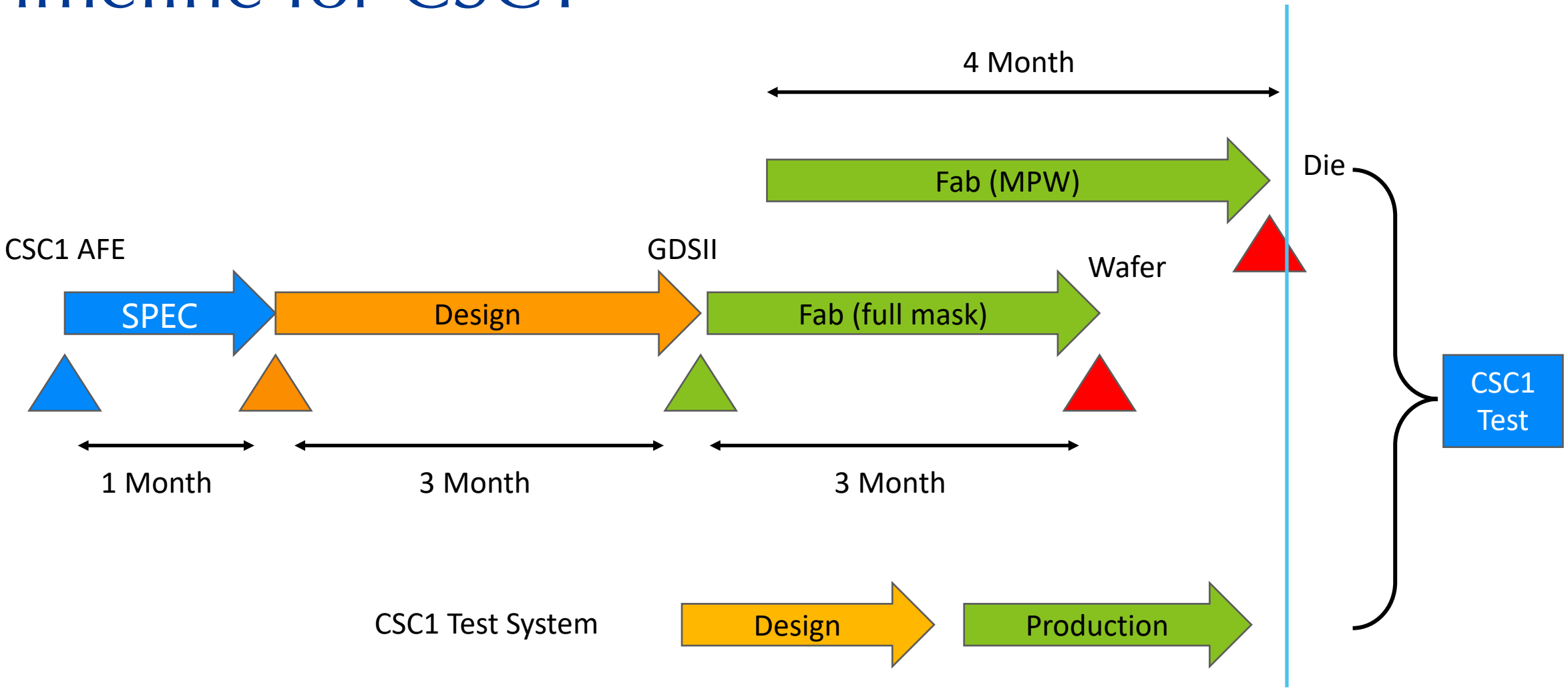
Available Foundries from domestic and abroad

- Foundry： Wuxi Huarun Shanghua Tech (无锡上华)
- Process：0.18μm BCD，8-inch wafer
  - Capable to process HR wafer
  - Capable for backplane implant and metallization for HV bias
  - Accept turning of injection depth and dielectric width
- Lfoundry: 0.15um will also be used along the line

Work Breakdown Structure (WBS)

1. Sensor -> Simulation on-going
2. ASIC
   - Amplifier / Shaper / Discriminator / TDC / FIFO / Serializer
3. Integration
4. Test System
5. Characterization

Timeline for CSC1



CSC1 and Beyond

- Explore the potential of CMOS strip technology

  Spacial resolution $< 4\mu m$
  Timing resolution $< 50ps$
  Charge resolution $< 10\%$

- Build a friendly radiation semiconductor ecosystem in China
  - Establish collaboration with institutions (IMECAS, ZJL, IAS, …) companies (Conveyi, …) and univerisities (SYSU, …)
  - Work together on novel sensor / ASIC design, build system test with open source/hardware and evaluations with frontier technologies ...

Welcome to join us!