Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169905

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Feasibility study of CMOS sensors in 55 nm process for tracking

Zhuojun Chen [a], Ruoshi Dong [b,c], Leyi Li [d], Yiming Li [b,*], Weiguo Lu [b], Yunpeng Lu [b], Ivan Peric [c], Jianchun Wang [b], Zhiyu Xiang [b], Kunyu Xie [b], Zijun Xu [b], Hui Zhang [c], Mei Zhao [b], Yang Zhou [b], Hongbo Zhu [e], Xiaoyu Zhu [f]

[a] Hunan University, Changsha, China
[b] Institute of High Energy Physics, Chinese Academy of Sciences, Beijing, China
[c] Karlsruher Institute for Technology, Karlsruhe, Germany
[d] Shandong University, Ji'nan, China
[e] Zhejiang University, Hangzhou, China
[f] Central China Normal University, Wuhan, China

ARTICLE INFO

Keywords:
CMOS sensor
MAPS
55 nm

ABSTRACT

High-Voltage CMOS (HVCMOS) sensors, featuring a deep n-well separating the transistors and the depletion region, are intrinsically radiation hard and a good candidate for tracking systems in future high energy physics experiments. In hope of reducing the power density and incorporating more functionality in the same area, we are looking for foundries where HVCMOS sensors can be implemented in smaller feature size. In this paper we report the feasibility study in two MPWs using 55 nm processes. Sensor diodes are designed with deep n-well serving as electrode in Low-Leakage process, and the test results are reported. Design and first results for MPW in 55 nm HVCMOS process will also be described.

Contents

1. Introduction

The CMOS monolithic active pixel sensors have become an attractive technology option for tracking detectors in high energy physics for their excellent spatial resolution [1,2]. High-Voltage CMOS (HVCMOS) sensors, featuring a deep n-well separating the electronics and the substrate, can achieve a large depletion volume which improves charge generation and collection [3]. The structure is also proven to be radiation hard [4]. Currently multiple HVCMOS sensors are successfully fabricated or under development, mainly using 180 nm [5,6] or 150 nm [7,8] CMOS processes. Smaller feature size allows for higher circuit density, hence more functionality in the same area probably with lower power consumption. Such development is under study for CMOS sensors with small electrode [9].

Driven by the demand of large-area tracking detectors in future experiments, such as LHCb Upgrade II [10] and Circular Electron Positron Collider (CEPC) [11], we have been looking for available HVCMOS process in feature size around 65 nm or smaller. In this paper we report two MPWs using SMIC 55 nm CMOS processes. The design and first characterization of two CMOS sensOrs in Fifty-FivE nanometer procEss, COFFEE1 and COFFEE2, are introduced in Section 2 and Section 3 respectively.

2. Design and first results of COFFEE1

The COFFEE1 chip is fabricated in 55 nm Low-Leakage process in an MPW in 2022. This is not a High-Voltage process but has a similar

* Corresponding author.
E-mail address: liyiming@ihep.ac.cn (Y. Li).

https://doi.org/10.1016/j.nima.2024.169905
Received 15 February 2024; Received in revised form 6 September 2024; Accepted 19 September 2024
Available online 24 September 2024

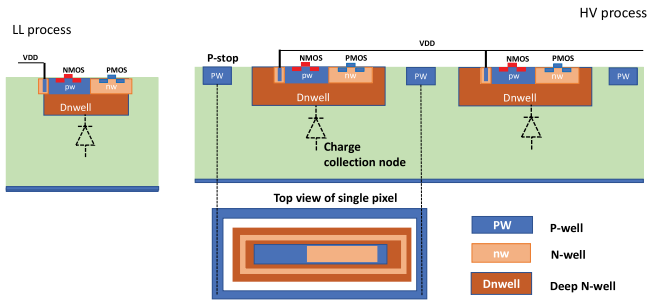

Fig. 1. Cross-section of the 55 nm Low-Leakage (left) and High-Voltage CMOS (right) processes.

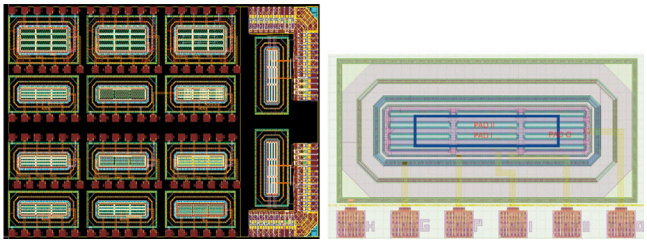

Fig. 2. (Left) COFFEE1 floorplan and (right) the structure of a 12-pixel diode array. The blue line indicates ten interconnected pixels in the array.

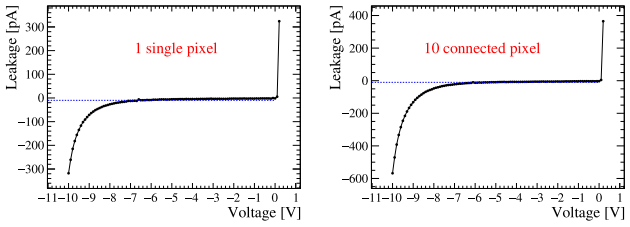

Fig. 3. The IV curves of (left) a single pixel and (right) 10 connected pixels.

deep n-well structure underneath the electronics which could serve as a large electrode, as illustrated in the right part of Fig. 1. The default wafers with low resistivity of a few Ω cm are used.

The COFFEE1 floorplan is shown in Fig. 2. It has an area of 3 mm × 2 mm, with twelve different variations of passive diode sensor arrays. Each array has 4 × 3 pixels. The design variations are:

- Pixel area $25 \times 150\,\mu m^2$ or $50 \times 150\,\mu m^2$;
- With or without p-stop between pixels;
- Gap of 5 µm, 10 µm or 15 µm between neighboring deep n-well.

Note that all dimensions quoted are designed value, while the actual size is scaled down by a factor of 0.9 for the 55 nm processes used. The choice of pixel sizes is driven by requirements of the future experiments. Preliminary design of the LHCb Upstream Tracker for Upgrade II assumes a pixel size of $50 \times 150\,\mu m^2$ to ensure the detector occupancy at a reasonable level. For the tracking detector at CEPC better spatial resolution is required in order to achieve desired momentum resolution, so smaller pixels of $25 \times 150\,\mu m^2$ are designed.

A typical array is shown in Fig. 2 (right). The middle two pixels can be read out individually, while the 10 pixels surrounding them are connected. The current–voltage curves for a single pixel or the 10 connected pixels are shown in Fig. 3. The breakdown voltage is around −9 V. The leakage current is as low as pA level before breakdown is reached.

The capacitance-voltage curves of a single pixel or 10 pixels are shown in Fig. 4. With offset subtracted, the capacitance of a single

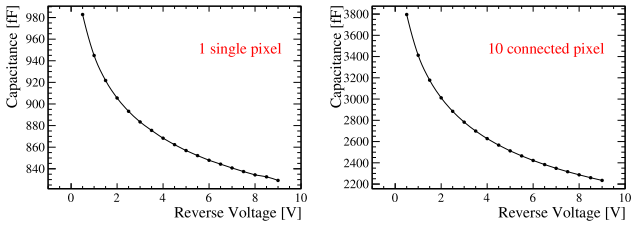

Fig. 4. The CV curves of (left) a single pixel and (right) 10 connected pixels.

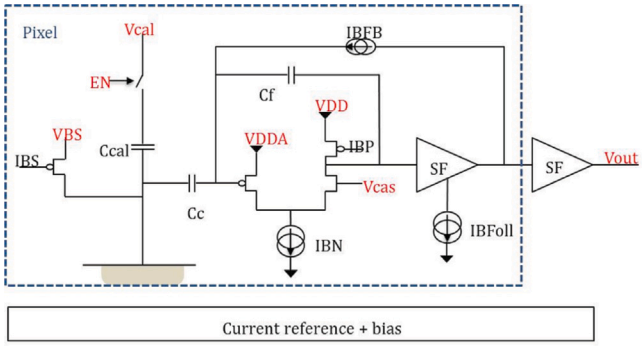

Fig. 5. Schematic design of in-pixel circuit in COFFEE1. VBS provides voltage to the sensor collection electrode through the PMOS transistor which implements active resistor controlled by IBS. The AC-coupled Charge Sensitive Amplifier (CSA) can be calibrated by integrated capacitor Ccal. The amplification stage of the CSA is based on the folded-cascode structure, and the feedback IBFB discharges the CSA with a constant current.

pixel of $25 \times 150\,\mu m^2$ is in the range of 150 ∼ 200 fF at the bias of −9 V, depending on the gaps between adjacent pixels.

Two pixel arrays are repeated on the right corner of COFFEE1, for which in-pixel circuits are implemented including charge sensitive amplifiers, source follower and charge injection. The schematics diagram is shown in Fig. 5.

As windows are left open in the metal layer for all diode arrays, we can use laser to study the signal response in the sensor when biased. The setup is illustrated in Fig. 6. A red laser with spot size around 0.5 mm is used. Ten connected pixels as shown in Fig. 2 are read out using an external charge sensitive preamplifier-shaper chip, IDE1140 [12] mounted on a custom-made readout board. The signal generated by the red laser is clearly visible comparing to the pedestal as shown in Fig. 6. The gain of the readout system is calibrated using other dedicated sensors and input sources, yielding one count of ADC corresponding to input charge of ∼ 87 e^-. Therefore the signal of 28 ADC counts in COFFEE1 indicates a total amount of ∼ 2400 e^- charge collected. The noise level of the readout system increases from 2.1 ADC to 3.8 ADC after connecting to the testing diode on COFFEE1, including contribution from noise in the sensor diode, the capacitance introduced by the connection and the instability of the laser. The frame rate capability of the readout system is estimated to be above 10 kHz, and the trigger rate was set to 500 Hz when performing the laser test to ensure there is no spill-over.

3. Design and test of COFFEE2

Following promising first results from COFFEE1, design of COFFEE2 was submitted to an MPW using HVCMOS process in 2023. The cross-section of the HVCMOS process is illustrated in Fig. 1. The process is a triple-well process, namely n-, p- and deep n-wells are available. Up to ten metal layers can be used for fine pitch routing, including two thick metal layers for power. In this MPW six metal layers are used including a thick metal layer for power lines.

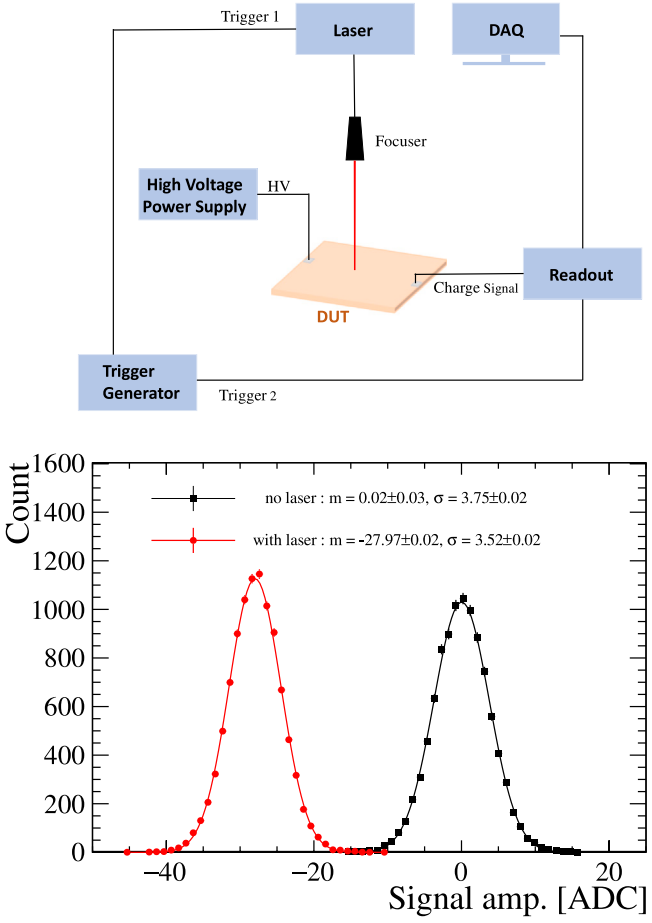

Fig. 6. Setup for laser test and signal generated in COFFEE1.

The floorplan and a photo of the COFFEE2 chip are shown in Fig. 7. The chip has an area of 4 mm × 3 mm.[1] There are three sections of different design purpose.

Section labeled "1" has a 32 × 20 pixel matrix with in-pixel circuit. Section "2" consists of passive diode arrays similar to COFFEE1. Pixels in both sections 1 and 2 have the same pixel sizes. The initial plan was to have pixels of $25 \times 150\,\mu m^2$ as the smaller pixels in COFFEE1; However this would be extremely challenging in the narrower side as a few micrometer of clearance has to be kept from the edge of the deep n-well, leaving no more than 10 μm in one side for the circuit. Therefore we adopted a less elongated pixel shape while keeping a similar pixel area, yielding a pixel size of $40 \times 80\,\mu m^2$. The schematic design of in-pixel electronics in Section "1" is shown in Fig. 8. A pixel consists of a charge-sensitive preamplifier (CSA) connected to the front-end collection electrode through AC coupling, a comparator via another AC coupling stage is connected to the output stage of the CSA. This arrangement ensures the transmission of the analog signal while isolating the different stages electrically. Only one pixel in the array can be read out at a time when the `column_select` and `row_select` are both selected. The variations in diode or in-pixel electronics in Section "1" include:

- Gaps between neighboring deep n-well are 10, 15 or 20 μm;
- With or without p-stop between pixels;
- Pixels with only amplifiers or with both amplifiers and comparators;

[1] All designed values are scaled down by a factor of 0.9.

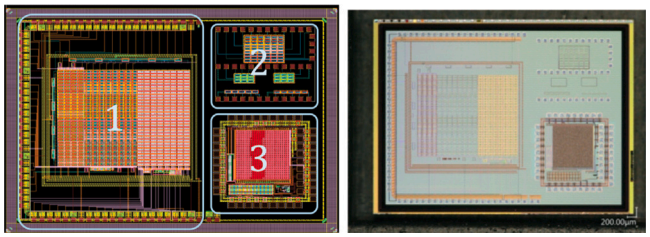

Fig. 7. COFFEE2 floorplan and photo.

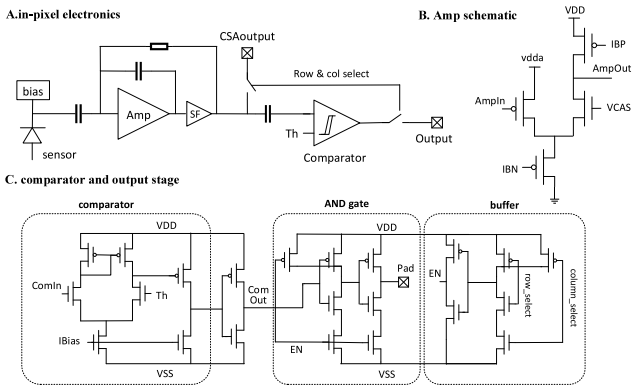

Fig. 8. The schematic diagram of in-pixel electronics in Section 1 of COFFEE2. In section A, the sensor generates a signal that is amplified by a charge-sensitive amplifier based on a gain stage (Amp) and a source follower (SF). The amplified signal, labeled as "CSAoutput", is fed into a comparator after AC coupling. The comparator, as depicted, converts the analog signal into a digital output, which is routed to the pixel's exterior. The digital signal output utilizes a shared output bus per column of pixels, with row and column select signals managing the address of the pixel to be read on the bus. Section B illustrates the amplifier (Amp) schematic. The amplifier uses "IBN" as current bias necessary for its operation. "VCAS" is a voltage bias signal. Section C shows detailed circuit elements in the comparator and output stage. The comparator processes the input signals "ComIn" and compares it with threshold reference "Th". The current bias is "IBias". The output of the comparator "ComOut" then passes through an AND gate and a buffer before reaching the external output pad. This configuration ensures robust digital signal readout controlled by enable signals "EN", and further facilitates the selection of rows and columns (row_select and column_select). ALL these bias signals are controlled externally from the array, allowing the amplifier to be tuned to its optimal operating point during testing.

- By default the comparators are implemented using both PMOS and NMOS, and in the left 4 columns comparators using only NMOS are designed. The NMOS-only design is aimed at mitigating possible crosstalk between deep n-well and n-well.

Section "3" was designed separately for imaging application. It has a 26 × 26 pixel matrix with digital readout periphery for novel electronics structure study. The pixel size is $25 \times 25\,\mu m^2$, and a 2 × 2 array forms a quad pixel unit. Out of the 26 columns, 24 columns have analog readout and 2 columns provide digital encoding of pixel address. The design and test of Section "3" will be detailed in other publications.

The IV curve of a typical diode in Section 2 is shown in Fig. 9. The breakdown voltage can be as large as −70 V. The increase of breakdown voltage of COFFEE2 with respect to COFFEE1 is due to the different CMOS process. The sudden increase of current beyond breakdown voltage may imply that the breakdown happens at the edge of the deep n-well. The leakage current is at a few pA level at low bias.

The capacitance as a function of bias voltage is shown in Fig. 10 for a single pixel and for 8 connected pixels. Full depletion is not reached when breakdown happens. The capacitance should be proportional to pixel area; however offset exists due to various reasons, for instance the parasitic capacitance of metal routing. We take the derivative of the CV curves and extract the ratio of 8-pixel versus a single pixel to eliminate the offset, and the ratio agrees well with eight, the ratio of their area,

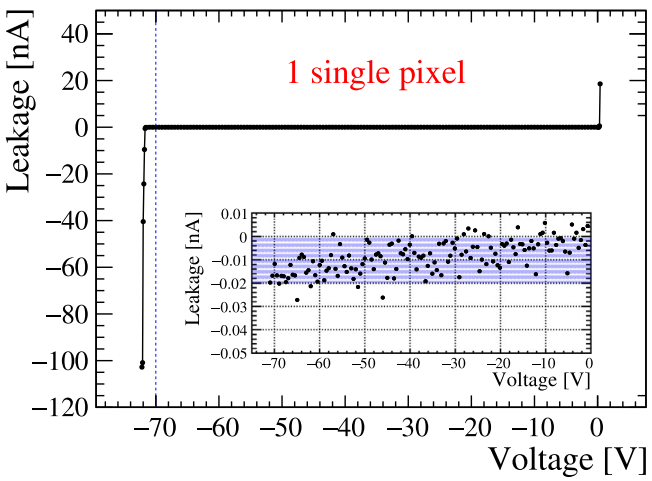

Fig. 9. IV curve of a pixel in COFFEE2 chip.

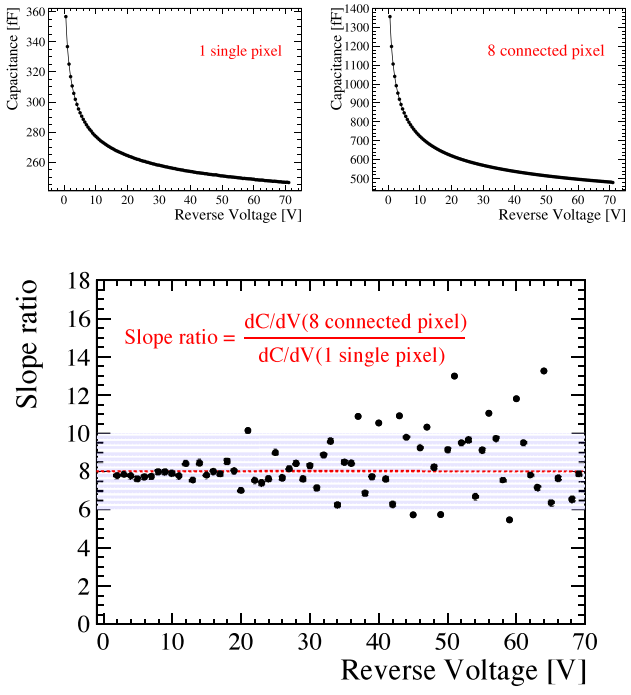

Fig. 10. CV curves of (top left) a pixel or (top right) 8 connected pixels in COFFEE2 chip. (Bottom) The ratio of capacitance of 8-pixel with respect to 1 pixel as a function of reversed bias.

as shown in Fig. 10. The raw capacitance of a single pixel at −70 V is ∼ 200 fF, which becomes 30 ∼ 40 fF after subtracting the offset.

More tests on COFFEE2 are expected. Dedicated readout boards are being designed and fabricated to allow tests with radioactive sources. Based on the current results more MPWs are planned using the 55 nm HVCMOS process in the future. In order to demonstrate the technology is a viable option for LHCb Upgrade II or CEPC tracker, we plan to implement the array readout scheme which will allow readout at 40 MHz.

4. Summary

Two chips, COFFEE1 and COFFEE2, are designed and fabricated in 55 nm low-leakage process and the HVCMOS process, respectively. The passive sensor diode in COFFEE1 is responsive to laser signal. The IV curve of COFFEE2 shows a high breakdown voltage up to −70 V. More characterization on the sensors will be carried out and further development on the 55 nm HV-CMOS process is foreseen for future tracking detectors in particle physics.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Yiming Li reports financial support was provided by National Natural Science Foundation of China. Yiming Li reports financial support was provided by National Key Research and Development Program of China. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was partially supported by the National Key Research and Development Program of China under Grant number 2023YFA1606300, the National Natural Science Foundation of China (NSFC) under Grant numbers 11961141015, 12188102 and 12175245, and the Chinese Academy of Sciences (CAS).

References

[1] W. Snoeys, CMOS monolithic active pixel sensors for high energy physics, Nucl. Instrum. Methods A 765 (2014) 167–171, http://dx.doi.org/10.1016/j.nima.2014.07.017.
[2] R. Turchetta, et al., CMOS monolithic active pixel sensors (MAPS): Developments and future outlook, Nucl. Instrum. Methods A 582 (2007) 866–870, http://dx.doi.org/10.1016/j.nima.2007.07.112.
[3] I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, Nucl. Instrum. Methods A 582 (2007) 876–885, http://dx.doi.org/10.1016/j.nima.2007.07.115.
[4] I. Mandić, et al., Neutron irradiation test of depleted CMOS pixel detector prototypes, JINST 12 (02) (2017) P02021, http://dx.doi.org/10.1088/1748-0221/12/02/P02021, arXiv:1701.05033.
[5] I. Peric, et al., High-Voltage CMOS Active Pixel Sensor, IEEE J. Solid State Circ. 56 (8) (2021) 2488–2502, http://dx.doi.org/10.1109/JSSC.2021.3061760.
[6] H. Augustin, I. Perić, A. Schöning, A. Weber, The MuPix sensor for the mu3e experiment, Nucl. Instrum. Methods A 979 (2020) 164441, http://dx.doi.org/10.1016/j.nima.2020.164441.
[7] C. Bespin, et al., DMAPS monopix developments in large and small electrode designs, Nucl. Instrum. Methods A 978 (2020) 164460, http://dx.doi.org/10.1016/j.nima.2020.164460, arXiv:2006.02297.
[8] P. Sieberer, C. Zhang, T. Bergauer, R.C. Mohr, C. Irmler, N. Karim, J.M. de Cos, B. Pilsl, E. Vilella, RD50-MPW3: a fully monolithic digital CMOS sensor for future tracking detectors, JINST 18 (02) (2023) C02061, http://dx.doi.org/10.1088/1748-0221/18/02/C02061, arXiv:2211.11244.
[9] S. Bugiel, et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, Nucl. Instrum. Methods A 1040 (2022) 167213, http://dx.doi.org/10.1016/j.nima.2022.167213.
[10] LHCb collaboration, Framework TDR for the LHCb Upgrade II: Opportunities in flavour physics, and beyond, in the HL-LHC era, Tech. rep, 2021.
[11] M. Dong, et al., CEPC conceptual design report: Volume 2 - physics & detector, 2018, arXiv:1811.10545.
[12] IDE1140. URL https://ideas.no/products/ide1140/.