The CEPC Clock

The definition and boundaries

- From the detector standpoint, the CEPC clock is the accelerator clock **that is delivered** to the detector electronics system. This clock, and the phase locked copies (multiplied or divided), are used to clock the whole digital circuits in the system.
- From the CEPC accelerator, the minimum bunch spacing is based on a clock that is nominally 130 MHz. The bunch spacing for the four running modes at different SR energies are in the following table:

SR 30 / 10 MW	H	Z		W	$t\bar{t}$
SR power per beam [MW]	30	30	10	30	30
Bunch number	268	11,934	3,978	1,297	35
Bunch spacing* [ns]	576.9	23.1	69.2	253.8	4523.1
[× 23.1 ns]	25	1	3	11	196
Train gap [%]	54	17	17	1	53
Luminosity/IP [$\times 10^{34}cm^{-2}s^{-1}$]	5.0	115	38	16	0.5

SR 50 MW	H	Z	W	$t\bar{t}$
SR power per beam [MW]	50			
Bunch number	446	13,104	2,162	58
Bunch spacing* [ns]	346.2	23.1	138.5	2700.0
[×23.1 ns]	15	1	6	117
Train gap [%]	54	9	10	53
Luminosity/IP [$\times 10^{34}cm^{-2}s^{-1}$]	8.3	192	26.7	0.8

- What is **very important** for the electronics system is that all the bunch spacing numbers are **INTERGER MULTIPLS of one base number**, which in the table is nominally 23.1 ns, or the period of the 43.3 MHz (130MHz/3) clock.

This was agreed upon in the Luo-Yang meeting, an update from the accelerator TDR.

Summary of the discussions in the electronics group

- The question: the base clock being 43.3MHz (130MHz/3) or 65MHz (130MHz/2)? We used one of the Thursday meetings (https://indico.ihep.ac.cn/event/23467/) to come to a consensus.
- We choose the 43.3MHz (130MHz/3) clock. We only require that the four running modes in each SR energy (8 combinations) each has a bunch spacing that is an integer multiple of the minimum spacing time.
- The main reasons (technical):
  - Electronics power consumption increases with clock frequency.
    - When the bunch spacing (23.1ns→15ns) shortens, the peak time of some analog circuit's needs to speed up, results in higher power consumption
      - e. g. TaichuPix, power may increase by a factor of 2
  - Faster clocks results in larger data volume & higher ambiguity during track reconstruction
    - Speed of the detector is limited, larger trigger error window needs to be applied (large data volume), and more overlapped events due to more bunches within one frame (reconstruction difficulty)
  - Timing sequence already sees some limit closed to 25ns
    - Large pixel chips, esp. in VTX & ITK, suffers from parasitics due to the long wire (R & C), impact to the timing sequence, and cannot gain much by using advanced technology node (180nm →65nm）
      - e. g. TaichuPix, already sees some bordering of 25ns for 40MHz clock

Summary of the discussions in the electronics group

- Other consideration:
  - All LHC chips are based on the 40MHz (nominal) base frequency, 43.3MHz is close, the circuits and transmission protocols may be compatible.
  - It's likely that we will not be able to directly use chips developed for LHC, but it is possible that international collaborators join our chip design, and their experiences are mostly based on 40MHz
    - To announce a different clock frequency (65MHz), it may discourage many collaborators from joining our design effort.
  - For an engineering project, it is important to have parallel schemes & cross-check. To have similar frequency, it can:
    - Enable cross-use some LHC chips in our detector R&D, to form a performance comparison for our production chips.
    - Save the effort for parallel schemes, avoiding the failure based on a single scheme.

Backup Slide

Sensors, ASICs and Optical Module for the CEPC Detector

名称	类别	描述	最可能来源	国际合作概率	国际目标芯片
ChiTu（赤兔）	通用电子学	For the Detector Data Link (DDL)	自研	芯片: 低 传输协议：高	lpGBT
KinWoo（金乌）	通用电子学	Optical Module, and ASICs	自研	芯片：低 光模块：中	VTRx
TaoTie（饕餮）	通用电子学	数据汇总ASIC	自研	很低（需定制）	GBTx、HCC
BaSha（霸下）	通用电子学	DC-DC电源模块	自研或国产商用	低	bPolx，FEAST
Taichu-stch（太初-缝合版）	VTX	顶点探测器-Stitching	自研	中	ALICE-ITS3
COFFEE	ITK	Tracker	自研	中到高	ATLASPIX3
TEPIX-TPC版	TPC	Pixel TPC前端	自研	高	Gridpix（Timepix3）
OTK-ROC	OTK	LGAD-TOF	自研	很低（需定制）	ALTIROC
SiPM-ROC	SiPM通用前端	ECAL, HCAL, Muon通用前端	自研	(很)高	HGCROC、SPIROC