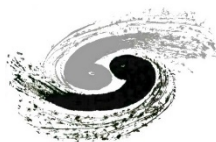


Pixel-based endcaps for CEPC silicon inner tracker

LI Yiming, XIA Tianji (夏天霁)
On behalf of the HVCMOS R&D team



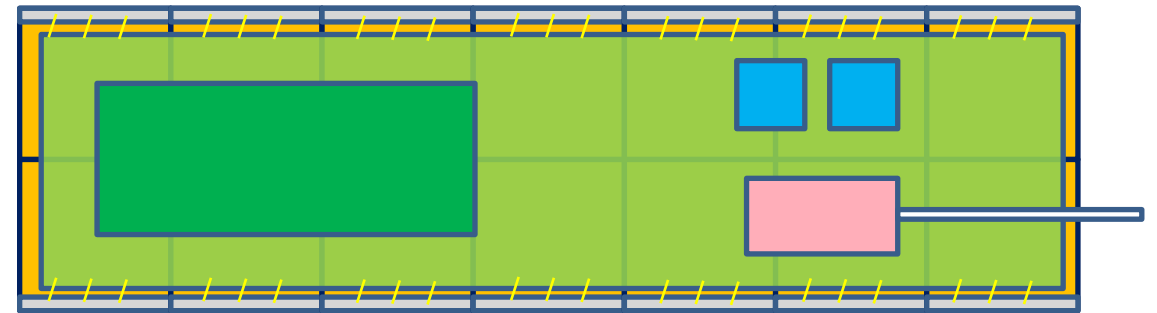
中國科學院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

- **Sensor chip and modules**
- **Ring-based endcap design**

Chip and modules for barrel

- COFFEE<N>: 20*20 mm²
 - Pixel size: 34 um * 148 um; array size: 512 row * 128 col
- Modules consisting of 7 pairs of chips
- Ideas for endcap design: as many common modules as possible



BaSha: DC-DC, 50 * 20 mm² * 6.7mm

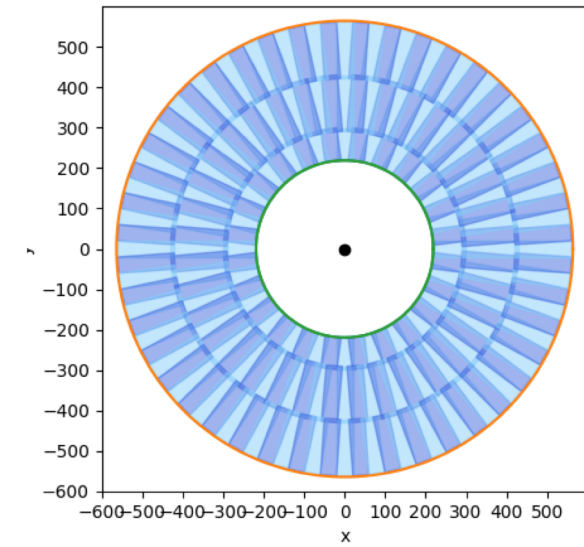
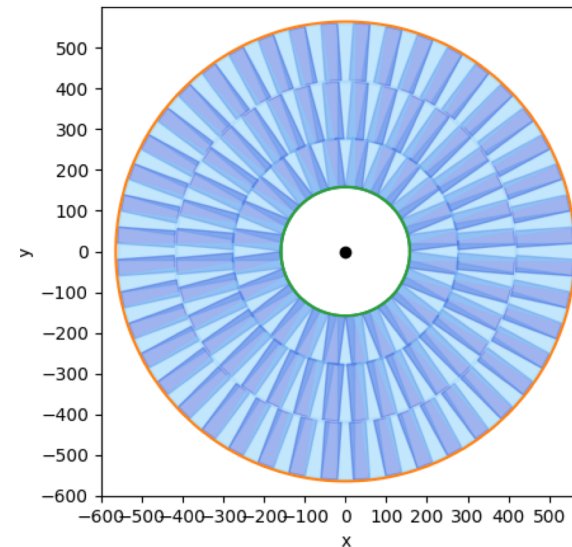
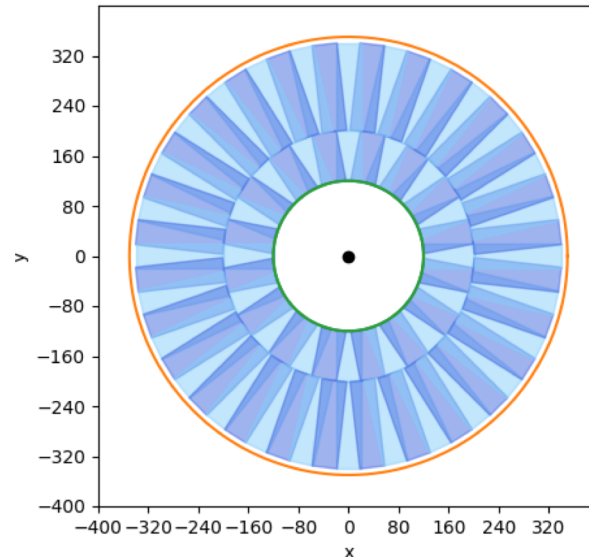
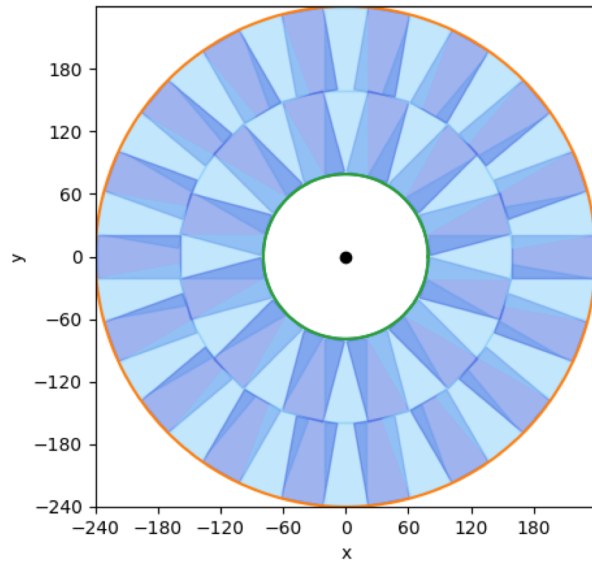
ChiTu & TaoTie: data aggregation, 9 * 9 mm²

KinWoo: optical conversion, 10 * 20 mm² * 3mm

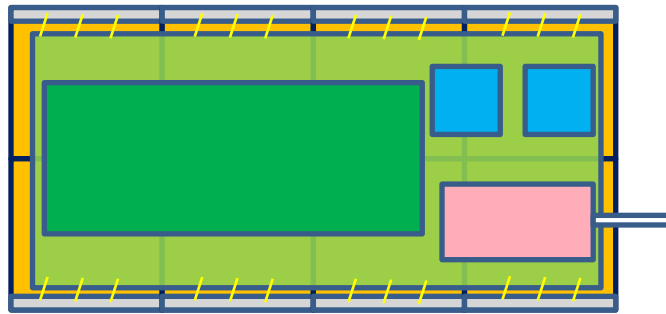
Ring-based endcap design (preliminary)

ring1 + ring2 (+ring3)	4+4	4+7	6+7+7	4+7+7		
R-innermost [mm]	79	114.4	158	219	"4" : 40.01 * 80.03 mm ²	92
R-outermost [mm]	240	350	564	564	"6" : 40.01 * 120.03 mm ²	48
					"7": 40.01 * 140.06 mm ²	376
# modules in ring1	24	32	48	48		
# modules in ring2	36	56	72	72		
# modules in ring3			88	88		

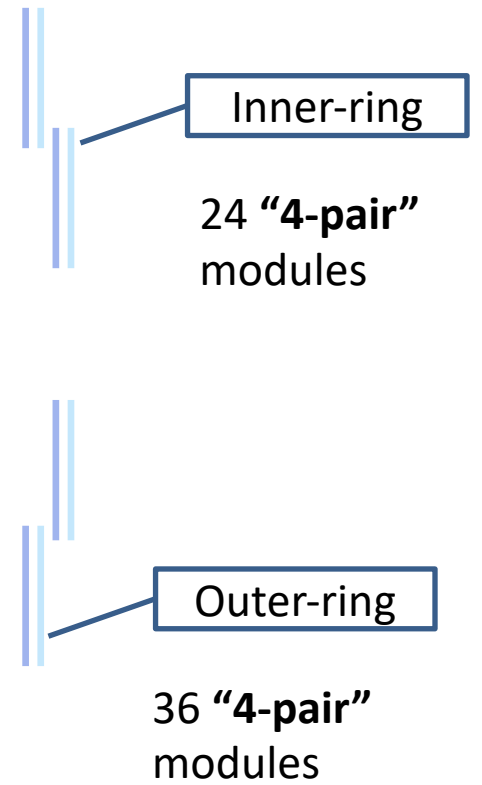
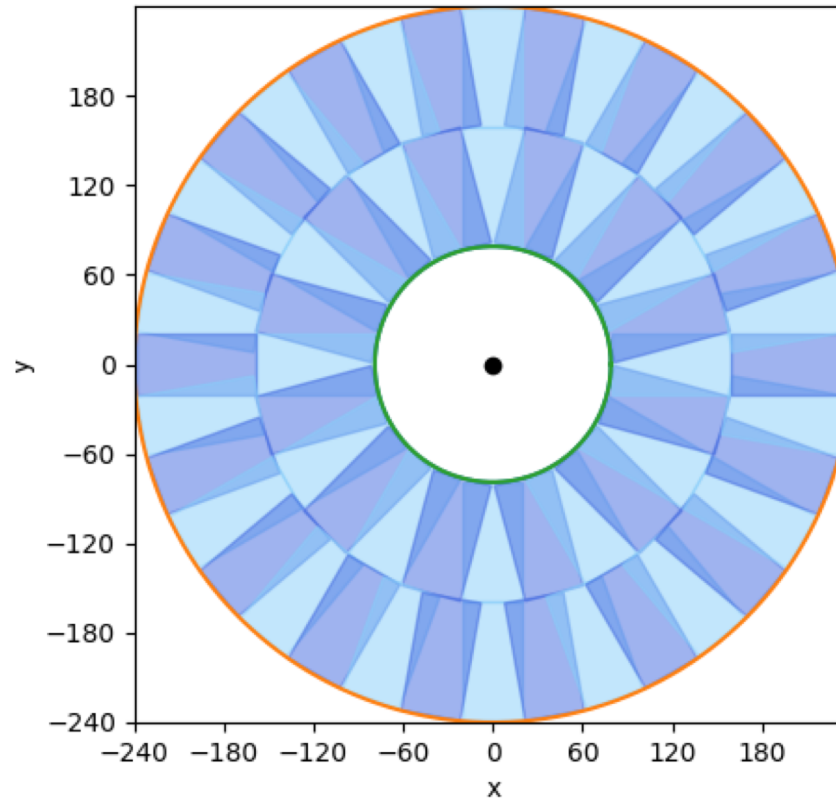
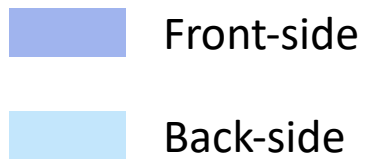
 Front-side
 Back-side



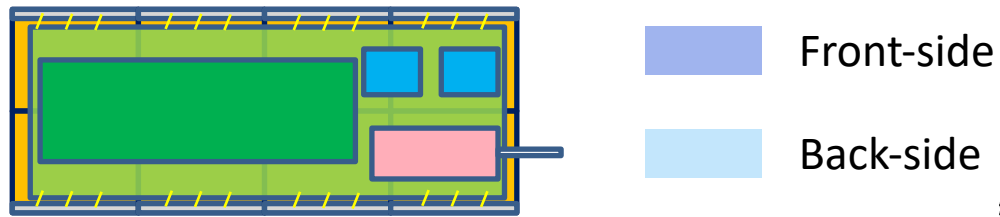
ITKE1



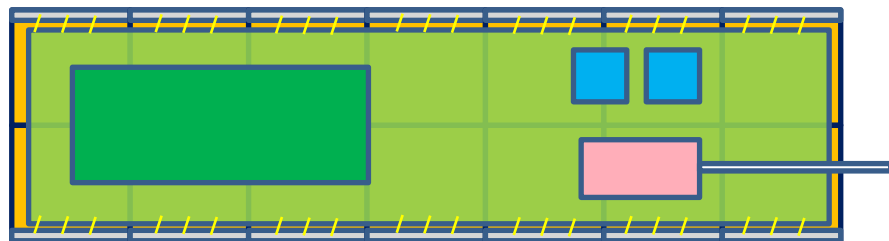
4*2-chip module



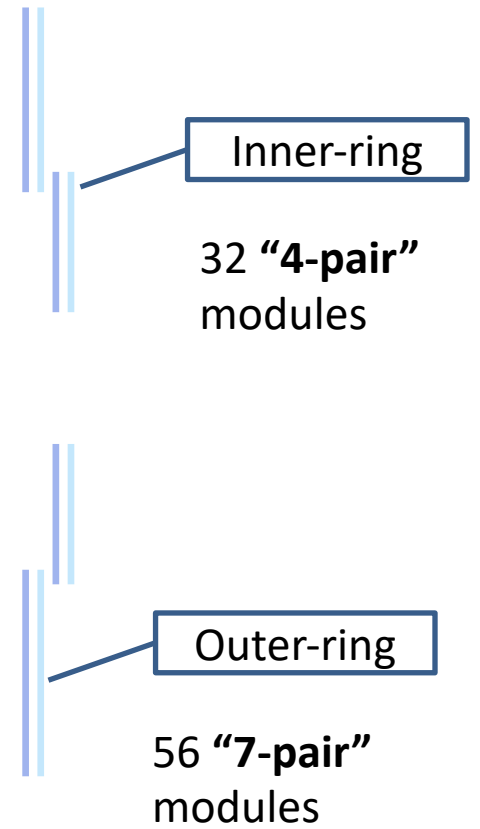
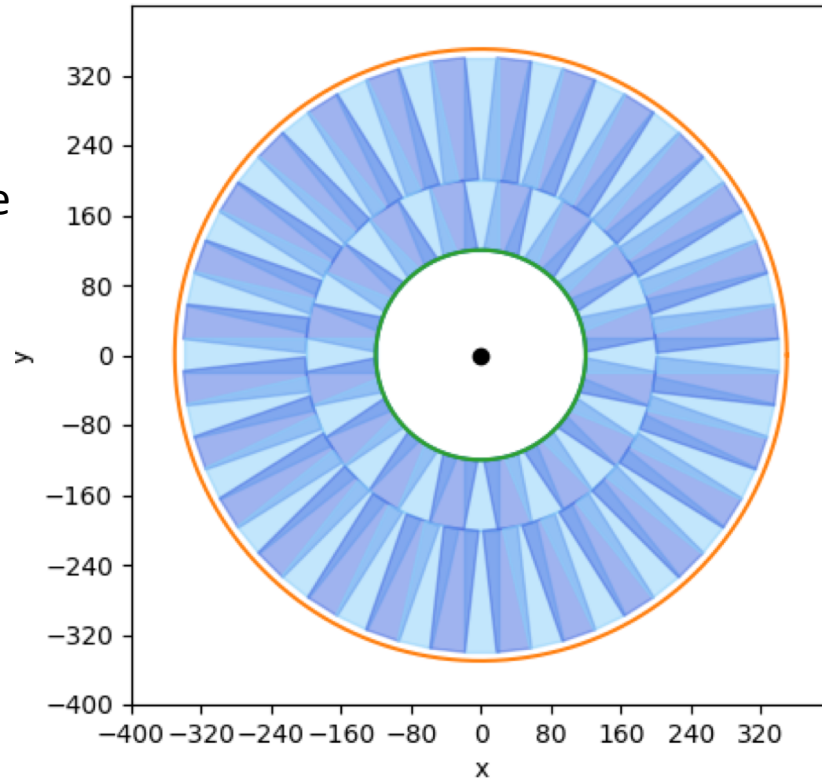
ITEK2



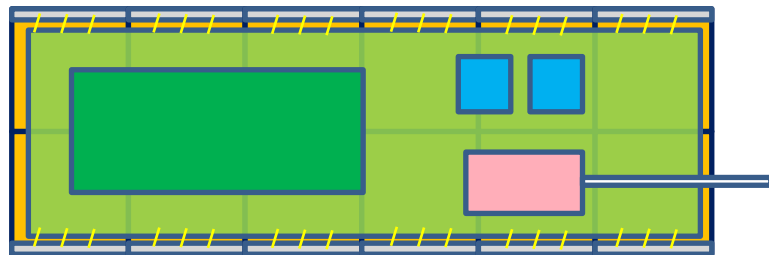
4*2-chip module



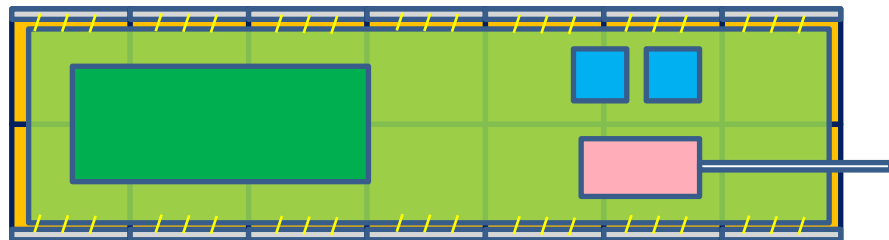
7*2-chip module



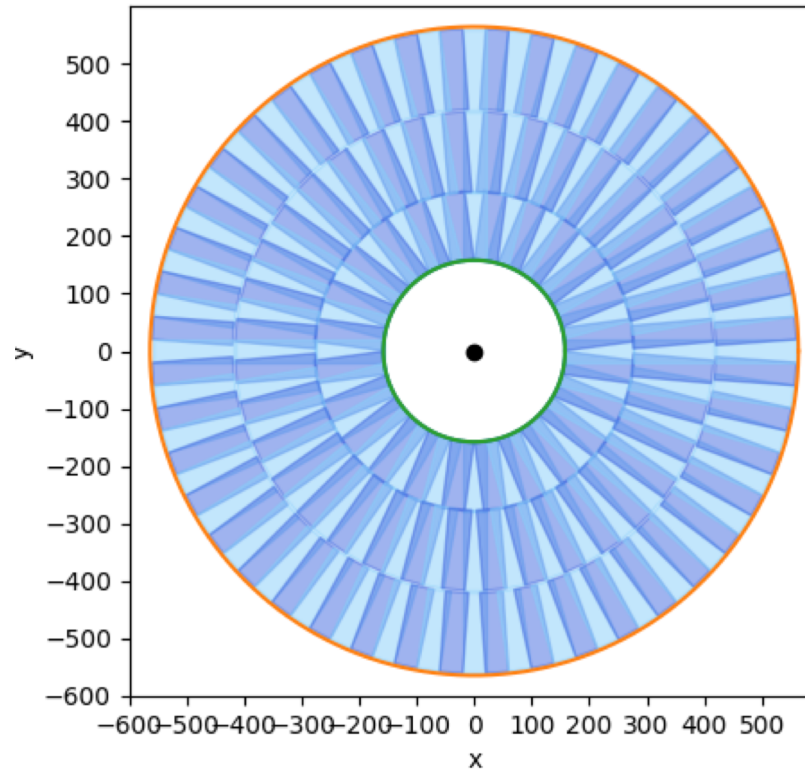
ITEK3



6*2-chip module

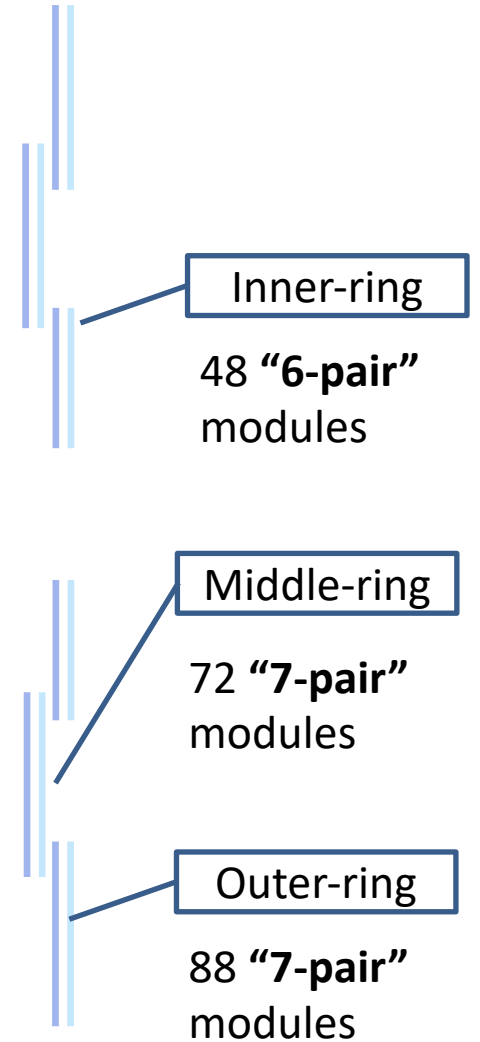


7*2-chip module

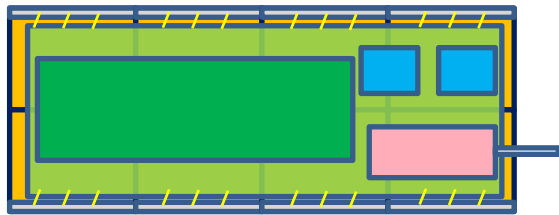


Front-side

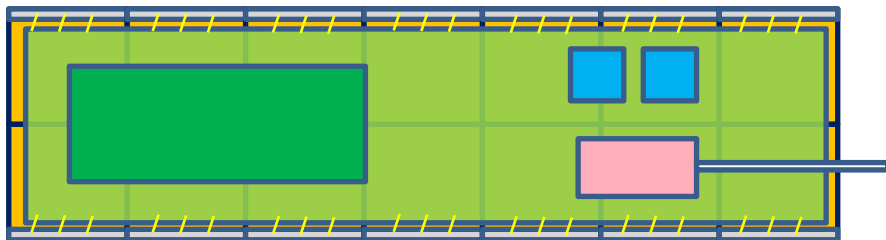
Back-side



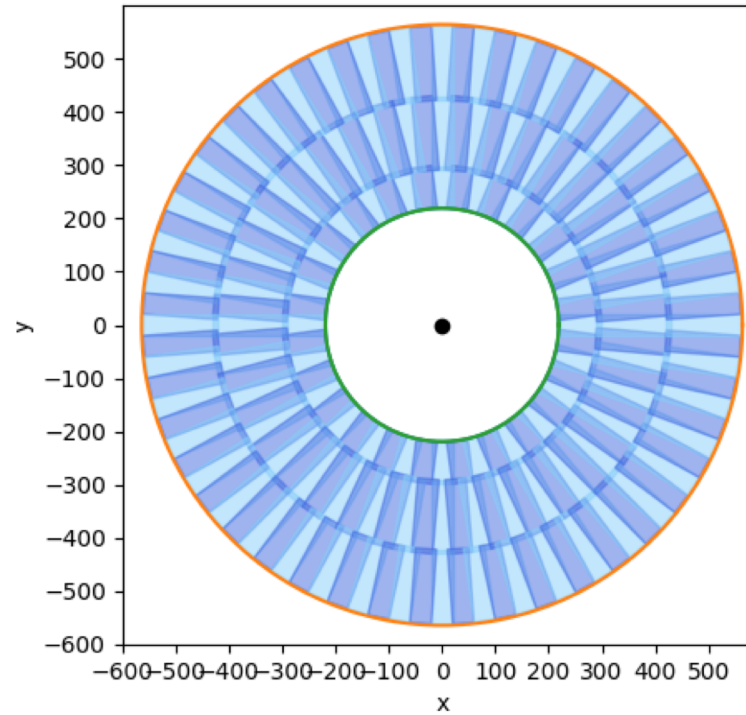
ITEK4



4*2-chip module

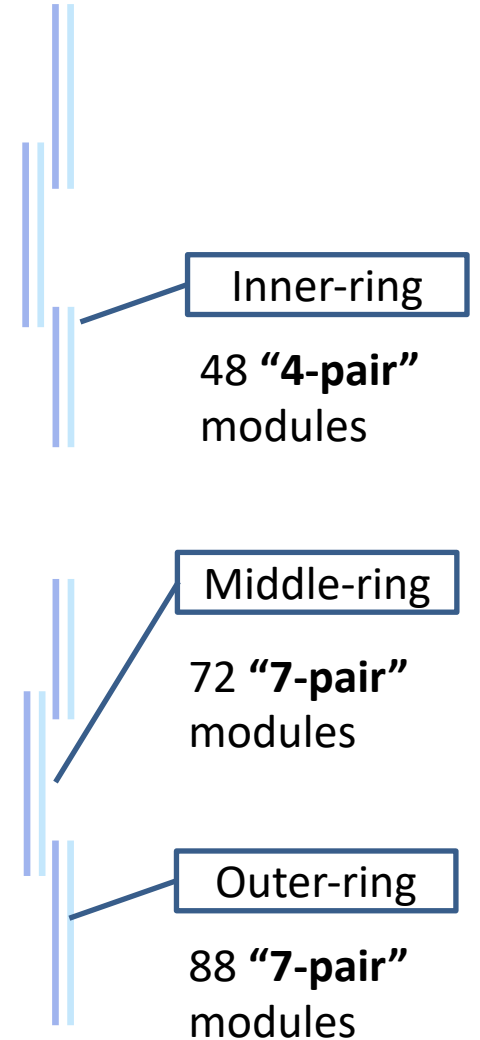


7*2-chip module



Front-side

Back-side

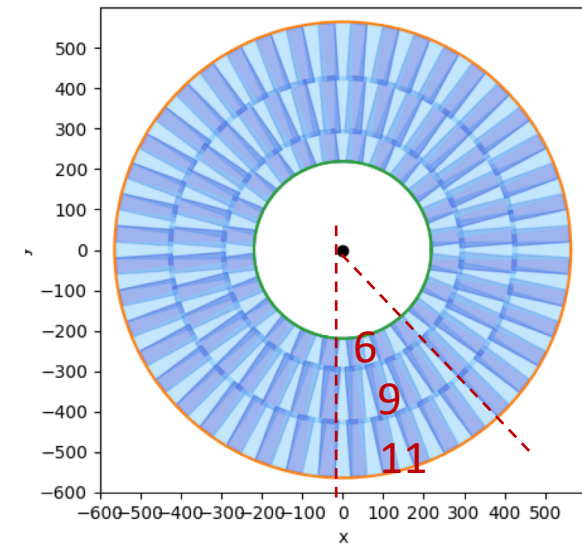
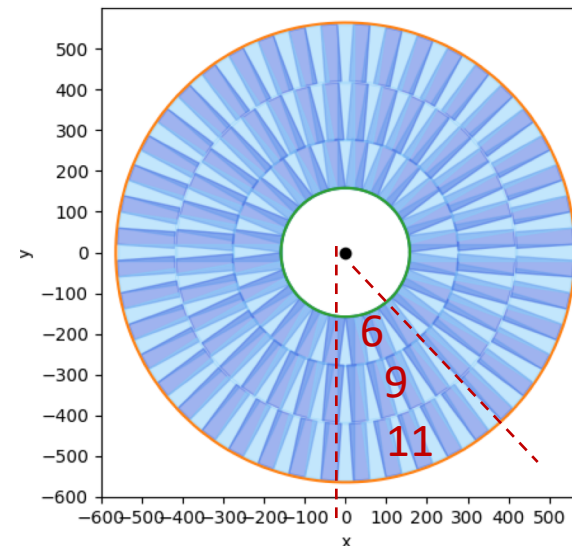
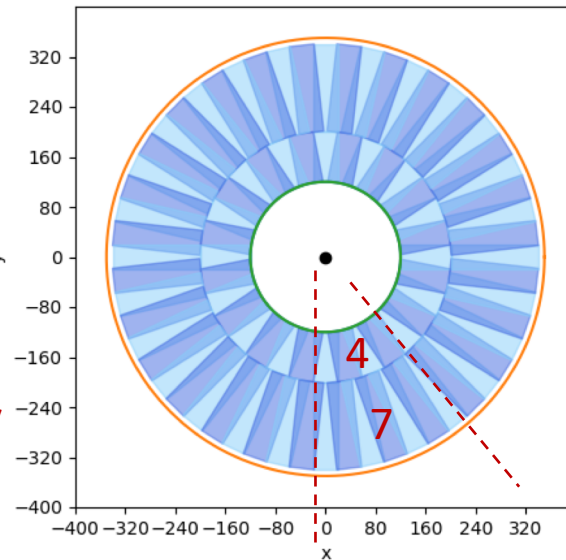
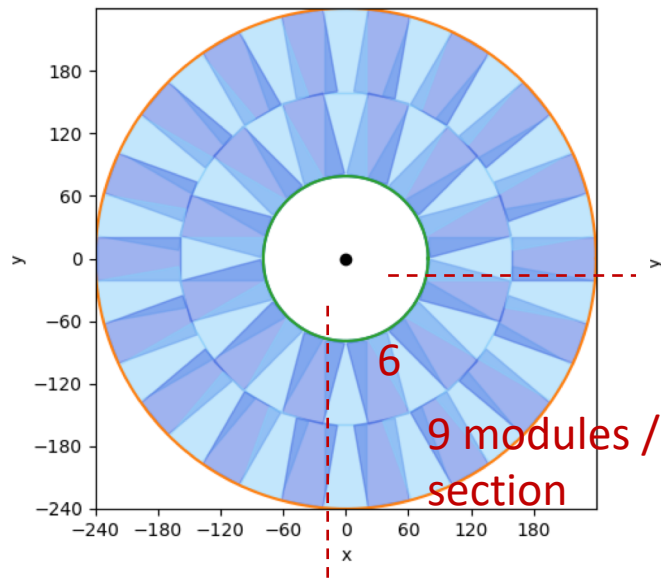


Ring-based endcap design (preliminary)

ring1 + ring2 (+ring3)	4+4	4+7	6+7+7	4+7+7		
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# modules in ring1	24	32	48	48		
# modules in ring2	36	56	72	72		
# modules in ring3			88	88		

Front-side
 Back-side

3 types of modules, one of which shared with the barrel;
 516 modules, 6576 chips in total



Division into 8 or 4 sections possible