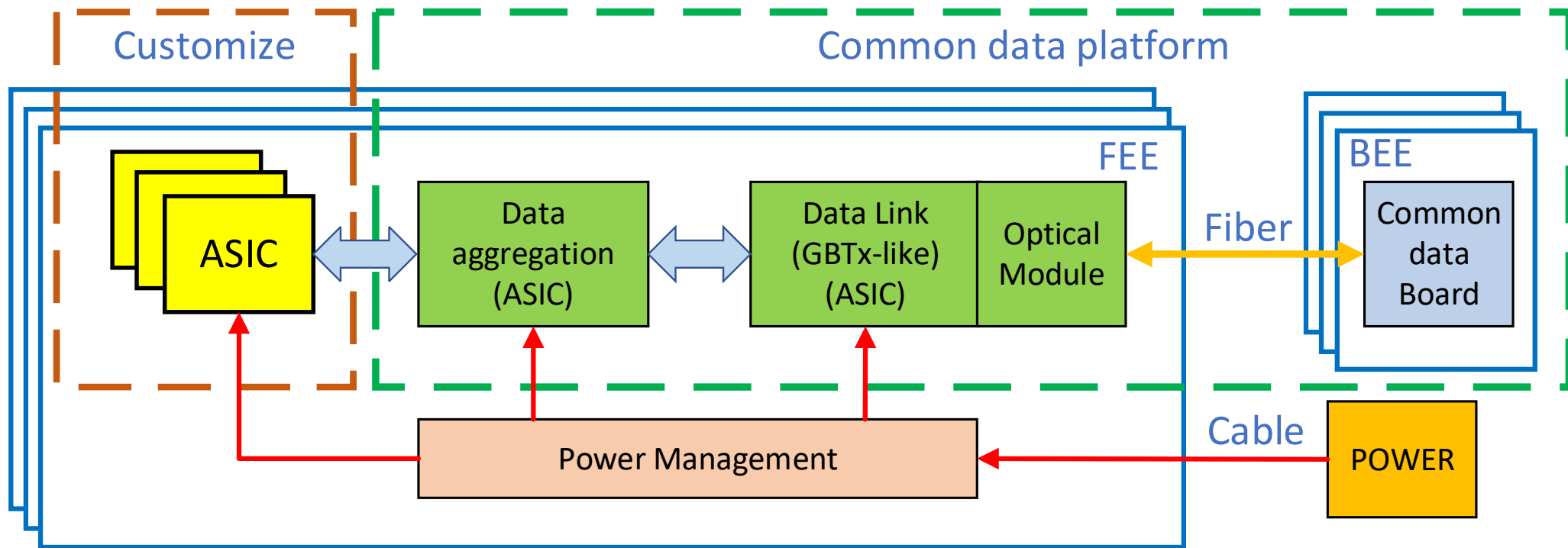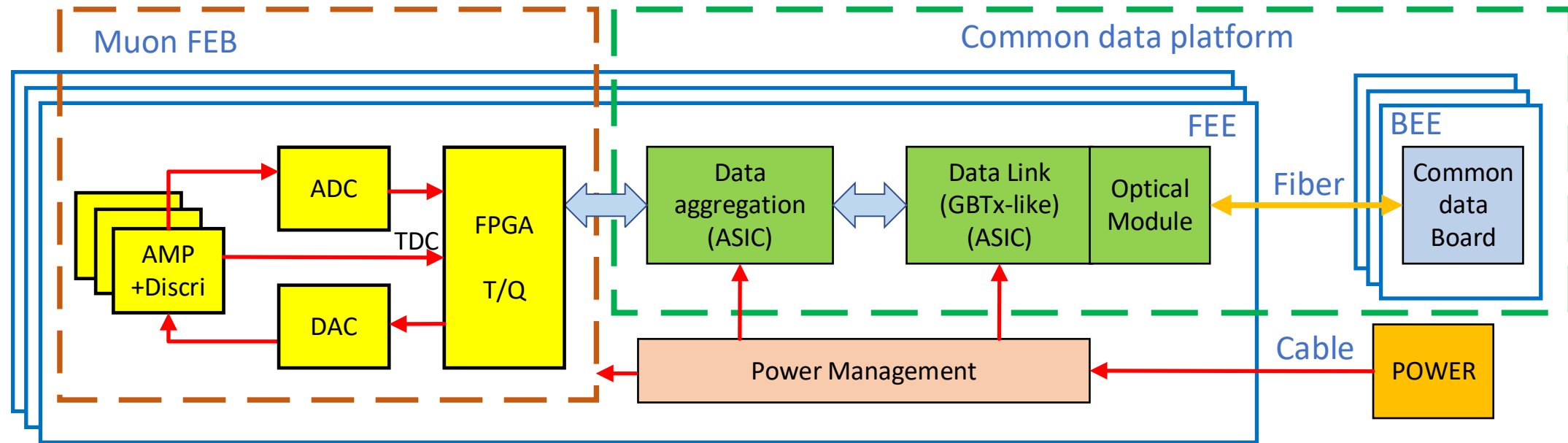# Baseline for SiPM readout

- Reuse the ASIC scheme from ECAL or HCAL
- Revise according to the constraints from cooling and mechanical structure of the detector

Alternative: discrete device scheme

- **FEB (Front-end Electronics Board)**

  - Commercial chips with radiation tolerance based on past studies for particle physics experiments
  - FPGA based TDC for TOA and TOT measurement with ~1 ns time resolution
  - ADC for charge measurement or TOT calibration
  - DAC for threshold setting or SiPM bias voltage adjustment

Near-term test environment
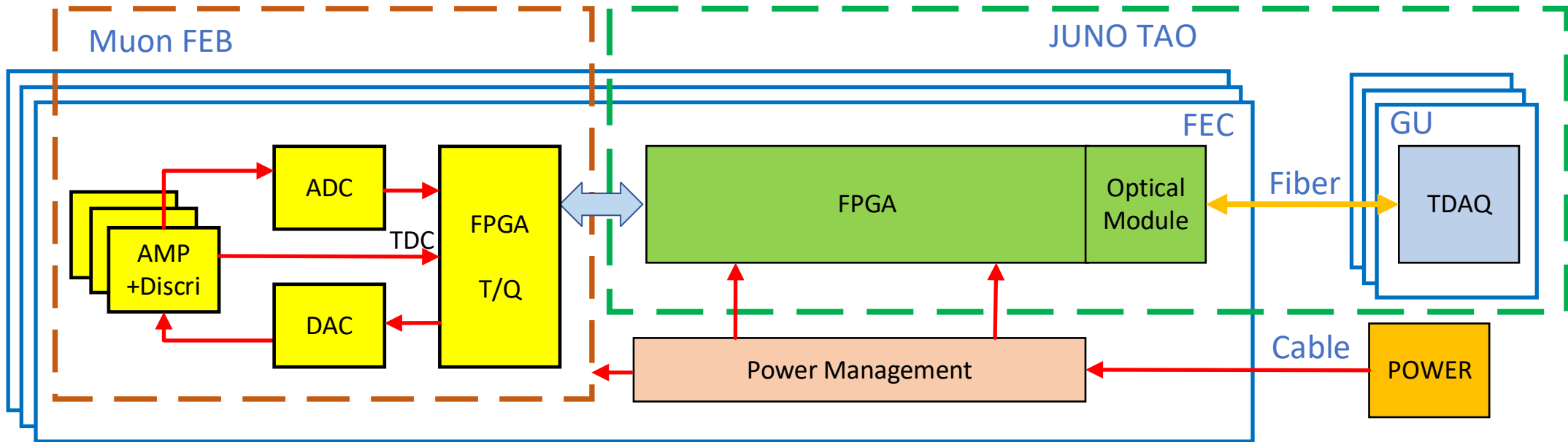
- Reuse JUNO-TAO electronics for readout, clock synchronization and TDAQ
  - To accelerate the development schedule