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Study of SEU Effects and Mitigation Measures for Kintex UltraScale FPGA using CSNS Neutron Beam Lines

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The damage effect caused by high energy particles, especially Single Event Upset (SEU), is one of the major factor of failure in SRAM-based FPGA components, for applications in harsh radiation environments, such as space-borne payloads and ground-based large scale particle experiments. With the advancement of the integrated circuit industry, in nowadays the feature size of high-performance FPGAs has entered the scale of nanometers, making SEU effects increasingly severe.
Traditionally, the evaluation of single-event effects (SEE), as well as the verification of mitigation measures, mainly rely on heavy ion beam testing, which has been regarded as the gold standard in the past years. However, the operation of SEE testing using heavy ion beam is relatively complex and expensive. Moreover, the availability of heavy ion beam facilities is limited, conflicting with the rising demand of chip testing and verification.
During the past several years, the presenter ' s team has been cooperated tightly with the CSNS Back-n group, to conduct research on radiation-hardening and high-reliability design methodologies for high-performance FPGA devices, using neutron beam lines. We employed neutron time-of-flight (TOF) methodology to characterize the correlation between single-event upset (SEU) cross-section (in BRAM and CRAM) and incident neutron kinetic energy in a Kintex UltraScale FPGA device, which is a representative high performance SRAM-based FPGA with 20 nm CMOS technology. Radiation-hardening measures for SEU mitigation were designed and experimentally validated, as well. The results have been published in the IEEE TNS and JINST journals.
The project will be further extended in future. Our hope is to systematically investigate the energy-dependent correlation between incident neutron kinetic energy and recoil ion's linear energy transfer (LET), both by Monte Carlo simulation for CMOS devices and by carrying out more experiments. We hope providing theoretical foundations for domestic radiation effects evaluation infrastructure development. Our ultimate goal is to establish an effective and systematic methodology for the research and evaluation of SEU in high-performance FPGA devices.

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