



# CEPC vertex Detector

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*Institute of High Energy Physics*  
*Chinese Academy of Sciences*

# Status of Software for Stitching Vertex Detector

## Geometry

- TaiCHu → STITCHing → composite (TCH+STT)

## Reconstruction

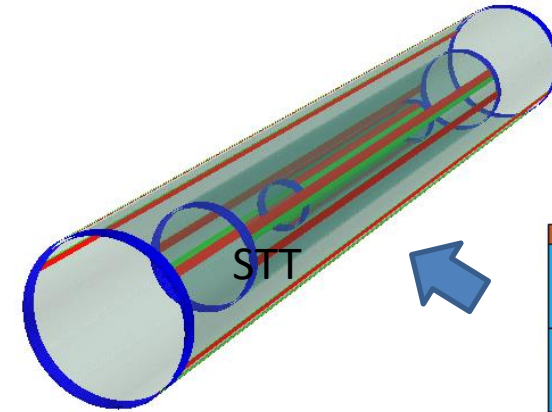
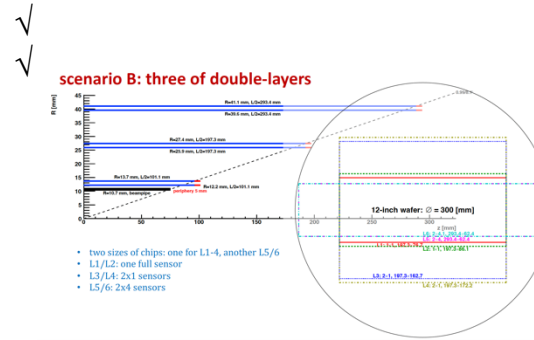
- Planar measurement → Cylinder measurement
- Processor for STT

## Validation

- STT VS TCH on three of double-layers

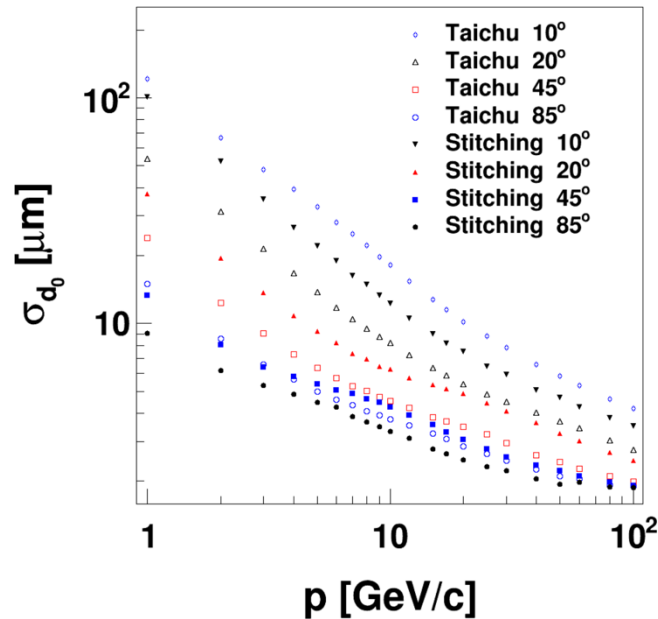
## Todo

- Reconstruction on STT+TCH
- Performance & layout

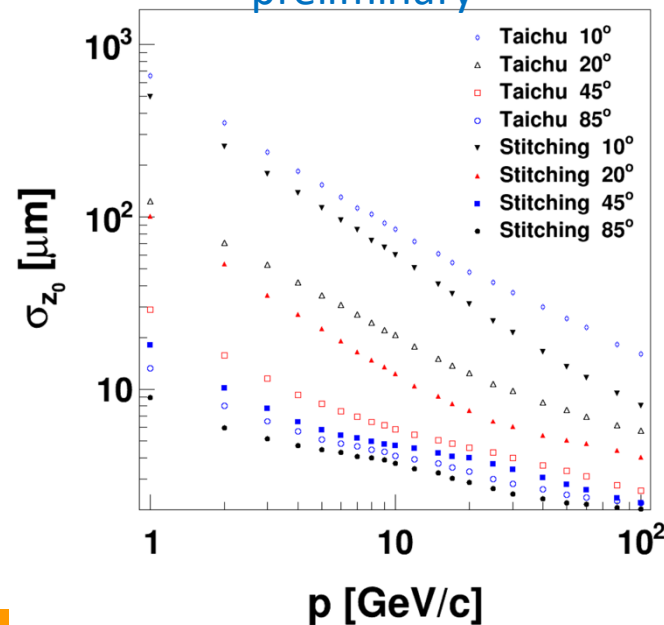


TL	Electronics	Electronics	Electronics	TR
L-drive	r by s PIXELS	r by s PIXELS	r by s PIXELS	R-drive
L-drive	r by s PIXELS	r by s PIXELS	r by s PIXELS	R-drive
BL	Readout	Readout	Readout	BR

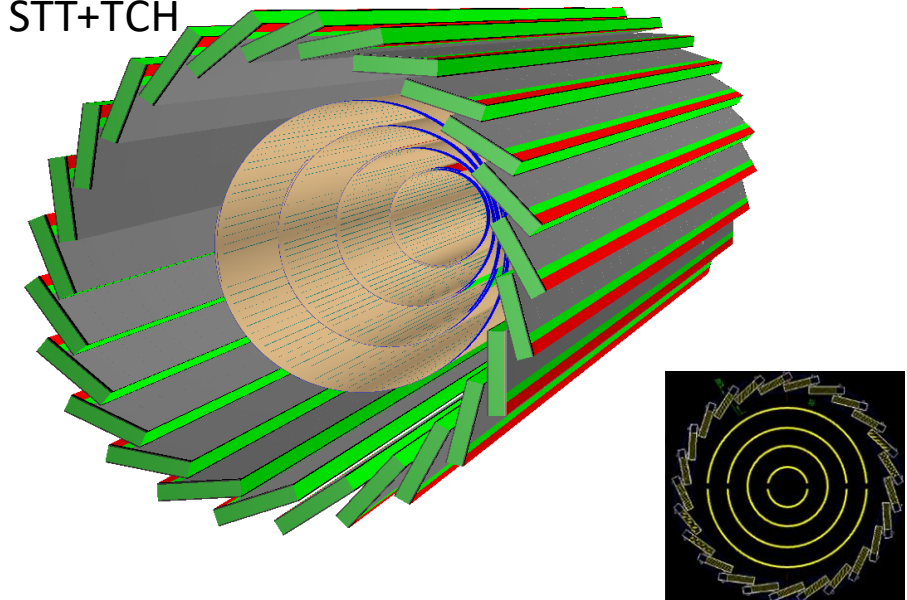
preliminary



preliminary



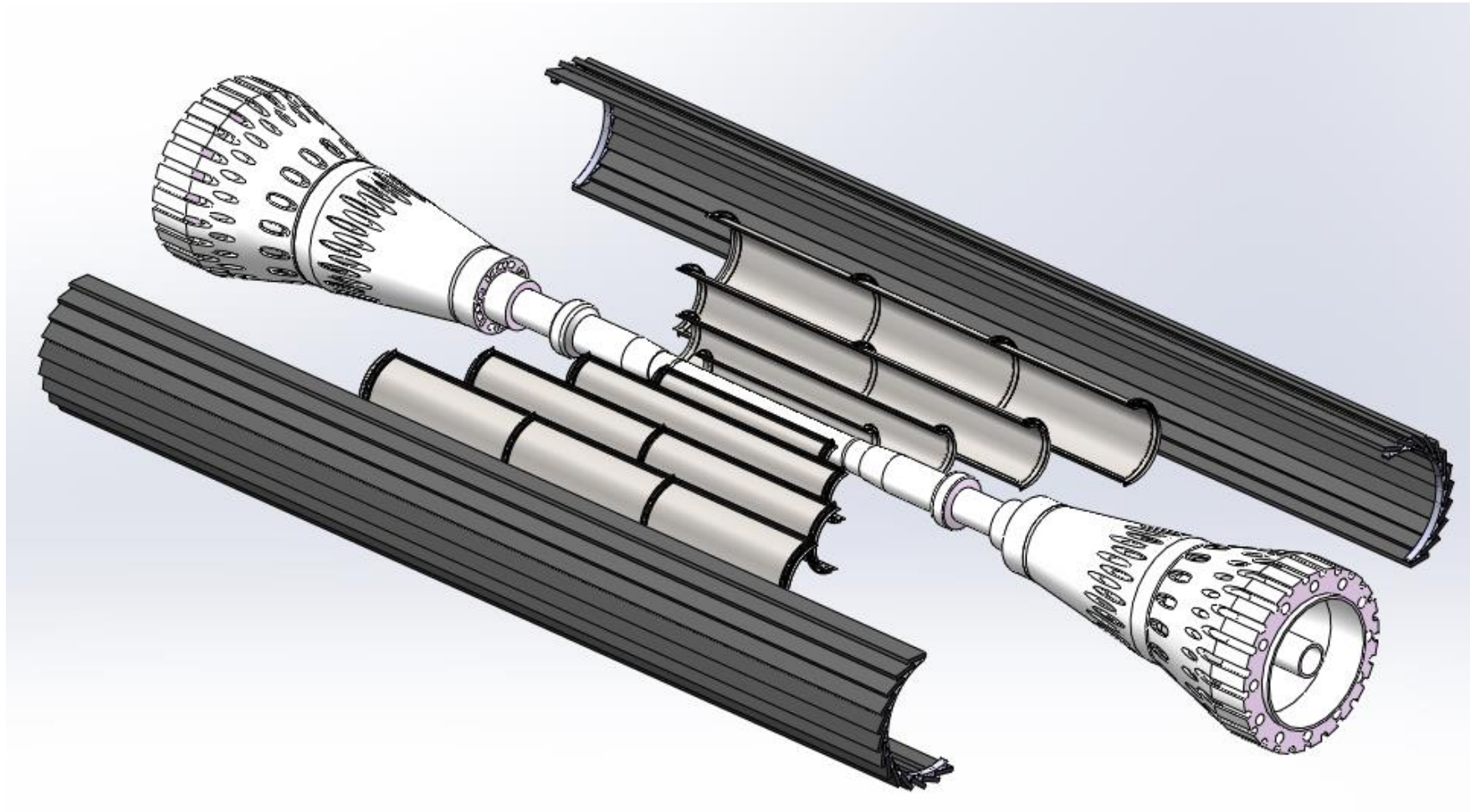
STT+TCH



# Mechanics update

By Jinyu

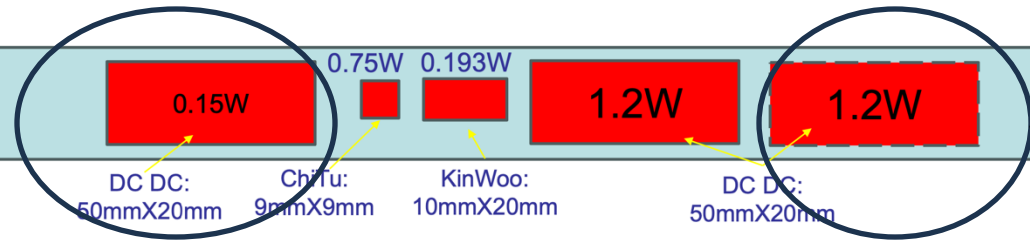
- Support structure update



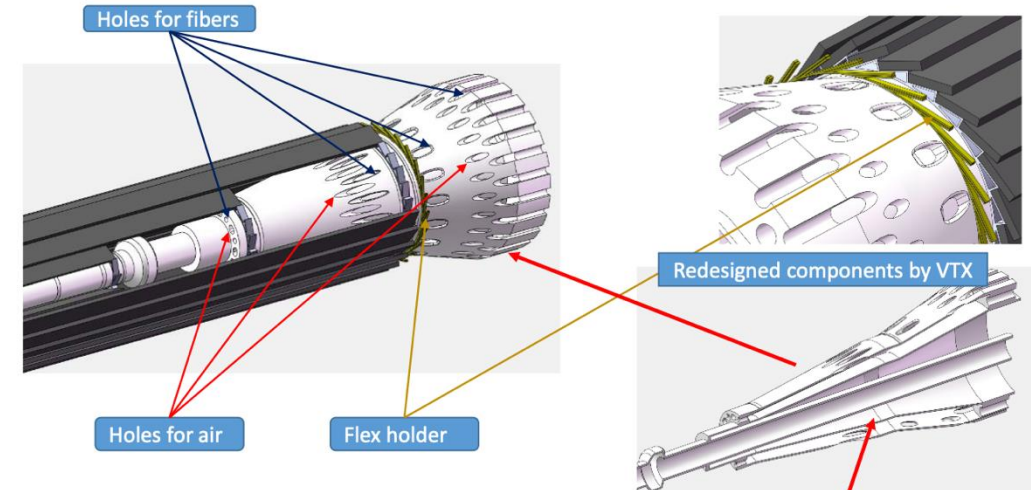
# Vertex technologies: Cable and service

## ■ Revisit the space in MDI region for cable and service

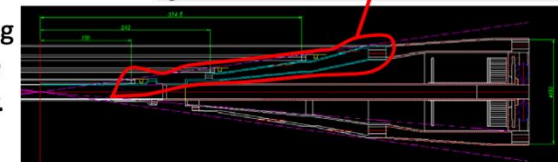
- Working to optimize the dimension on flexible PCB and components



Two DC-DC components can be removed in inner layers



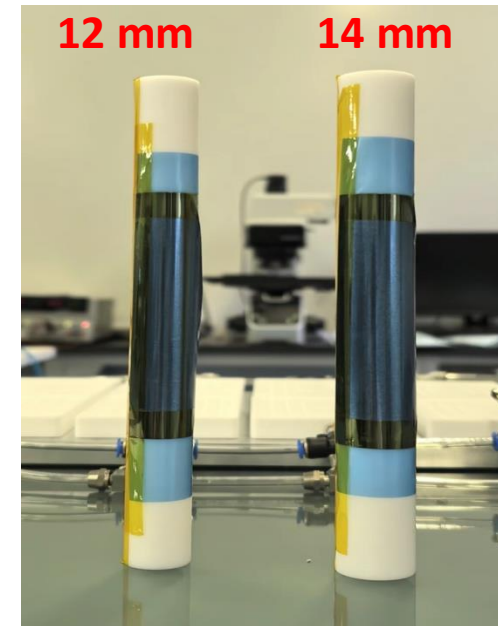
According to the current plan, assuming the flex will be switched to fiber where beyond and near the end of the ladder.



# Stitching R & D

- New thinned dummy wafers received.
  - Thinned to ~30um
  - Expected to bent it to ~11mm radius

By Mingyi



	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

# International collaboration

- Contacting with Jérôme Baudot, vertex group leader in IPHC/CNRS
- Jérôme Baudot is planning to join CEPC workshop 2024 in person
- Wei Wei, Ying, Yunpeng and I will join PIXEL2024 in IPHC in person
  - A few talks about the CEPC vertex accepted in PIXEL2024 (Nov 18-22)

# Summary

- Software for Stitching Vertex Detector is in good progress
- In progress of optimizing PCB, service and cable space for inner layer

# Status of Software for Stitching Vertex Detector

## Geometry

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## Reconstruction

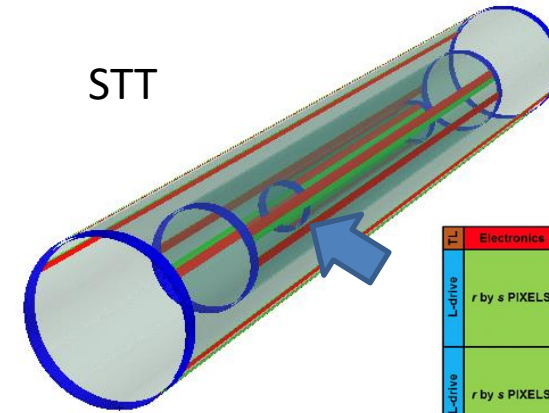
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## Validation

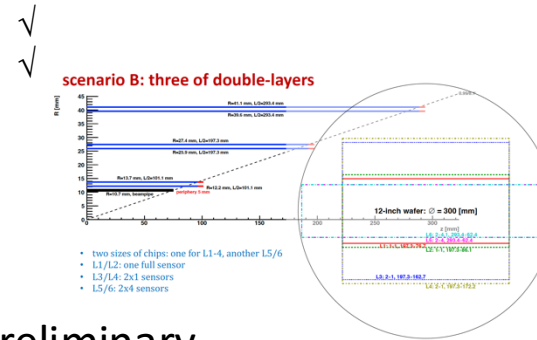
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## Todo

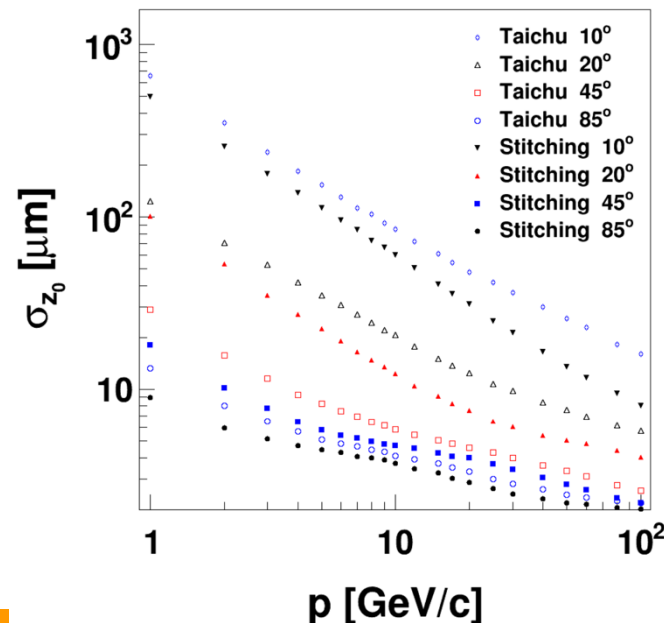
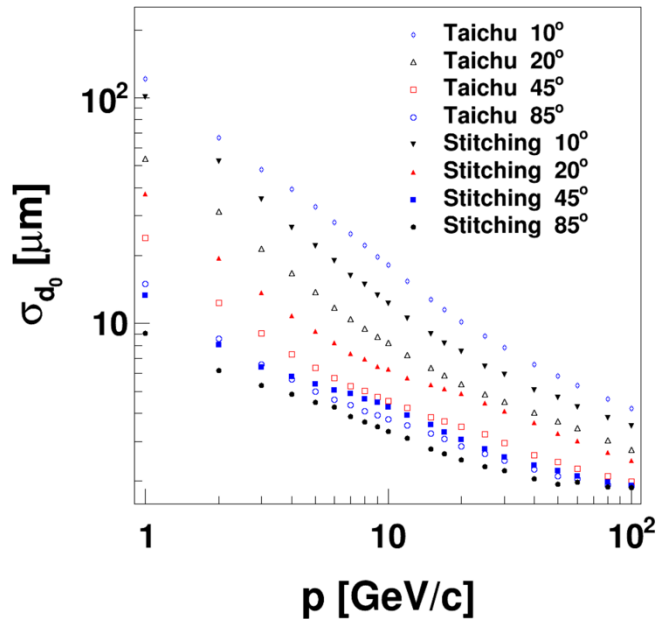
- Reconstruction on STT+TCH
- Performance & layout



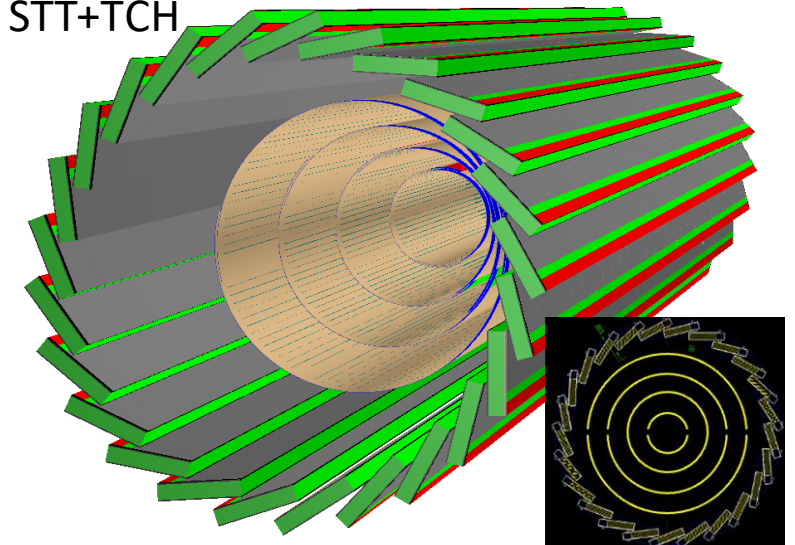
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preliminary



STT+TCH

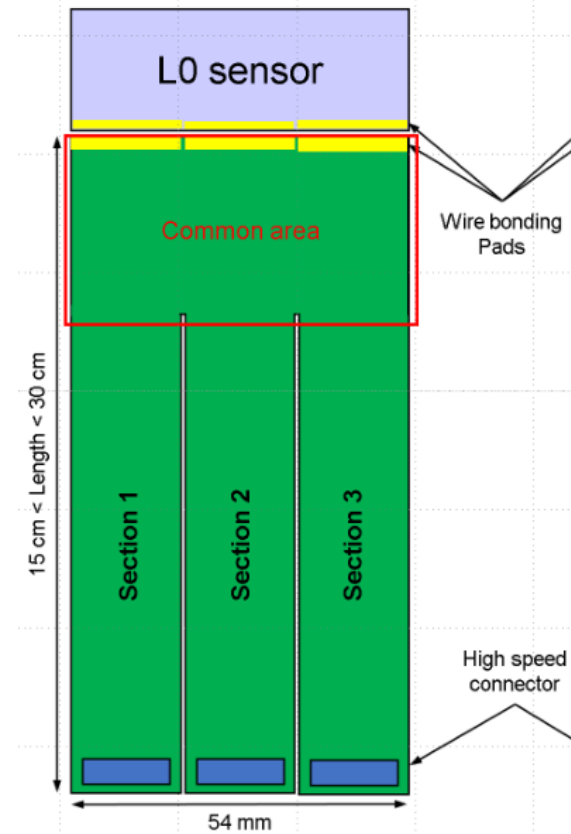
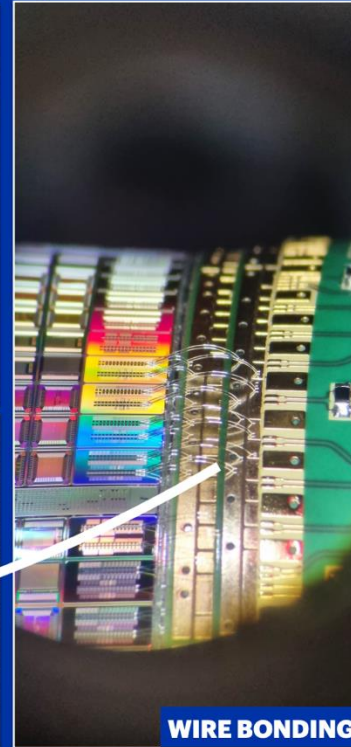
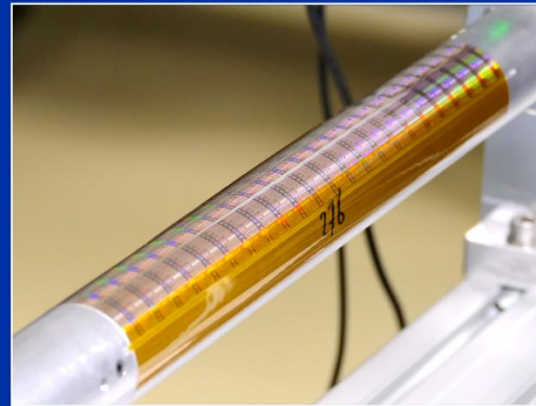
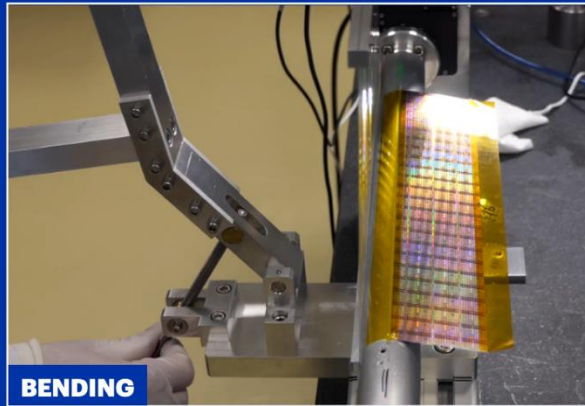




# Vertex technologies: Cable and service

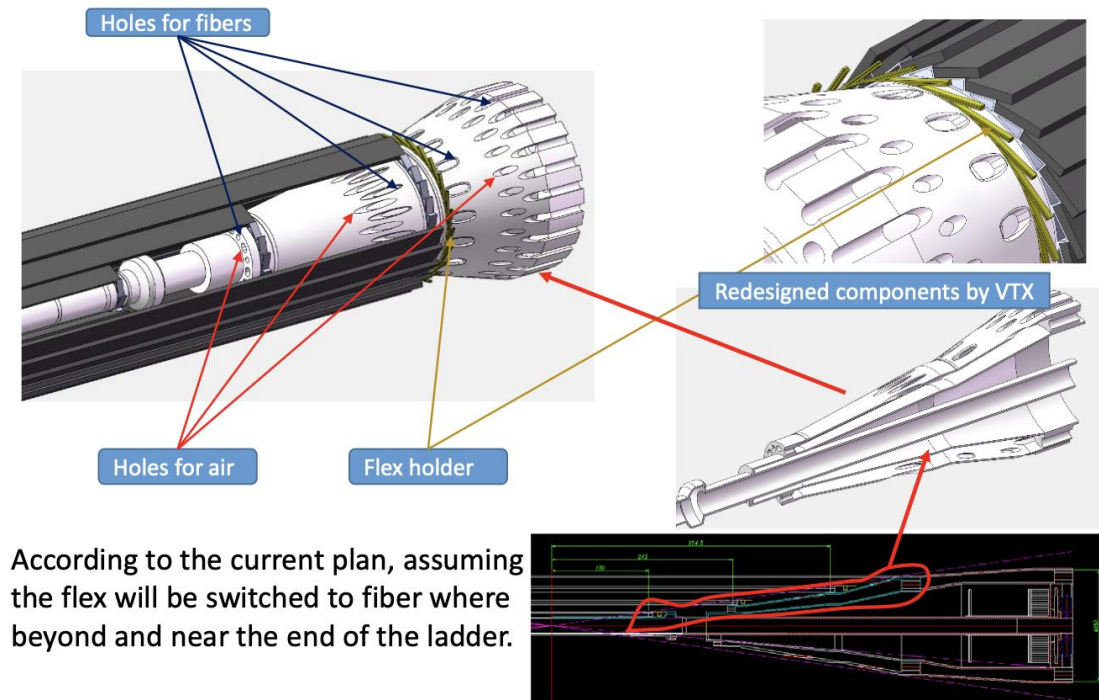
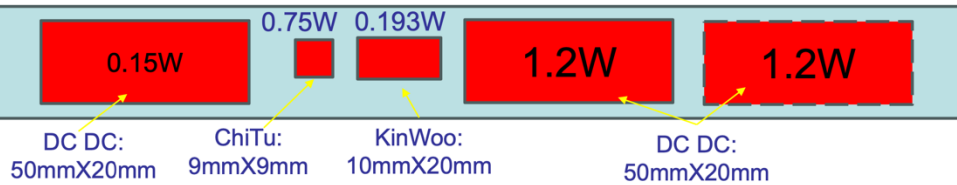
- Refine the design for wire bonding and PCB

## ITS3 bending/interconnection procedure



# Vertex technologies: Cable and service

- Refine the design space in MDI region for cable and service
  - All fast signal transferred into optical fiber in service region
  - 6.7mm thick (including PCB)



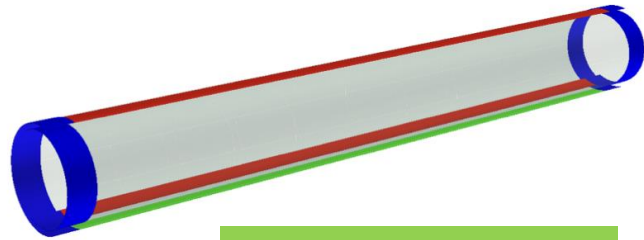
According to the current plan, assuming the flex will be switched to fiber where beyond and near the end of the ladder.

# Update in CEPCSW

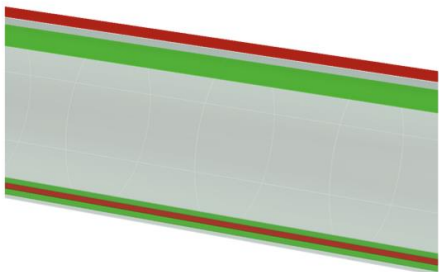
## Stitching layer layout is implemented in CEPCSW

- Dead area is also considered
- Digitization is OK now, can be used for BG simulation
- Code for reconstruction is still under development

Module -> Layer

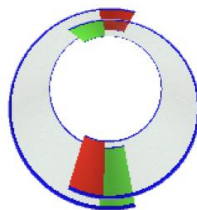


By Chengdong Fu

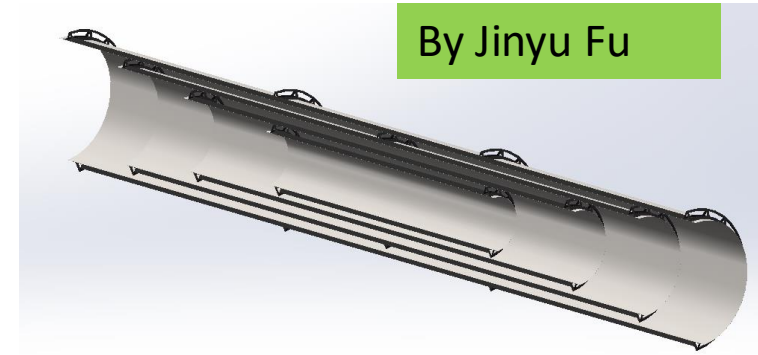


```
<modules>
<module type="Module1A" radius="12.2*mm" nx="10" ny="2" dead="0.1*mm" material="G4_Si">
  <sensor thickness="50*um" width="20*mm" length="20*mm" material="G4_Si" vis="VXDVis"/>
  <flex vis="GrayVis">
    <slice thickness="12.5*um" material="Kapton"/>
    <slice thickness="10.0*um" material="G4_AL"/>
  </flex>
  <electronics thickness="100*um" width="5*mm" material="Kapton" vis="RedVis"/>
  <readout thickness="100*um" width="5*mm" material="Kapton" vis="GreenVis"/>
  <driver thickness="100*um" width="8*mm" material="Kapton" vis="BlueVis"/>
</module>

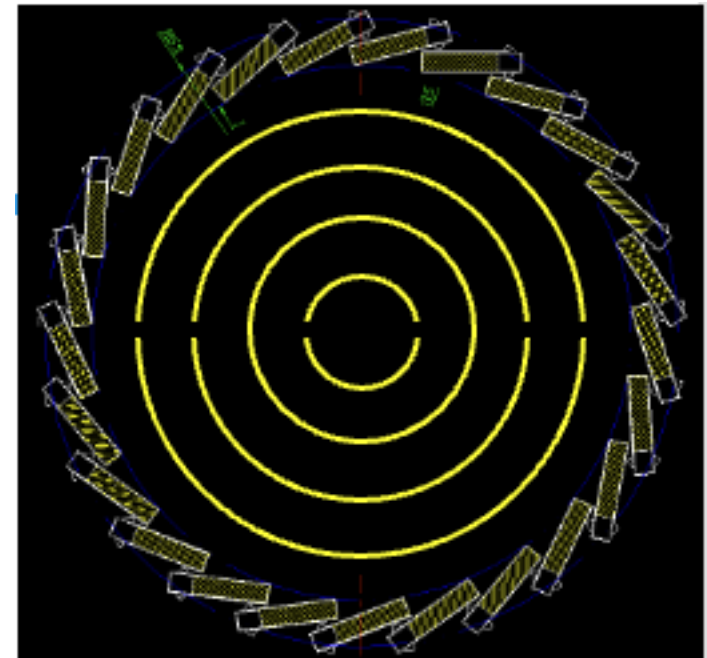
<module type="Module1B" radius="13.7*mm" nx="10" ny="2" dead="0.1*mm" material="G4_Si">
  <sensor thickness="50*um" width="20*mm" length="20*mm" material="G4_Si" vis="VXDVis"/>
  <flex vis="GrayVis">
    <slice thickness="12.5*um" material="Kapton"/>
    <slice thickness="10.0*um" material="G4_AL"/>
  </flex>
  <electronics thickness="100*um" width="5*mm" material="Kapton" vis="RedVis"/>
  <readout thickness="100*um" width="5*mm" material="Kapton" vis="GreenVis"/>
  <driver thickness="100*um" width="8*mm" material="Kapton" vis="BlueVis"/>
</module>
</modules>
```



Parameter to confirm

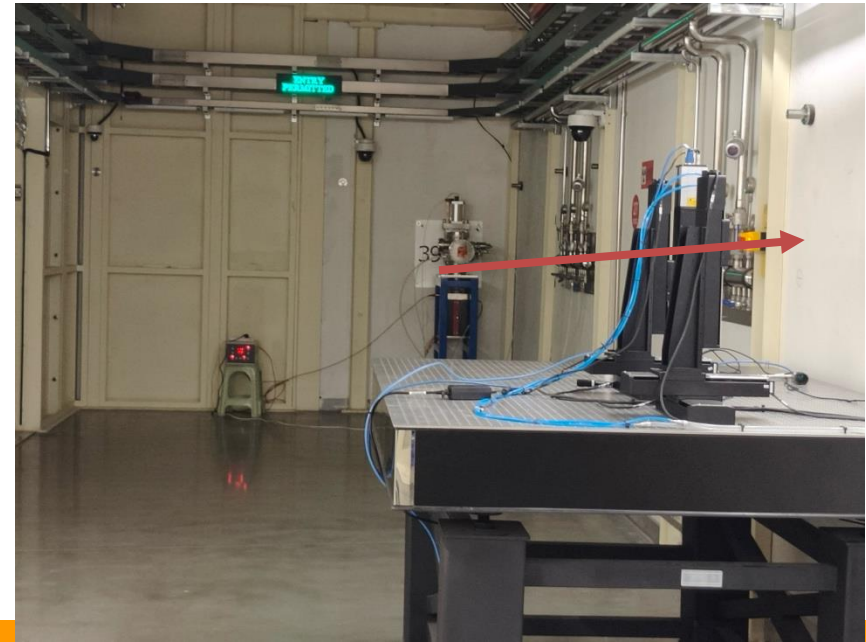
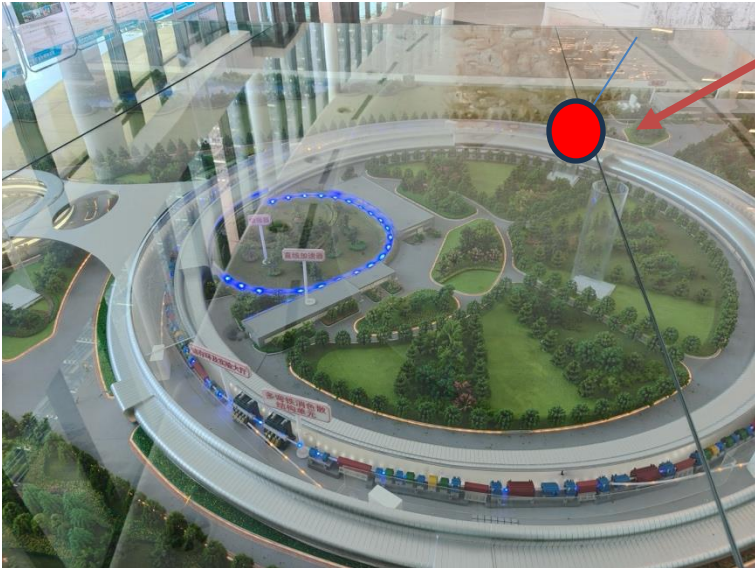


By Jinyu Fu



# Testbeam @ HEPS

- Discussed the testbeam@HEPS in CEPC day steering meeting
- A visit to HEPS last Friday, Yuhui Li, Jianchun Wang, Zhijun Liang
  - Identified one station for testbeam for temporary solution (束测线站)
  - Long term solution could be building testbeam hall in booster (HEPS2)



# Total power

by Wei Wei

## VTX-Power Link



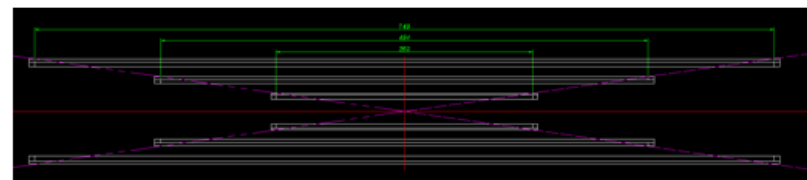
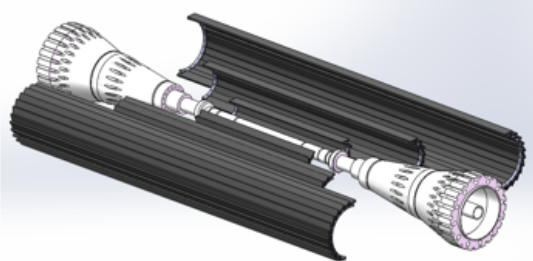
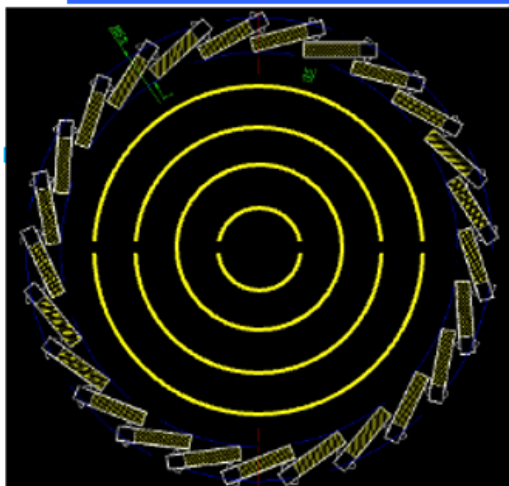
Layer	Comment	Power/chip	Chips/Row	Power/row	Rows	Chip Power of Layers	Power consumed of BaSha (15%)	Total Power/Layer
1	Stitching	200mW	8	1.6W	2*2=4	6.4W	0.96W	8.51W
2	Stitching	200mW	12	2.4W	3*2=6	14.4W	2.16W	17.71W
3	Stitching	200mW	16	3.2W	4*2=8	25.6W	3.84W	30.59W
4	Stitching	200mW	20	4W	5*2=10	40W	6W	47.15W
5	Ladder-side0	200mW	29	5.8W	25	145W	21.75W	167.9W
6	Ladder-side1	200mW	29	5.8W	25	145W	21.75W	167.9W

- 探测器前提假设一致，每芯片功耗估算为200mW ( $40\text{mW}/\text{cm}^2 * 2.6\text{cm} * 1.6\text{cm}$ )
- @40MHz (BX=25ns)，如按15ns，功耗将成倍增加
- 主要功耗贡献：模拟静态功耗+数据接口，不随本底数据率变化，因此不考虑按各层本底的功耗 scaling down
- 设BaSha DC-DC效率为85%，则功耗开销为15%
- 每行固定功耗：数据接口1W+数据接口开销0.15W=1.15W
- 总功耗439.8W（可按1~3层、4层各一个电源通道，5、6每层各两个电源通道@100W/ch考虑，共6个电源通道）

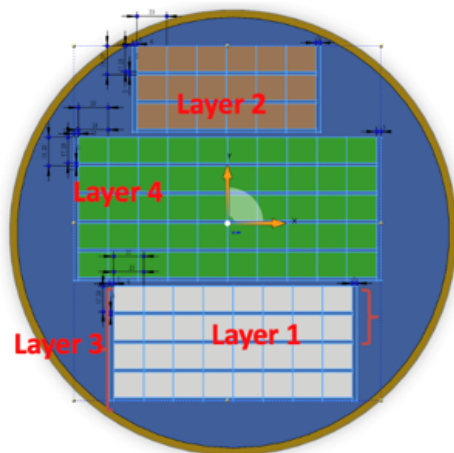
# Total Data rate

by Wei Wei

VTX



- 安全因子1.5，加速器50MW，按内层2Gbps/chip为数据率基准，按higgs mode本底比例计算各层，各层芯片数量内四层以RSU为单位，外两层（double sided）以芯片为单位



Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25