CGEM DAQ Status

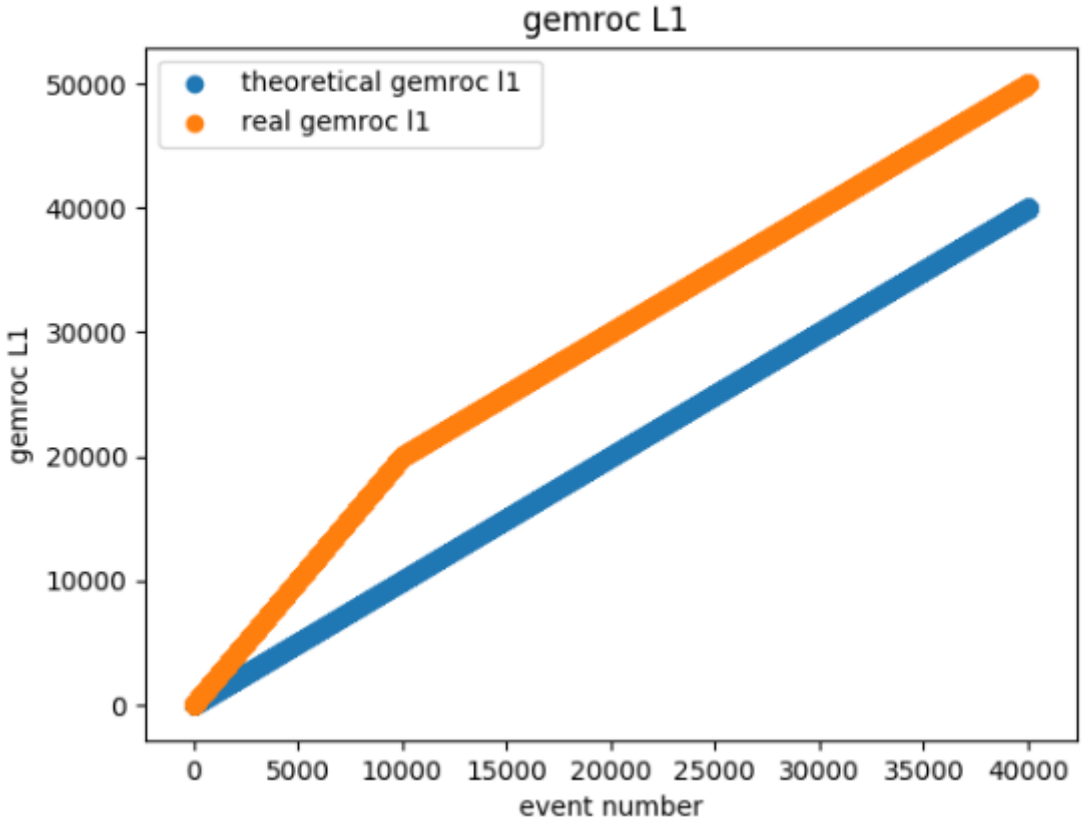
Tingxuan Zeng

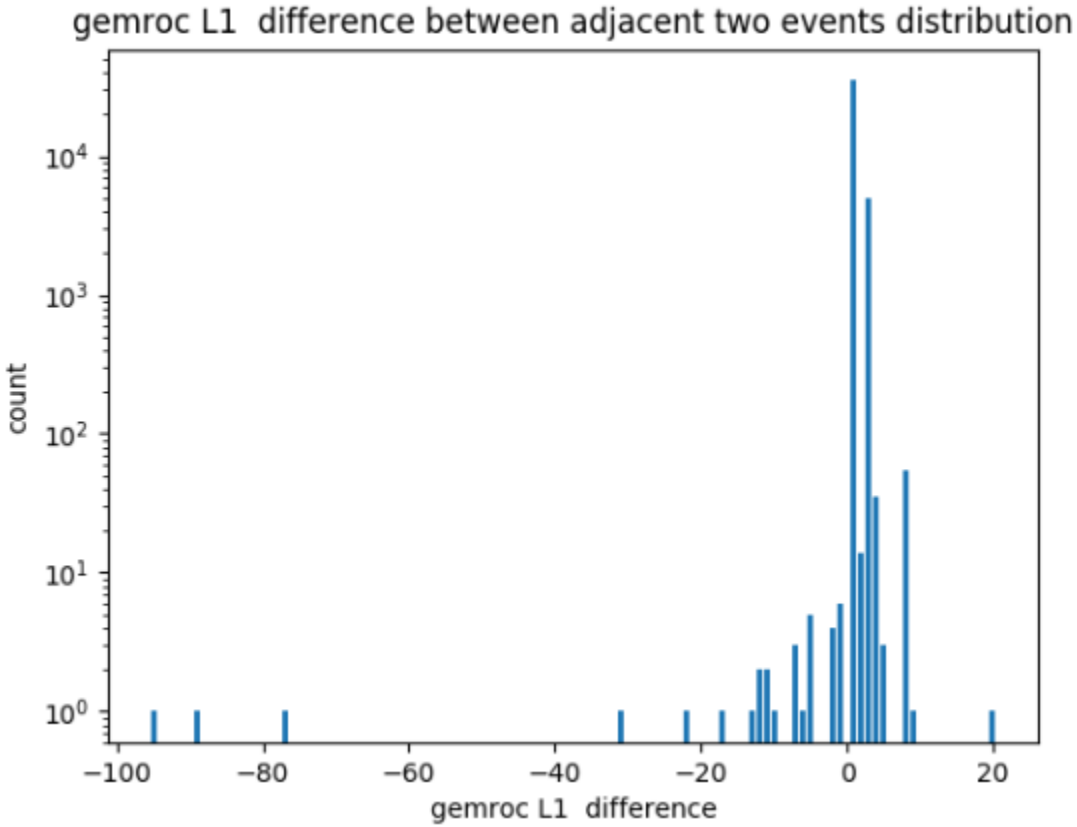
2024-09-16

Test Progress

- Pawel updated all 4 DCs' firmware.
  - Send out 1 event per interrupt
  - 3 of them can work standalone on interrupt 0x4003.Two boards can not work together.
- Preliminary test FEE configuration code in Hall 3
  - Test with two GEMROCs in parallel : it can config the GEMROC rightly. (with Giulio)
  - Revised the config procedure. (with Michela, Angelo)
- Test with Full Signal in Experiment Hall (with Giulio, Jingzhou, Wenxuan, Sheng)
  - The MTI board has some issues, Dong sheng is testing another MTI board.
- Take data with DAQ software and GUFI at the same time and cross check the data file. (with Alberto, Giulio, Angelo)
  - 500Hz random trigger, 1DC-1ROC
  - Compared to GUFI data:
    - There had been data packets dropped with data taking from VME crate.
    - The GEMROC L1 count had many problems.
    - Still investigating the reasons.

Data file checked on my side





- 40044 full event.
- the first DC packet has 4 bytes missing. The other DC packet format is right, while the L1 count has many problems.
- Most Packets dropped in the first 20 seconds.

Data file checked on Alberto's side

- The data now make more sense, but many problems remain:
  - 1- The first packet that makes sense as content is the one with L1 count == 12, the preceding packets show malformed headers and data (while they are correctly present in the data acquired via UDP).
  - 2- Several packets are missing, which are instead present in the data acquired via UDP.
- Specifically:
  - -- 49999 different L1counts and 50000 packets are present in the UDP data acquired with GUFI (the first 2 packets have both L1count==0 due to the first trigger reset procedure). In the DC data we have 40043 packets, all with different L1 counts.
  - -- In the UDP data acquired with GUFI there are 57529 hits, while in the DC data we have 45267 hits.

Thanks for the Italian Group’s Help!

- backup

Overall status

	Planned tasks	Time needed	status
1	DC board Firmware test	Not sure(1 week ?)	3 boards can work standalone. Two boards can not work together. (9.2~9.13 had been updating firmware triple times.)
2	FEE standalone configuration test with all GEMROCs	Need 1 week when all GEMROCs can be tested.	Parallel config 2 GEMROCs successfully. Config Document Revised.
3	FULL signal test	Not sure (1 week?)	MTI board has some issues. (9.2~9.13 had been testing it.)
4	1 DC board 11 GEMROCs long time data taking test	Need 1 week, After 1,3 finished/ Or have time to test in Hall 3 ?	Not started yet.
5	2 DC boards 21 GEMROCs long time data taking test	Need 2 weeks, After 1,3 finished/ Or have time to test in Hall 3 ?	Not started yet.

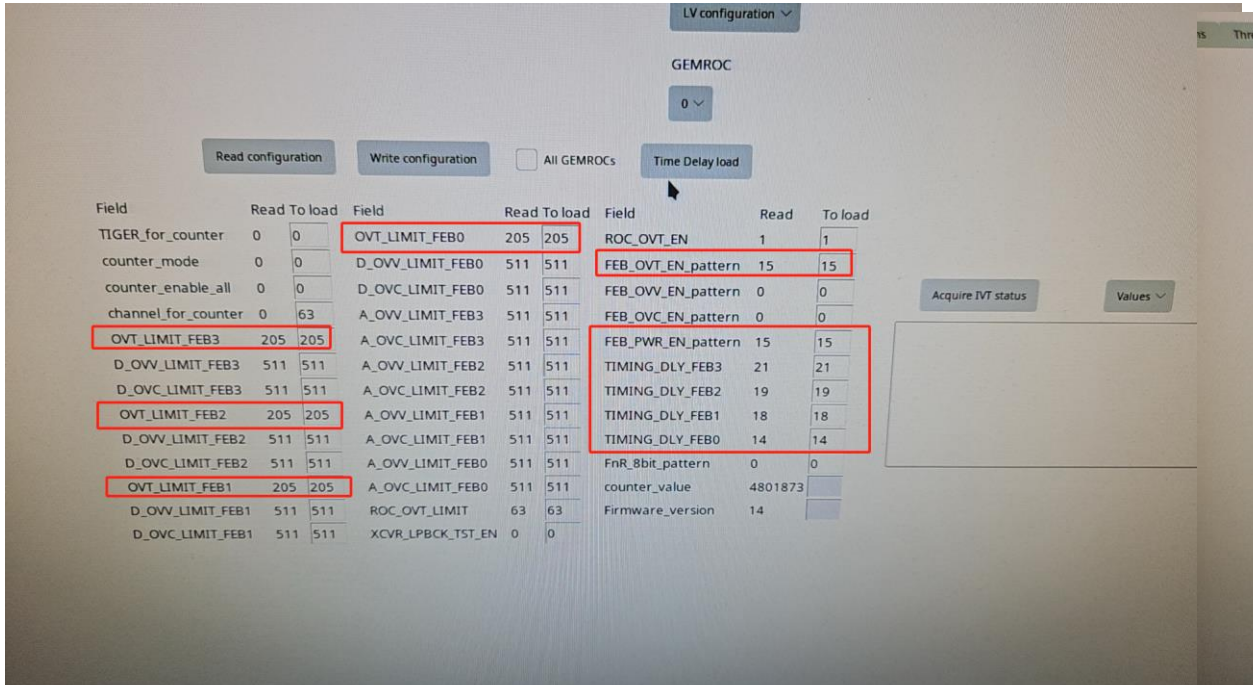
Firmware flash status

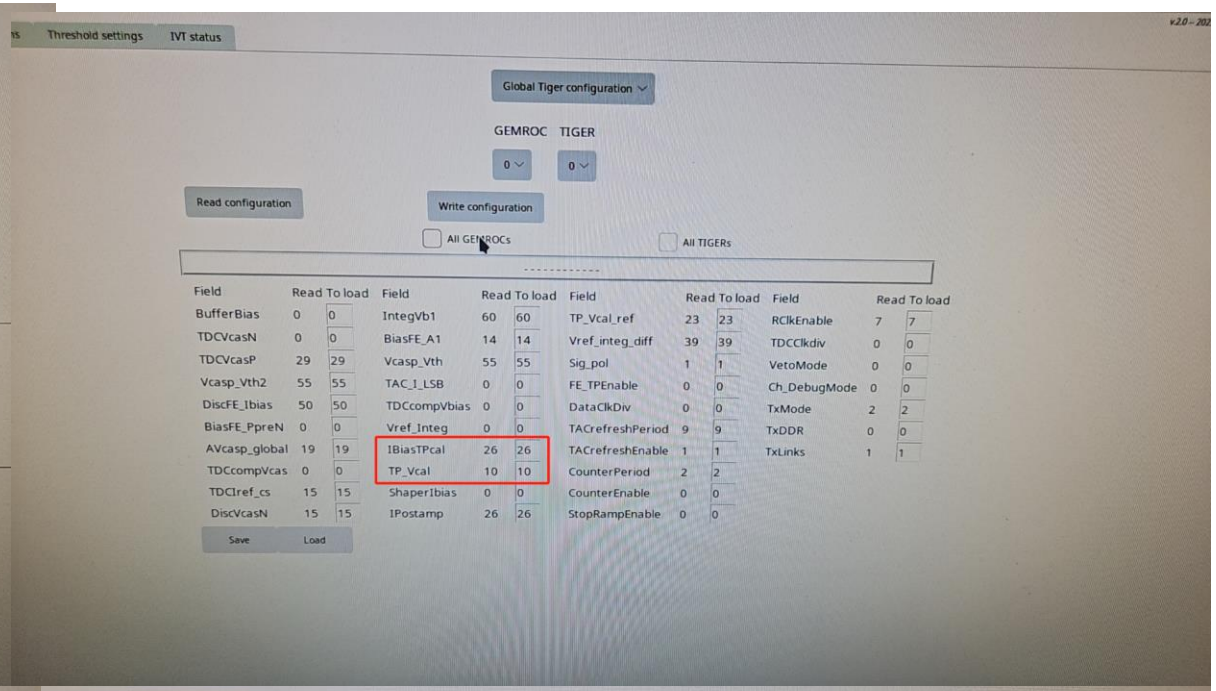
DC 1 and 2 can work respectively, can not work together. DC 3 and DC 4 Register are all 0xffffffff

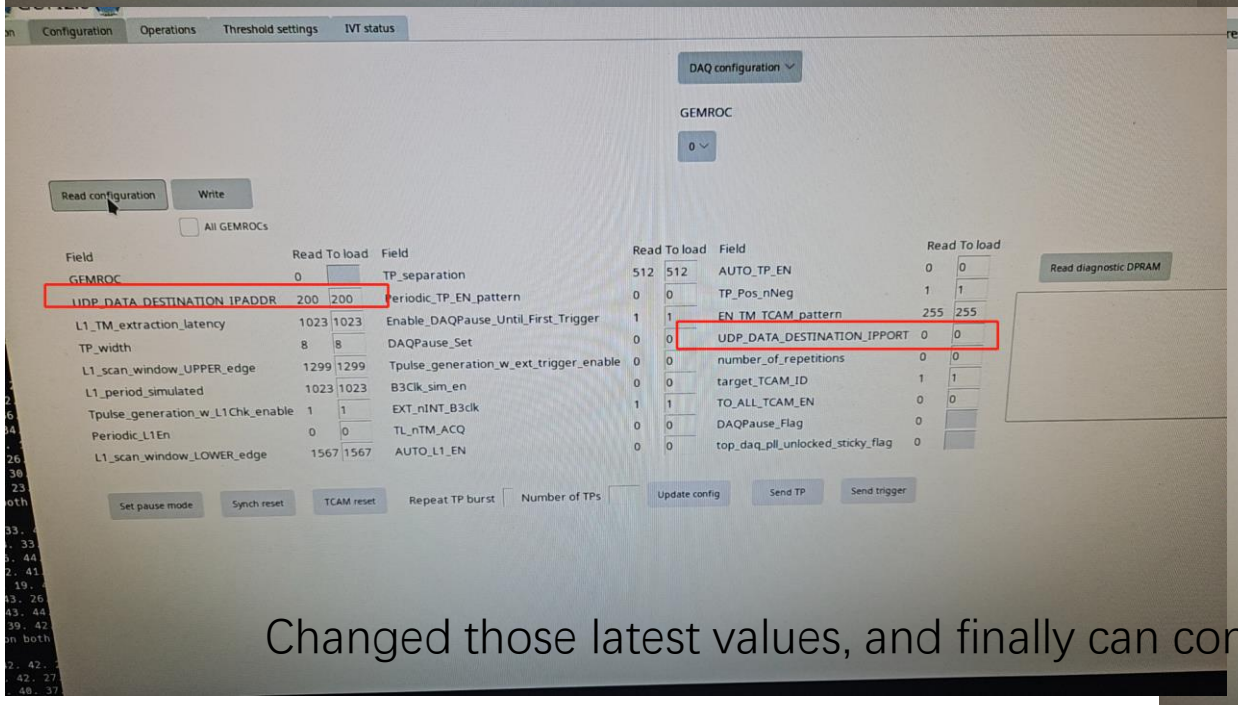
Board ID	DC board 1	DC board 2	DC board 3	DC board 4
DIP switch (sw5-0)	0000 01	0000 00	0000 00	0000 01
CSR Address	0x04000000	0x00000000	0x00000000	0x04000000
Irq vec, irq line	0x3f, 0x04	0x40, 0x03	0x40, 0x03	0x3f, 0x04
Jtag cable connected	no	yes(updated)	yes	no
Place	Hall 3 106	DAQ lab	Hall 3 106	DAQ lab
firmware updated? (9.2~9.9)	yes	yes	flashed. Register all 0xffffffff	flashed. Register all 0xffffffff
firmware updated?	same as last week,	same as last week,	Yes	same as last week,

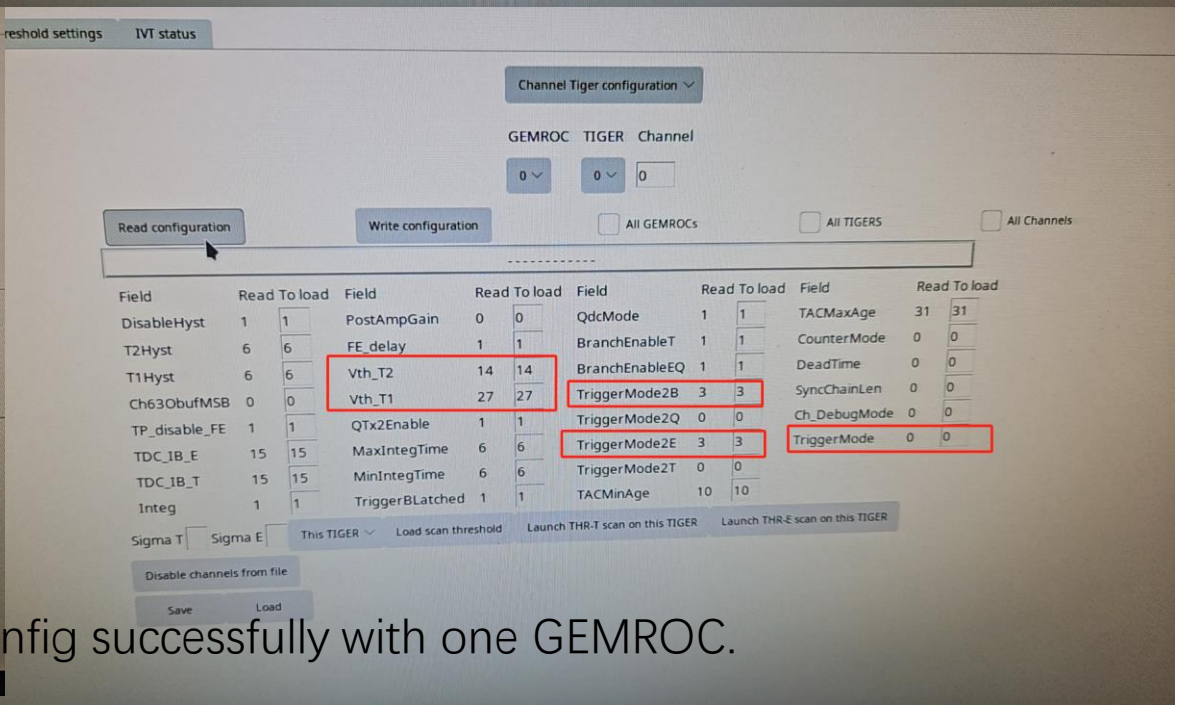
```
undefined symbol: DC3
-> WriteToVme32(0x04400000, 0x20000000, 0x00003f04)
value = 0 = 0x0
-> check_interrupt(0x04400000)
DC_INT : 0x3f04
value = 17 = 0x11
-> WriteToVme32(0x00400000,0x20000000,0x00004003)
value = 0 = 0x0
-> check_interrupt(0x00400000)
DC_INT : 0x600
value = 16 = 0x10
->
```

Two DC boards can not work together. Only one board's interrupt vec and interrupt line can be set correctly.









Changed those latest values, and finally can config successfully with one GEMROC.

- FEE configuration procedure confirm
- The GEMROC Fanout Module output voltage will become zero when the full signal cable connected to the MTI module.
  - After changing the ground wire, the FULL light on the MTI turned on.
  - MTI board has some issues.

Issues found during last data taking

1. ~~GEMDC packet L1 count not increasing when working with dummy GEMROC data.~~
2. The first GEMDC packet length is wrong.
3. The GEMROC data format in the first GEMDC data packet is wrong.
4. ~~Found DC buffer pile up, multiple DC packets has been read out in one DMARun.~~
5. GEMROC L1 counter not start from 0.
6. GEMROC L1 counter is increasing by 4 most time, sometimes by 3 or 5.
7. ~~DAQ software is able to acquire data for 2 minutes, after that, no interrupts happened.~~
8. Sometimes data format of GEMROC 5 is wrong.(new found)
9. ~~Link NO in DC packet is not corresponding to the GEMROC ID.(new found)~~

Our Analysis:

1. ~~1 maybe cause to 2 different GEMROC data formats: confirming with Pawel if the DC firmware support two GEMROC data format .~~
2. 2,3,5,~~8,9~~ data format issue.
3. ~~4 is correct according to current design of DC firmware.~~
4. ~~7 interrupt issue~~
5. 6 need my recheck.

Interrupt issue solved.
remaining some data format issues.

Outline

- Test the configuration in Hall 3
- FEE configuration integration

- If there are ongoing issues with hardware testing, the software testing time will be compressed.
- We cannot guarantee that there will be no delay before installation.

How does CGEM Sync with other subsystem?

- FULL Signal: When DC buffer is almost full , How does it notify GEMROC fanout module ?
  - Does DC board have connection to GEMROC Fanout Module?
  - Or DC board notify the MCC module directly ?
  - Or DC board will just notify the GEMROCs?
- When DC buffer is almost full , what will be done to protect the buffer?
  - When read out is slow, will DC board ensure that one or several complete events will be thrown away?

ISSUE I : The generation of issue 1 is due to the difference in parsing L1 count between dummy data packets and real data packets. For dummy data packets, it is fixed at 0xe0, while for real data packets, it increases based on the trigger number.

HEADER = 0xC08765432001ABCD
HIT = 0x0FFEDCBA36543210;
TRAILER = 0xea864207088ba3a3;
UDPSEQNO = {'0100000',GEMROC_ID[4...0],0xFEDCBA98765, TEST_TM_SENT_PKT_COUNT_8bit};
where TEST_TM_SENT_PKT_COUNT_8bit is an 8 bit counting field incrementing at each packet sent

- GEMROC packet length is consistent with dummy and real data.
  - Length: hit number * 2+3*2 word , hit number = (header >>16)&0xff
    - For dummy GEMROC packet: Length is fixed: just 8 words.
    - Hit num (0xc08765432001abcd >> 16)&0xff == 1 , length = 1*2+3*2=8 word
- GEMROC Local L1 count has difference with dummy and real data.
  - Dummy data : ((0x2001abcd>>24)&0x3f) + ((0xc0876543&0x3fffff)<<6) , fixed, the low 8 bit is 0xe0(224)
  - Real data : (((*(buffer+1))>>24)&0x3f) + (((*buffer)&0x3fffff)<<6), is increasing
  - When working with dummy gemroc ,the DC L1_count_LSB is not increasing, fixed to 0xe0.(issue 1 is explained.)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Packet Header	1	1	0	L1_HEADER_STATUS_BITS[2..0]			LOCAL L1 COUNT [31 : 6]																									
	0	0	LOCAL L1 COUNT [5 : 0]						COUNT OF MATCHED HIT IN THE PACKET								LOCAL L1 Timestamp															
Hit record 1	0	0	TIGER_ID			LAST TIGER FRAME NUMBER [2:0]			TIGER RAW DATA [53 : 30]																							
	0	0	TIGER RAW DATA [29 : 0]																											
Hit record N	0	0	TIGER_ID			LAST TIGER FRAME NUMBER [2:0]			TIGER RAW DATA [53 : 30]																							
	0	0	TIGER RAW DATA [29 : 0]																											
Packet Trailer	1	1	1	LOCAL L1 FRAMENUM [23 : 8]																LOCAL L1 FRAMENUM [7 : 0]								GEMROC_ID				
	0	0	TIGER_ID		LOCAL L1 COUNT [2 : 0]				LAST COUNT WORD FROM TIGER: CH_ID[5 : 0]								LAST COUNT WORD FROM TIGER: DATA[17 : 0]															
UDP Sequence Counter	0	1	0	0	L1_HEADER_STATUS_BITS[5..3]			GEMROC_ID									UDP packet count[47:28]														
	1	0	1	0	UDP packet count[27:0]																											

CGEM DAQ discuss

Documentation

My Thesis -> Overview of the chain and details about GEMROC's and GUFI

Fabio Cossio's Thesis -> details about TIGER

The CGEM readout chain -> JINST article about the whole electronic chain

Fabio's presentation about TIGER pass: Cgem2023

UDP format file -> GEMROC packet format pass: Cgem2023

We are working on a complete wiki, expecially for GEMROCs, I will keep you updated.

---

1. what is the config process before physics data taking mode ? Can you provide me a document about this topic ?
    - I will provide a specific document for it.