**BESIII Inner Tracker Upgrade Meeting**

**(Sep.23, 2024) 14:00 - 16:00pm (Beijing Time)**

**Meeting agenda and minutes**

* Indico page: https://indico.ihep.ac.cn/event/23665/
* Participants:
	1. Present in the meeting room

Haibo Li, Zheng Wang, Qun Ouyang, Mingyi Dong, Jing Dong，Zeng Tingxuan，Ma Si, Fu Jinyu, Liangchenglong Jin, Stefano Graminia

* 1. Online at ZOOM

Xiaoyan Shen, Gianliugi Cibinetto, Michela Greco, Giulio Mezzadri, Liangliang Wang, Linghui Wu, Fei Li, Hongliang Dai,Yunhua Sun

**Schedule and Progress last week: Mingyi Dong**

* **Summary of the report：** ( **Slides by Mingyi Dong:** [**Slides**](https://indico.ihep.ac.cn/event/23665/contributions/167539/attachments/82566/104328/progress%20and%20plan_20240923.pdf))
1. Progress last week



1. Plan for the next week



* **Questions during the slides or planning:**

Stefano asked the tetails about the new shielding plate and the cavity measurements after the installation of the CF cylinder

Mingyi : (1) The new cable shielding is necessary to protect the feedthroughs of the step section and separate the shielding of the drift chamber and CGEM (as required by Yifang). Jin Yu will send Stefano the drawings. If there are any problems, we can arrange a discussion.

(2)We will arranged the laser measurement for the drift chamber, including the cavity of the CF cylinder (The central part of the carbon fiber may has a relatively large measurement error, but we will try to measure it).

(2)The laser measurement of the connection flanges have been finished. This week, we will arrange the laser measurement for CGEM after the connection flanges are fixed on the CGEM

**CGEM DAQ status: Tingxuan Zeng (**[**Slides**](https://indico.ihep.ac.cn/event/23665/contributions/167541/attachments/82203/103730/cgem%20daq%2020240923.pptx)**)**

* **Summary of the report：**
1. Data taking progress last week



**Conclusion:** By swapping boards, locations, and data acquisition modes, it is now confirmed that interrupts can work normally in dummy mode, but there are still issues of interrupts in real physical mode.

2. Full Signal Test

1. The L1 signal can be observed on the FCDB, so the fiber downlink is verified.
2. The voltage output of the tester is not yet fully understood. Now the output is always 0V, so we can not use it to test full signal right now.
3. Block the readout of ZDD DAQ; the full signal **VOLTAGE** changes is observed at TP1, but the voltage standard is not as expected, and the full led is always down.

3. HV Requirements Update

1. Change the ramping method from pre state to work state.
2. Basically determined the workflow when a TRIP occurs, the details are still under discussion with CGEM experts.
3. New requirements with alarm state

4. Slow Control Progress:

1. We were updating the program to meet the latest requirements last week.
2. The program has been mostly updated, waiting for commissioning.
* **Questions during the slides or planning:**

Haibo: How long does it take from pre high voltage to working high voltage, and if there is a high voltage trip, how long does it take to reach working high voltage? The time for CGEM to raise high voltage needs to be matched with the BESIII detector and cannot be slower than the drift chamber.

Michela: Yes, we will optimize the rising time of high voltage. Less than 90s from pre high voltage to working high voltage.