# Progress of AC-LGAD sensor development

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# Content

- LGAD development and status

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- AC-LGAD development and performance
- Proposal of AC-LGAD as OTK&TOF for CEPC
- Issues
- Plan
- Collaboration

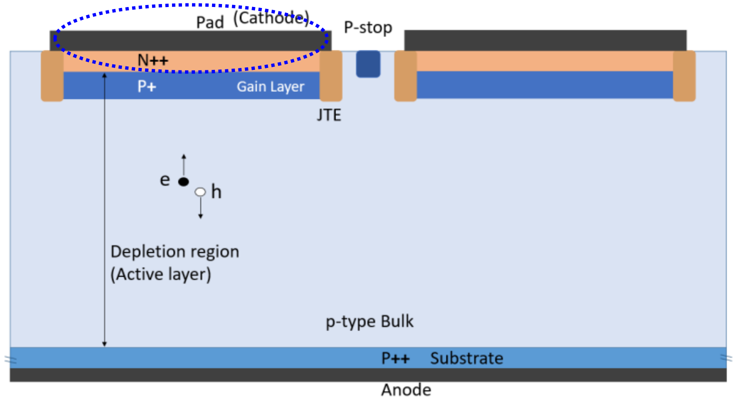
# LGAD and AC-LGAD

- **Low gain avalanche detector** be demonstrated to have timing resolution <35ps and will be used to provide precise timing information in ATLAS HGTD and CMS ETL for address pile-up issues.

- **AC-LGAD**, a 4D detector, provides both timing and position information at the same time.

**LGAD (Low-Gain Avalanche Diode)**

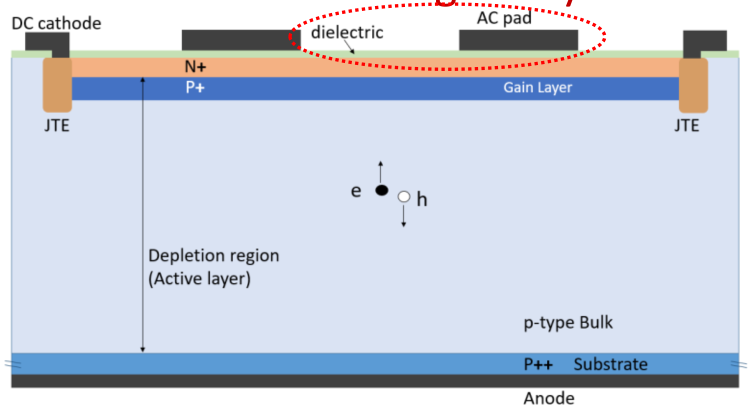
Segmented gain layer




- The read-out electrode is placed and connected to the N++ layer.

**AC-LGAD (AC-coupled LGAD)**

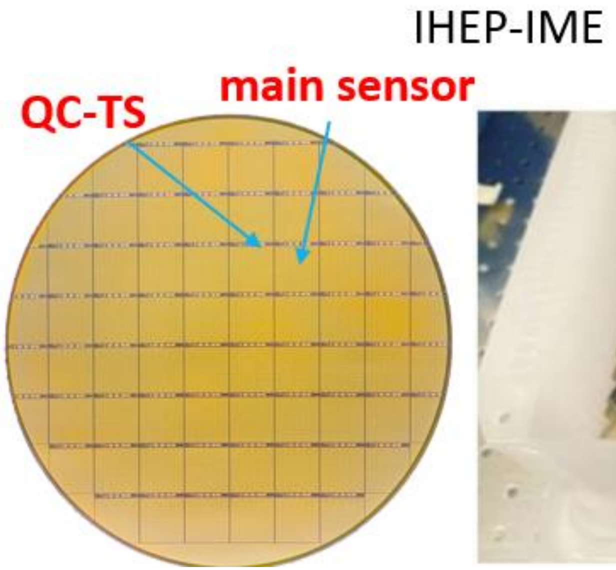
Continuous gain layer

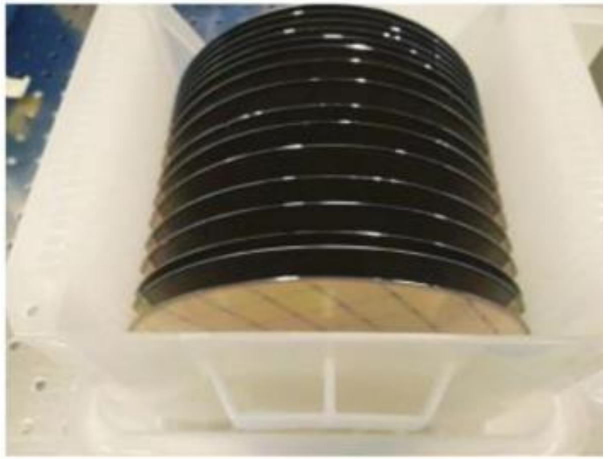


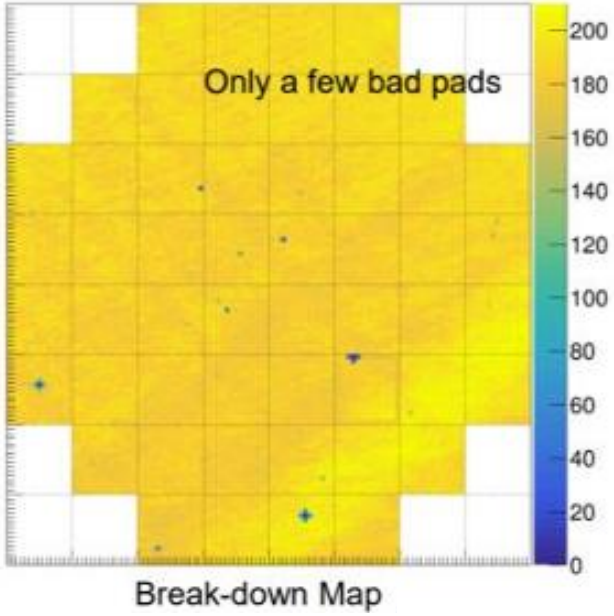

- metal AC readout electrode and a thin dielectric layer ($Si_3N_4$, $SiO_2$) above the N+ layer
- Less dead area and better position resolution
- Research institute: FBK, HPK,INFN, BNL, CNM, USTC, IHEP…

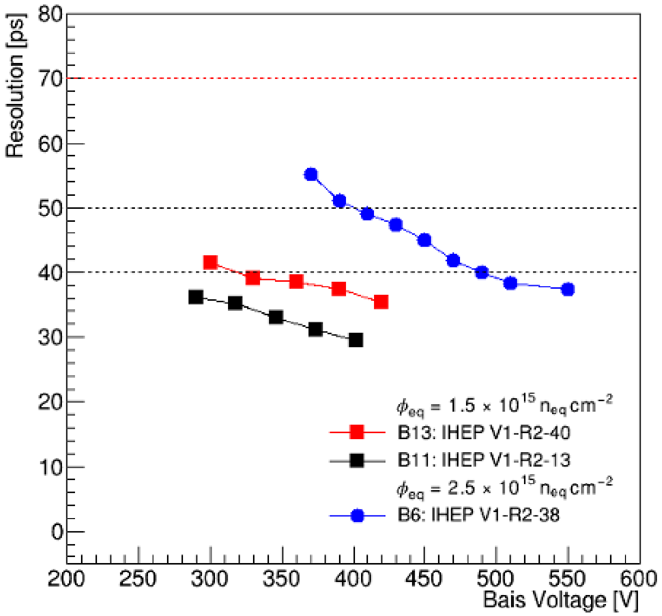
# LGAD development and status

- LGAD designed by IHEP will contribute to 90% of ATLAS HGTD sensors, owning to its good radiation hardness.
- IHEP LGAD sensors pre-production has been finished(90 wafers fabricated). The performance meets the specification, and sensor production readiness review passed successfully in July, 2024. Final fabrication commenced.





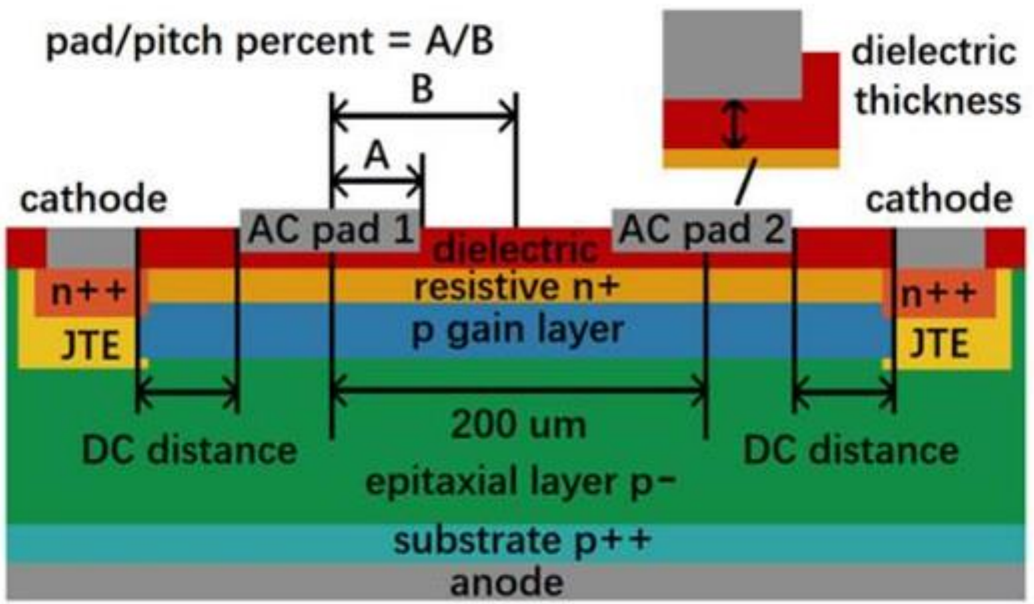



# AC-LGAD R&D

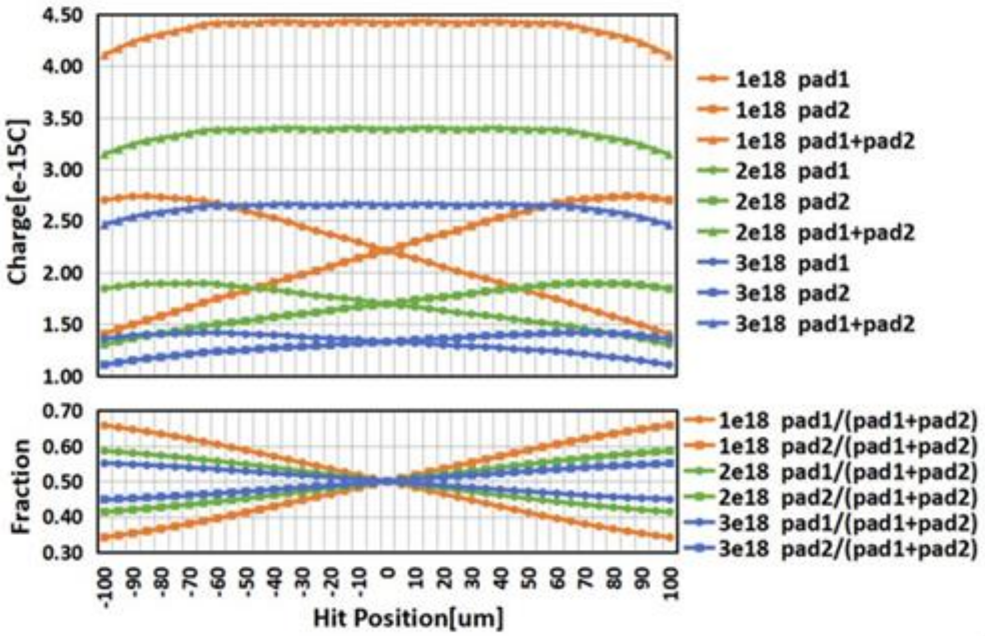
**AC-LGAD sensor simulation:** **Optimization of process and structure parameters**

Process parameter: n+ layer dose, AC dielectric material and thickness

Structure parameter: pad shape, pad-pitch size




TCAD model of AC-LGAD for simulation

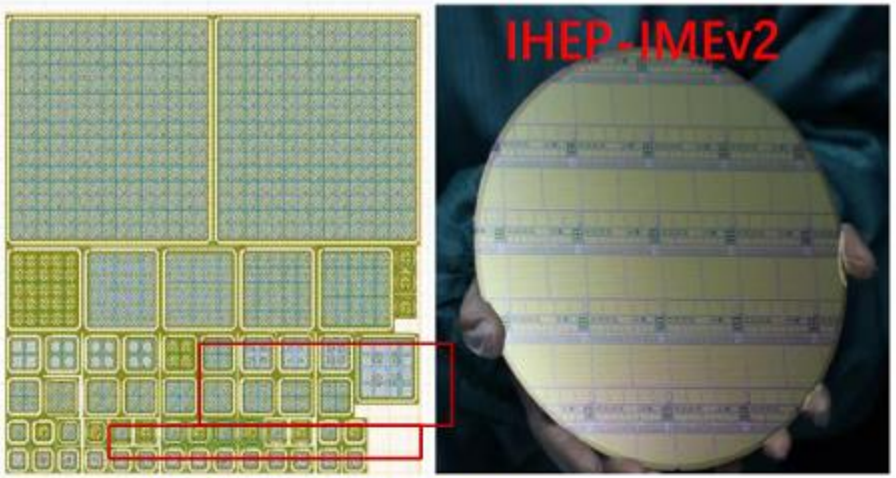



Lower n+ dose→ Large resistivity →good spatial resolution

Design of AC-coupled low gain avalanche diodes (AC-LGADs): a 2D TCAD simulation study, JINST, 2022.9, DOI:10.1088/1748-0221/17/09/C09014

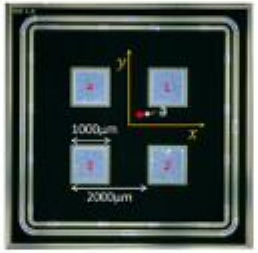
# AC-LGAD development

2022




**AC-LGAD R&Dv1:**

**Pixelated AC-LGAD** One wafer

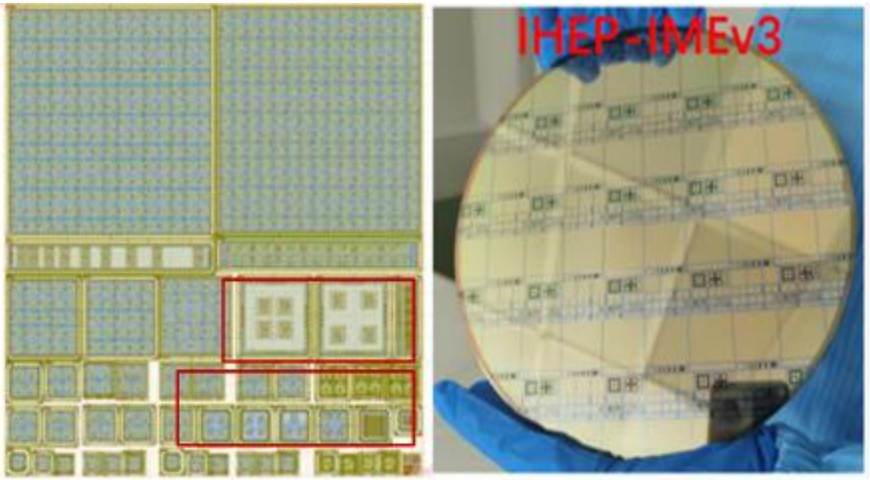



- With different pad-pitch size
  1000-2000um
  100-500um
  100-200um
  50-100um
- wafers: with different n+ dose: 10P to 0.2P

Process parameters be studied.

**The performance of large-pitch AC-LGAD with different N+ dose， Trans. Nucl. Sci.， 2023.6**

2023




**AC-LGAD R&Dv2:** One wafer

**Pixelated and strip AC-LGAD**

- With different pad-pitch size
  1000-2000um pixel
  100-250um strip
  100-150um strip
  50-100um strip
- wafers: with different n+ dose:0.2P to 0.01P

**The performance of AC-coupled Strip LGAD developed by IHEP, NIMA, Volume 1062, May 2024, 169203**

# AC-LGAD R&D

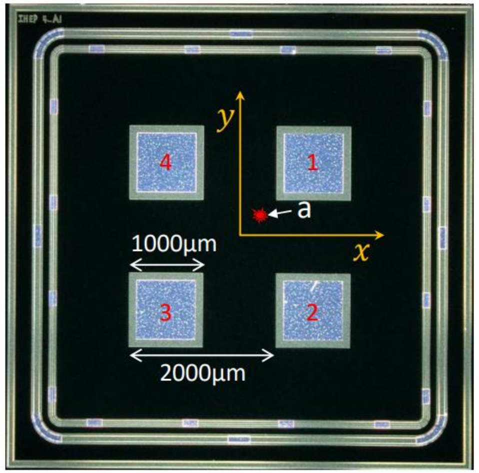
- **AC-LGAD R&Dv1: pixelated AC-LGAD**

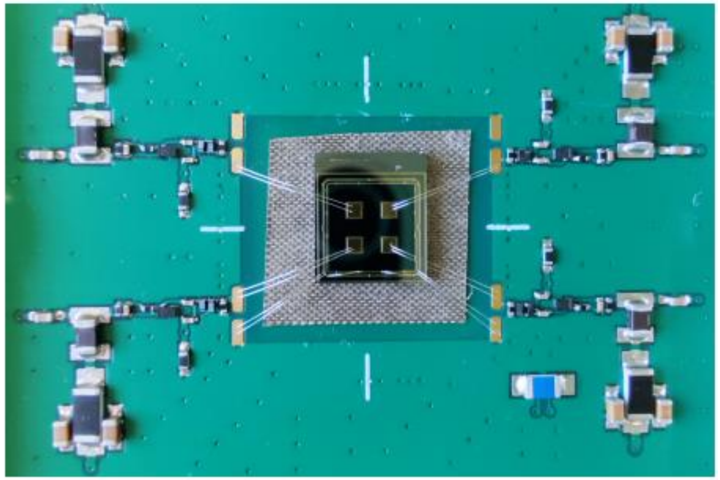
  Large pad-pitch size: 1mm-2mm

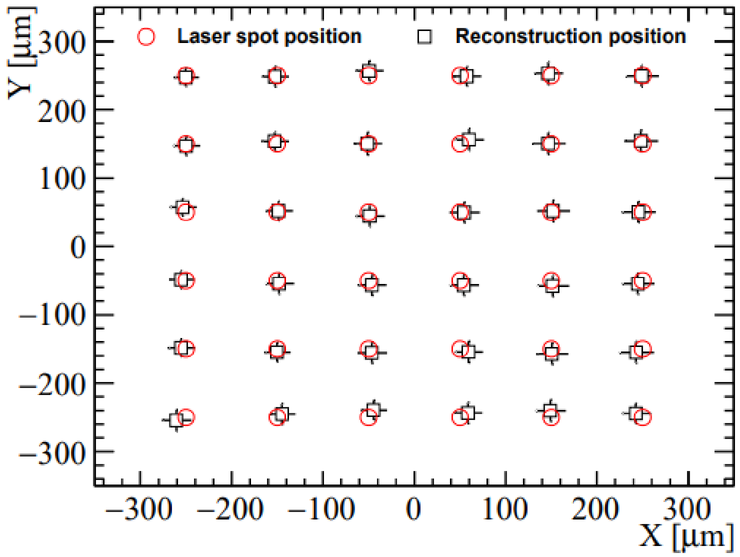
  To study the process parameter

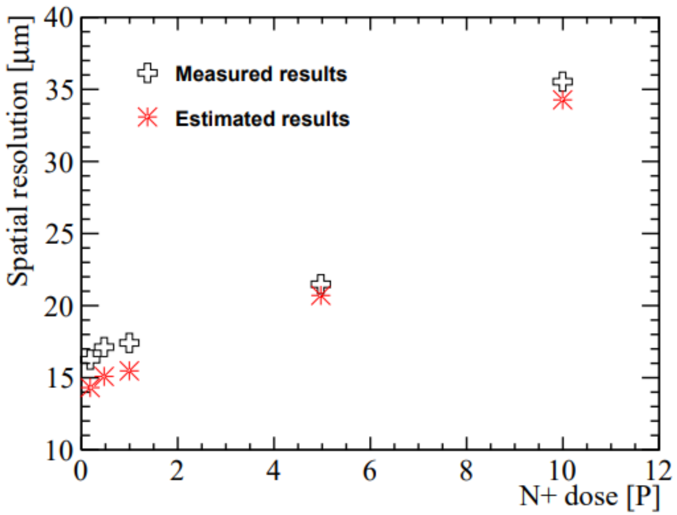
- Spatial resolution be better

  as decreasing the n+ dose(10P to 0.2P)

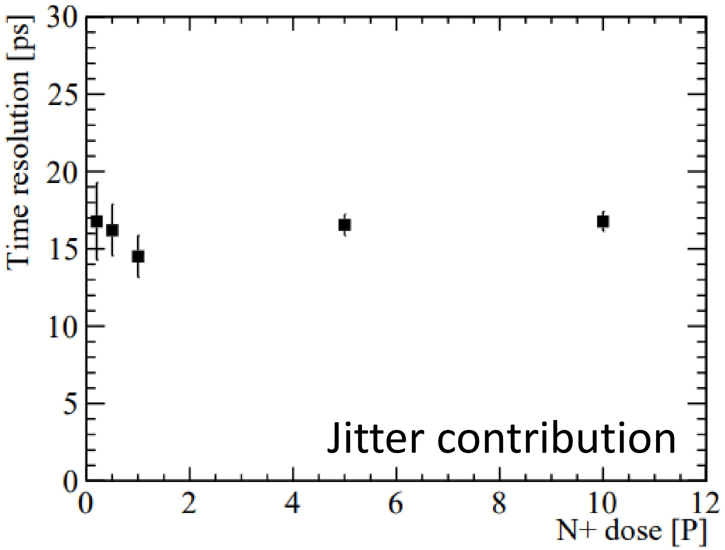





Spatial resolution: 15um




Timing resolution: 15-17ps

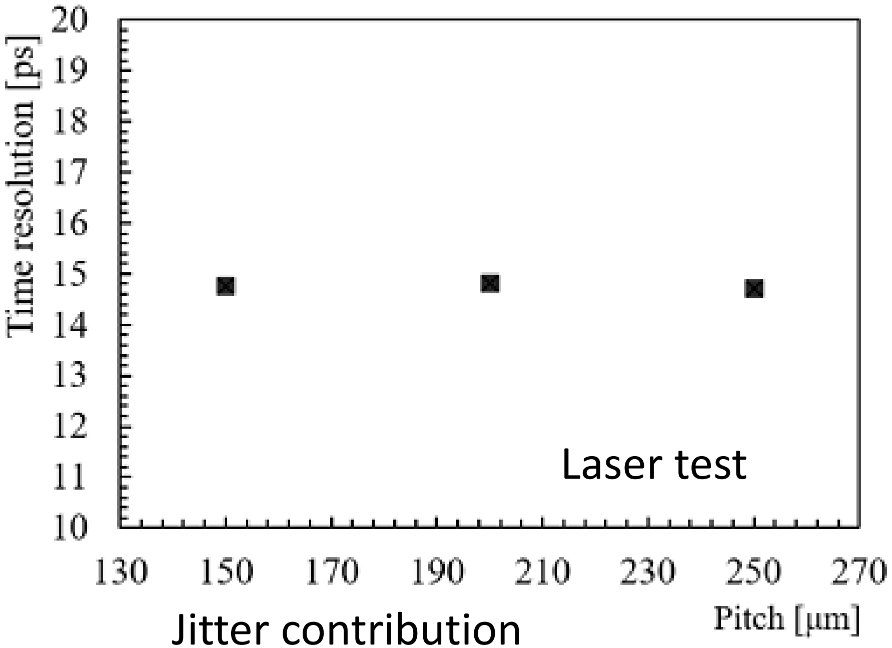
# Strip AC-LGAD R&D

**Strip AC-LGAD:** Strip length:5.65mm

pad-pitch size: 100-250um, 100-200um, 100-150um

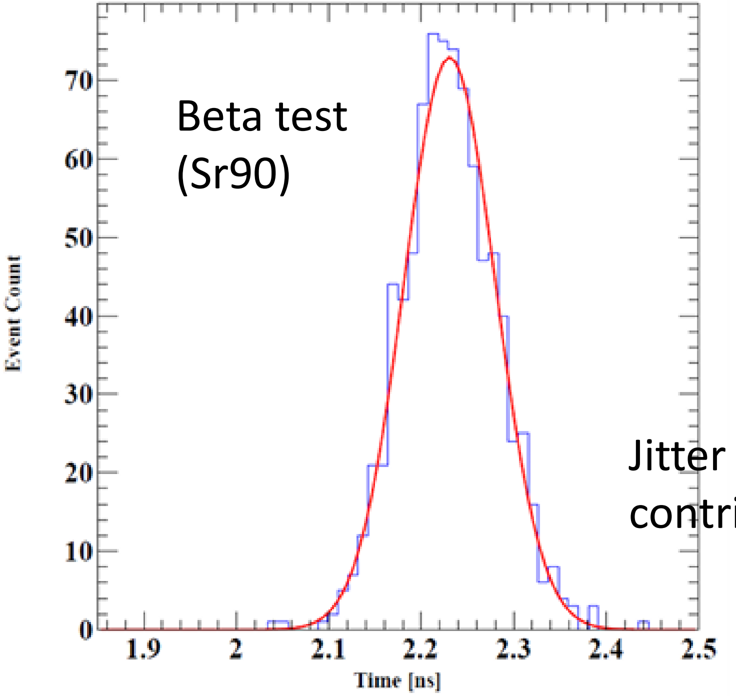
$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{Landau}^2 + \sigma_{Jitter}^2$$

constant fraction discriminator (CFD) method




Jitter contribution

The timing resolution: 15~17ps



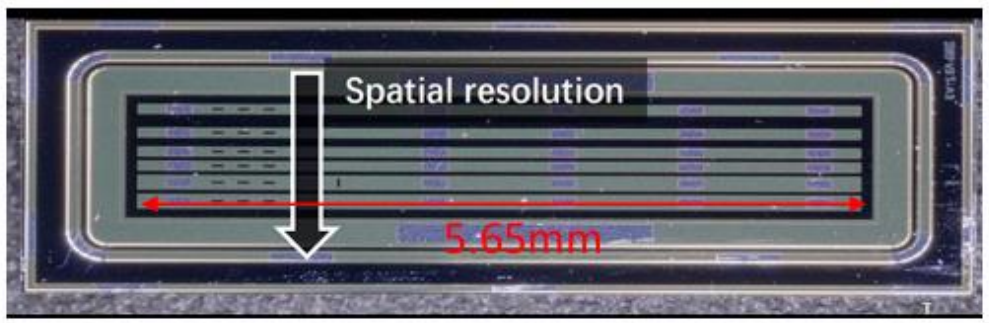

Jitter and Landau contribution

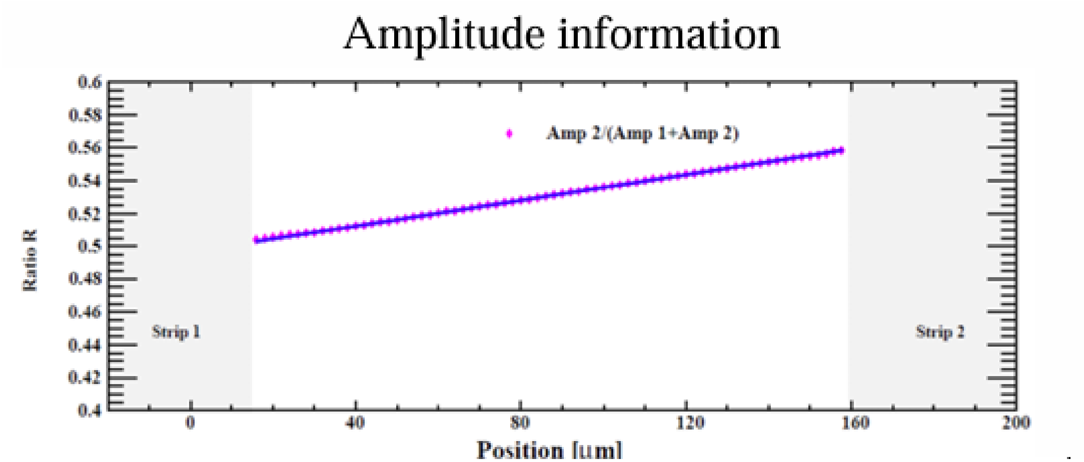
Time residual sigma: 47.1ps
Time resolution: 37.5ps

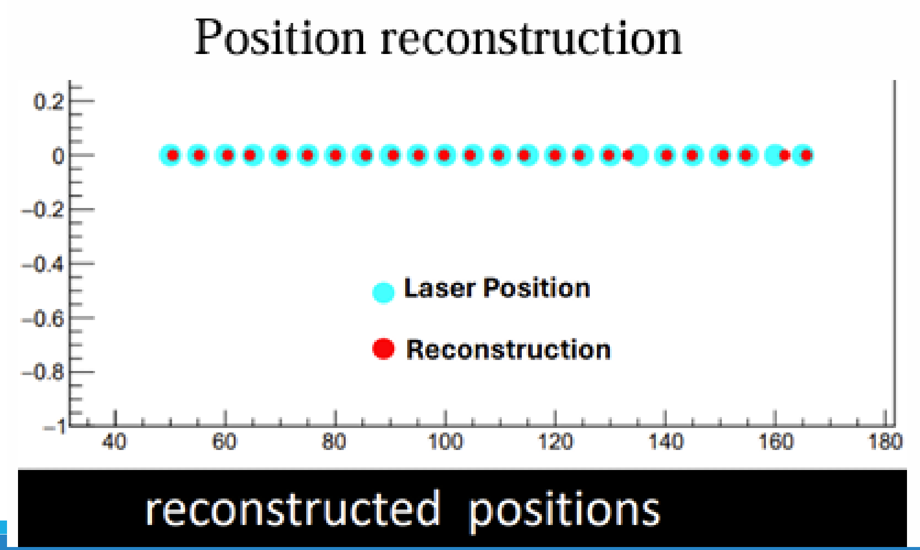
# Strip AC-LGAD R&D

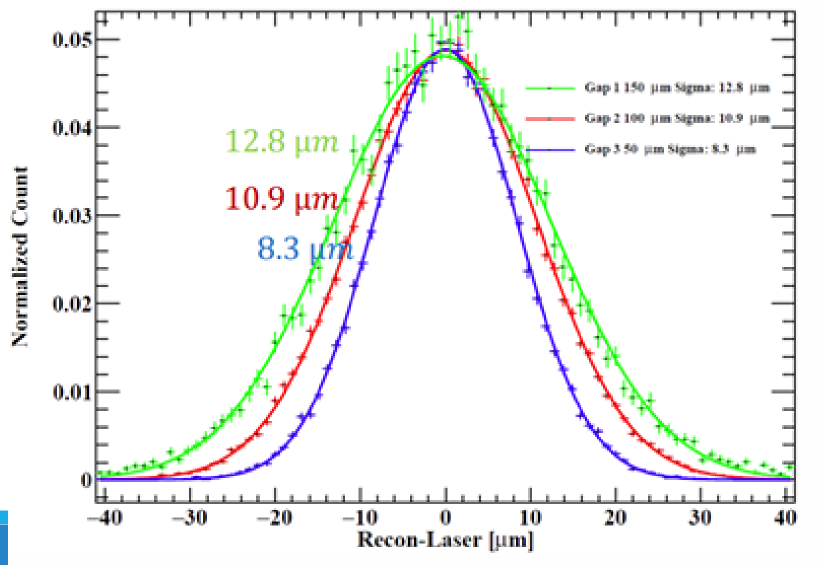
## Strip AC-LGAD: Spatial resolution( Laser testing)

Amplitude information of two electrodes → position reconstruction → Spatial resolution



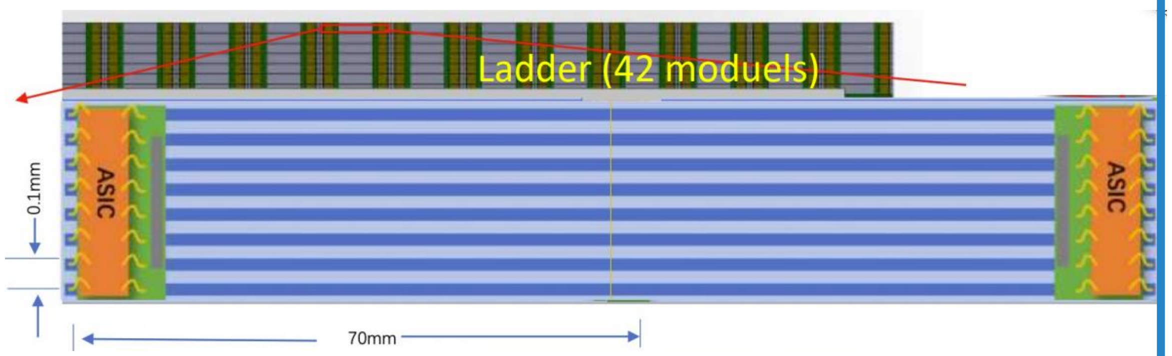




Best result: 8.3um
[Pitch size:150um]

# Proposal of AC-LGAD as OTK&TOF

CEPC OTK&TOF Barrel:



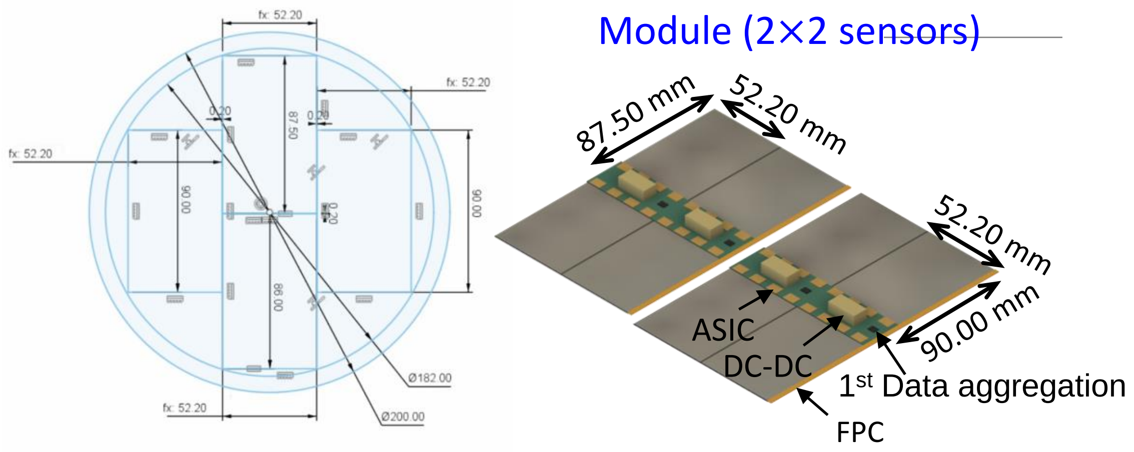

Sensor size: 140mm x 160mm(may change a little)

Strip length: 70mm

Pitch: 100um

Capacitance: 10pF

One 8 inch wafer one sensor
Large capacitance
High ASIC power consumption(20mW/Channel)
Transmission line affect, charge sharing




Sensor size: 87.5 mm x 52.2 mm, 90.00 mm x 52.2 mm

Strip length: 87-90 mm

Pitch: 100um

Capacitance: >10 pF

one 8 inch wafer four sensors
Large capacitance
High ASIC power consumption(20mW/Channel)
Transmission line affect, charge sharing

# Issues or questions

- The discharge of generated electrons through n+ layer may be affected by radiation damage and can change during the lifetime of the detector. → Irradiation hardness
- The capacitance of some sensors will be large (up to ~10 pF) which will make the noise jitter and rise time such that it will be difficult to achieve the desired time resolution. → Timing performance
- Operation of AC-LGADs can be susceptible to high particle rate effects and make sure that you understand that well (also related to size of LGADs).
- For the given pitch and thickness a charge-sharing mechanism and by that the position resolution should be carefully studied for different electrode dimensions taking possible variations of gain layer properties across the large detector into account. → Spatial resolution
- The localized power dissipation at the ASIC should be taken into account in the cooling design and performance evaluation. → ASIC's power consumption

**Recommendations:**

- Reconsider the size of the AC-LGADs and take both the performance (rate effects, time resolution and achievable position resolution) and expected yield into consideration in order to reach a cost effective solution.

**Irradiation hardness:**

DC-LGAD be demonstrated to have very good radiation hardness(TID, neutron, proton) by HGTD groups.

AC-LGAD, TID affect to the dielectric layer (TID Testing)

**Timing resolution:** **capacitance** (power consumption )→ **short length, optimized design**

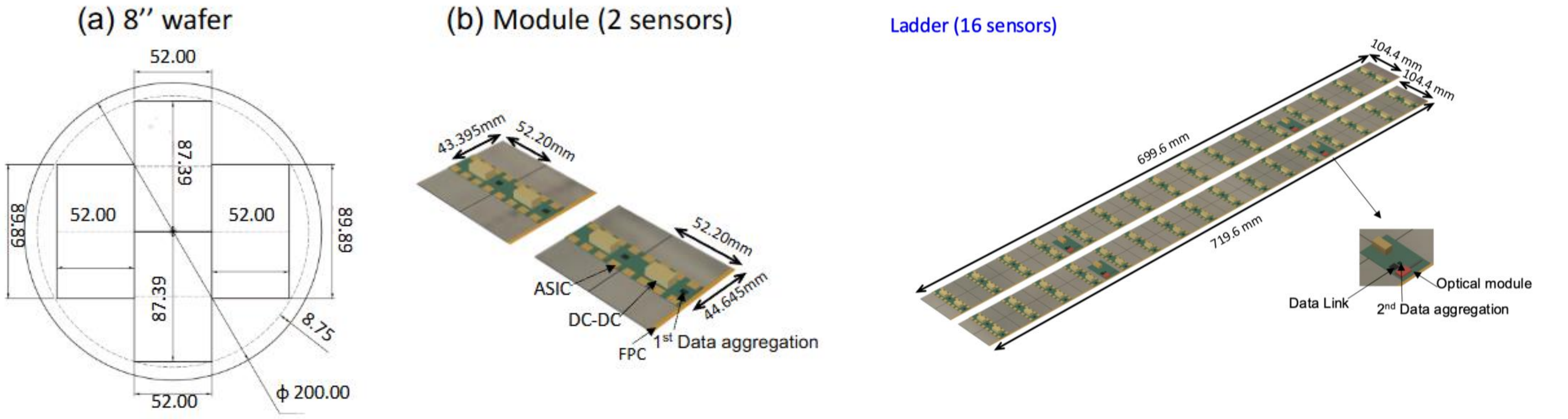
**Spatial resolution:** variation of gain layer, electrode dimensions→ **New design to check this**

**Sensor size**: particle rate, yield → Physics simulation or calculation, yield calculation

**Size < -- > Performance**
**Large size, maintain the performance**

# Proposal of AC-LGAD as OTK&TOF

CEPC OTK&TOF Barrel: Changed by Qi Yan




Sensor size: 87.39 mm x 52 mm, 89.89 mm x 52 mm

Strip length: 43-45mm

Pitch: 100um

Capacitance: 6-7pF

one 8 inch wafer four sensors

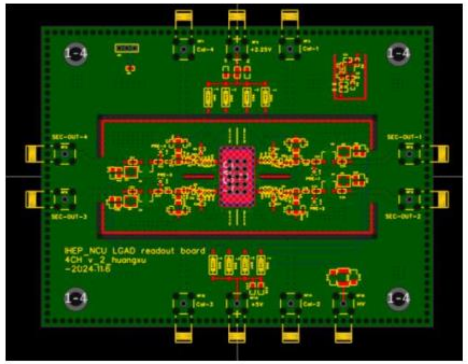
less capacitance, more readout channels, Power consumption?

Transmission line affect, charge sharing

The performance of sensors with ~4cm long strips needs to be demonstrated.

# Plan

## Short term plan: (2024.12-2025.2)



### Simulation:

Simulation of Strip length and its affect (signal shape)

Simulation of method to reduce capacitance (isolation structure)

Simulation of process parameters to optimize spatial resolution (AC coupling capacitor, n+ dose)

### Testing:

Multi-channel readout board with low noise design and fabrication(2 stages of amplifier)

Testing of short strip connected together, radiation testing(TID)

### New submission 1:

Strip AC-LGAD with different length and pad-pitch size, [1cm, 2cm, 4cm] [50um, 100um to 500um]

Strip AC-LGAD with different process parameters: n+ dose, dielectric material and thickness, …

Strip AC-LGAD with different isolation structure →Capacitance

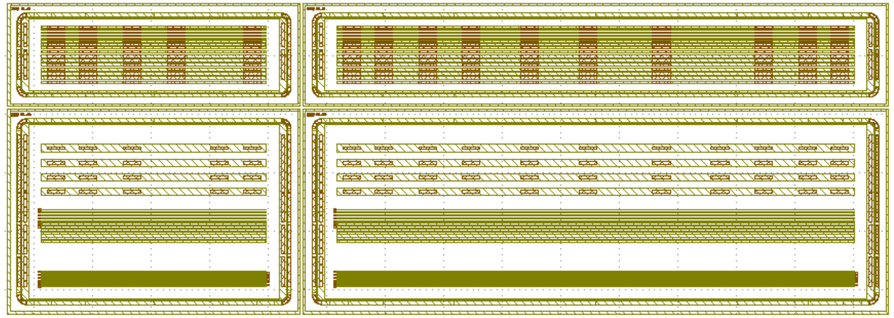
Strip DC-LGAD

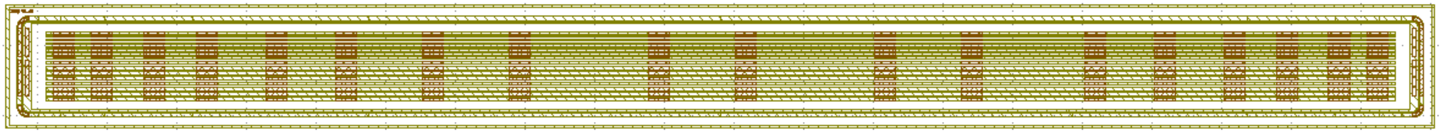
sensors with EPI layer of different thickness(50um, 65um, 80um)

**4cm x 100um pitch**

**2cm x 250um pitch**

**1cm x 500um pitch**





# Plan

## Long term plan

| time | work |
|---|---|
| 2025 | • Testing the sensors from first submission, clarify the sensors performance and requirement (include Test beam and radiation test)<br>• Find out how to optimize the sensor performance(structure and process)<br>• Submission 2<br>Based on the results from first version and more simulation<br>sensors with strip length ~4cm |
| 2026 | • Test of sensors from submission 2(basic properties and together with ASIC and BEE?)<br>• Submission 3<br>large area sensor design and fabrication |
| 2027 | • Submission 4 if needed<br>• module: sensor + ASIC module built and test |

# Collaboration

- **Project be proposed:** DRD3 WG2: LGAD based timing tracker development for electron collider
- **First discussion meeting** be held on Nov. 26th

Good suggestion be given by Gregor and Gordana about the new layout , testing and how to include more institute to join the collaboration.

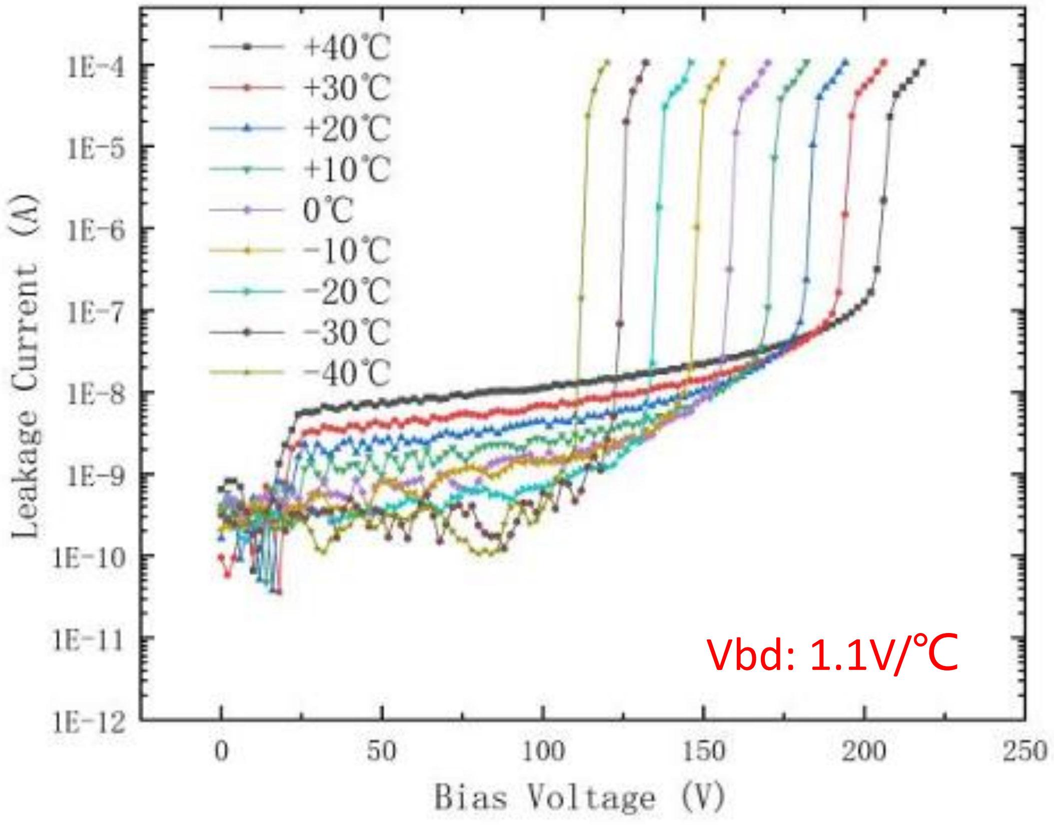
Topic：
1、AC-LGAD simulation, design and fabrication
2、 AC-LGAD testing： IV, CV, timing, spatial resolution, etc
3、AC-LGAD Test beam testing
4、Radiation performance（TID, neutron, proton）
5、Reconstruction methods
6、Design optimization for electron collider
7、Sensor with ASIC(TDC board) testing

- Institute of high energy physics, Chinese Academy of Sciences(IHEP)

  Mei Zhao, Zhijun Liang
- Institute of Microelectronics, Chinese Academy of Sciences(IME)
- Jozef Stefan Institute, Ljubljana (JSI), **Gregor (DRD3 management)**
- University of Montenegro, **Gordana**
- Shanghai Jiao Tong University(SJTU), Kun Liu
- Shandong University (SDU), Kun Hu
- Nankai University (NKU), Bo Liu
- Zhengzhou University (ZZU), Yi Liu

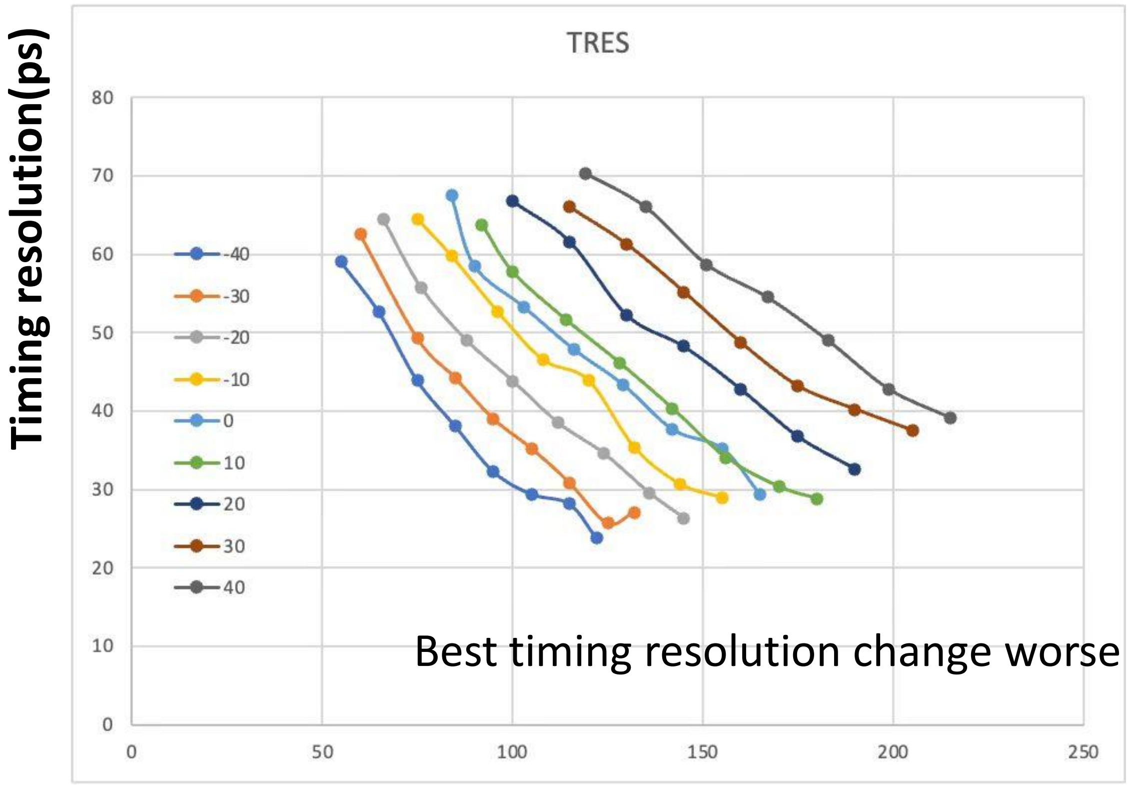
# Backup

LGAD performance with operation temperature changing(before radiation)



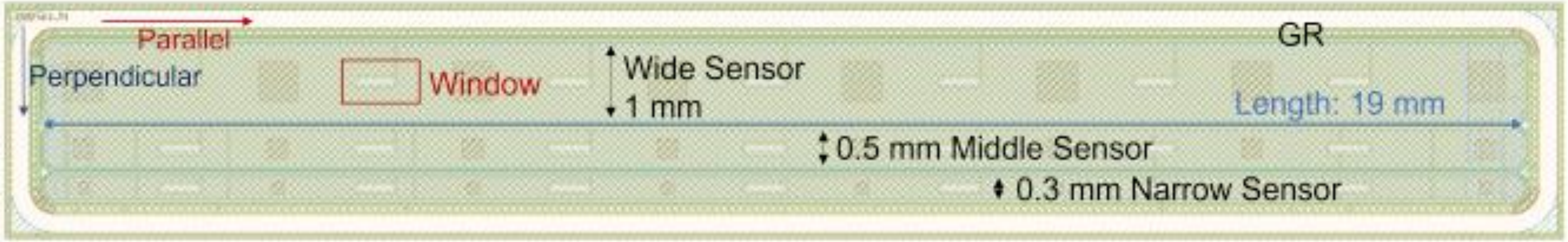

Need to change operation voltage

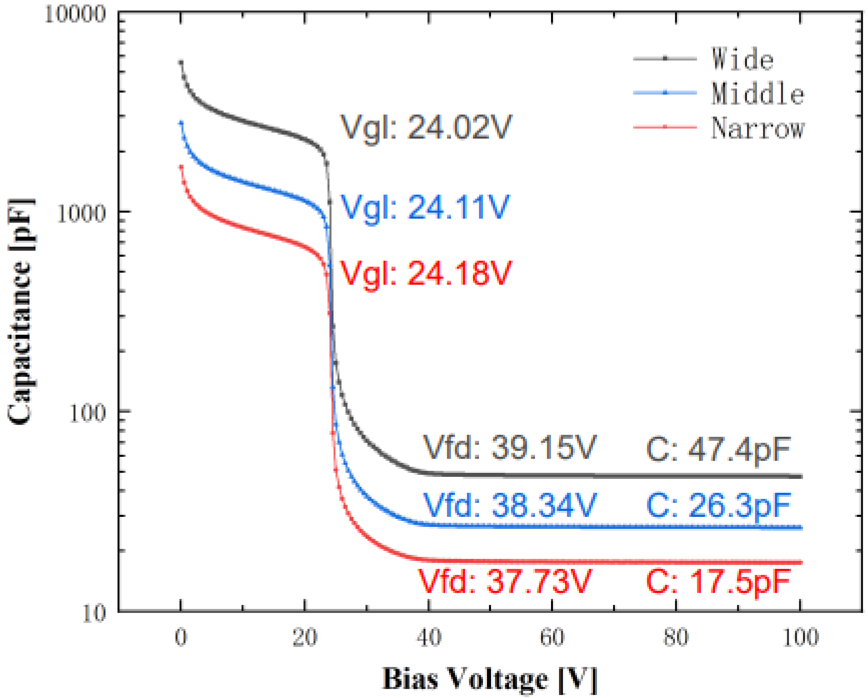
Sr90 testing results

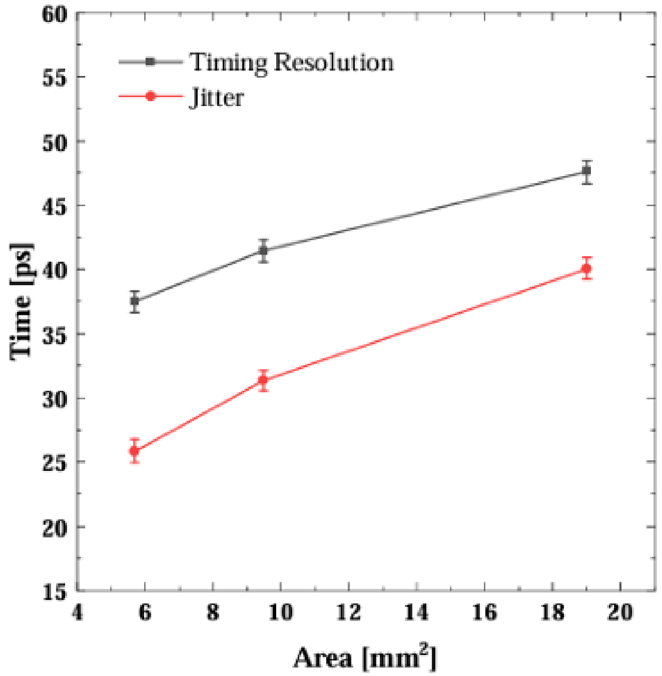


# Backup

DC-LGAD with long strip(1.9cm) and  large capacitance




Sr90 testing results

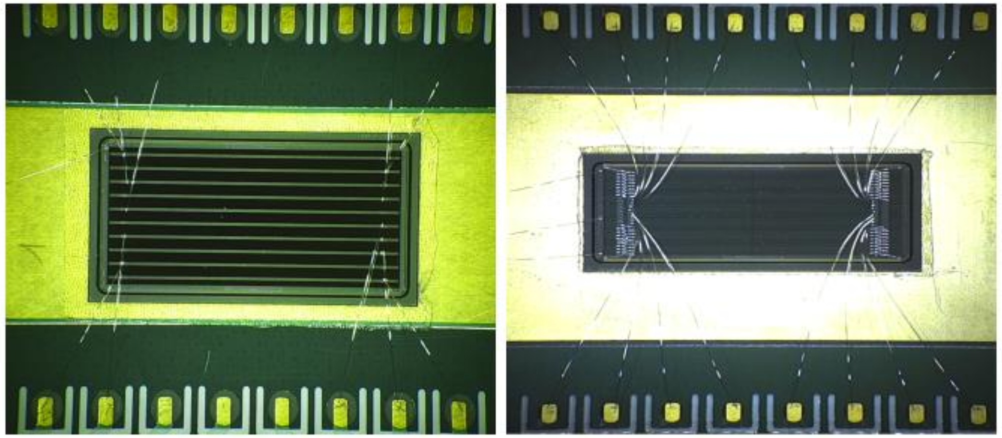
# Backup

HPK
**Strip length:1cm**
**Pitch size:500um**

EIC: barrel strip LGAD baseline design

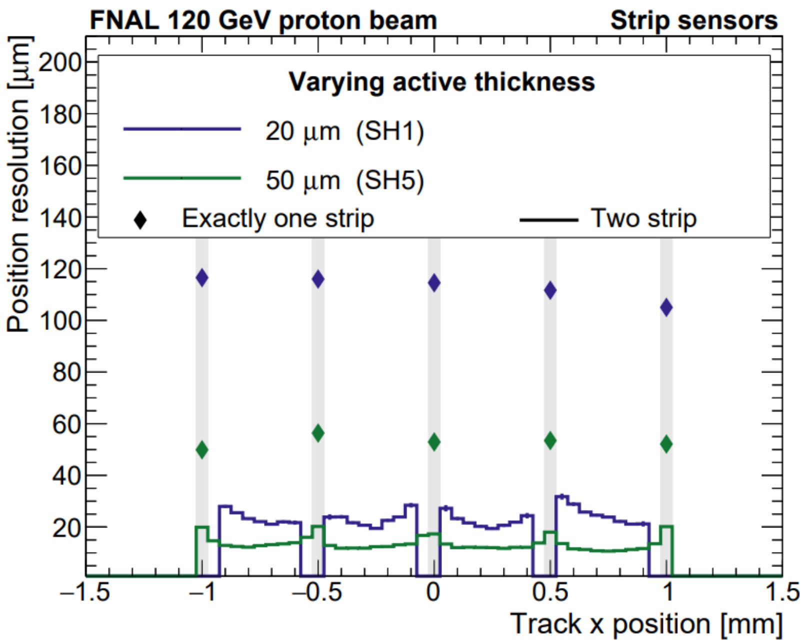
| Name | Wafer | Pitch [µm] | Strip length [mm] | Metal width [µm] | Active thickness [µm] | Sheet resistance [Ω/□] | Coupling Capacitance [pF/mm²] | Optimal bias voltage [V] |
|---|---|---|---|---|---|---|---|---|
| HPK Wide strip | | | | | | | | |
| SH1 | W9 | | | | 20 | 1600 | 600 | 114 |
| SH2 | W4 | | | | | 400 | 240 | 204 |
| SH3 | W8 | | | 50 | 50 | | 600 | 200 |
| SH4 | W2 | 500 | 10 | | | 1600 | 240 | 180 |
| SH5 | W5 | | | | | | 600 | 190 |
| SH6 | W9 | | | 100 | 20 | 1600 | 600 | 112 |
| SH7 | W8 | | | | 50 | 400 | 600 | 208 |
| HPK Narrow strip | | | | | | | | |
| SHN1 | WN1 | 80 | 10 | 60 | 20 | 1600 | 240 | 112 |
| SHN2 | WN2 | | | | 50 | 1600 | 240 | 190 |
| BNL Wide strip | | | | | | | | |
| SB1 | WB1 | 500 | 10 | 50 | 50 | 1400 | 270 | 170 |
| SB2 | WB1 | | | 100 | 50 | 1400 | 270 | 160 |

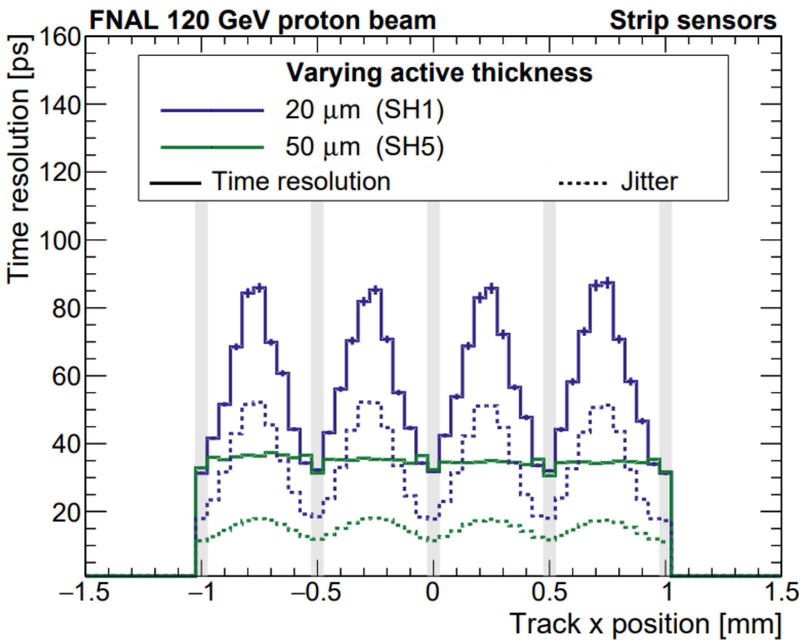
Table 1: Summary table with the name, geometrical parameters, and other characteristics of interest of the strip sensors used in this study.



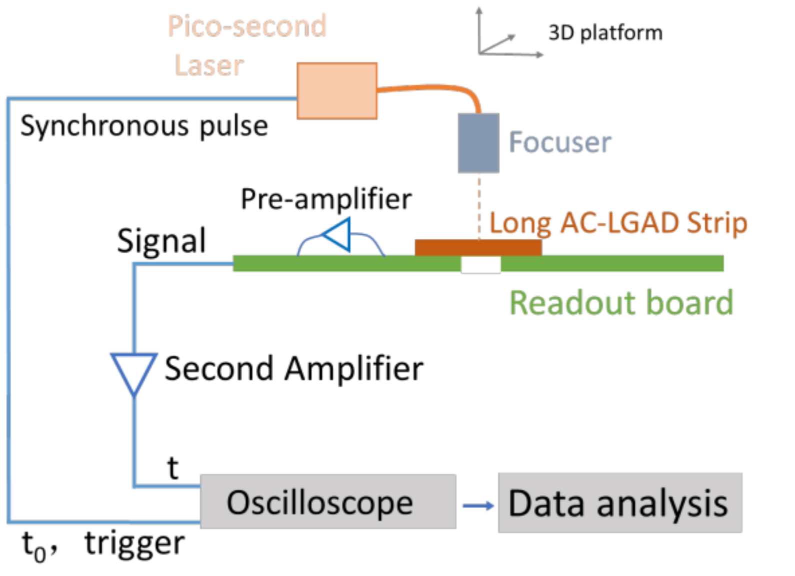
(a) (b)

Results

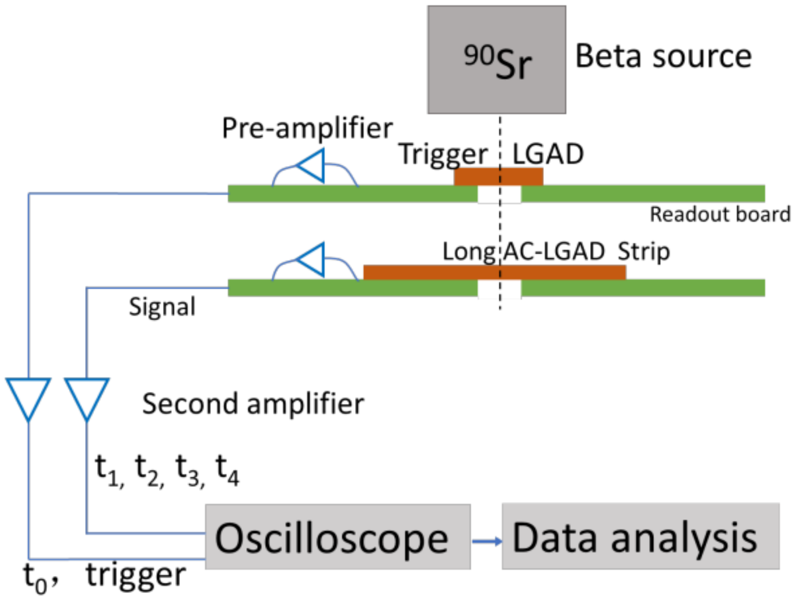


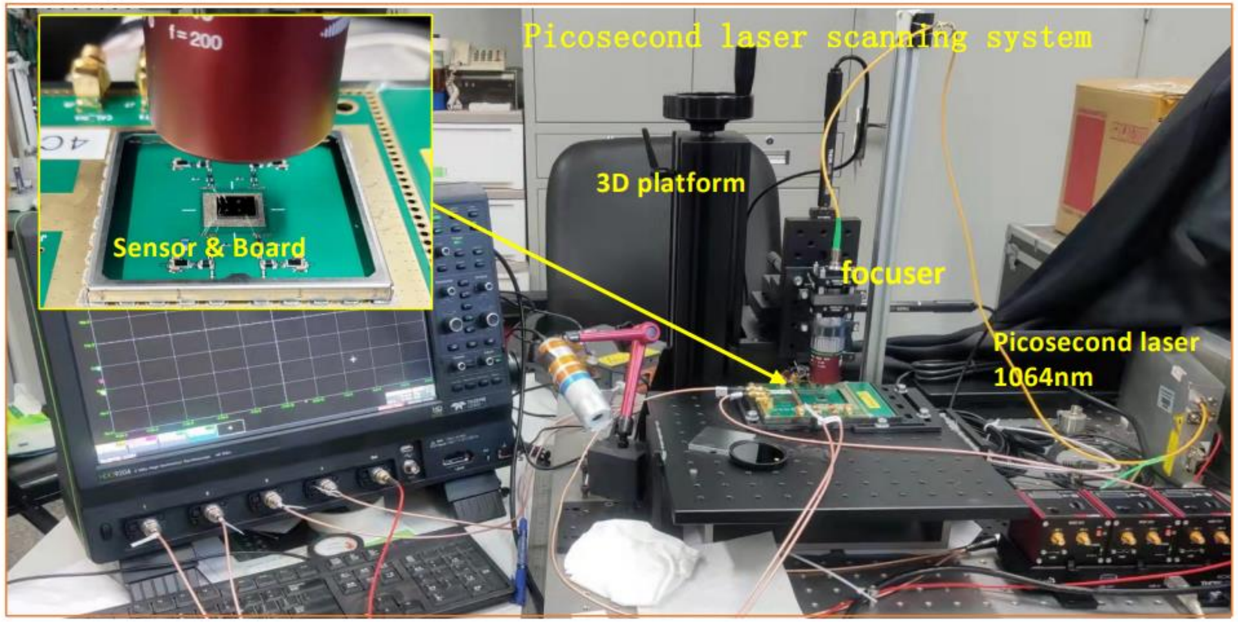
# Testing setup




(a)



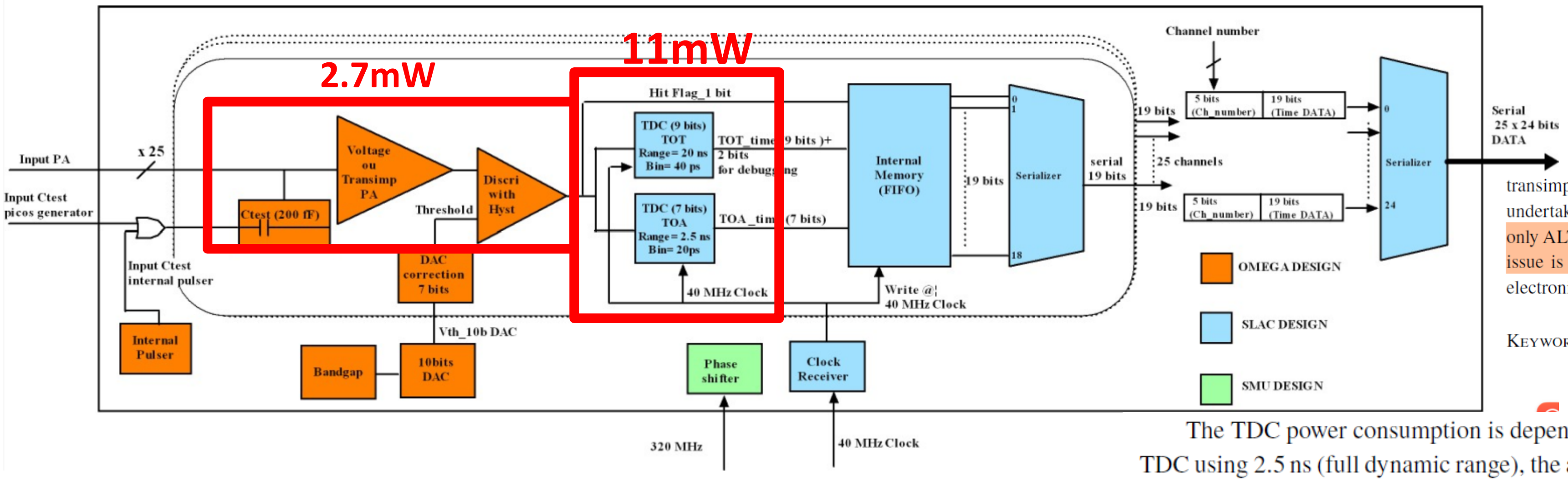

(b)




Picosecond laser scanning system

- Displacement accuracy 1 μm
- Automated scanning
- Picosecond laser 1064nm
- Spot size 2~5 μm

# ALTIROC power consumption



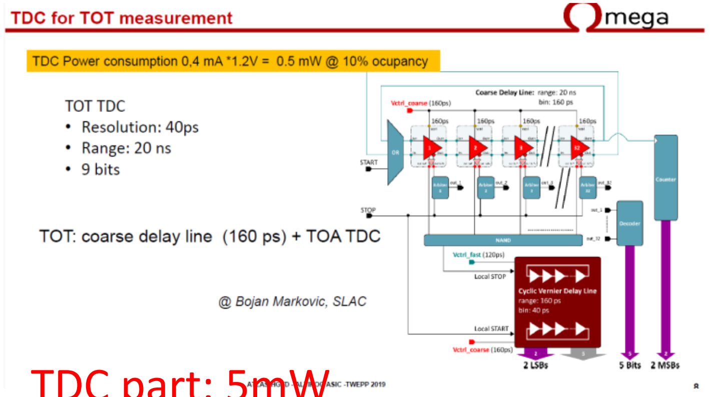

**By Xiongbo Yan**

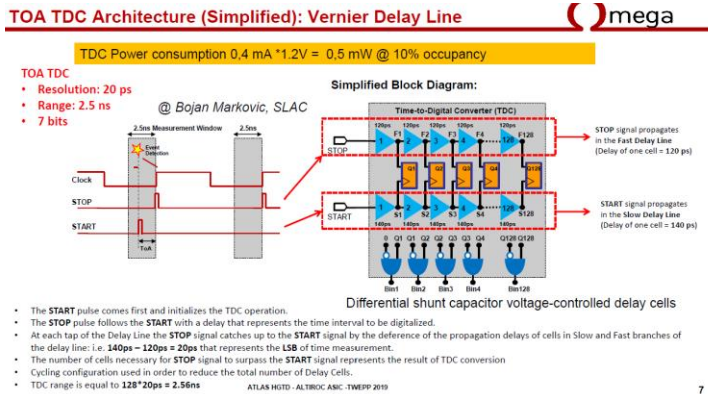
transimpedance preamplifiers. Beam test measurements with a pion beam at CERN were also undertaken to evaluate the performance of the module. The best time resolution obtained using only ALTIROC TDC data was 46.3 ± 0.7 ps for a restricted time of arrival range where the coupling issue is minimized. The residual time-walk contribution is equal to 23 ps and is the dominant electronic noise contribution to the time resolution at 15 fC.

KEYWORDS: Front-end electronics for detector readout; Timing detectors

The TDC power consumption is dependent on the time-interval being measured. For the TOA TDC using 2.5 ns (full dynamic range), the average power consumption over the 25 ns measurement period is about 5.2 mW. It is only 3.5 mW for a time-interval equal to half the dynamic range. Thanks to the reverse START-STOP operation, the power consumption of the TDC is much lower in the absence of a hit over threshold. This results in an average power consumption per channel of 1.1 mW for both TDCs, assuming a time interval uniformly distributed (1.25 ns average) and a maximal channel occupancy of 10%.

Both preamplifiers are built around a cascoded common source NMOS amplifier to ensure high bandwidth (see figure 2). The drain current ($I_d$) of the input transistor is adjustable between 200 μA and 1 mA. The transistor size is optimized to operate close to weak inversion while keeping its capacitance small compared to that of the sensor. The operating current is chosen to minimize the series noise while not dissipating too much power (< 2.25 mW/ch for the analog part). A PMOS follower is added to isolate the load from the discriminator. The total preamplifier power consumption is 0.85 mW using a nominal current $I_d$ = 600 μA in the input transistor. A bank of seven capacitors (from 0 to 3.5 pF) can be connected by slow control to the preamplifier input to emulate the sensor capacitance when measuring the ASIC alone. They are not used when the ASIC is connected to the LGAD sensor array.




TOA measurement. Each discriminator output is sent to a sampling cell to generate a "Hit Flag" bit, that is equal to 1 in case of a hit or to 0 in case of no hit. The discriminator's power consumption is slightly less than 0.4 mW.

ALTIROC Cd： 4pF

OTK Cd： 10pF

FEE power consumption: 15mW

$$\sigma_{\text{jitter}} = \frac{e_n C_d}{Q_{\text{in}}} \sqrt{t_d}.$$

$$e_n = \sqrt{2kT/g_{m1}}.$$

$$g_{m1} = q \times I_d / 2kT$$

TDC part: 5mW

Not include Clock system and other digital part