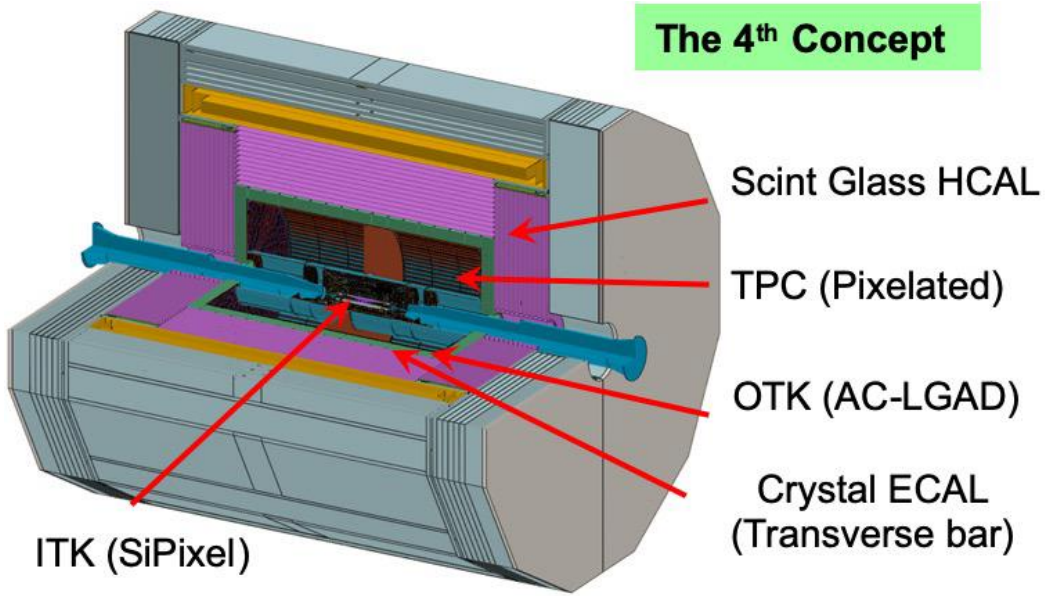
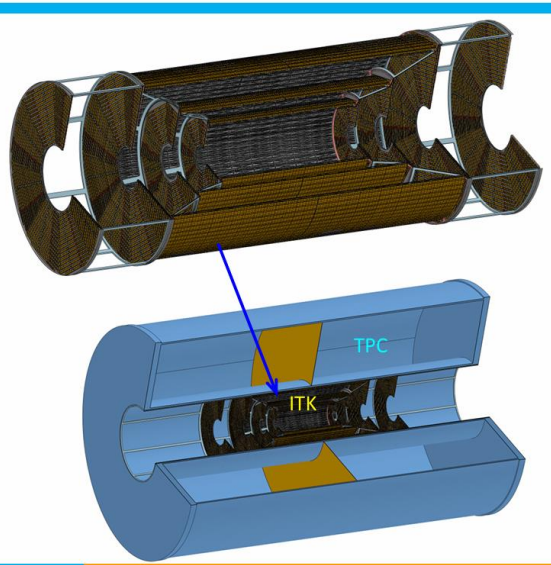
CEPC ITK/OTK Survey

10/31/2024

dongsheng@ihep.ac.cn



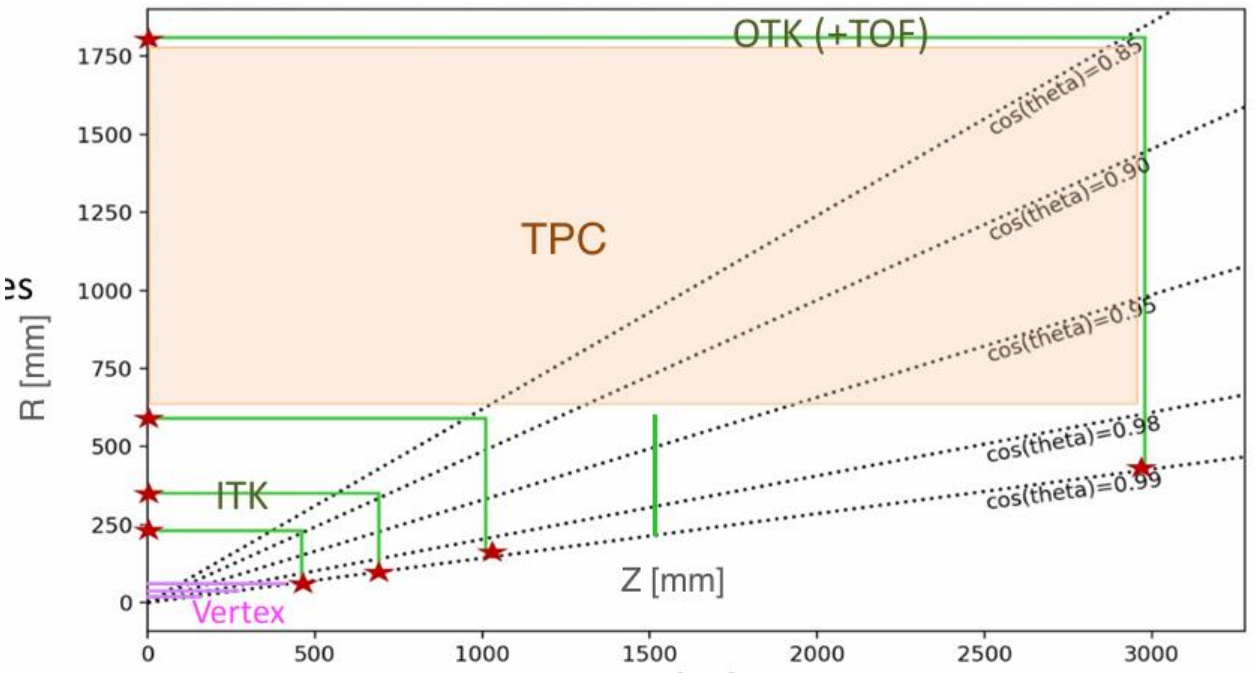
CEPC ITK Mechanics and Installation Design

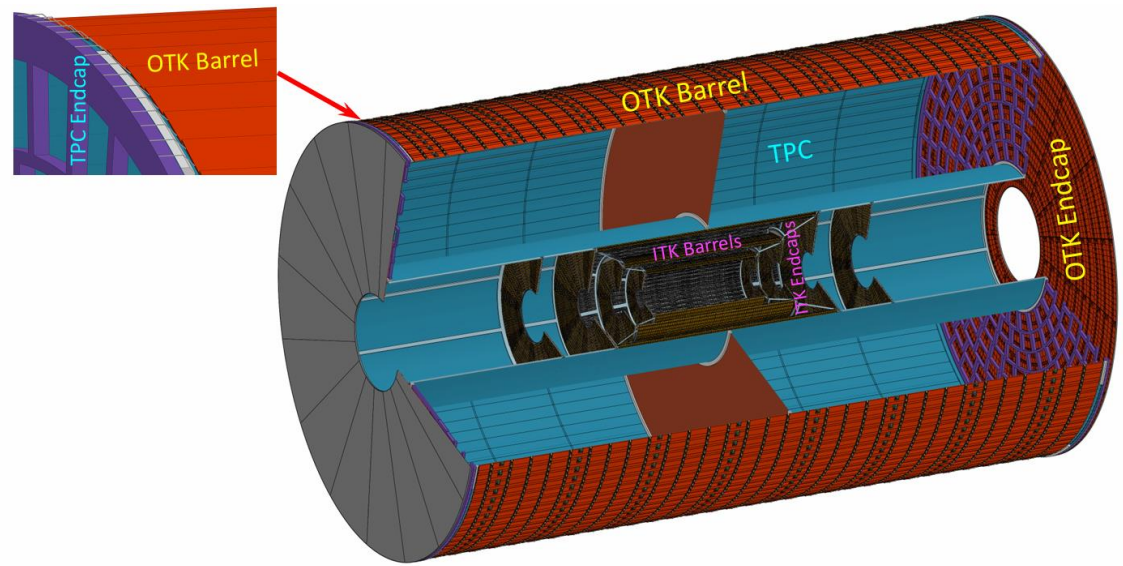


	Sensors	Sensor area
Barrels		
ITKB1	3,920	1.6 m²
ITKB2	7,840	3.1 m²
ITKB3	18,032	7.2 m²
Total	29,792	11.9 m²

Endcaps		
ITKE1	1,536	0.74 m²
ITKE2	3,136	1.51 m²
ITKE3	8,288	4.00 m²
ITKE4	7,520	3.63 m²
Total	20,480	9.89 m²

16





21

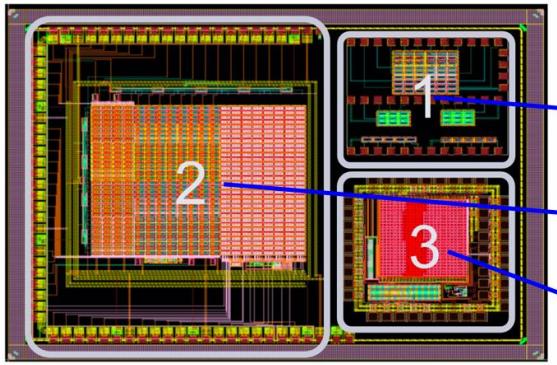
OTKB ~ 70 m^2, OTKE ~ 20m^2

HVCMOS R&D for ITK

R&D: CMOS Chip Development

- CMOS pixels (COFFEE2): SMIC 55 nm CMOS process

  Submitted in Aug 2023, received in Dec 2023

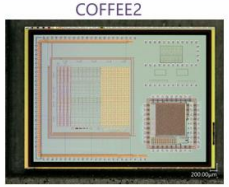


COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

KIT

COFFEE2



Three sections in the chip:

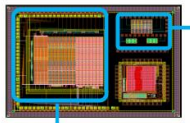
1: Passive diode arrays:
- Including 6 different signal collection structures for studying diodes and charge sharing.

2. Pixel arrays with diodes and in-pixel electronics:
- Features 6 types of diodes and 3 types of in-pixel electronics.

3. Pixel arrays with peripheral digital readout:
- Used for validating readout strategies

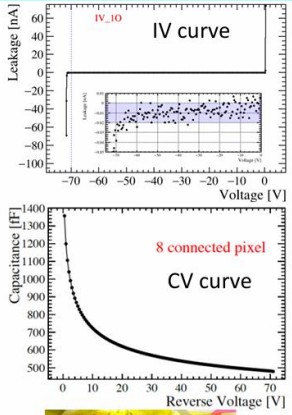
The COFFEE2 chip test is progressing well, the tape-out of the first CMOS strip chip (CSC1) for CEPC is scheduled for submission in 1-2 months.

HVCMOS (COFFEE2) Chip Test

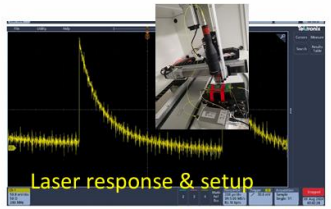


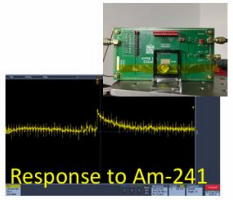
- So far tests have been focused on passive diode arrays
  - IV (breakdown at –70 V)
  - CV (single pixel ~30-40 fF)
  - Leakage current increased from 0.01 nA to ~1 nA after $10^{14} n_{eq}/cm^2$ radiation
  - Laser response observed
  - Radioactive source observed

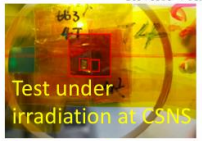
- Circuit test almost ready
  - Carrier board fabricated
  - Caribou system installed, final firmware debugging




Caribou setup

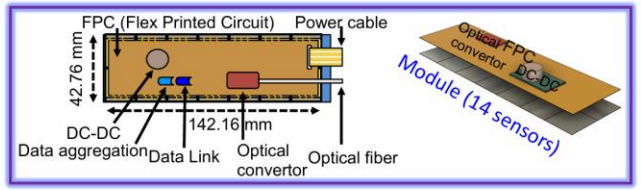

Laser response & setup

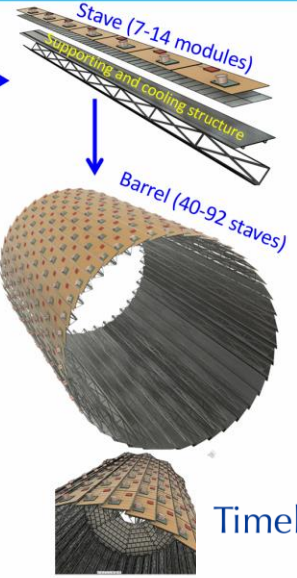

Response to Am-241


Test under irradiation at CSNS

The tape-out of the next HVCMOS (COFFEE3) chip is planned for the first half year of 2025.

CEPC ITK Barrel Design (HVCMOS Pixels)

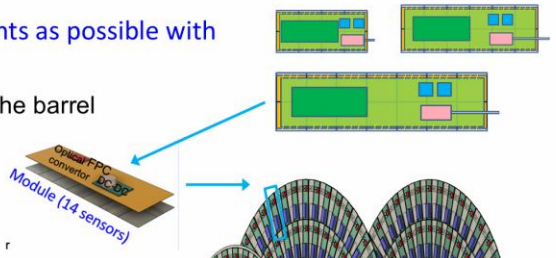


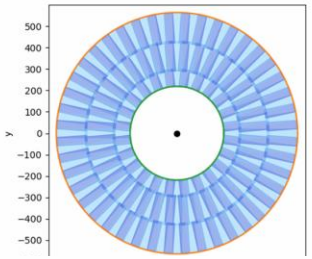


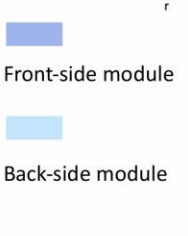
- HVCMOS pixels for CEPC:
  - Utilizes 55 nm process
  - Wafer resistivity: 1k-2k Ω·cm
  - Chip size: 2 cm × 2 cm
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm
  - Time resolution: 3-5 ns
  - Power consumption: ~200 mW/cm²

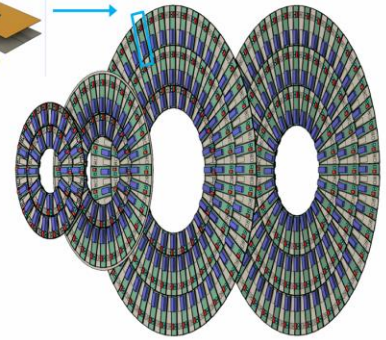
Preliminary endcap design using pixels

- Endcap using HVCMOS share as many components as possible with the barrel
  - 3 types of modules, one of which the same as the barrel
  - 516 modules, 6576 chips in total
  - Division into 8 or 4 sections possible

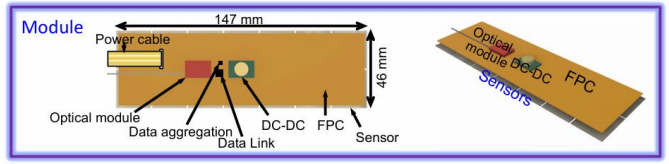


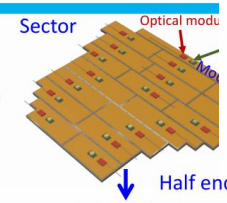






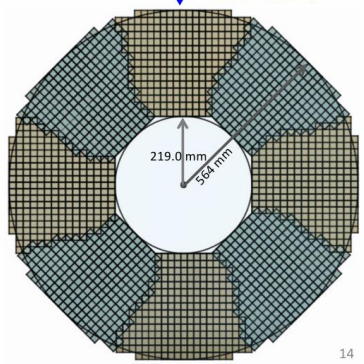
CEPC ITK Endcap Design (CMOS Strips)



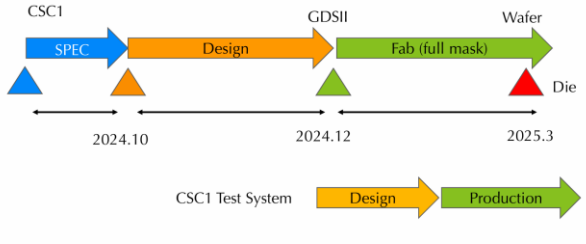


- CMOS Strip Chip (CSC) for CEPC:
  - Utilizes 180 nm process (CSMC, Wuxi Shanghua)
  - Wafer resistivity: 2k Ω·cm
  - Chip size: 2.1 cm × 2.3 cm
  - Strip number per chip: 1,024
  - Strip pitch size: 20 μm (spatial resolution <5 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~80 mW/cm²

Each half endcap is divided into 8 sectors, with each sector consisting of CMOS strip modules. The overlapping areas between the neighboring sectors are designed to be minimal.



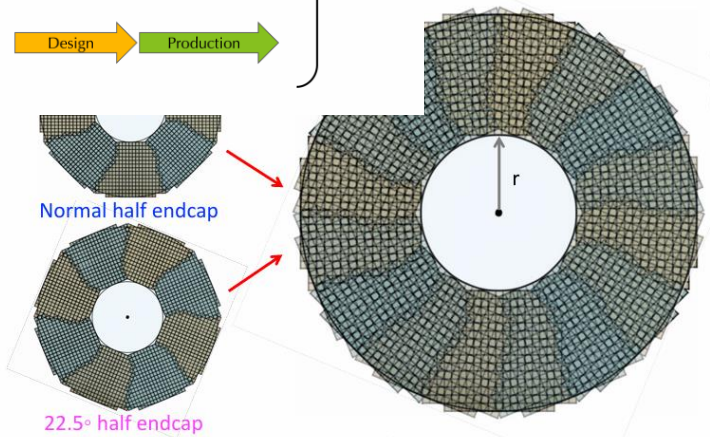
Timeline for CSC1

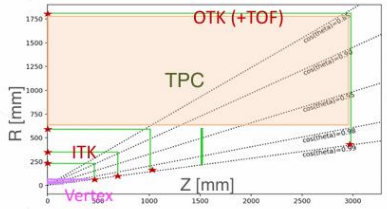


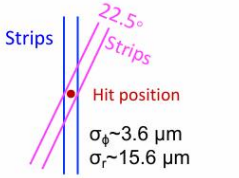
CSC1 Test

ap Design (CMOS Strips)

other to form one complete endcap:







Detection precision using 20 μm pitch strips

The CEPC ITK barrels using pixels is considered for minimal material, while ITK endcaps using strips is optimized for high momentum measurement and particle identification (no TPC).

Poster ID: 344

The 2024 international workshop on the high energy Circular Electron-Positron Collider (CEPC) , Hangzhou, Oct 22 – 27, 2024

Geometry implementation of CEPC Tracker in CEPCSW and full simulation validation

Xiaojie Jiang (姜啸捷)
on behalf of the CEPC ITK working group

Contact:
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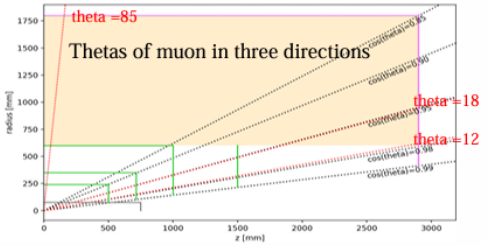
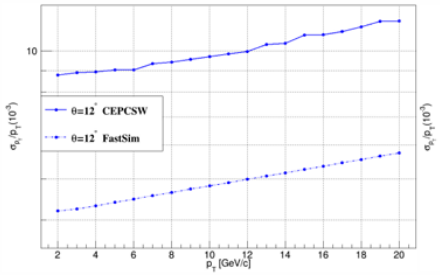
Institute of High Energy Physics,
Chinese Academy of Sciences

3. ITK momentum resolution

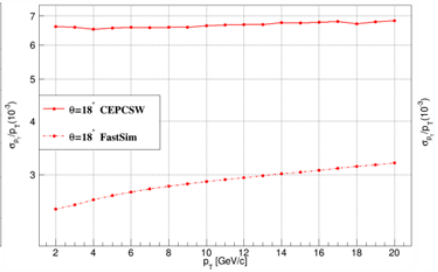
- Setting
  - Momentum resolution studied using muon events in range [2,20] GeV, for each momentum point 30k events are generated
- Three geometrical regions are studied separated



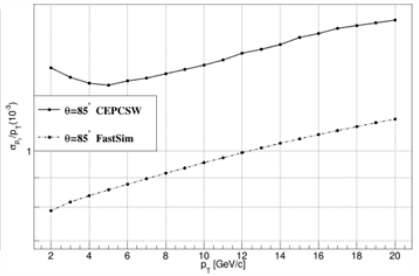
Theta = 12°, Only-ITKE



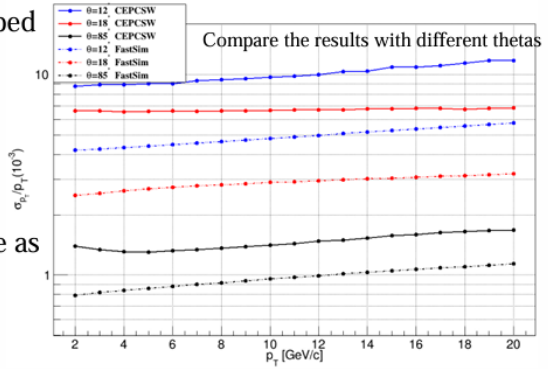
Theta = 18°, ITKE + part TPC



Theta = 85°, ITKB + TPC

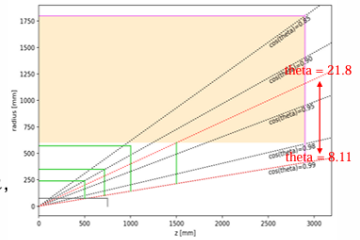


- FastSim : a matlab fast simulation package developed by Wiener group
  - Data provided by Qinglin Geng
  - A reference
- CEPCSW results have the **similar trends** with FatSim
- The pT resolution of full CEPCSW is about twice as bad as FastSim, but still meet CDR requirements
- Need further study: a strange lift at the low momentum end of full simulation

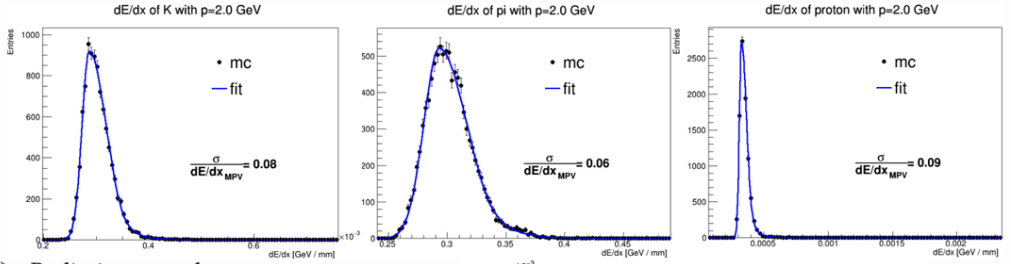


5. PID capacity of ITK endcap

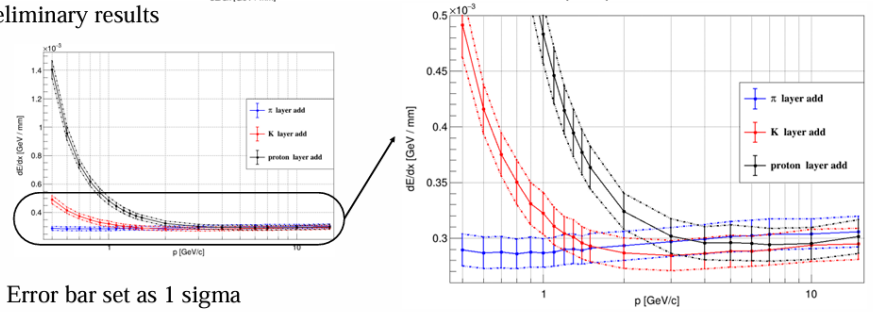
- Setting
  - 4 **double-layers** ITKE, **300μm** silicon per layer
  - Particles: e-, mu-, pi-, K-, proton, but not show e-, mu- results here
  - Momentum: 19 points in 0.5 - 15 GeV
  - Theta: 8.11° - 21.8°, to make sure only ITKE hit
  - 10k events to get Most Probable Values of $\sum \frac{dE}{dx}/hits\_num$, **removed the outlier** for every track



- Fitting
  - dE/dx distribution fitted by crystal ball PDF, examples @ p = 2 GeV



- Preliminary results

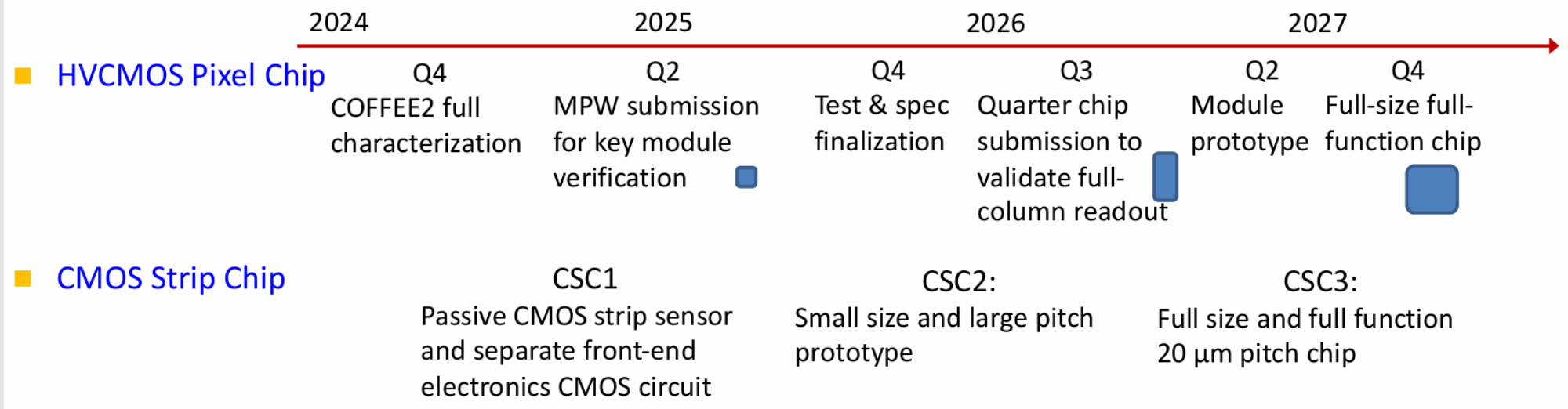


- Error bar set as 1 sigma
- Can distinguish kaon, pion, proton when momentum < 1GeV
- No distinguishing power for any particles with p > 2 GeV

Summary

- The design of silicon inner tracker in preparation of the CEPC reference detector TDR is proposed, based on R&D of advanced detector technologies
- A lot more development in sensor technology, electronics, mechanics and physics benchmarking expected, for the Ref-TDR and beyond
- Collaboration & your participation welcome

Working Plan



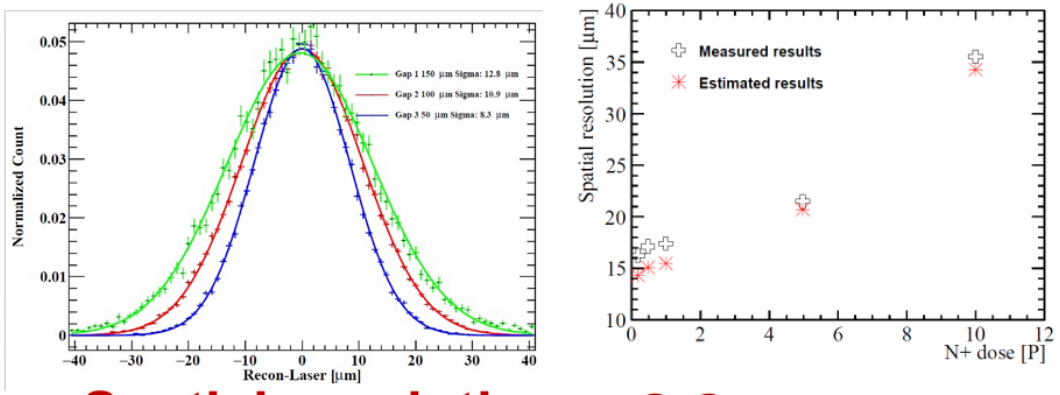
Poster #49

Design of AC-LGAD for CEPC Outer Tracker (OTK)

Weiyi Sun[1 2] (sunwy@ihep.ac.cn), Mei Zhao[1], Mengzhao Li[1], Yunyun Fan[1], Zhijun Liang[1]

1.Institute of High Energy Physics, CAS 2. University of Chinese Academy of Sciences

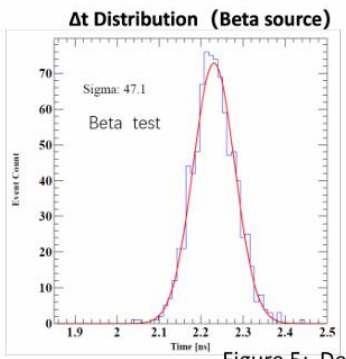
The spatial resolution of the strip AC-LGAD were tested by the Laser. The spatial resolutions of strip AC-LGADs with different pitches (150 μm, 200 μm and 250 μm) are 8.3 μm, 10.9 μm and 12.8 μm



Spatial resolution： 8.3 μm with 150 μm pitch

Figure 4: (Left) Distribution of the difference between the reconstructed position and the true position under different pitches.
(Right): Relationship between spatial resolution and gain layer concentration.

The time performance of the strip AC-LGAD were tested by the Beta source. The delta t was the difference between the arrival time of the trigger and the AC-LGAD. The sigma of the delta t distribution is combination of the time resolution of trigger and AC-LGAD. Thus according to the formula, the time resolution of **the whole AC-LGAD** is 37.5 ps.



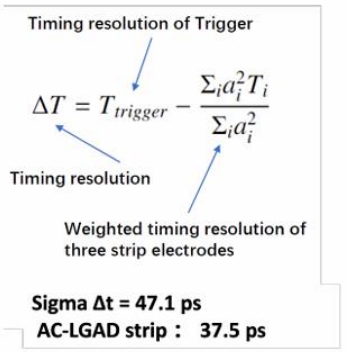


Figure 5: Delta t distribution of AC-LGAD at the Beta test

Time resolution: 37.5 ps

LGAD sensor development:

From ATLAS high granularity timing detector to future collider

MEI ZHAO

INSTITUTE OF HIGH ENERGY PHYSICS, CAS

2024-10-24

CEPC OTK Barrel Design (AC-LGAD Strips)

- CEPC outer silicon tracker (OTK) utilizes AC-LGAD (Low Gain Avalanche Detector) developed by IHEP-IME:
  - Sensor size: 8.75 cm × 5.22 cm
    9.00 cm × 5.22 cm
  - Strip number per sensor: 512
  - Strip pitch size: 100 μm
  - Spatial resolution: 10 μm
  - Time resolution: 50 ps
  - Power consumption: ~300 mW/cm^2

Maximum usage of silicon wafers for OTK barrel: a total 3,520 wafers, with 15% higher efficiency compared to a conventional single-piece sensor cut from a wafer.

LGAD sensor development:

From ATLAS high granularity timing detector to future collider

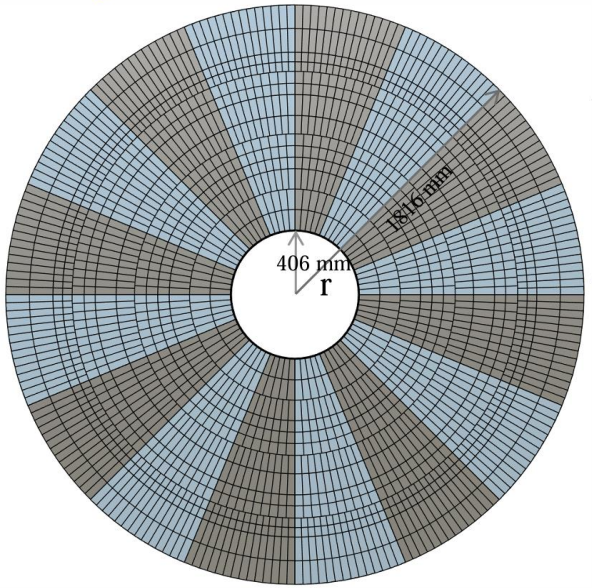
MEI ZHAO

INSTITUTE OF HIGH ENERGY PHYSICS, CAS

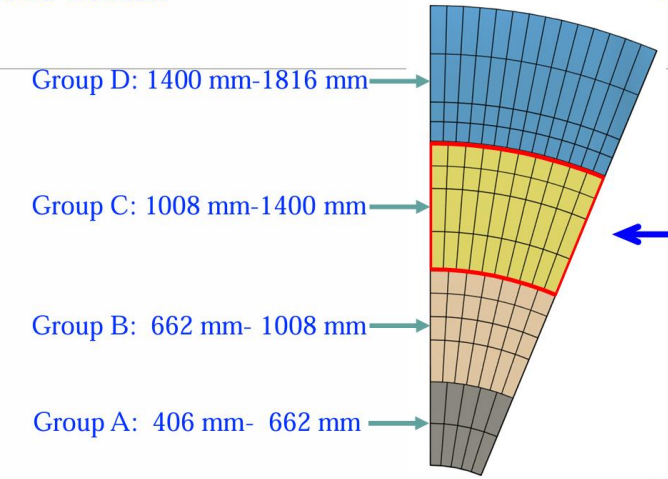
2024-10-24

CEPC OTK Endcap Design (AC-LGAD Strips)

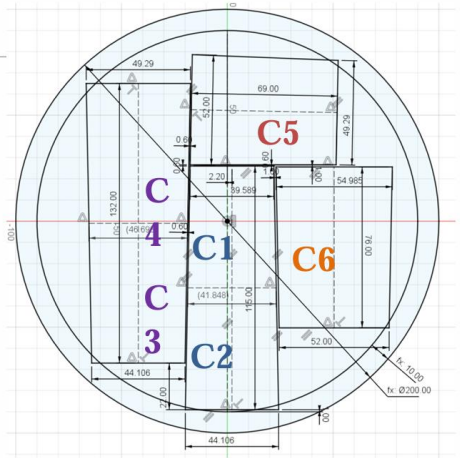
Endcap (16 sectors, 10 m^2):



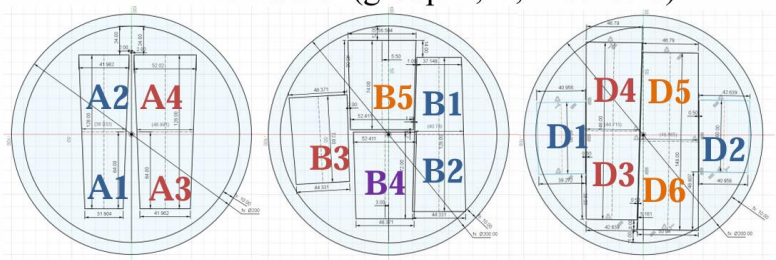
1/16 Sector:



Sensor: 8” wafer (group C sensors)



8” wafer (group A, B, D sensors)



- OTK endcap consists of 14 rings, arranged into 4 groups.
- Each group contains 2-4 types of trapezoid sensors, which can be fitted to one 8’’ silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
- The long sensor contains 2 sets of short-strip sensors.

Maximize the use of silicon wafers and facilitate detector assembly.

PosterID 346

Simulation result of CEPC OTK with CEPCSW

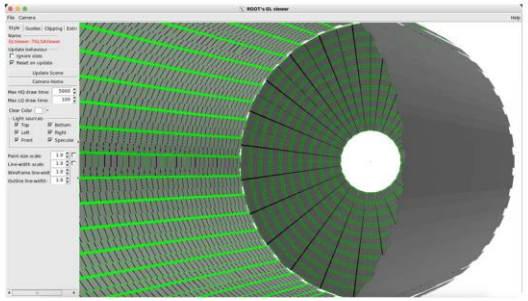
Dian Yu, on behalf of the ToF team

The 2024 international workshop on the high energy Circular Electron Positron Collider

TSUNG-DAO LEE INSTITUTE

CEPCSW Progress for ToF&out tracker

- Got the geometry of barrel and endcap into CEPCSW
  - Good for full simulation and future physics performance study
- Estimated the maximum occupancy: 0.35% at z pole, OK

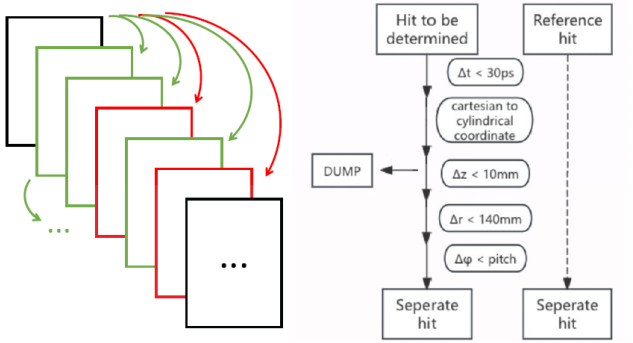


Details in Dian Yu's poster

Simulation

CEPCSW The geometry design of OTK is added to /Detector/DetCRD/compact/CRD_common_v01/ and simulation truth details will be saved into OTKBarrelCollection and OTKEndcapCollection.

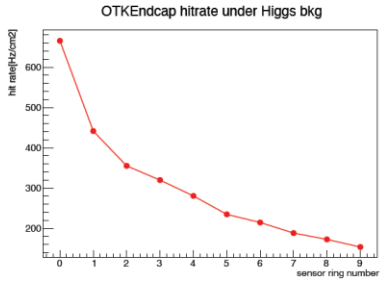
Hit Rate Utilizing new geomerty in CEPCSW, 10000 and 2000 hits are simulated for Higgs and Zpole background, respectively. Priliminary results are given with truth information with a algorithm as follows. Further developing in adding detailing structure to the detectors in the future will give out more precise result.

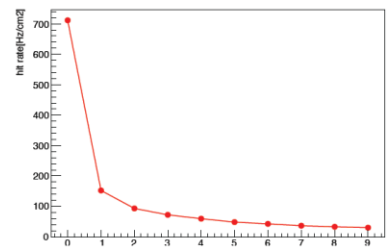


Results

Higgs By calculation, higgs bkg has maximum hit rate of 665.6Hz/cm², average hit rate of 253.7Hz/cm². The maximum electronic occupancy is 0.35%.

Zpole This bkg is still under optimization. Maximum hit rate is 711.594kHz/cm² and average 81.131kHz/cm².





CEPC Inner Tracker towards Ref-TDR

LI Yiming 李一鸣
on behalf of the CEPC Silicon Inner Tracker team

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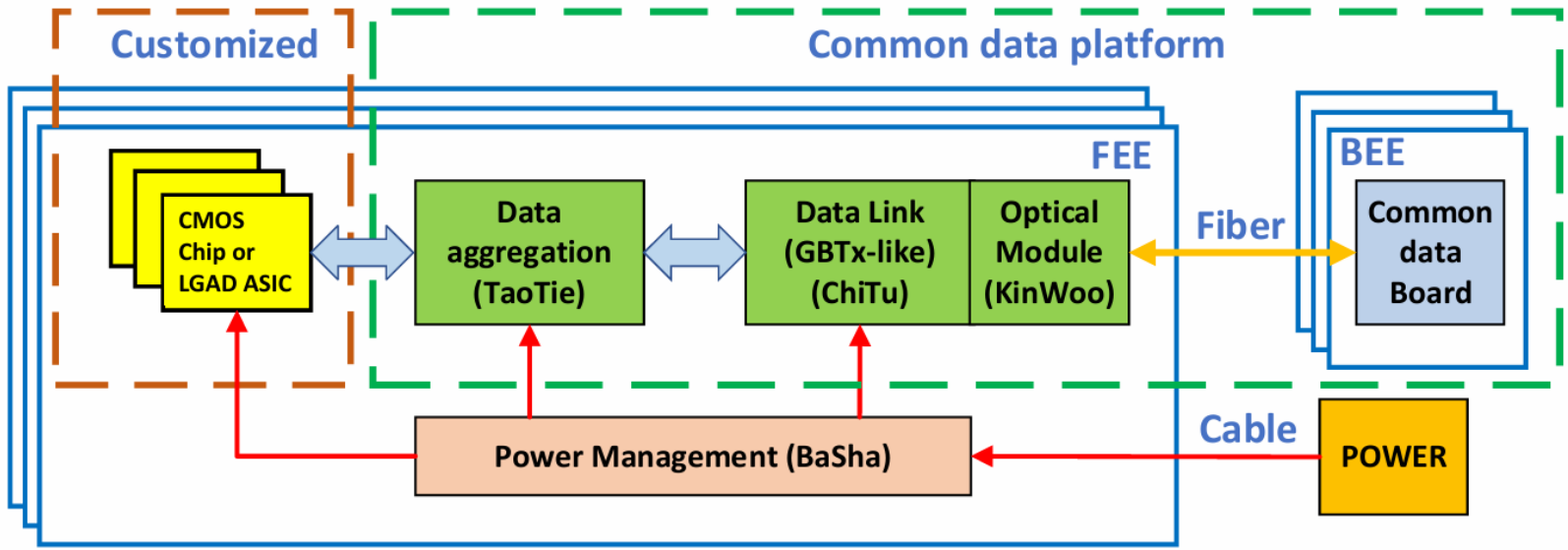
Silicon Tracker Common Electronics



- Data transmission: common data platform
- Trigger mode: triggerless

Requirement from Sub Detectors (@Higgs)

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit	42bit	32bit	40~48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg: 2.9Mbps/chip Max: 3.85Mbps/chip	Avg: 38.8Mbps/chip Max: 452.7Mbps/chip	~70Mbps/module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)	Needs detector finalization	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	Needs detector finalization	Needs detector finalization
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	Needs detector finalization
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization

CEPC ToF & Outer Trakcer Detector

Yunyun Fan on behalf of ToF & Outer tracker detector group

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Summary and Working plan

- **Designed an AC-LGAD based detector as ToF + Outer Traker for CEPC**
  - **50 ps** time resolution and **10 μm** spatial resolution (4D detector)
  - aim to design **70 mm** long strip AC-LGAD
  - cover the barrel and endcap region: **~90 m²**
- **Prototype**: AC-LGAD sensor with **5.6mm** strip length and **150 um** pitch, timing resolution is **37.5 ps** (Beta test), spatial resolution is **8.3 μm** (laser test).
- **Working plan for ToF & Outer Tracker**
  - Optimized the barrel and endcap design
  - Test beam for the long strip AC-LGAD
  - Sensor design: 3 steps (20mm, 40mm, 70 mm) towards the large area, long strip, sector sensor
  - High precision electronics optimization, such as the power consumption
  - Design and Optimize the cooling system (cooling pipe et. al.)
  - Physics performance study
  - **A lot to be done…**

Welcome to join us !

Working Plan

2024 2025 2026 2027

- HVCMOS Pixel Chip

2024 Q4	2025 Q2	2026 Q4	2026 Q3	2027 Q2	2027 Q4
COFFEE2 full characterization	MPW submission for key module verification	Test & spec finalization	Quarter chip submission to validate full-column readout	Module prototype	Full-size full-function chip



- CMOS Strip Chip

CSC1	CSC2:	CSC3:
Passive CMOS strip sensor and separate front-end electronics CMOS circuit	Small size and large pitch prototype	Full size and full function 20 μm pitch chip

- AC-LGAD Sensor and ASIC

Towards large area, long strip, and sector (trapezoidal) sensor

20 mm 40 mm 80 mm

Towards development of high precision, low-power consumption AC-LGAD ASIC