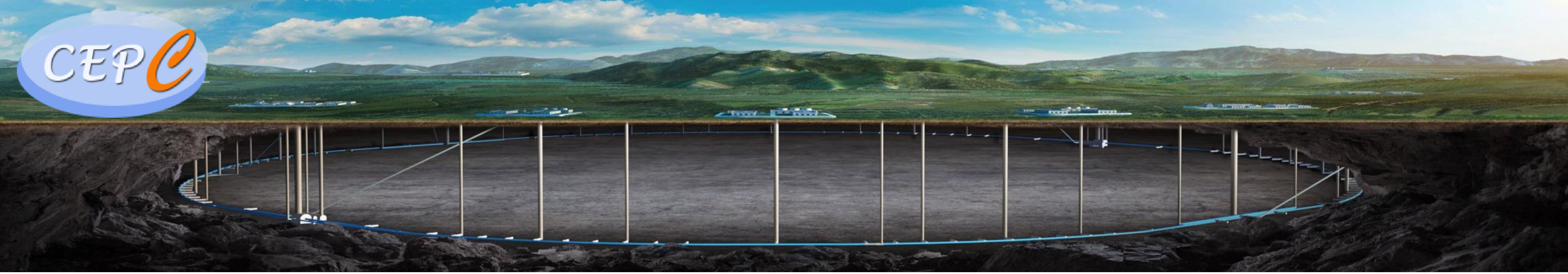


CEPC TDAQ and Online

Fei Li

On behalf of CEPC TDAQ Group

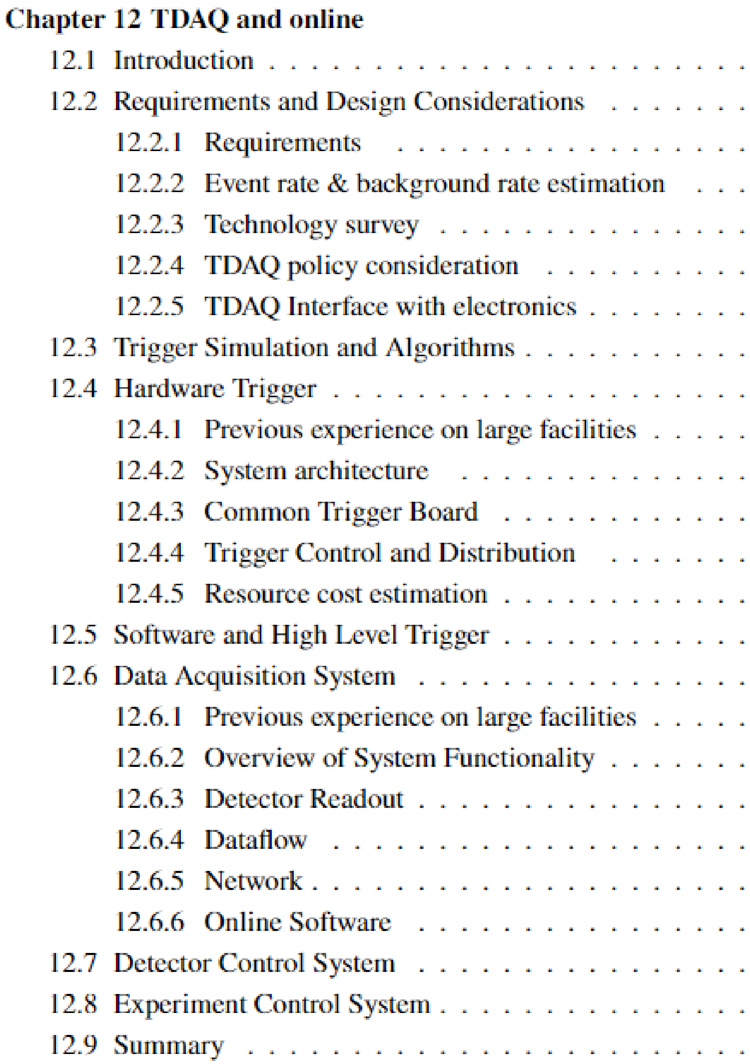
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Oct. 21th, 2024, CEPC Detector Ref-TDR Review

Content

Introduction

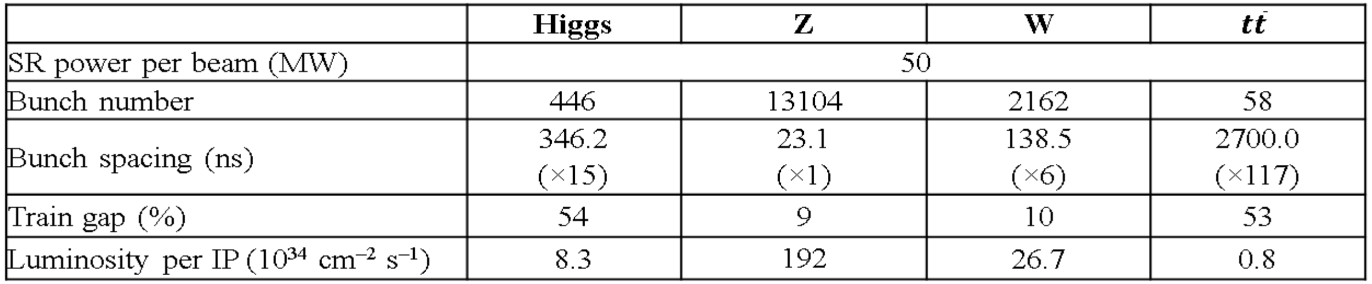
- This talk is about the design and development of the TDAQ and online
- This talk relates to the Ref-TDR Ch 12.
- Questions for physics and simulation
  - What kind of events need to be saved?
  - How to identify these events?
  - Background level?
- Questions for each detectors and electronics
  - Raw data readout bandwidth?
  - How much latency is acceptable?
  - What trigger primitives can be provided?
  - Noise level itself?
  - Control and monitoring requirements?



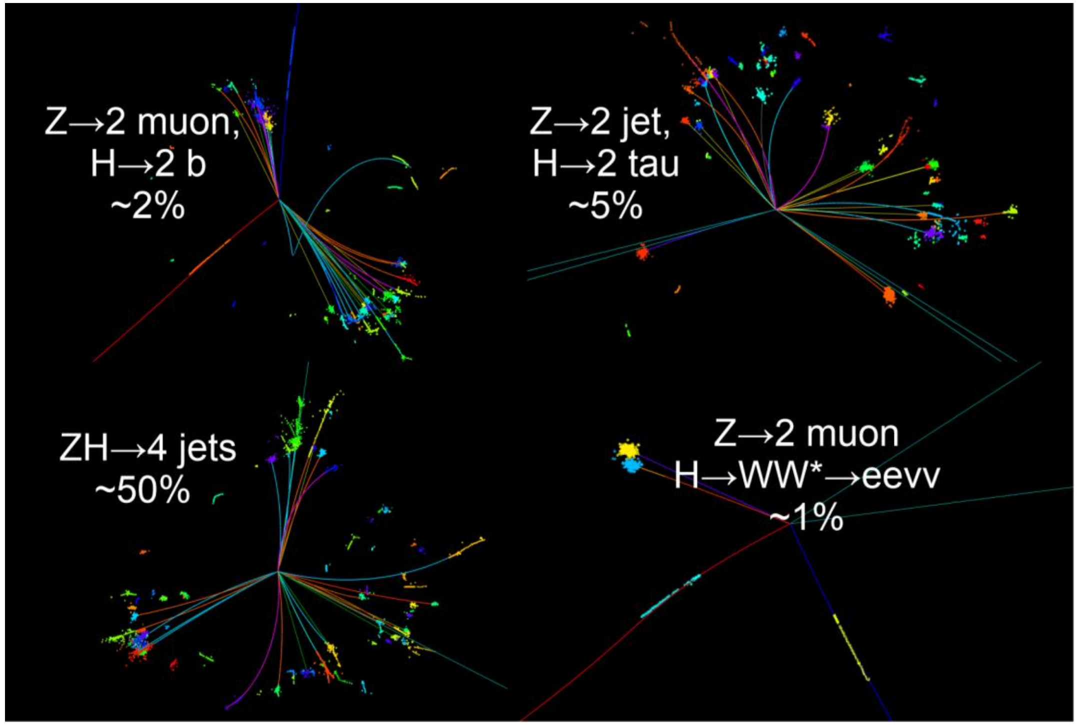
Chapter 12 TDAQ and online

Requirements: Physical Event Rate

- 8 Hz @ Higgs 240GeV(50MW)
  - Bunch crossing rate: 2.889 MHz
  - Higgs: ~0.02Hz
- 82 kHz @ Z pole 91GeV(50MW)
  - Bunch crossing rate: 43.3 MHz
- Physical event rates are sufficiently low relative to the bunch crossing rate.
- Keep physical events as more as possible
  - By a rough selection of the relevant objects (jet, e, muon, tau,v, ...) and their combinations.
  - Required detailed signal feature extraction and simulation studies.



	Higgs	**Z**	**W**	***tt̄***
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 (×15)	23.1 (×1)	138.5 (×6)	2700.0 (×117)
Train gap (%)	54	9	10	53
Luminosity per IP (10^{34} cm^{-2} s^{-1})	8.3	192	26.7	0.8



Ref: CEPC Physics at a glance, Lomonosov Conference 2021, by Manqi Ruan

Requirements: Data Rate

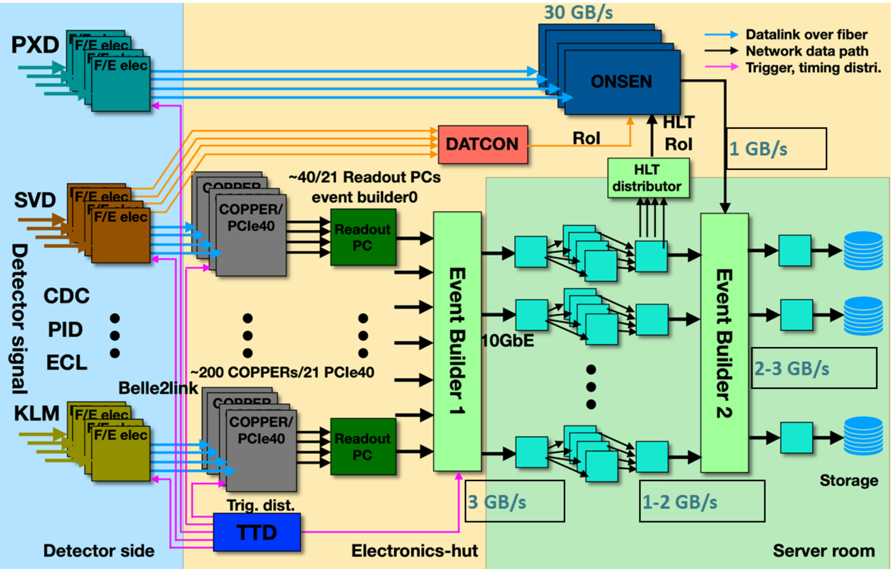
- Data rate before trigger
  - ~1 TB/s @ Higgs
  - Several TB/s @Z
- L1 trigger rate
  - O(1k) Hz @ Higgs
  - O(100k) Hz @ Z
- Event size < 2 MB
  - Related to occupancy and read out window
- Storage rate after HLT
  - <100 Hz(200 MB/s) @Higgs
  - 100 kHz (200 GB/s) @Z

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024	512*128	1024	128		128	8~16				
Data Width /hit	32bit	42bit	32bit	48bit		48bit	48bit				
Avg. data rate / chip	0.18Gbps/chip, 1Gbps/chip inner	3.53Mbps/chip	21.5Mbps /chip	2.9Mbps/chip	38.8Mbps/chip	~70Mbps/module Inmost	10kHz/ch	100kHz /ch	3kHz/channel	25kHz/channel	10kHz/channel, 20kHz/inner endcap
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.39 M chn	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43,176 chn(iner end-cap 6912), 288 modules
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1 Gbps	27.9Gbps	34.4Gbps	460.8Gbps	1.87Tbps	811.2Gbps	2.688Tbps	24Gbps
Occupancy	0.22e-4	2.5e-4				2.8e-4	58e-4			19.5e-4	
Sum	7.1 Tbps										

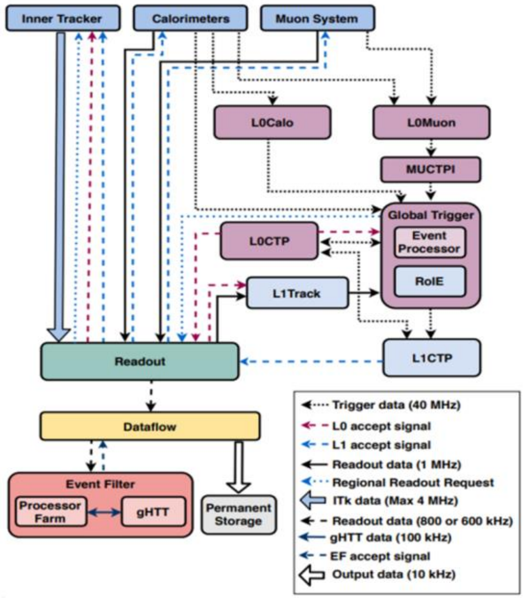
Preliminary background and data rate estimation

Technology survey

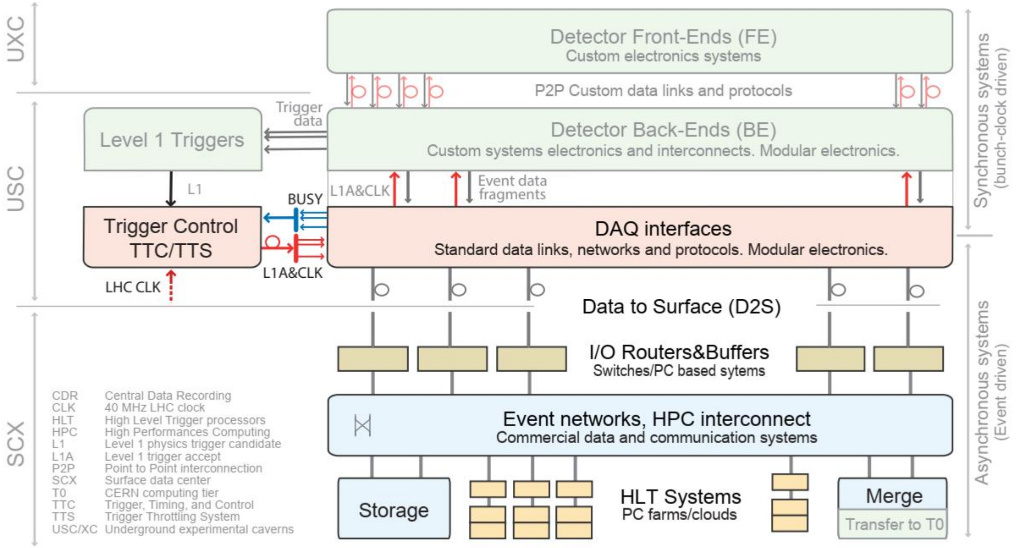
BELLE II



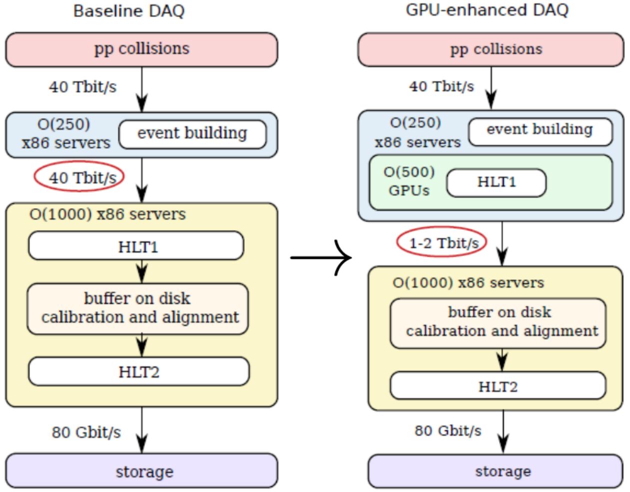
ATLAS Phase II



CMS Phase II



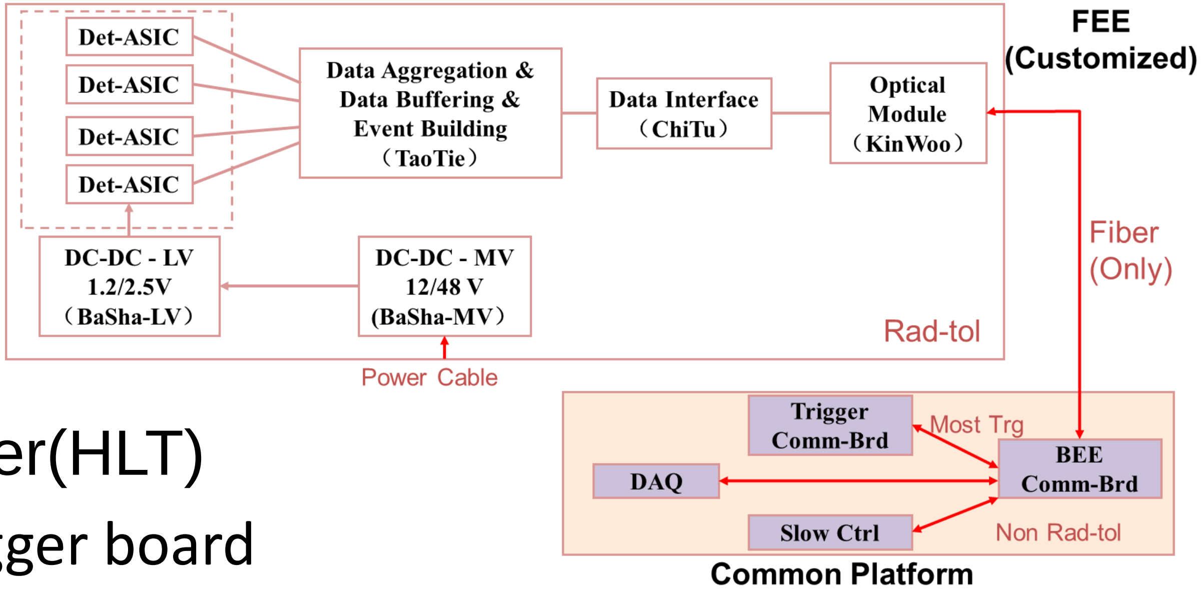
LHCb Phase II



- A few common backend boards (ATCA)
- Network or PCIe bus readout
- GPU/FPGA acceleration at HLT
  - GPU power has increased 1,000 times in the last decade
- Full software trigger @LHCb
  - Deal with higher occupancy and more accurate tracking.

Our choices

- Fewer and cleaner physical processes @CEPC
- Electronics framework schema
  - Full data transmission from Front-End Elec.
  - Connect trigger with Back-End Elec.



- Trigger solutions
  - Hardware trigger(L1) + high level trigger(HLT)
    - A single type of common hardware trigger board
      - Collect trigger primitives from BEE common boards
      - Send back trigger accept signal to BEE
    - Provide fast and normal trigger menu
    - Network readout

Main Technical Challenges

- High efficiency algorithms in trigger and background compression
  - 2.887MHz->O(1k)Hz @Higgs
  - 43.3MHz->O(100k)Hz @Z
- Trigger primitive synchronization control with asynchronous data readout from electronics
  - Manage data disorder due to data transfer queuing and delay
  - Align sub-detector data of each bunch crossing within limited time and resource

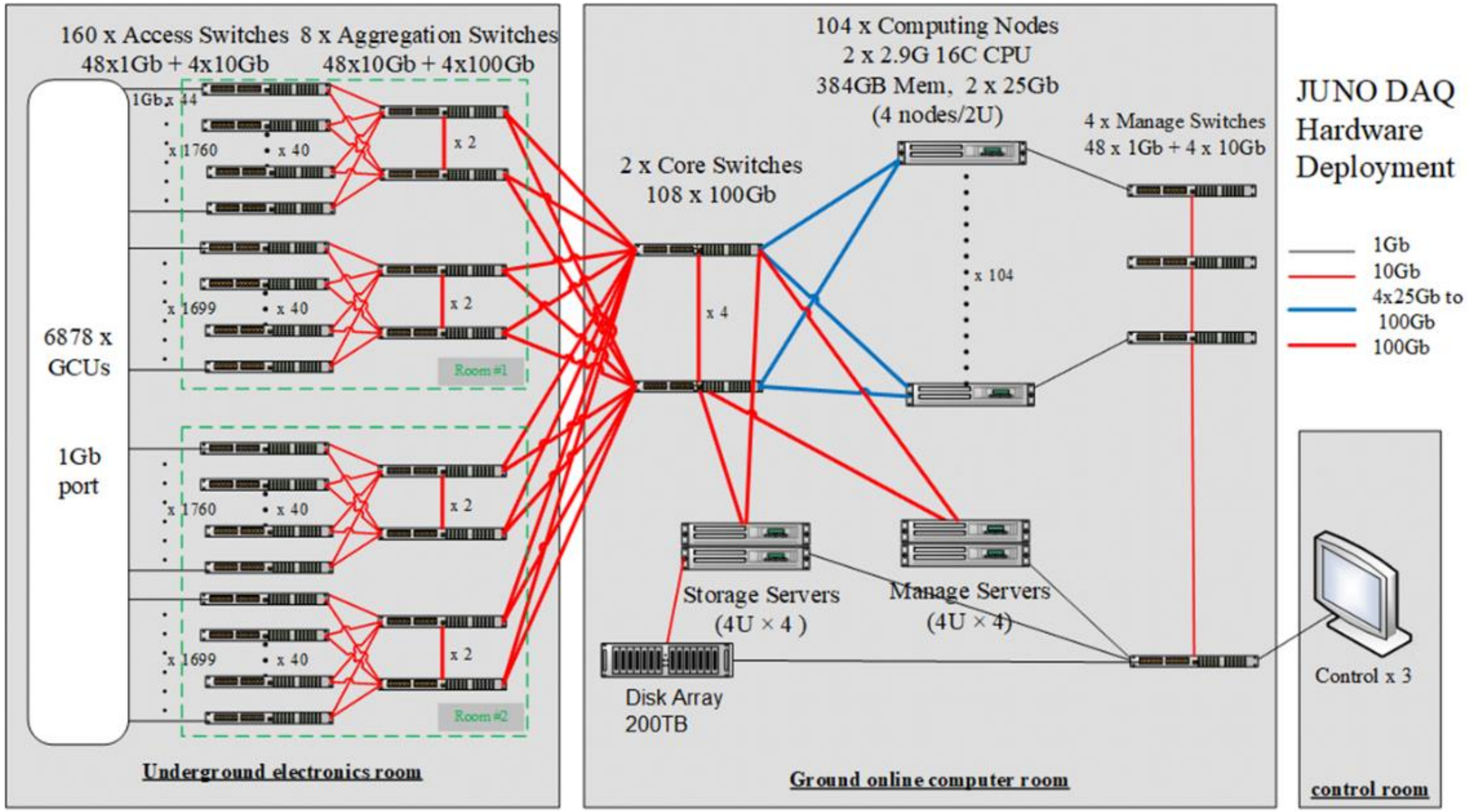
Previous experience with TDAQ Hardware

- Designed BESIII trigger system
  - Comprehensive trigger simulation/hardware design/core trigger firmware development
- GSI PANDA TDAQ R&D
  - Designed HPCN board for TDAQ
- Designed Belle2Link and HPCN V3 as ONSEN for Belle II
- Designed CPPF system for CMS Phase-I
  - Design MTCA board, Cluster finding and fanout to EMTF/OMTF
- Designing iRPC/RPC Backend/Trigger for CMS Phase-II
  - ATCA common Backend and trigger board

Extensive experience in TDAQ system design, algorithm and hardware development

Previous experience with DAQ&DCS

- BESIII DAQ & DCS
  - Running since 2008
- Dayabay experiment DAQ&DCS
  - Operated from 2011 to 2020
- LHAASO DAQ
  - Operated since 2019
  - Full software trigger
- JUNO DAQ&DCS
  - Two types of data stream
    - HW trigger for waveform
    - Software trigger for TQ hits
  - Online event classification

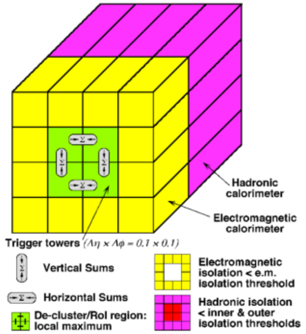


Extensive experience in DAQ&DCS development and operation, including software trigger

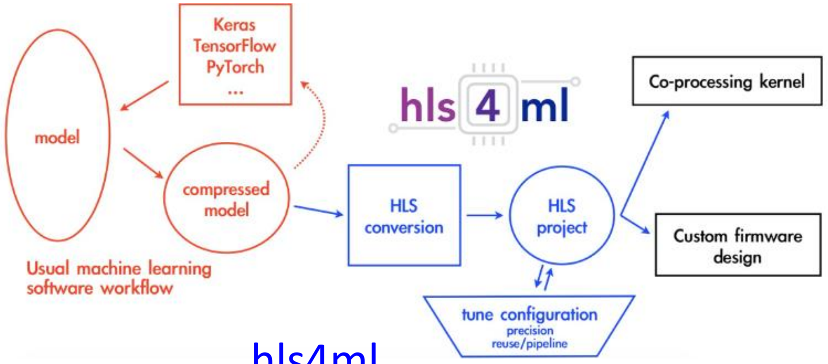
Previous experience with ML algorithm

Neural network used in ATLAS global trigger

- Example: tau reconstruction at the hardware trigger level
- Train the neural network (NN) with ROI
- Use hls4ml to convert NN model to hls project

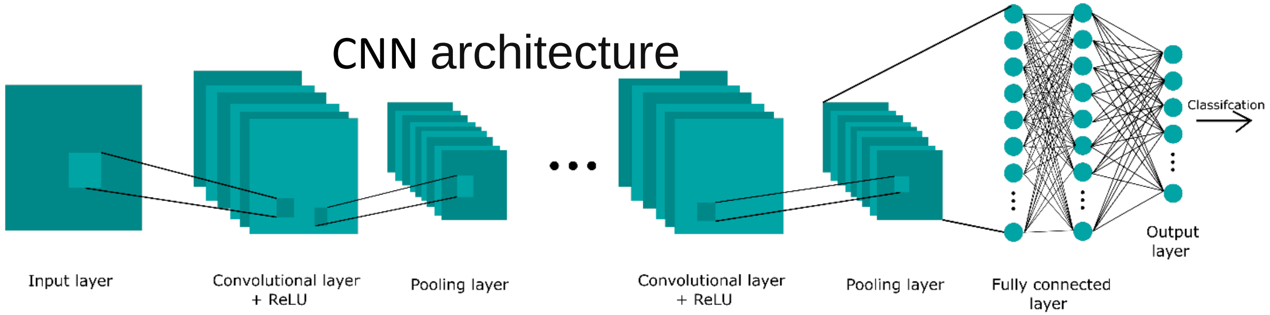


Seed and cluster



hls4ml

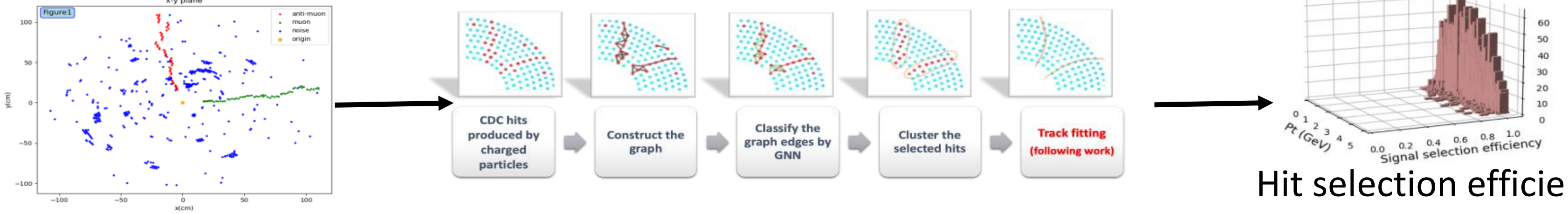
CNN architecture



HLT Acceleration on FPGA platform

μ+ μ- (particle gan)

GNN based tracking algorithm for BESIII/Belle II



Hit selection efficiency: 98.4%

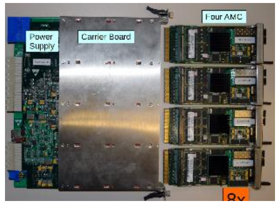
Hit selection purity : 97.9%

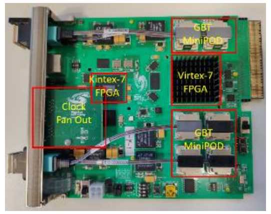
Some experience in ML algorithm development on FPGA for L1 and HLT

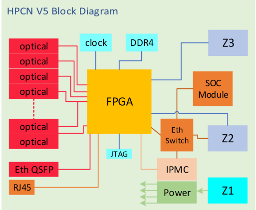
R&D efforts and results

- Started the design of an ATCA common trigger board for CEPC
  - Based on a series of designed xTCA boards







Version	HPCN V1	HPCN V2	HPCN V3	CPPF	HPCN V4	Serenity	HPCN V5
Line rate	3Gbps	3Gbps	6Gbps	10Gbps	16Gbps	25Gbps	10-25Gbps
Num. of ch	8 ch	8ch	8-16ch	36ch	48ch	124ch	36-80 ch
Buffer	2GB	2GB	4GB	—	48GB	—	TBD
Ethernet	1GbE			1/10GbE	10GbE	100GbE	40-100GbE
Aplication	PANDA		Belle II/PXD	CMS Phase-I	CMS Phase-II		CEPC R&D
Time	2006-		2009-	2013-	2017-		2024-

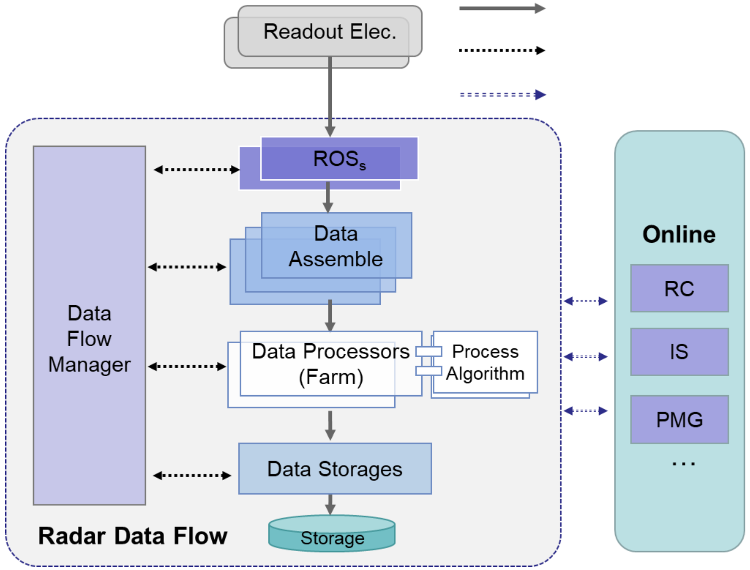
Streaming Software Framework – RADAR

heteRogeneous Architecture of Data Acquisition and pRocessing

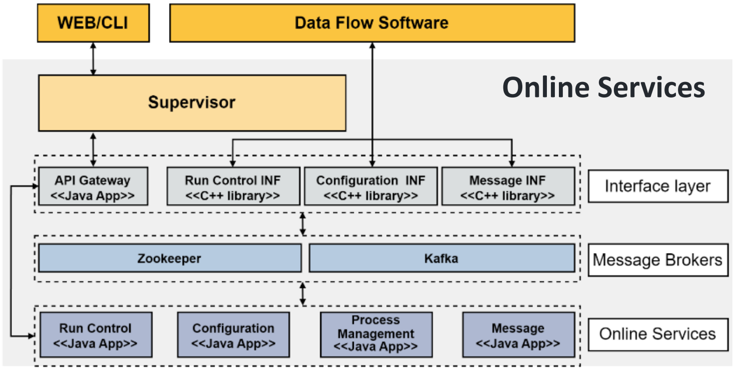
- **V1:** deployed in LHAASO (3.5 GB/s data rate), *software trigger mode*
- **V2:** upgraded for JUNO (40 GB/s data rate), *mixed trigger mode*
  - Containerized running
- **V3:** **CEPC-oriented** (~ TB/s data rate) , under development

- **Motivation:**
  - High-throughput data acquisition and processing
- **Current Status:**
  - Over a decade of work led to significant progress, validated through experiments
- **Recent Focus:**
  - **Heterogeneous online processing platforms with GPU**
  - **Real-time data processing acceleration solutions**
- **Expansion:**
  - **Application across various domains** (DAQ, triggering, control, etc.)
  - **Integration of AI technologies** (ML, NLP, expert systems, etc.)

Start to develop new version with GPU acceleration.

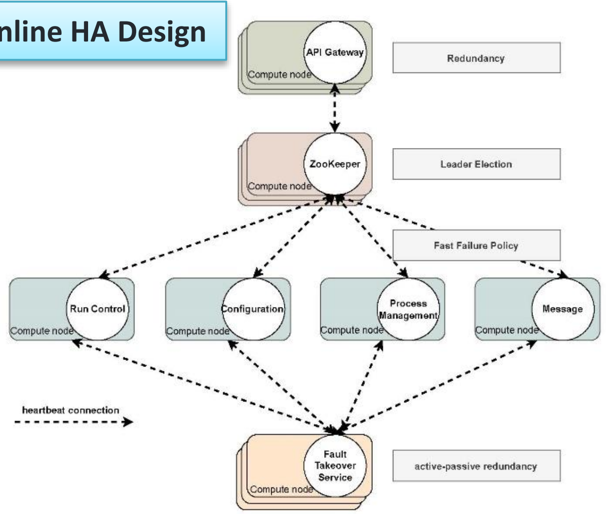


- **General-purpose distributed framework**
- **Lightweight structure**
- **Plug-in modules design**
- **Microservices architecture**

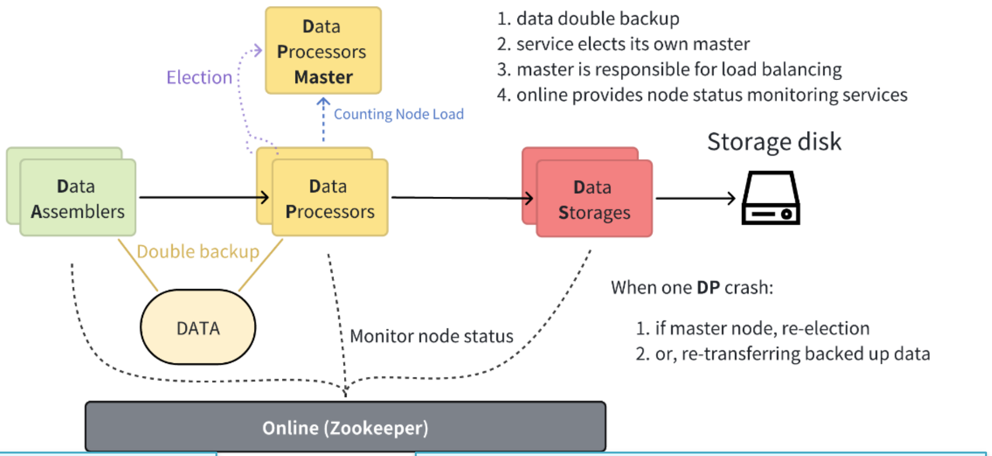


R&D efforts and results

Online HA Design



Dataflow HA Design



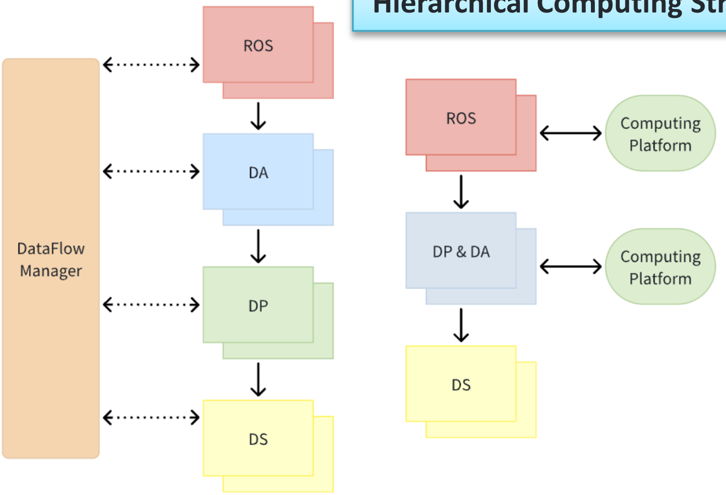
High Availability (HA):

1. data double backup
2. service elects its own master
3. master is responsible for load balancing
4. online provides node status monitoring services

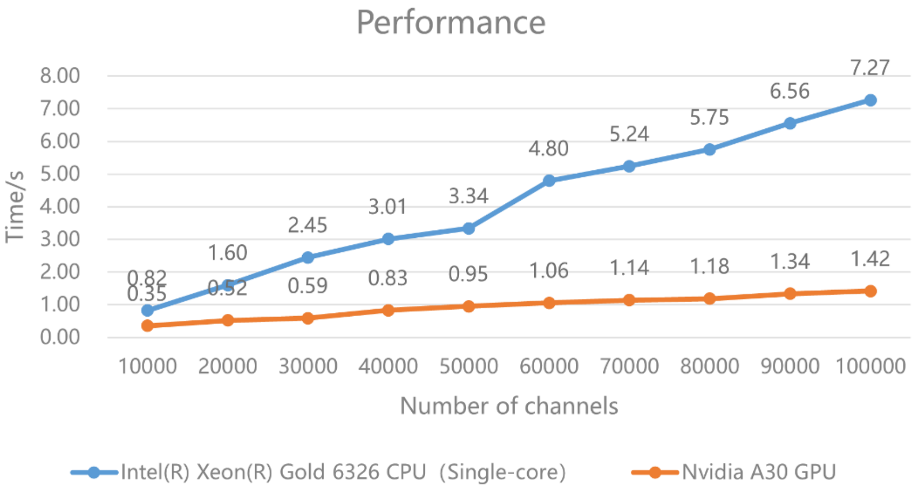
When one **DP** crash:

1. if master node, re-election
2. or, re-transferring backed up data

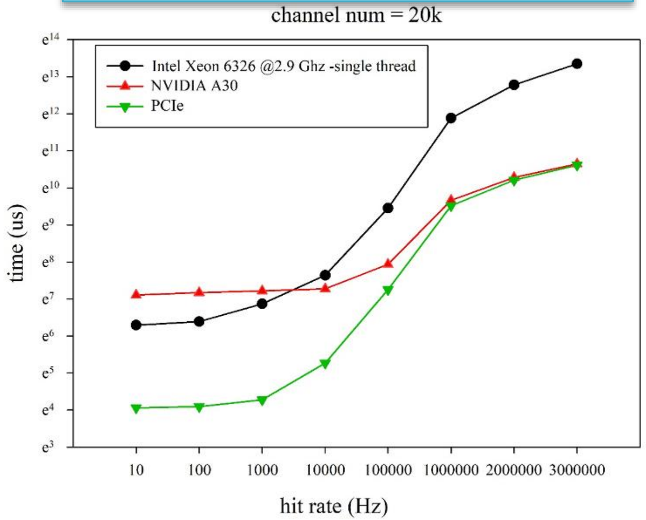
Hierarchical Computing Strategy



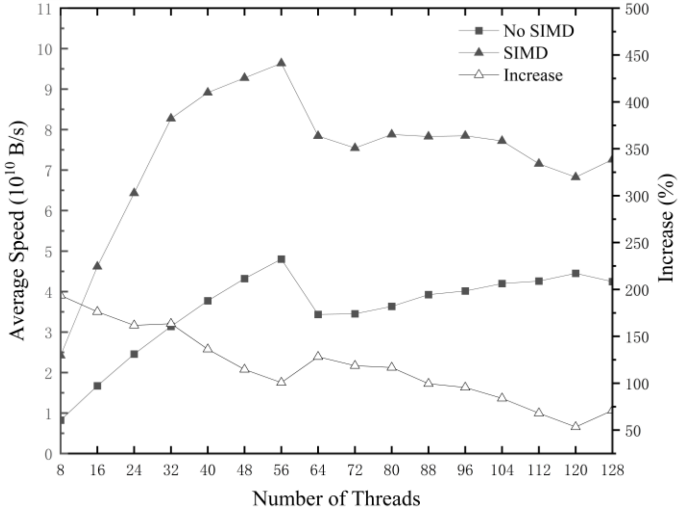
GPU based online waveform reconstruction in JUNO



GPU based nHit trigger algorithm study



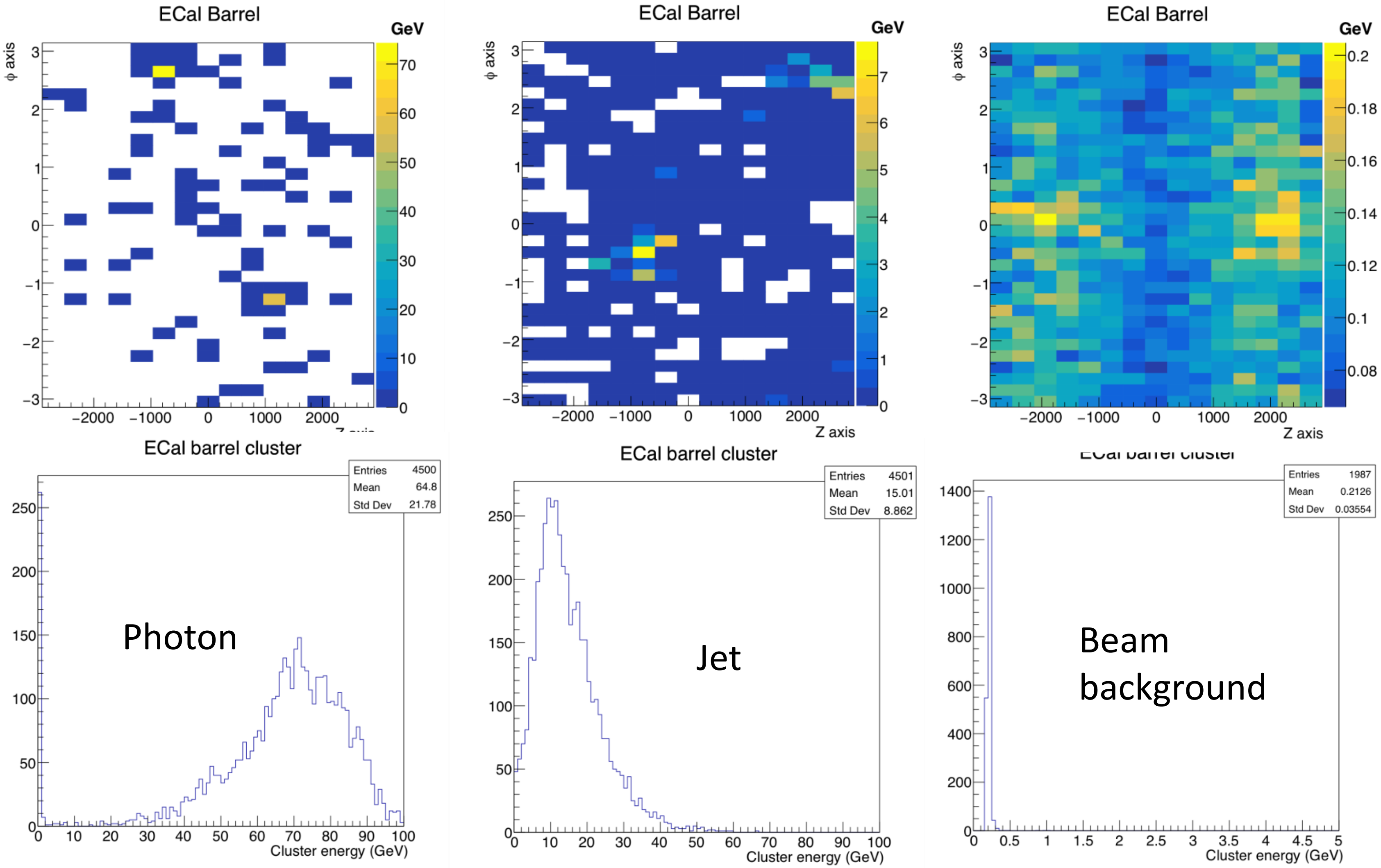
SIMD based CPU processing acceleration



Acceleration progress for waveform reconstruction and software trigger algorithm.

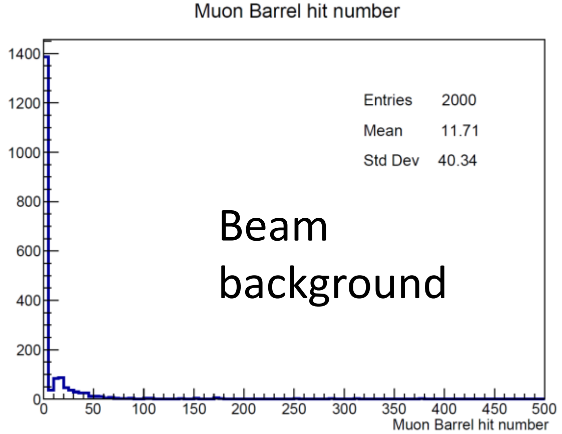
Preliminary Trigger Simulation with Cal.

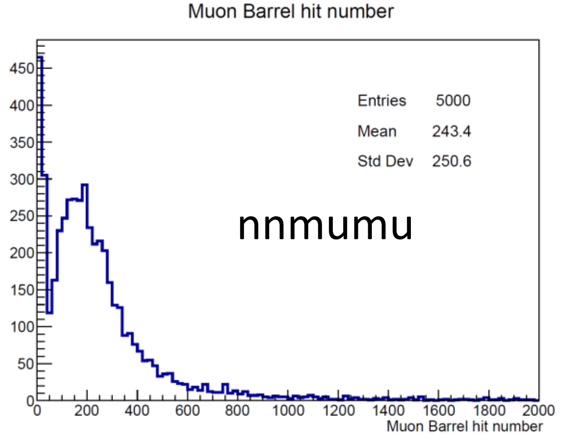
- Physical events signature at ECal&HCal
  - Energy deposition is relatively large and concentrated
- Trigger primitive and condition
  - Two clusters with the highest energy
  - Ecal/HCal barrel >0.5GeV
  - ECal end-cap >5GeV
  - Hcal end-cap >50Gev
- Trigger efficiency
  - nnaa:100%
  - nnbb:100%
  - nnaZ:99.7%
  - nntautau:96.7%
  - nnWW:99.1%
  - nnZZ:95.8%
  - Beambkg:4.8%

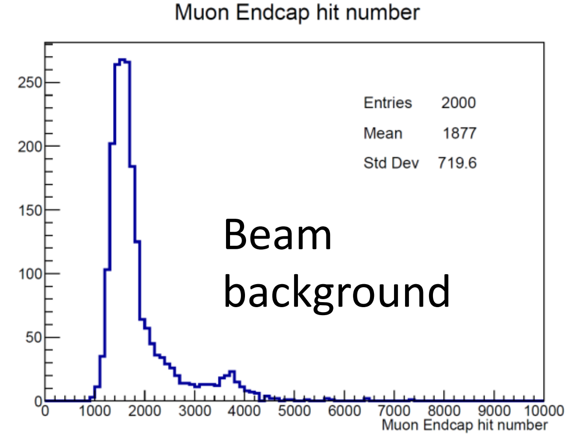


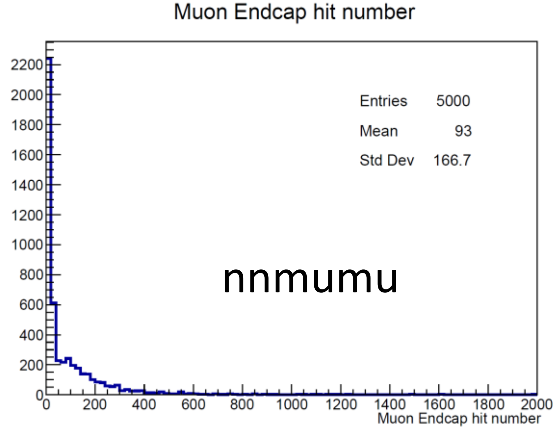
Preliminary Trigger Simulation with Muon

- Left: 2000 background events(10BX), Right: 1000 ZH→nnμμ events
- Up：Barrel
  - – Number of hits(Barrel) > 10
  - – nnμμ efficiency:100%
  - – Background: 19%
- Down：Endcap
  - – Higher background hits





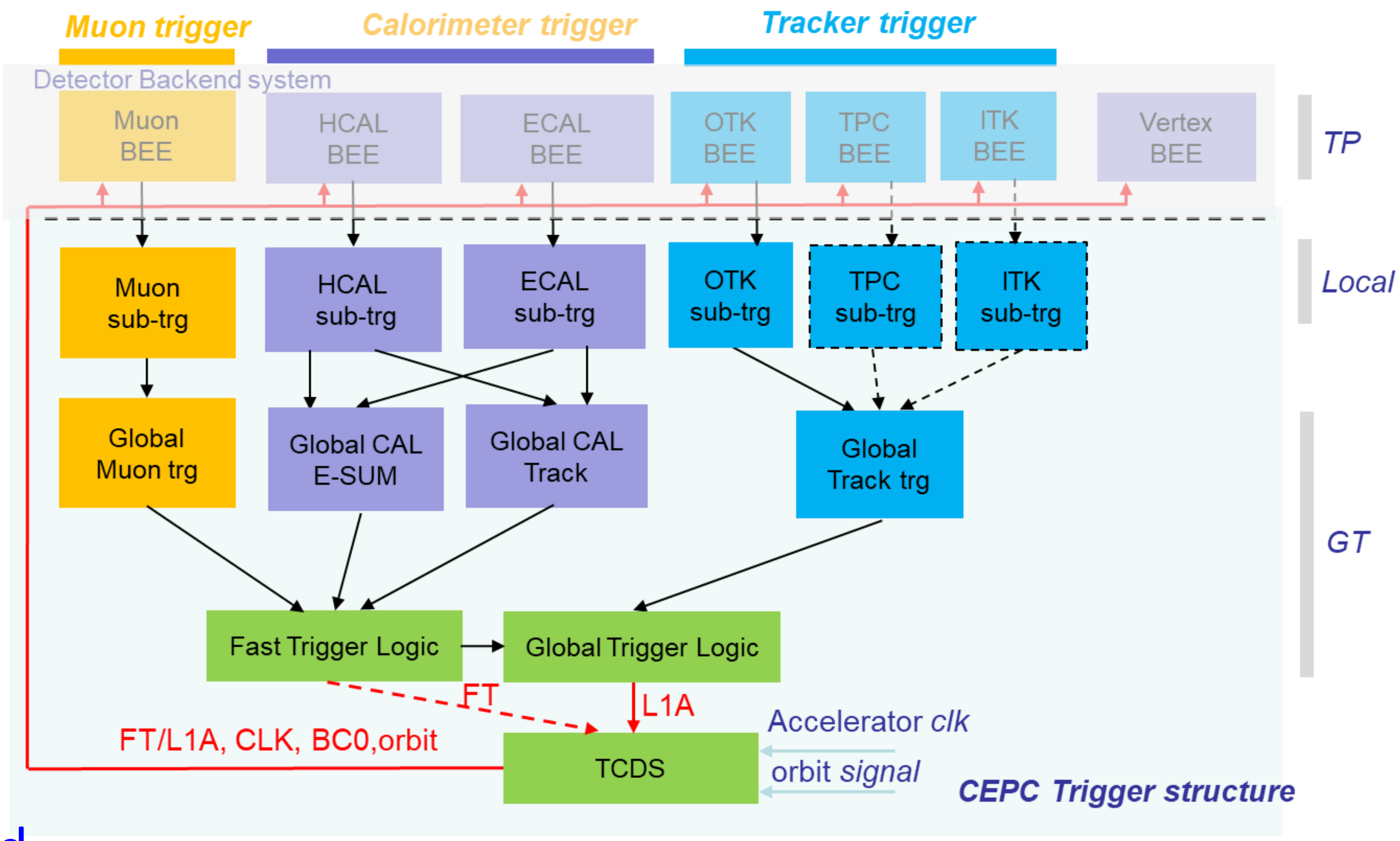




A lot of simulation and research need to be done

Design of Hardware Trigger Structure

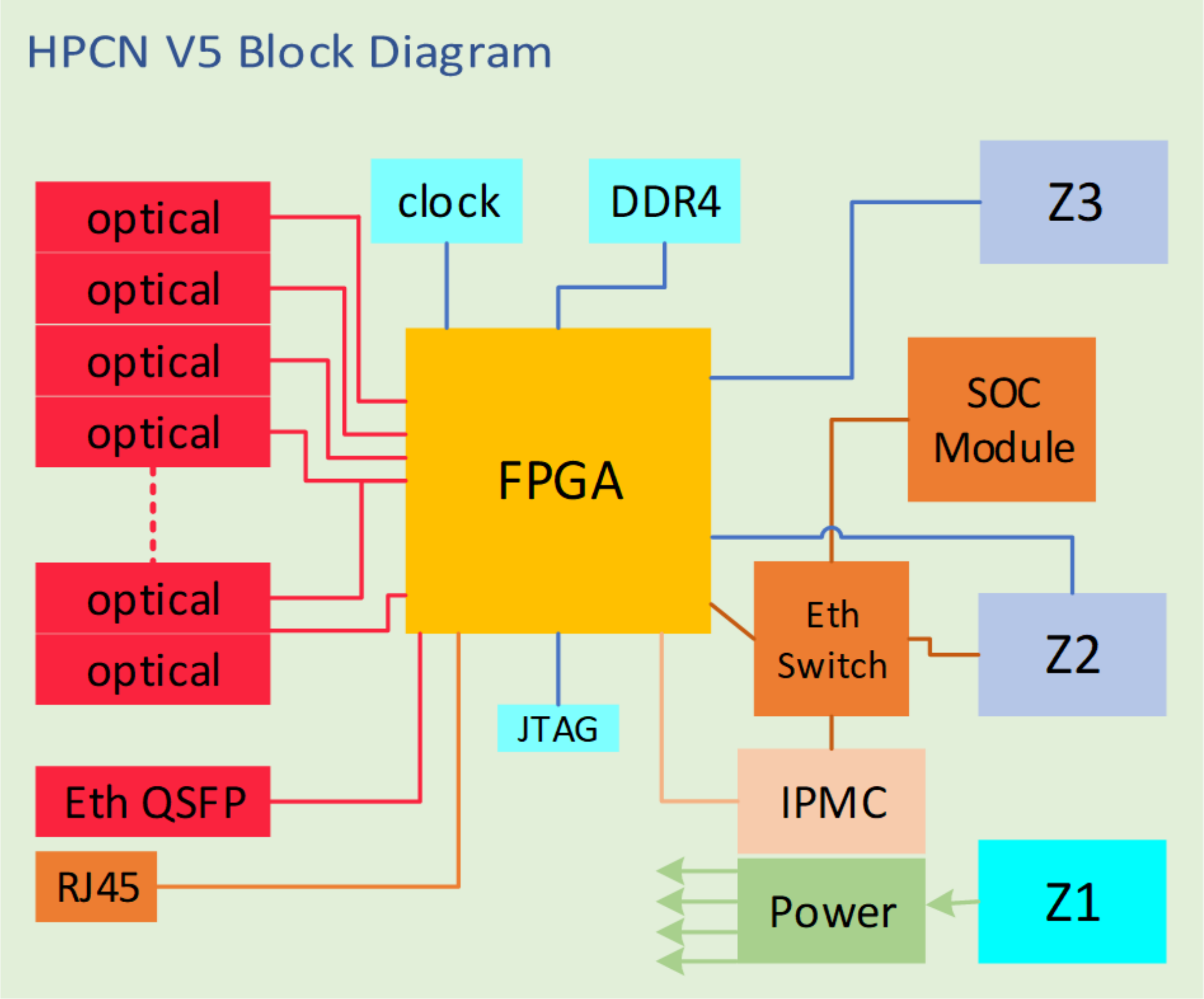
- Trigger primitive(TP)
  - Extracted by BEE
- Local detector trigger
  - Sub energy and tracking…
- Global trigger
  - E-sum and tracking
  - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied



CEPC Trigger structure

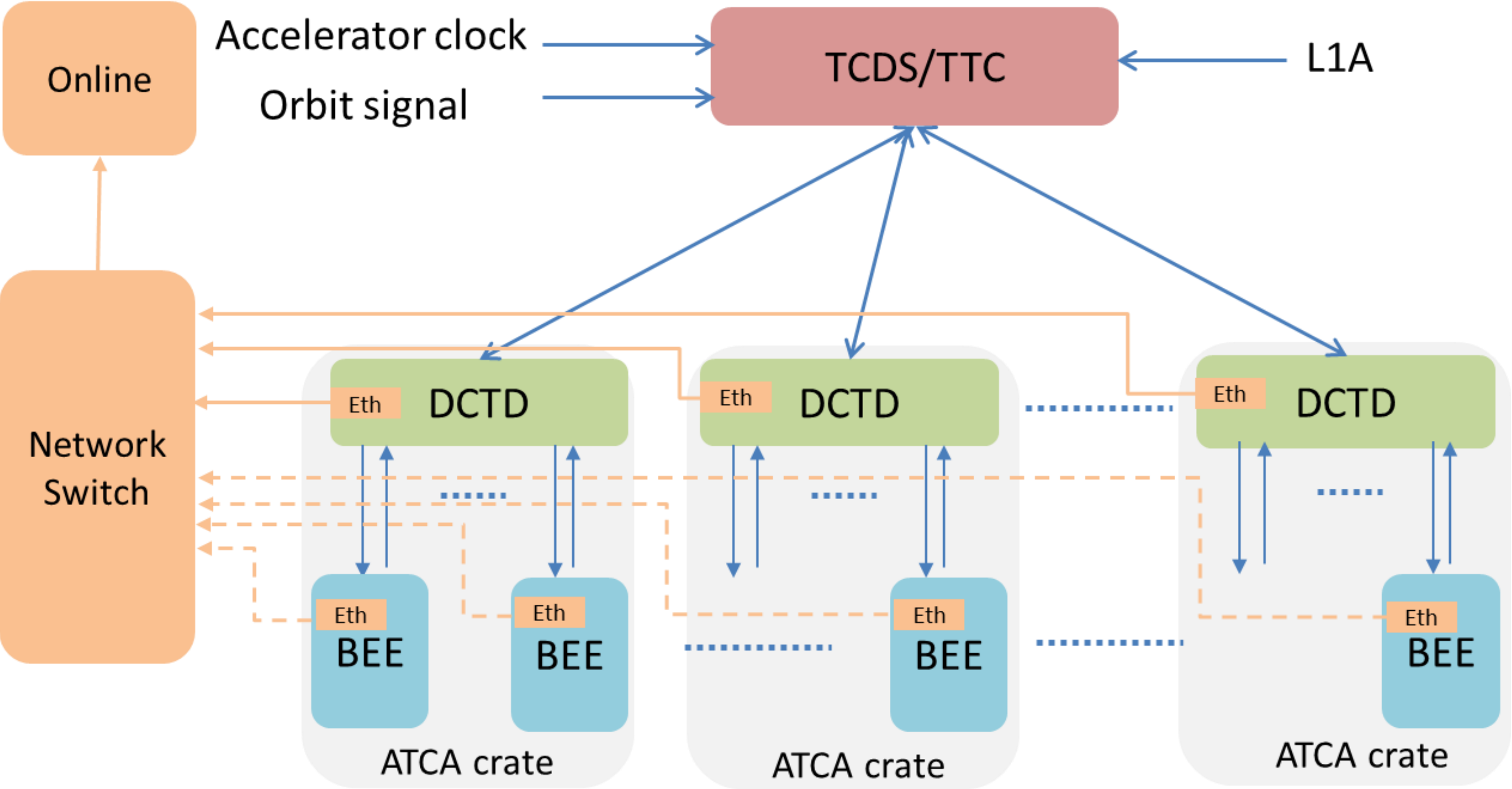
Preliminary design of the common Trigger Board

- Common Trigger board function list
  - ATCA standard
  - Virtex-7 FPGA
  - Optical channel: 10-25 Gbps/ch
  - Channel number:36-80 channels
  - Optical Ethernet port: 40-100GbE
  - DDR4 for mass data buffering
  - SoC module for board management
  - IPMC module for Power management



Preliminary design of TCDS and Readout

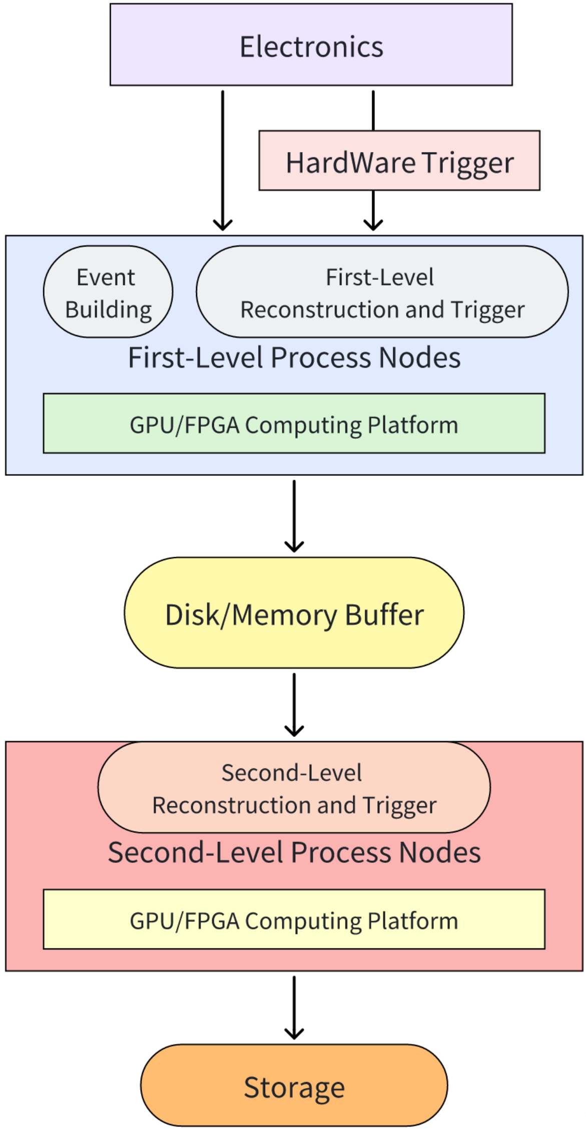
- TCDS/TTC
  - Clock, BC0, Trigger, orbit start signal distribution
  - Full, ERR signal feed back to TCDS/TTC and mask or stop L1A
- Data readout from BEE
  - Read out directly or concentrated by DCTD board
  - Depending on the size of the data volume



- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD-Data Concentrator and Timing Distribution
- BEE-Backend board Electronic

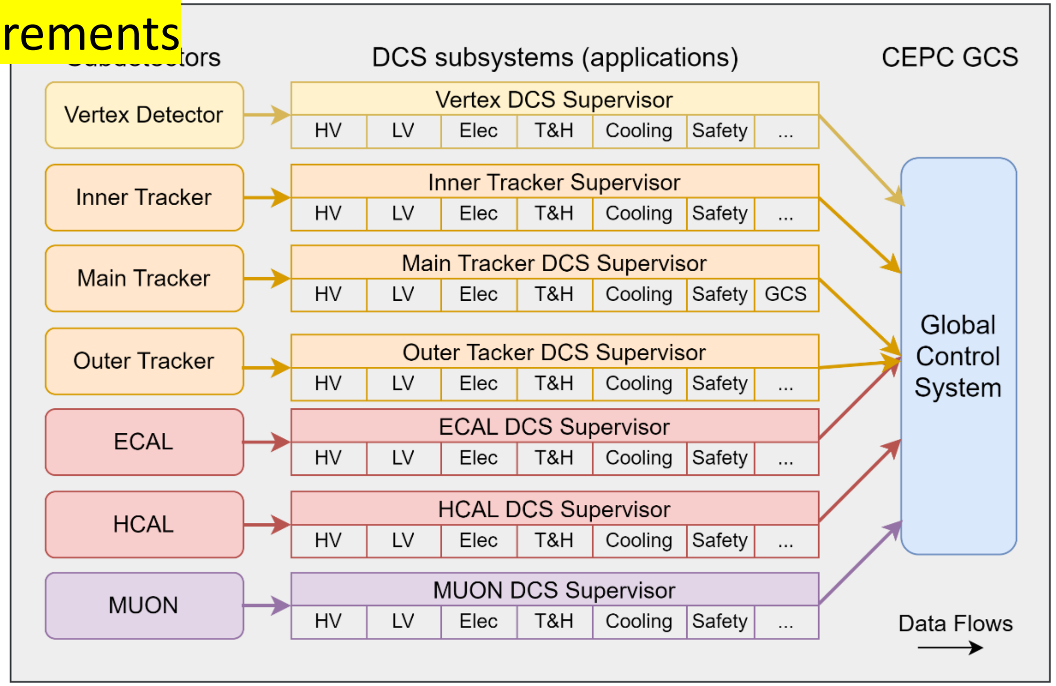
Architecture Design of DAQ

- Compatible design with or without HW trigger
- Full COTS(commercial-off-the-shelf) hardware
- Readout interface and protocol
  - Ethernet 100Gbps
  - TCP or RDMA
- RADAR software framework
  - Heterogeneous computing
- GPU/FPGA acceleration for HLT
- Disk or memory buffer
  - Decouple computing environments
  - Complete offline algorithm can be run online



Preliminary design of DCS

Requirements

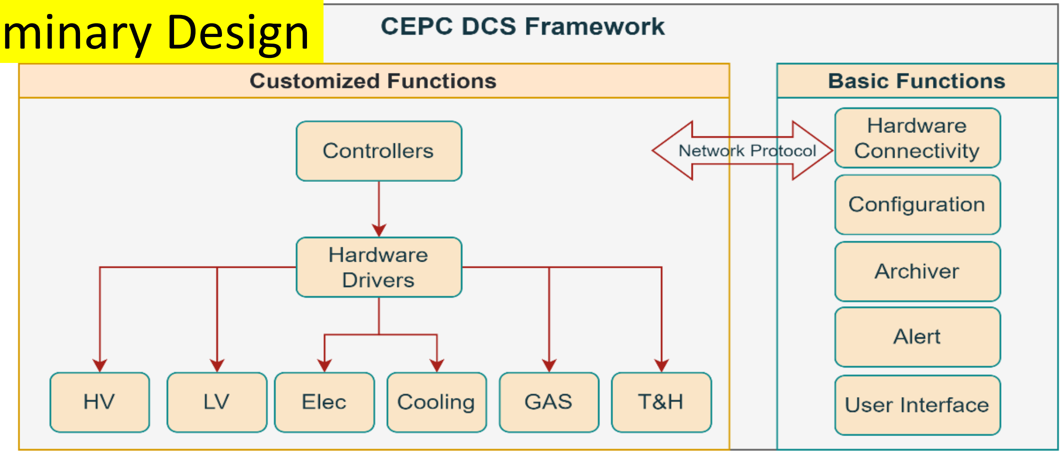

Subdetectors
DCS subsystems (applications)
CEPC GCS

Vertex Detector → Vertex DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...
Inner Tracker → Inner Tracker Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...
Main Tracker → Main Tracker DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | GCS
Outer Tracker → Outer Tacker DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...
ECAL → ECAL DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...
HCAL → HCAL DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...
MUON → MUON DCS Supervisor: HV | LV | Elec | T&H | Cooling | Safety | ...

Global Control System

Data Flows →

Preliminary Design


CEPC DCS Framework

Customized Functions

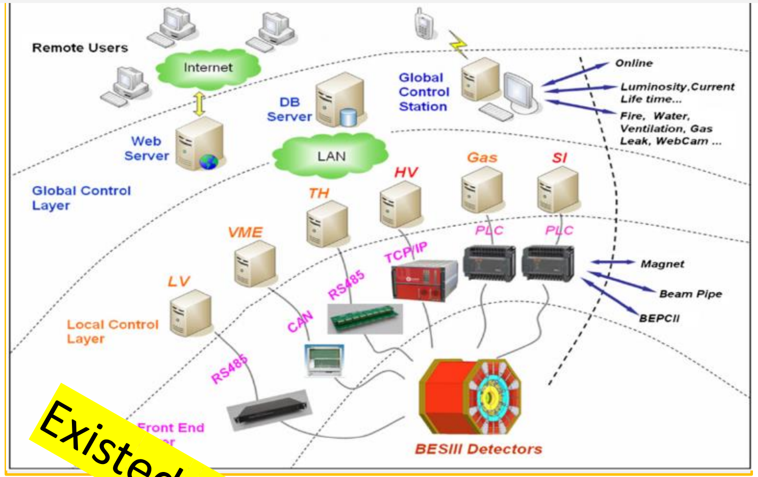
Controllers
Hardware Drivers
HV
LV
Elec
Cooling
GAS
T&H

Network Protocol

Basic Functions

Hardware Connectivity
Configuration
Archiver
Alert
User Interface

BESIII Detector Control System *Based on LabVIEW*



Existed Solutions

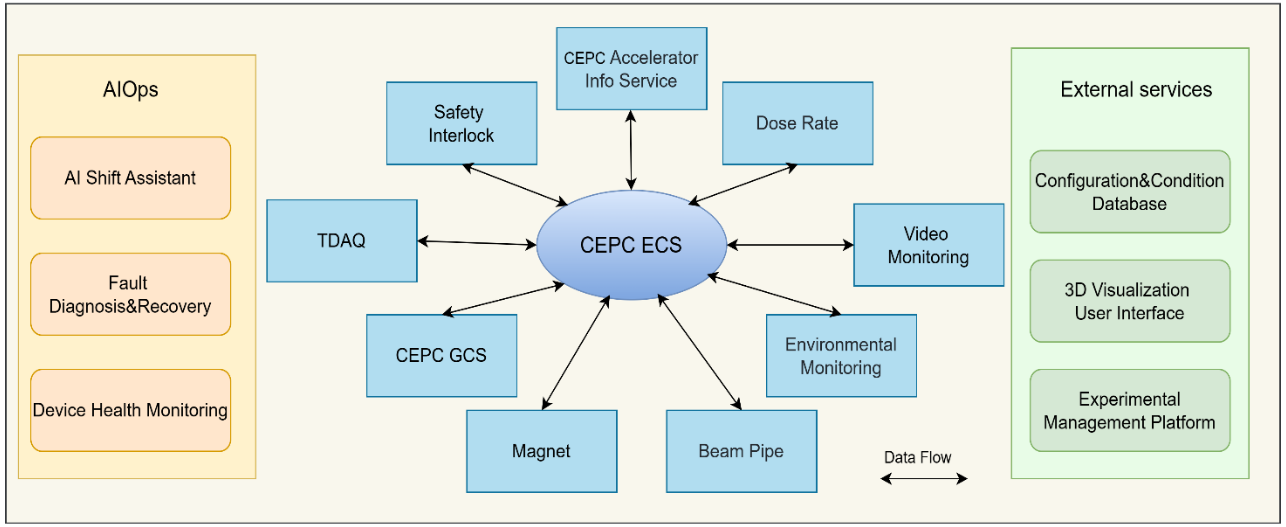
JUNO DCS

Based on EPICS

Designed framework based on existed solutions

Preliminary design of ECS

Main components of the Experiment Control System


AIOps

AI Shift Assistant

Fault Diagnosis&Recovery

Device Health Monitoring

CEPC Accelerator Info Service

Safety Interlock

Dose Rate

TDAQ

CEPC ECS

Video Monitoring

CEPC GCS

Environmental Monitoring

Magnet

Beam Pipe

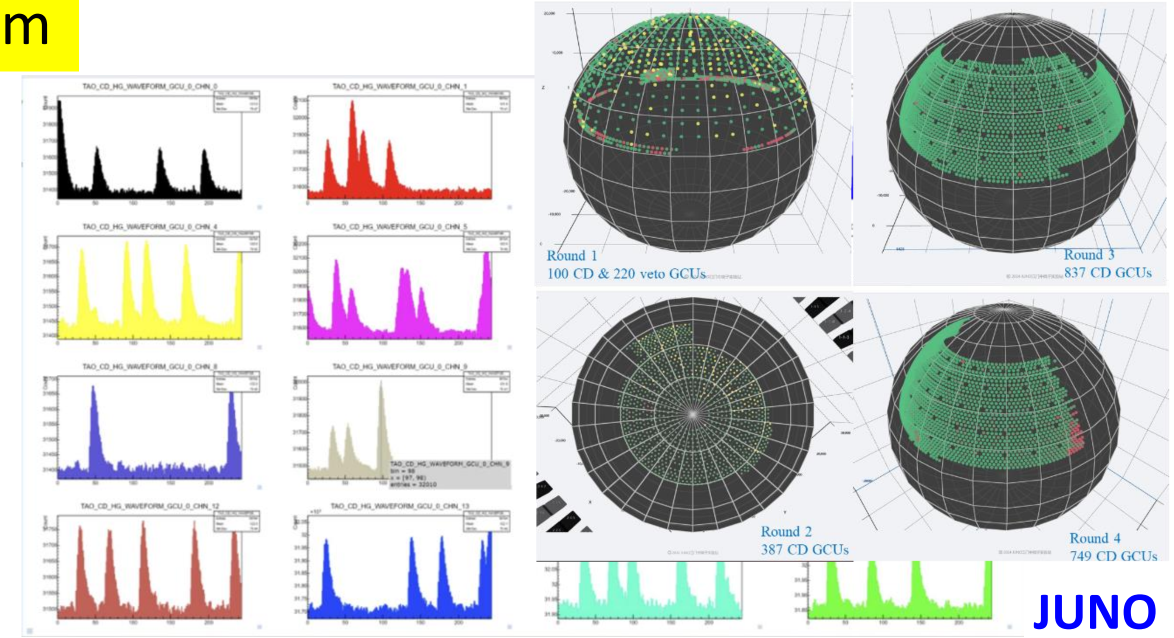
Data Flow

External services

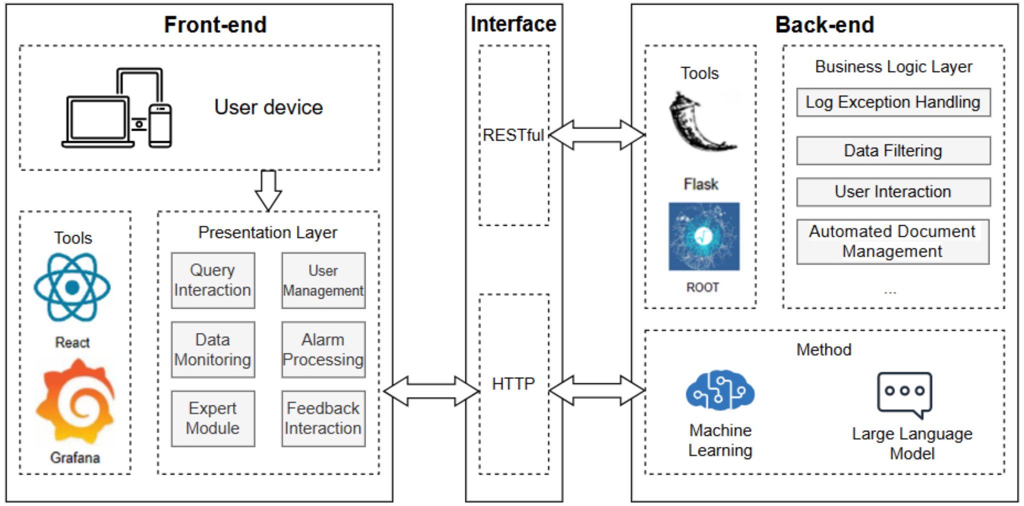
Configuration&Condition Database

3D Visualization User Interface

Experimental Management Platform



- R&D progress from JUNO and BESIII
  - 3D Visualization Monitoring
  - AI shift assistant based on LLM+RAG (TAOChat)
  - ROOT-based Online Visualization System
- Unified control and monitoring for all system
  - TDAQ, DCS, electronics, accelerator and others


Front-end

User device

Tools

React

Grafana

Presentation Layer

Query Interaction

User Management

Data Monitoring

Alarm Processing

Expert Module

Feedback Interaction

Interface

RESTful

HTTP

Back-end

Tools

Flask

ROOT

Business Logic Layer

Log Exception Handling

Data Filtering

User Interaction

Automated Document Management

...

Method

Machine Learning

Large Language Model

Research Team

- 15 staff of IHEP TDAQ group
- DAQ
  - Fei Li (DAQ, team leader)
  - Hongyu Zhang (readout)
  - Xiaolu Ji (online processing)
  - Minhao Gu (software architecture)
- Trigger
  - Zhenan Liu (trigger schema)
  - Jingzhou Zhao (hardware trigger)
  - Boping Chen (simulation/algorithm)
  - Sheng Dong (firmware/DCS)
- DCS/ECS
  - Si Ma

- IHEP Students(20 totally)
  - 2 PhD and 3 master
- New member planned
  - 1 staff next year
  - 2 postdoc
- Collaborators
  - Qidong Zhou (HLT, SDU)
  - Yi Liu (HLT, ZZU)
  - Junhao Yin(HLT, NKU)
  - 3 students planned
- We’re looking for more collaborators

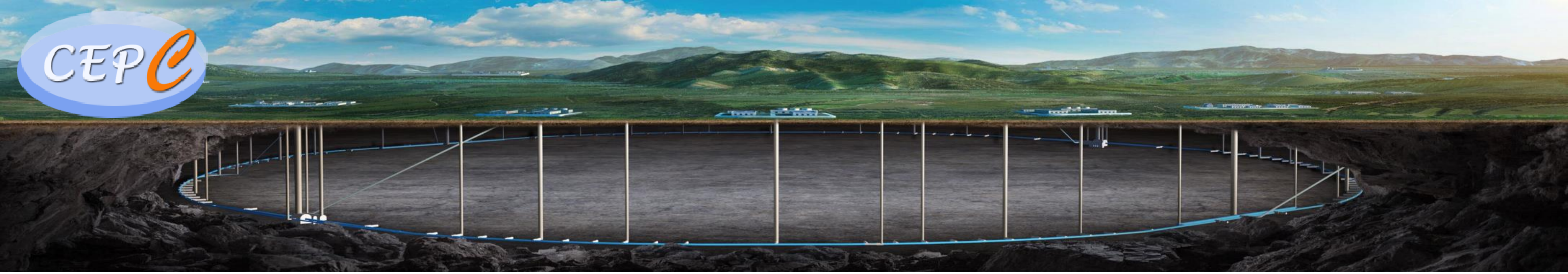
Gathering manpower for R&D, 9 staff and 5 students involved part of the time

Working plan

- TDR related
  - Basic trigger simulation and algorithm study
    - Background event study and basic algorithm scheme for each detector
  - Detailed hardware trigger and interface design
  - Finalize TDAQ and online design scheme
- R&D directions
  - Trigger hardware, fast control and clock distribution
  - TB/s level high throughput software framework(RADAR)
    - FPGA/GPU acceleration and heterogeneous computing
    - Memory-based distributed buffer
  - Detailed trigger simulation and algorithm
  - ML/AI algorithm application
    - Trigger/data compression/ AI operation and maintenance
  - ROCE/RDMA readout protocol and smart NIC
- Joined DRD WP7.5(Backend systems and COTS components) as an observer.

Summary

- Following sub detectors design and simulation
- Completed architecture design of TDAQ and online
  - Hardware and high level trigger – default choice
- No show-stopper found for TDAQ and online scheme
  - Challenges: efficient trigger algorithm and handling TB/s level data rate at manageable hardware scale
- More R&D efforts needed to move forward



Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences