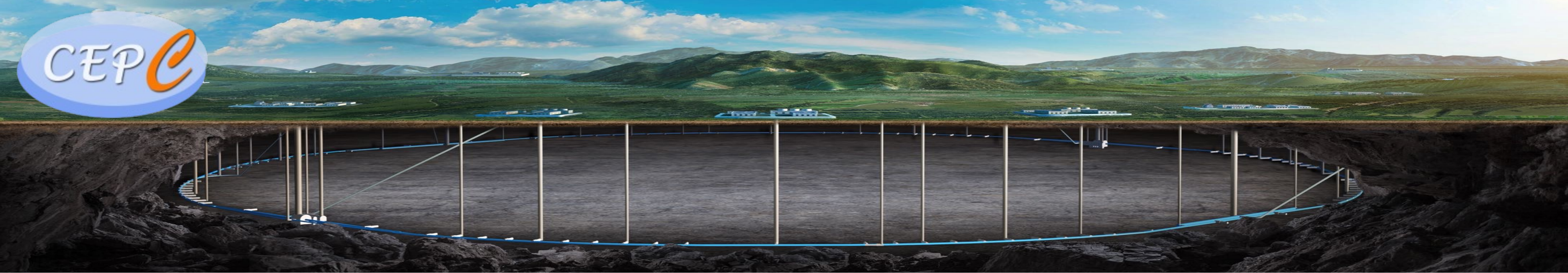


CEPC Silicon Tracker Detector

Qi Yan

On behalf of the CEPC Silicon Tracker Group

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

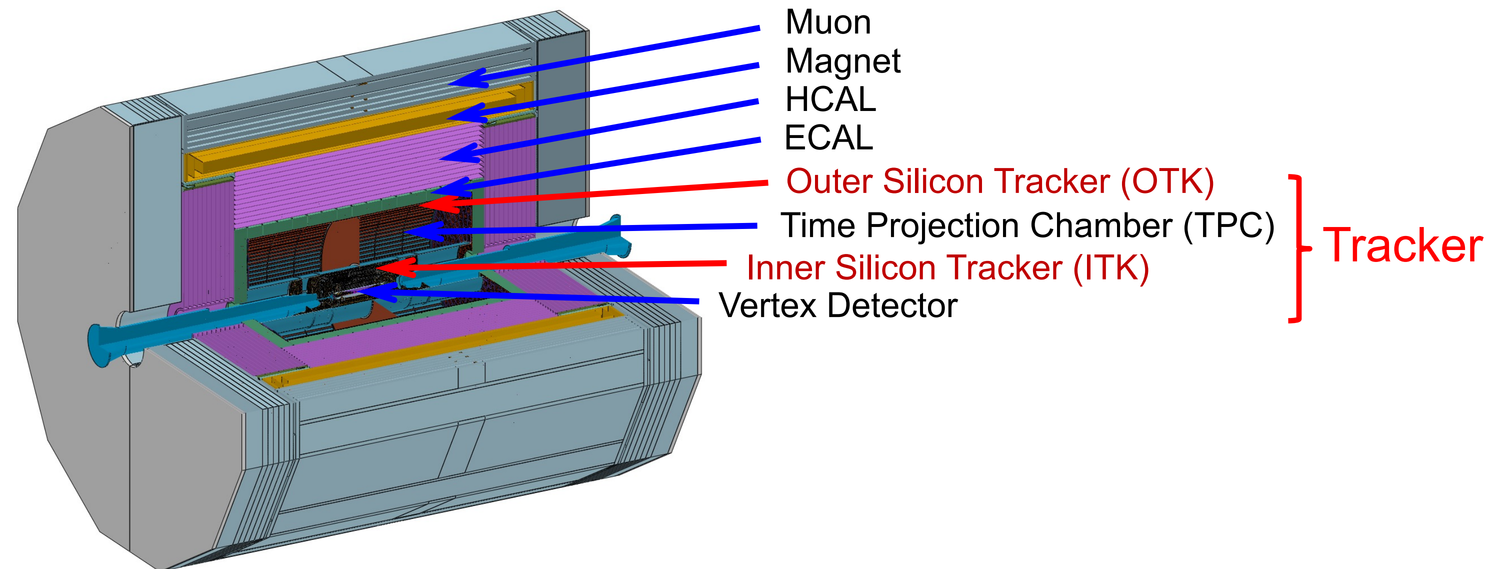
Oct. 21st, 2024, CEPC Detector Ref-TDR Review

Introduction

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker. This presentation will focus on the Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK).

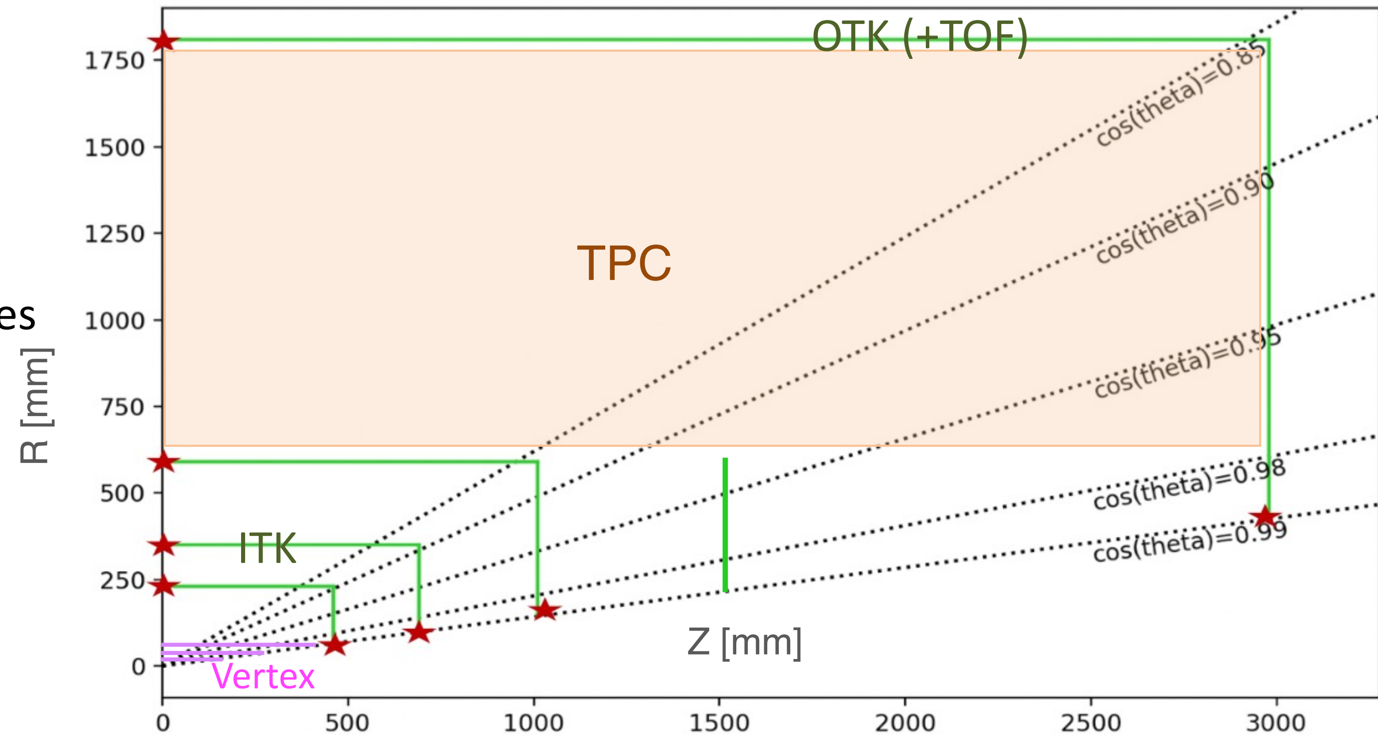
- The ITK employs advanced sensor technologies, including HV-CMOS pixels and CMOS strips, to achieve precise position measurements for accurate particle trajectory determination.

- In addition to position measurement, the OTK incorporates the AC-LGAD semiconductor detector for precision time measurement of charged particles, significantly enhancing particle identification capabilities.



Requirements

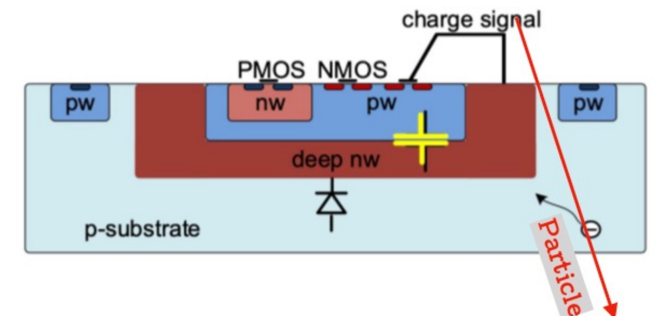
- Inner silicon tracker (ITK)
  - Spatial resolution:
    Barrel: σ_ϕ< 10 μm (bending), σ_z< 50 μm
    Endcap: σ_ϕ< 10 μm (bending), σ_r< 100 μm
  - Material budget:
    <1% X_0 per layer
  - Luminosity ~115×10^{34} $cm^{-2}s^{-1}$ (Z-pole):
    A few ns timing resolution to tag 23 ns bunches
    Maximum hit rate ~10^6 Hz/cm^2
  - Cost effectiveness:
    ~20 m^2 area
- Outer silicon tracker (OTK) with TOF
  - Spatial resolution:
    σ_ϕ< 10 μm (bending)
  - Timing resolution:
    σ_t<50 ps
  - Cost effectiveness:
    ~85 m^2 area



The overall track momentum resolution requirement: better than 0.3% for momenta below 100 GeV/c.

Technology Survey and Our Choice for ITK

- CMOS sensor technology:
  - Cost-effective: CMOS technology is widely used in the semiconductor industry, offering a unique opportunity for development of advanced semiconductor detectors for HEP.
  - Simplified: The active detection layer and readout electronics are integrated into a single chip.
- HVCMOS pixels:
  - Large depletion depth (full depletion), large signal, and good time resolution.
  - Radiation hard.
  - Low materials.



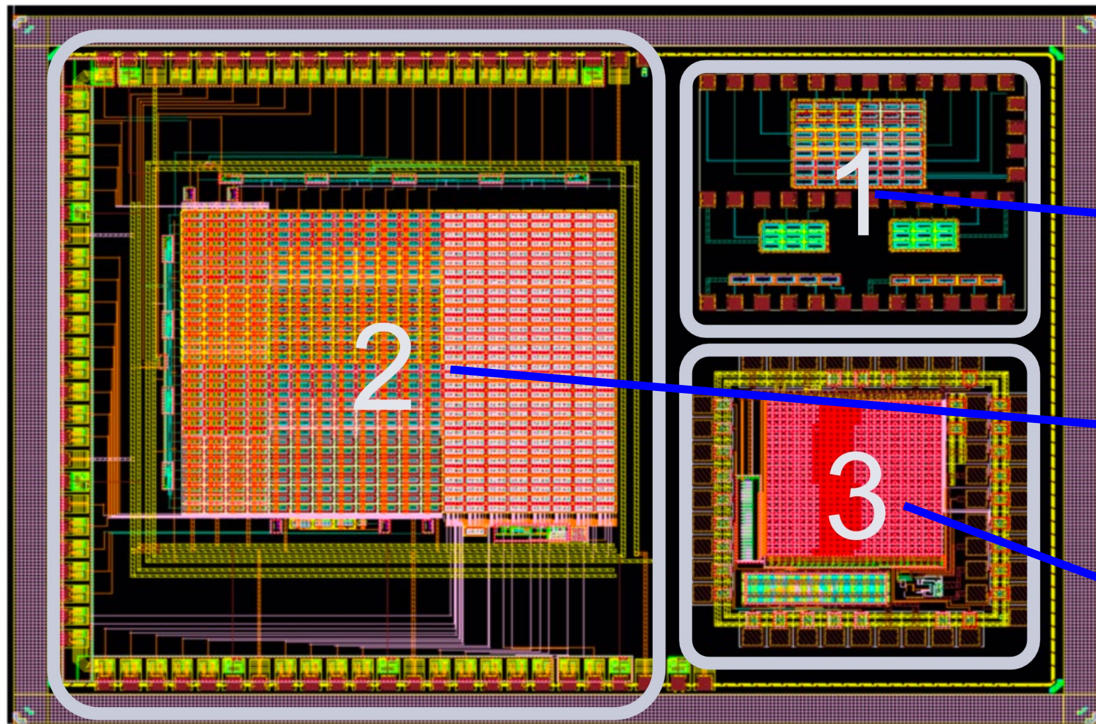
- CMOS strips compared with CMOS pixels:
  - Lower cost and power consumption per chip.
  - Simpler readout with fewer technical barriers for chip development, as there is no interference between the readout circuit and sensor due to the detection distance.
  - Comparable or even better spatial resolution, and negligible track ambiguity through specific detector layout design.
  - The CEPC ITK endcap is designed with strip sensors featuring a 22.5◦ cross angle between 2 half-layers.

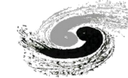
    Advantages: Better intrinsic spatial resolution in bending direction (~3.6 µm) and improved charge resolution for PID.
    Disadvantages: Compared to pixel detectors, it requires twice the number of detector chips, along with a certain increase in materials budget.

R&D: CMOS Chip Development

- CMOS pixels (COFFEE2): SMIC 55 nm CMOS process

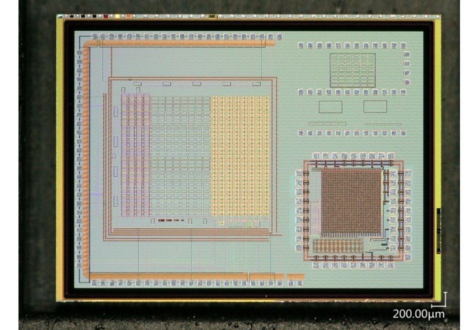
Submitted in Aug 2023, received in Dec 2023





CMOS SENSOR IN FIFTY-FIVE NM PROCESS

COFFEE2



Three sections in the chip:

1: Passive diode arrays:

- Including 6 different signal collection structures for studying diodes and charge sharing.

2. Pixel arrays with diodes and in-pixel electronics:

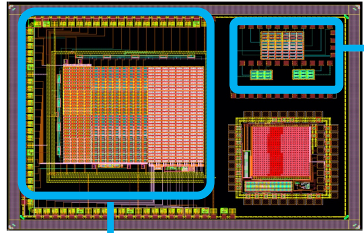
- Features 6 types of diodes and 3 types of in-pixel electronics.

3. Pixel arrays with peripheral digital readout:

- Used for validating readout strategies

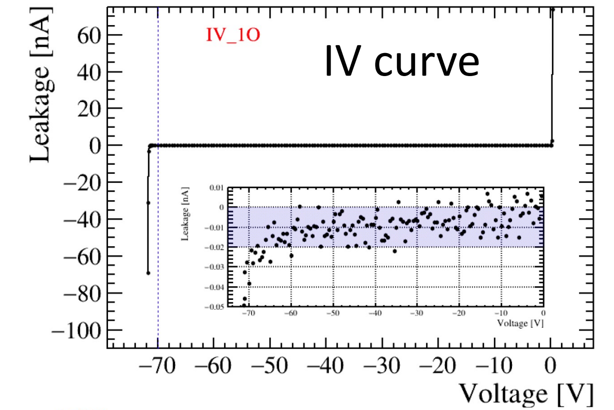
The COFFEE2 chip test is progressing well, the tape-out of the first CMOS strip chip (CSC1) for CEPC is scheduled for submission in 1-2 months.

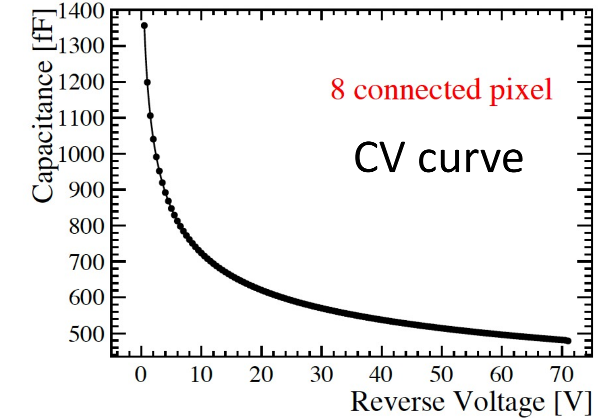
HVCMOS (COFFEE2) Chip Test

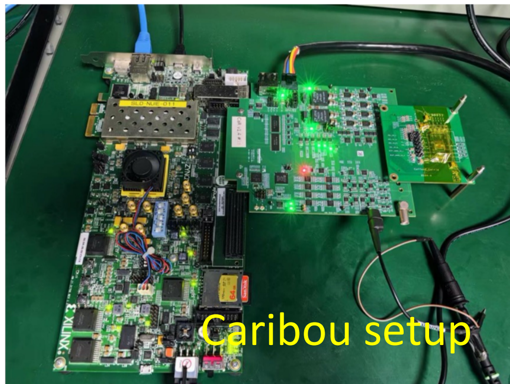


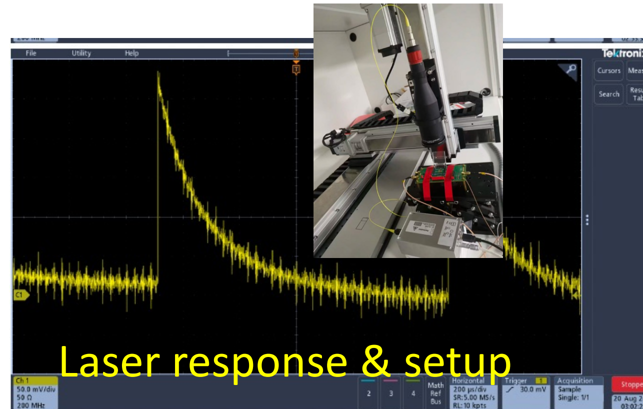
- So far tests have been focused on passive diode arrays
  - IV (breakdown at –70 V)
  - CV (single pixel ~30-40 fF)
  - Leakage current increased from 0.01 nA to ~1 nA after $10^{14} n_{eq}/cm^2$ radiation
  - Laser response observed
  - Radioactive source observed

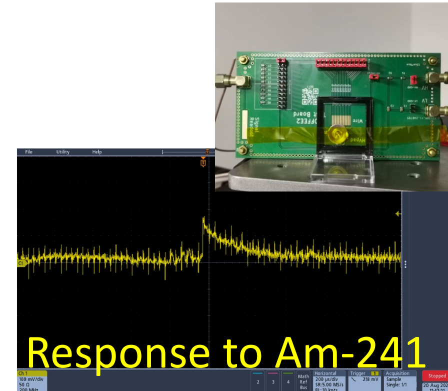
- Circuit test almost ready
  - Carrier board fabricated
  - Caribou system installed, final firmware debugging

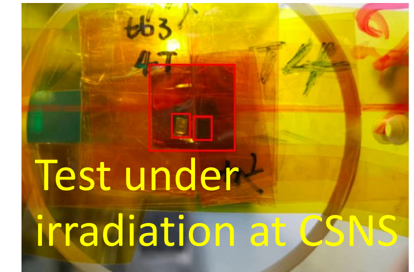





Caribou setup


Laser response & setup


Response to Am-241

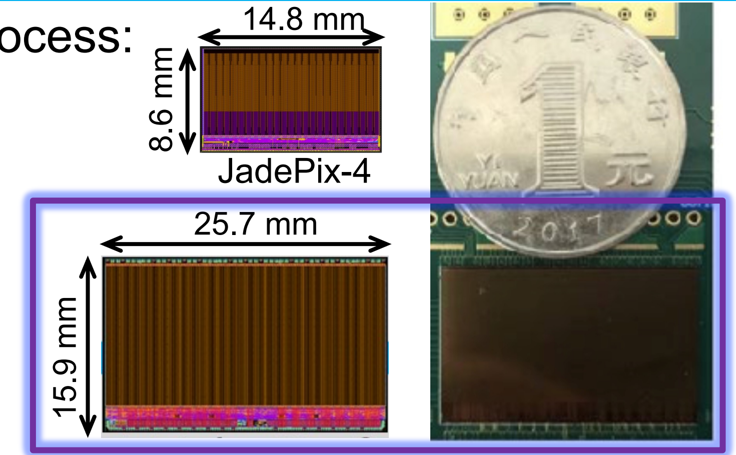

Test under irradiation at CSNS

The tape-out of the next HVCMOS (COFFEE3) chip is planned for the first half year of 2025.

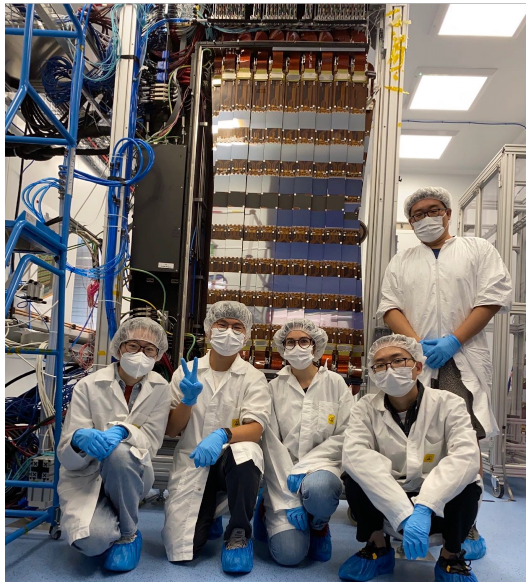
Experience in Silicon Detector Development

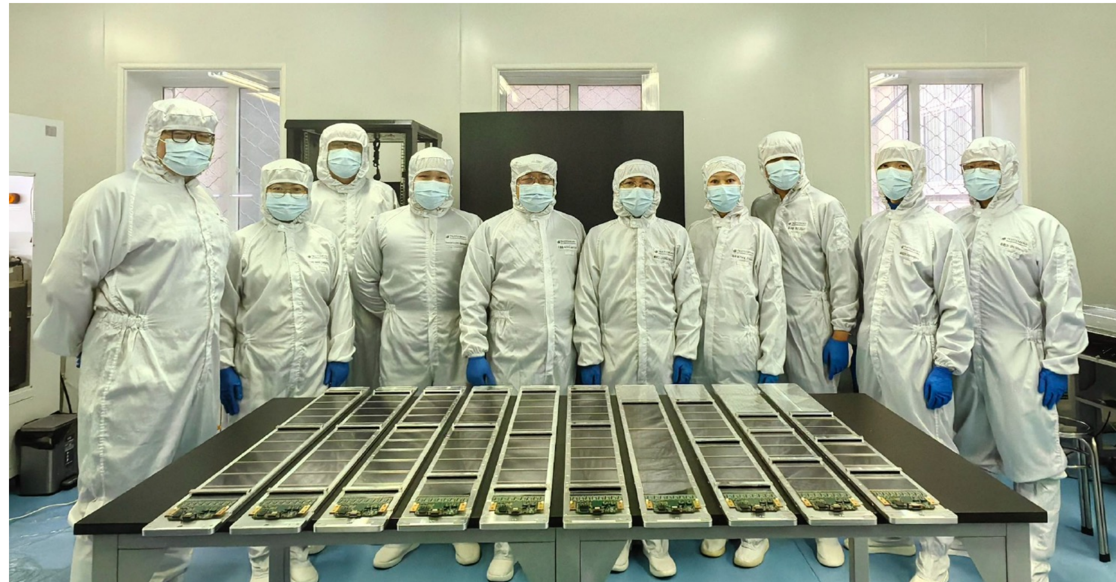
- The IHEP team has successfully developed several fully functional MAPS:
  - JadePix, TaichuPix, CPV, etc.

- Major contributions to silicon detector construction, testing, integration, and operation:
  - LHCb Upstream Tracker, AMS L0 upgrade, ATLAS ITK, ATLASPix, CHESS, etc.



TaichuPix-3

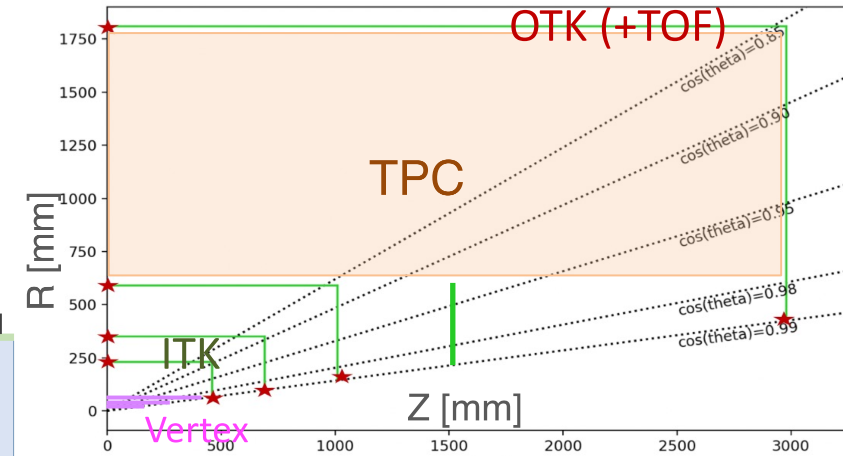

LHCb UT A-side assembly


AMS L0 ladder production

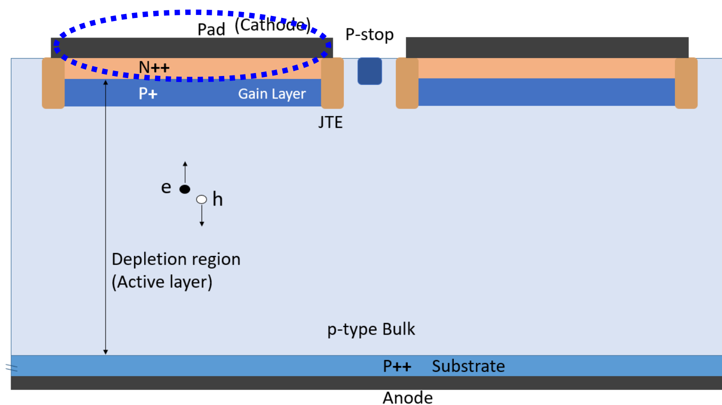
ATLAS ITK strip module

OTK (+TOF): Technology Survey and Our Choice

- The outer silicon tracker (OTK) uses AC-LGAD microstrip sensor:
  - Spatial resolution: 10 μm (with a strip pitch of 100 μm)
  - Time resolution: 30-50 ps

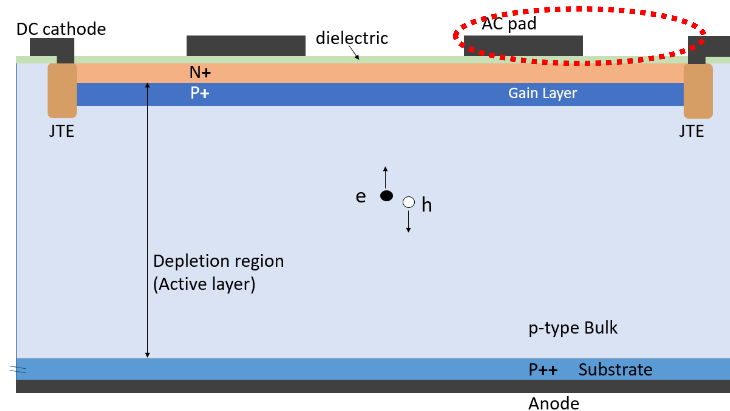


LGAD (Low-Gain Avalanche Diode)
Segmented gain layer



- The read-out electronics is connected to the N++ layer.

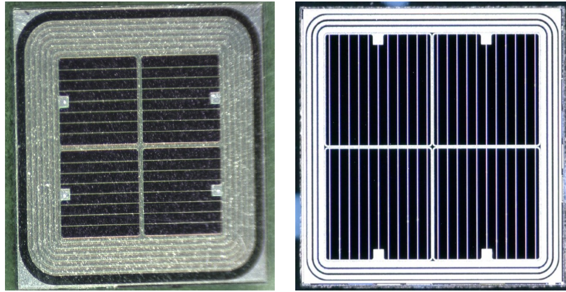
AC-LGAD (AC-coupled LGAD)
Continuous gain layer



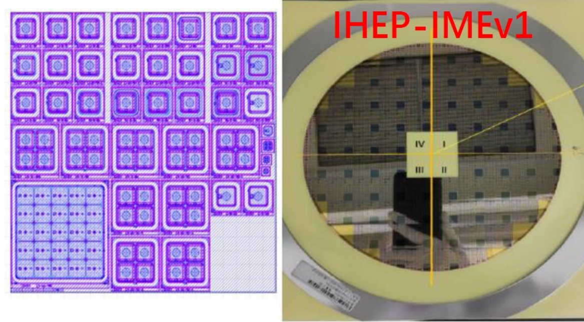
- A thin dielectric layer (Si_3N_4, SiO_2) separates the metal AC pads from the N+ layer.
- Less dead area and better position resolution.

LGAD Development at IHEP

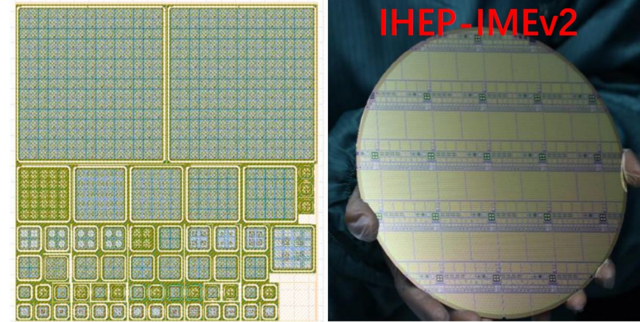
IHEP-NDL(2019)



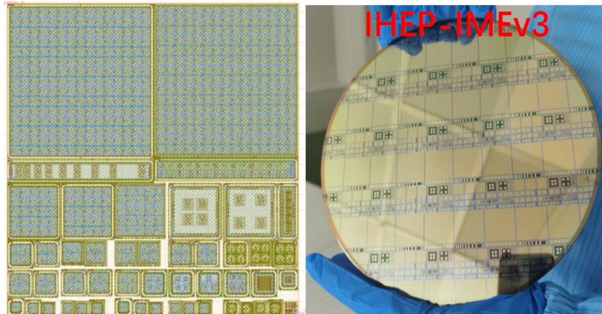
IHEP-IMEv1(2020.9)



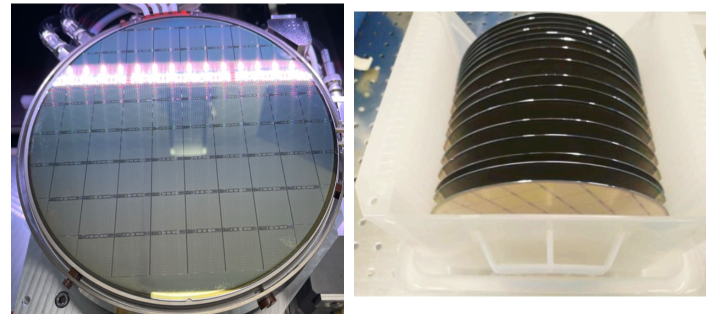
IHEP-IMEv2(2021.6)



IHEP-IMEv3(2022.5)



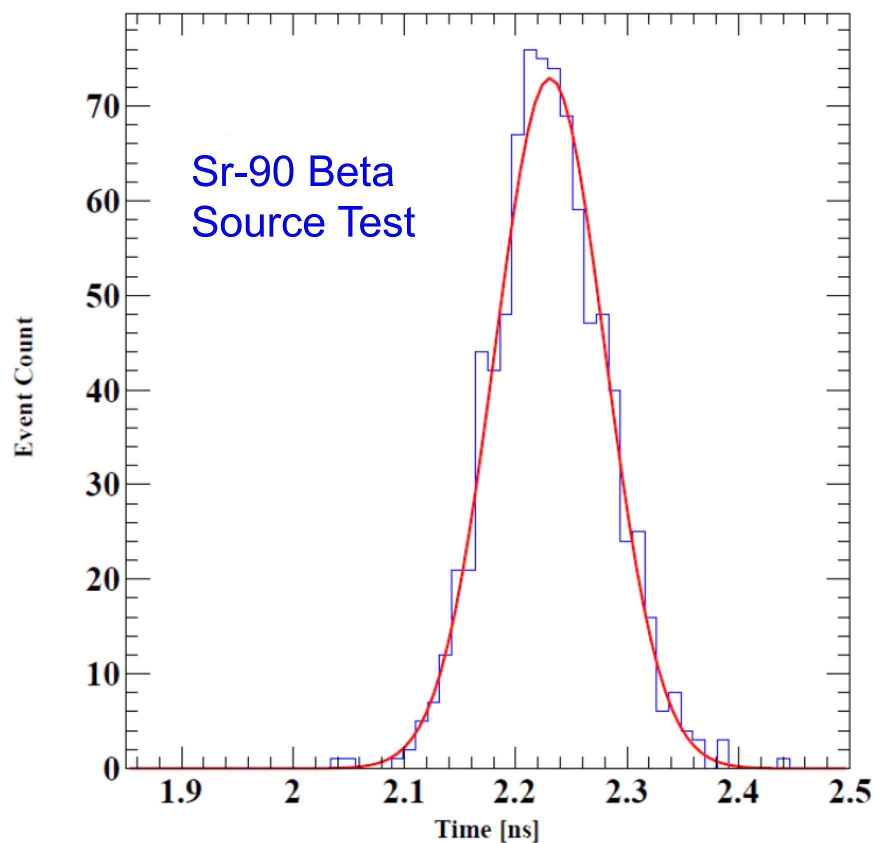
Pre-production for ATLAS (2023.7)



Mass production for ATLAS (2024.6)

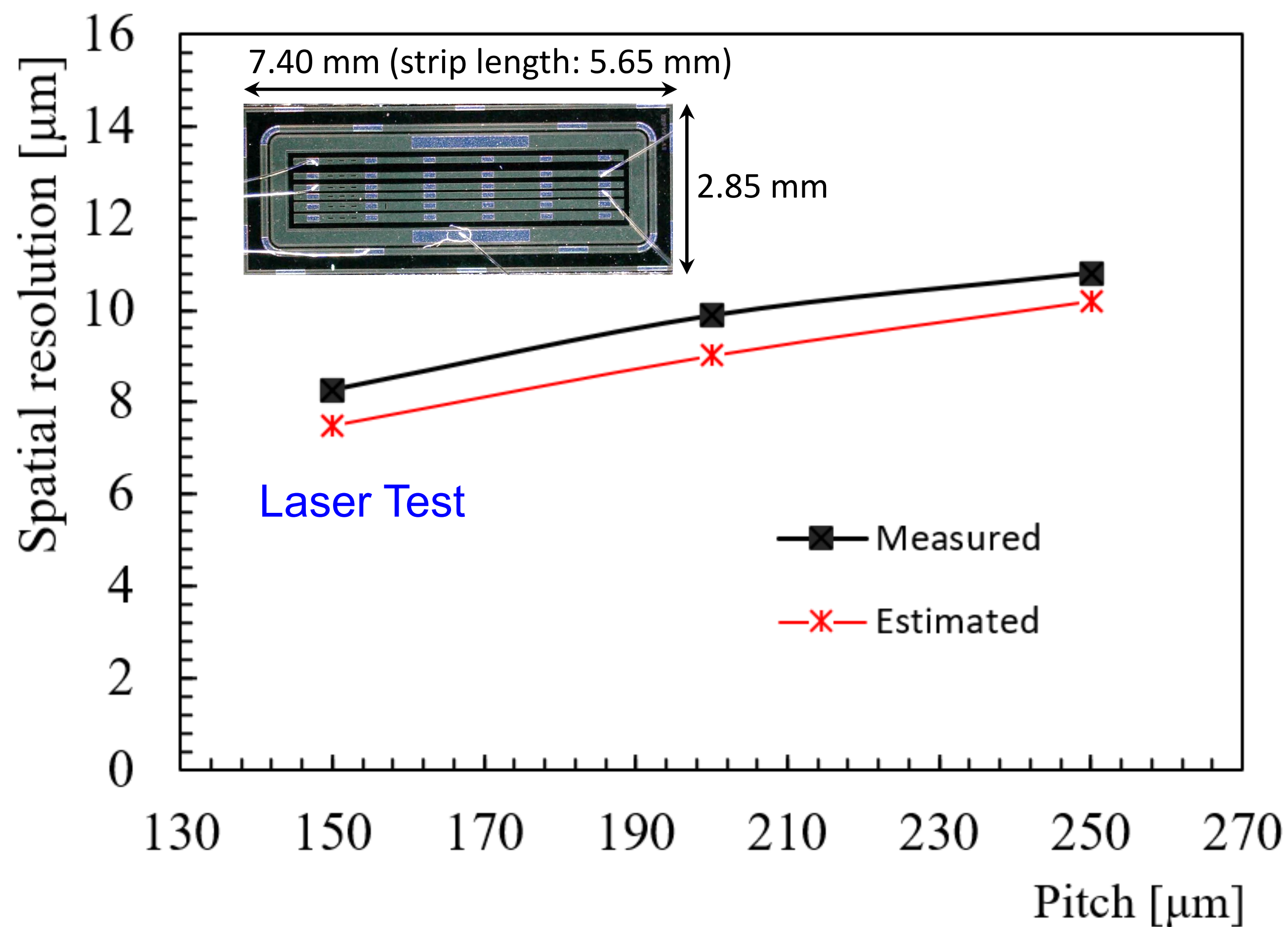
- In May 2023, CERN selected IHEP-IME in the HGTD sensor tendering process:
  - First time a domestic silicon sensor was chosen by CERN for an LHC experiment.

AC-LGAD Performance: Time and Spatial Resolution



Time residual sigma: 47.1 ps

Time resolution: 37.5 ps



Spatial resolution: 8 μm for 150 μm strip pitch size

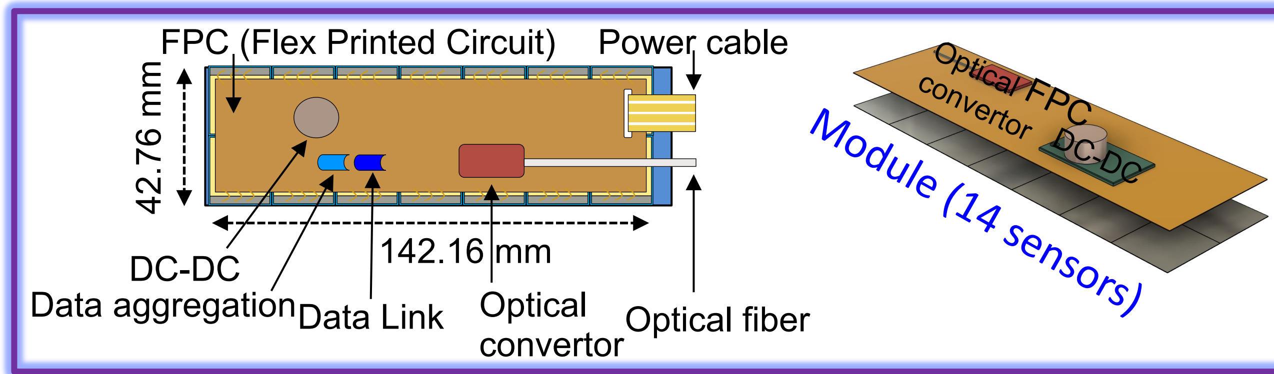
10

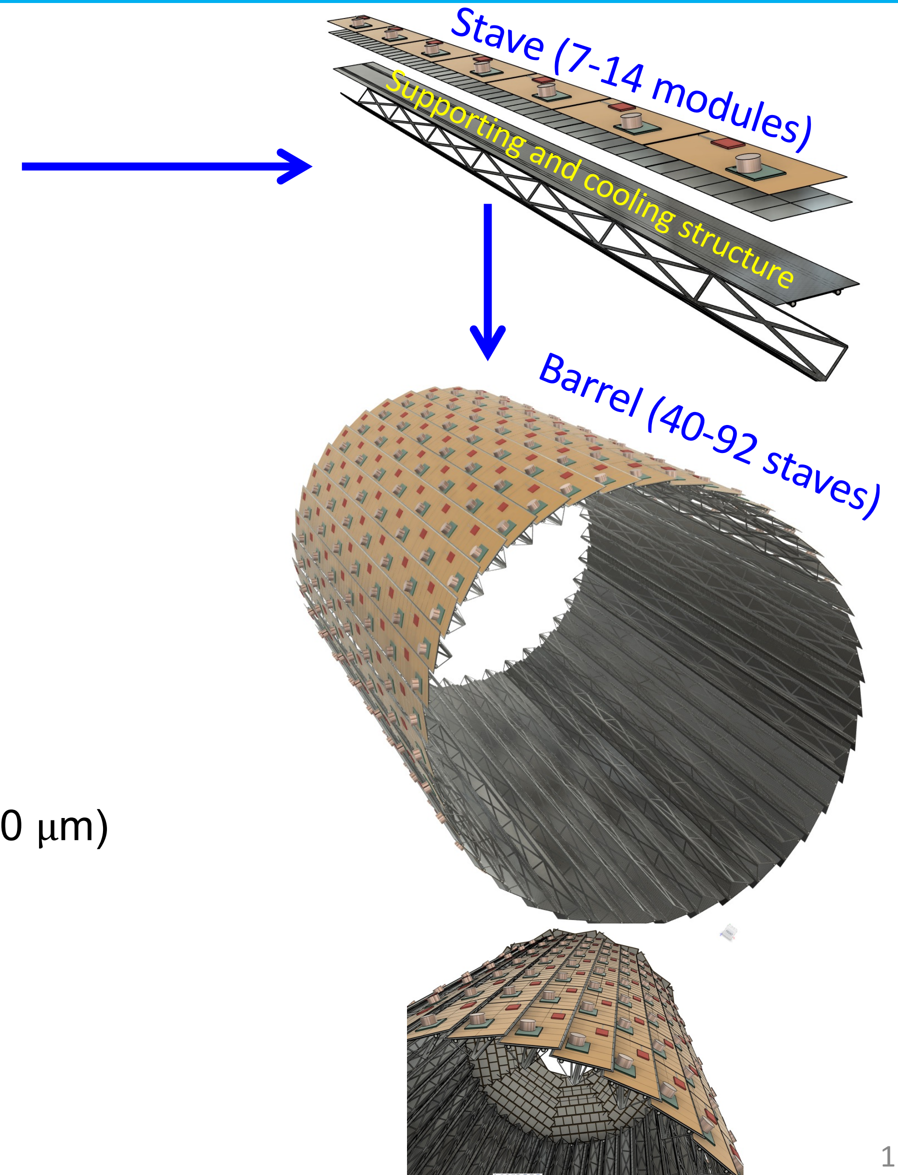
Summary of Sensor Parameters

	Monolithic HVCMOS pixels	Monolithic CMOS strips	Hybrid AC-LGAD strips
Pixel Size (Strip Pitch Size)	34 μm × 150 μm	20 μm	100 μm
Sensor size	2 cm × 2 cm (active area: 1.92 cm x 1.74 cm)	2.1 cm × 2.3 cm (active area: 2.05 cm x2.05 cm)	(6-9) cm × (3-5) cm
Array size (Strip number)	512 rows × 128 columns	1,024	384-512
Spatial resolution	σ_{φ} ~8 μm (bending), σ_z~40 μm	σ~5 μm	σ~10 μm
Timing resolution	~3-5 ns	~3-5 ns	~50 ps
Data size per hit (1 readout)	42 bits (14b BXID, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)	40-48 bits
Data rate per sensor	Maximum ~0.1 Gbps* (pair production)	Maximum ~0.2 Gbps* (pair production)	Maximum ~0.15 Gbps* (pair production)
LV / HV	1.2 V / 150 V	1.8 V / 150 V	1.2 V / 200 V

* Maximum hit rate: ITK barrel~4.1×10^5 Hz/cm^2, ITK endcap~7.5×10^5 Hz/cm^2, OTK barrel~0.9×10^4 Hz/cm^2, OTK endcap~3.5×10^4 Hz/cm^2

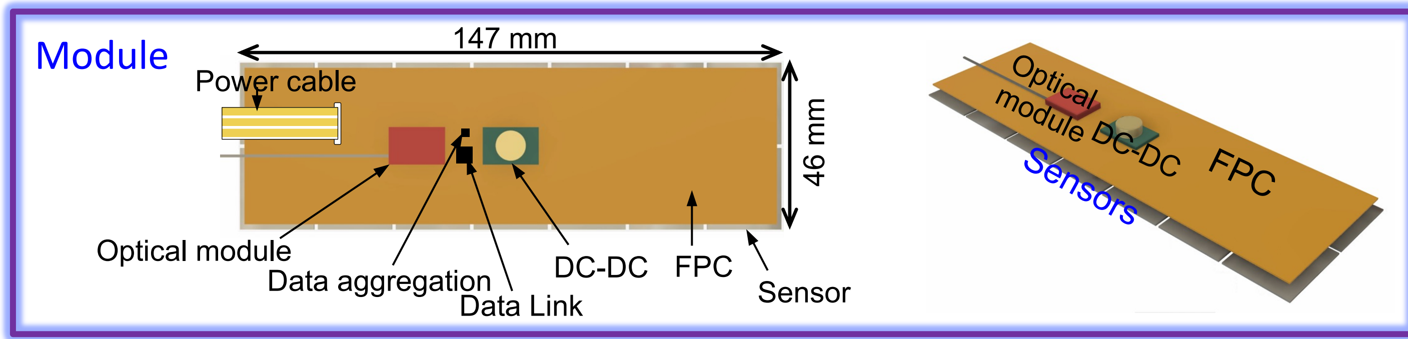
CEPC ITK Barrel Design (HVCMOS Pixels)

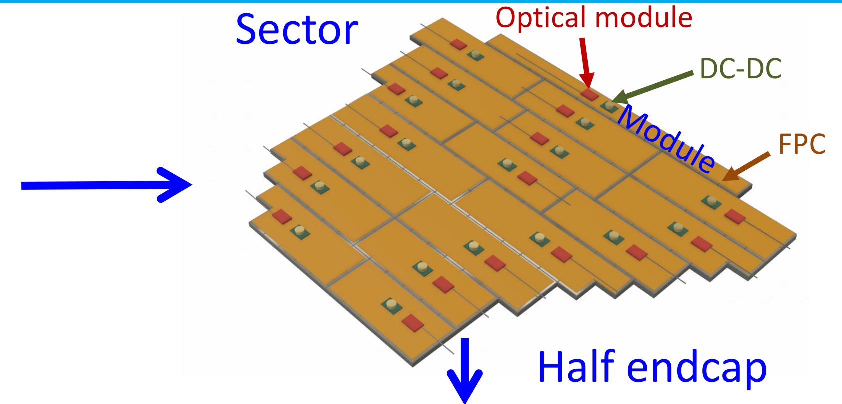




- HVCMOS pixels for CEPC:
  - Utilizes 55 nm process instead of the 180 nm used in ATLASPix3
    More functionality and less power consumption
  - Wafer resistivity: 1k-2k Ω·cm
  - Chip size: 2 cm × 2 cm
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~200 mW/cm^2

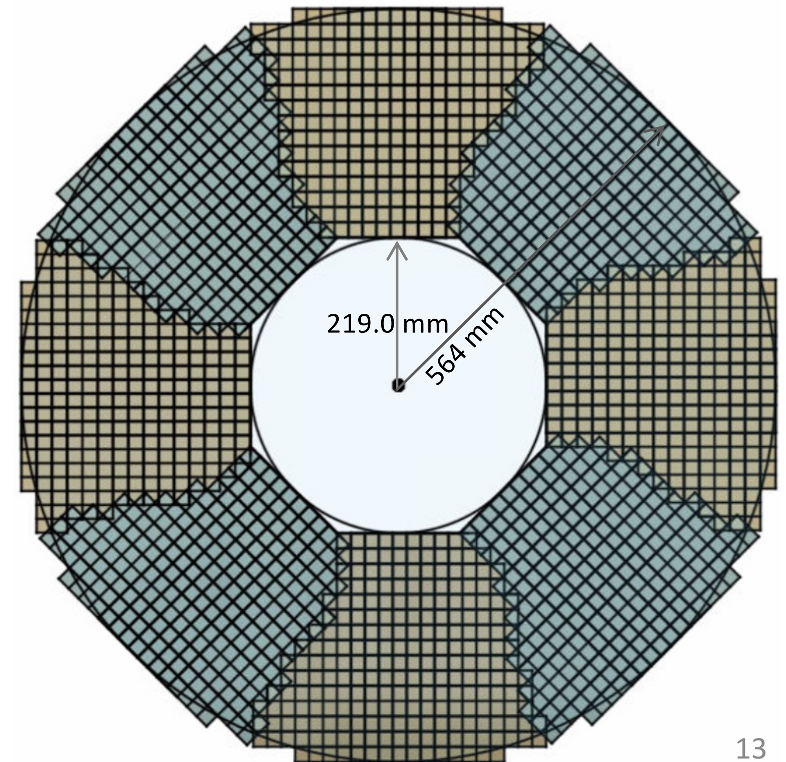
CEPC ITK Endcap Design (CMOS Strips)





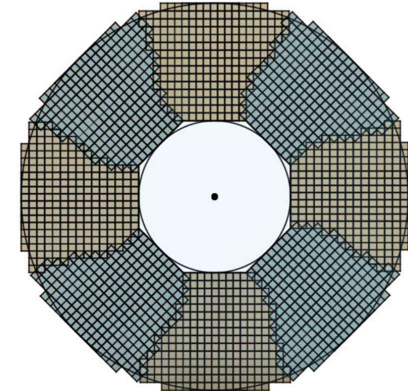
- CMOS Strip Chip (CSC) for CEPC:
  - Utilizes 180 nm process (CSMC, Wuxi Shanghua)
  - Wafer resistivity: 2k Ω·cm
  - Chip size: 2.1 cm × 2.3 cm
  - Strip number per chip: 1,024
  - Strip pitch size: 20 μm (spatial resolution <5 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~80 mW/cm^2

Each half endcap is divided into 8 sectors, with each sector consisting of CMOS strip modules. The overlapping areas between the neighboring sectors are designed to be minimal.

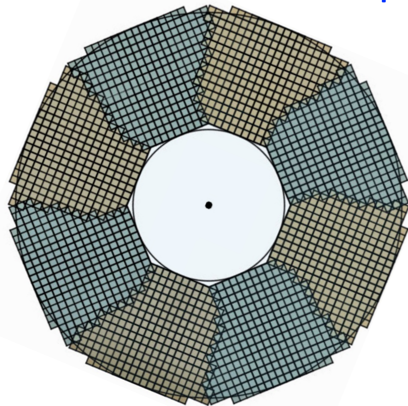


Two half endcaps are rotated 22.5◦ relative to each other to form one complete endcap:

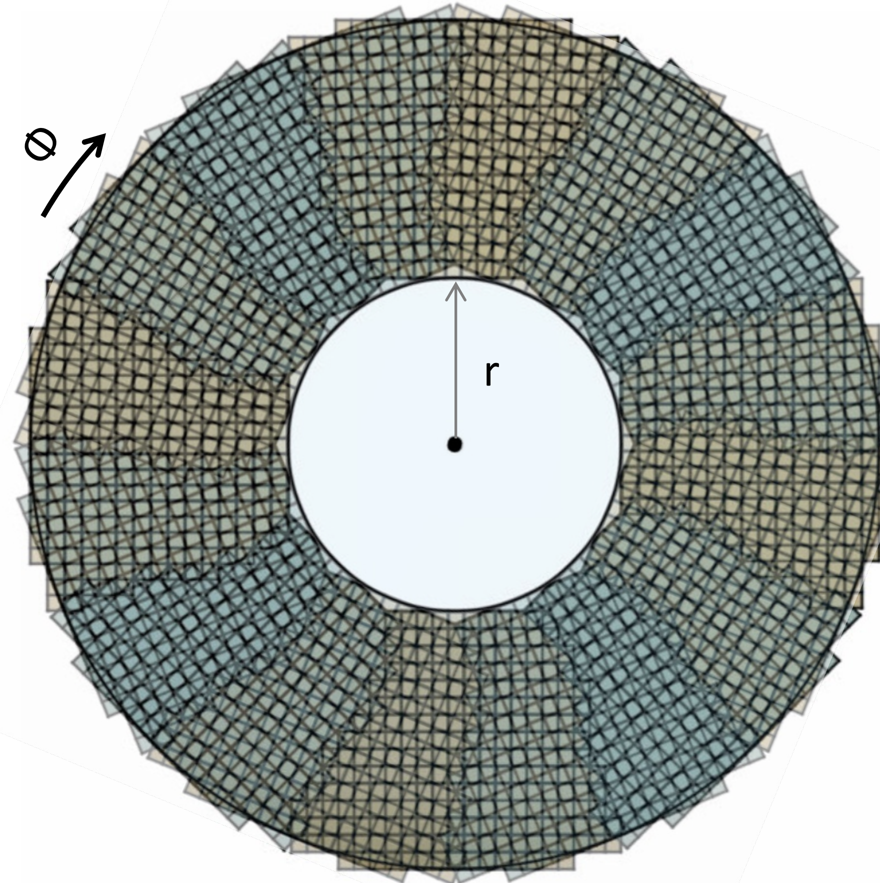
- Maximize track resolution in bending direction ϕ
- Minimize track ambiguity

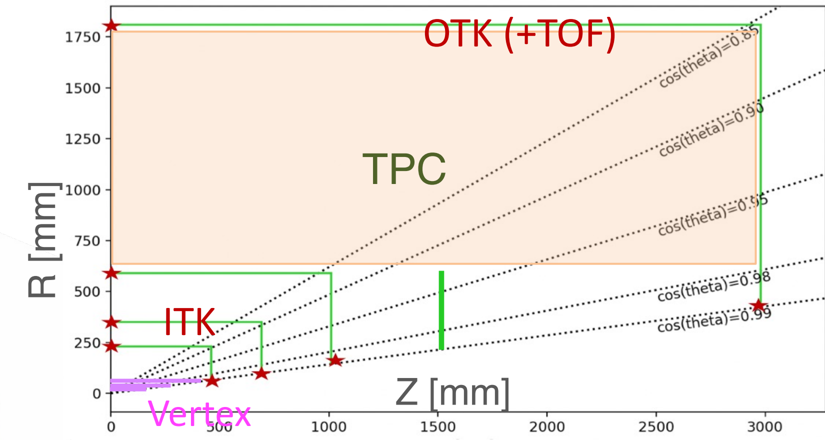


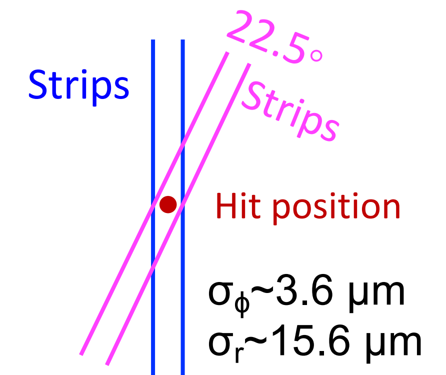
Normal half endcap



22.5◦ half endcap



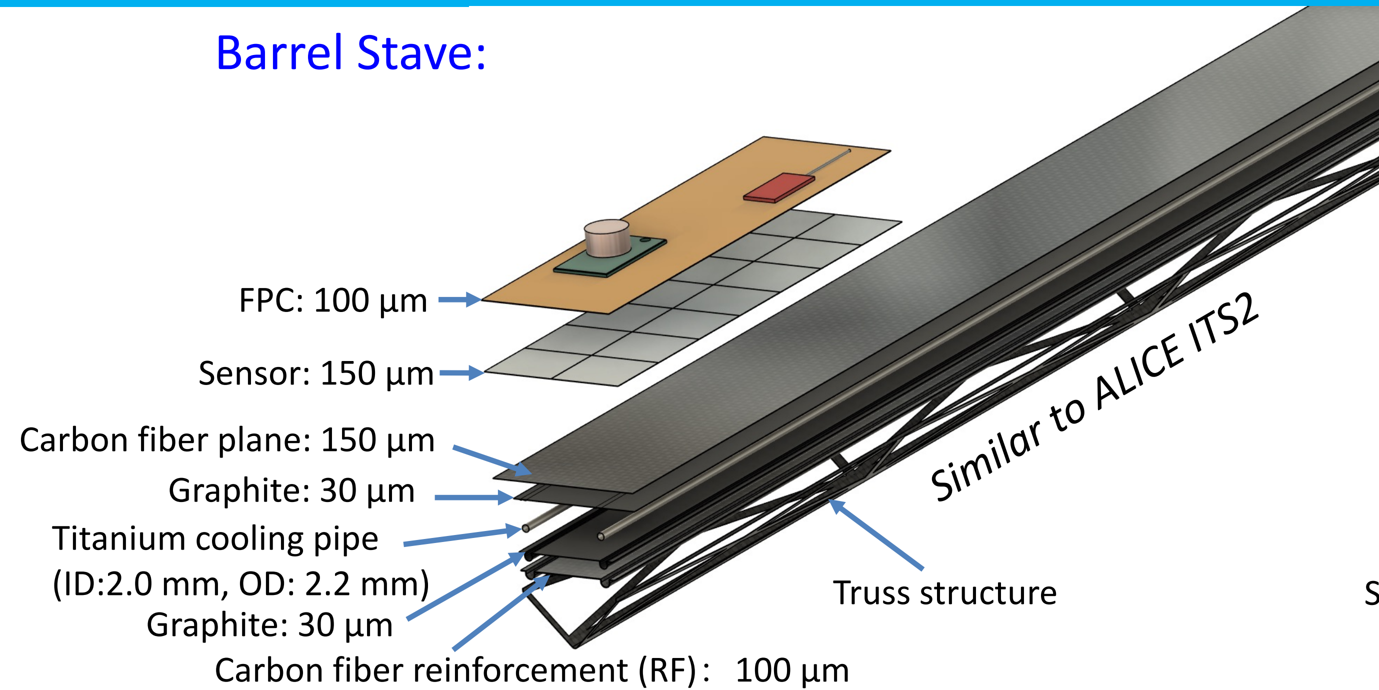


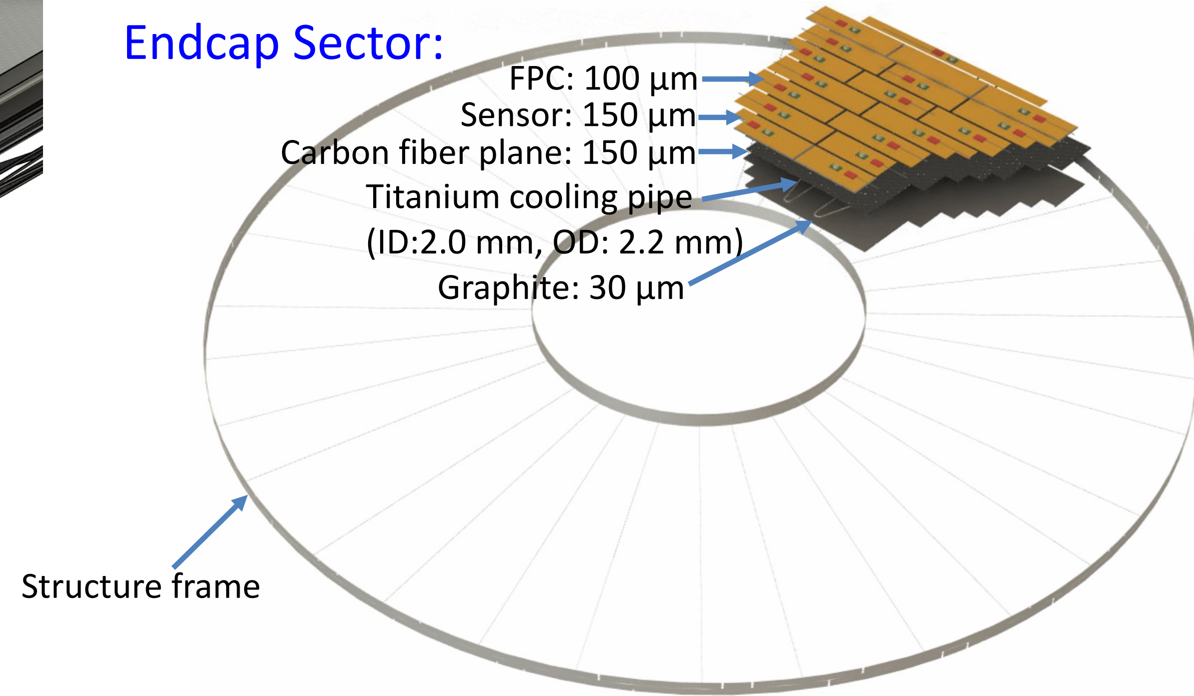


Detection precision using 20 μm pitch strips

The CEPC ITK barrels using pixels is considered for minimal material, while ITK endcaps using strips is optimized for high momentum measurement and particle identification (no TPC).

ITK Mechanical and Cooling Structure

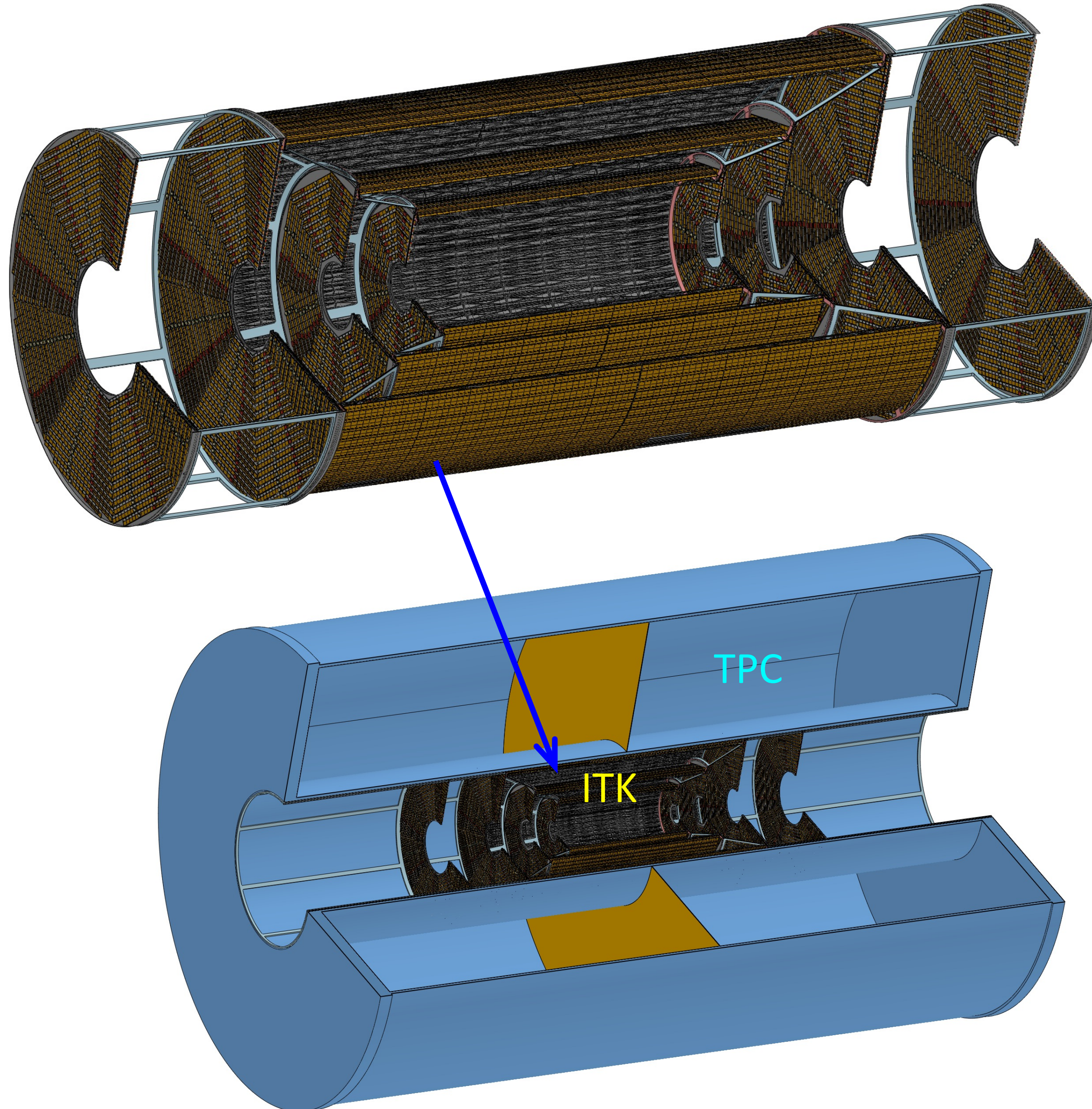




Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Sensor	0.15	0.18
Carbon fiber×2	0.25	0.10
Graphite×2	0.06	0.03
Others		0.05
Total		0.50

Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Sensor	0.15	0.18
Carbon fiber	0.15	0.06
Graphite	0.03	0.02
Others		0.03
Total		0.43

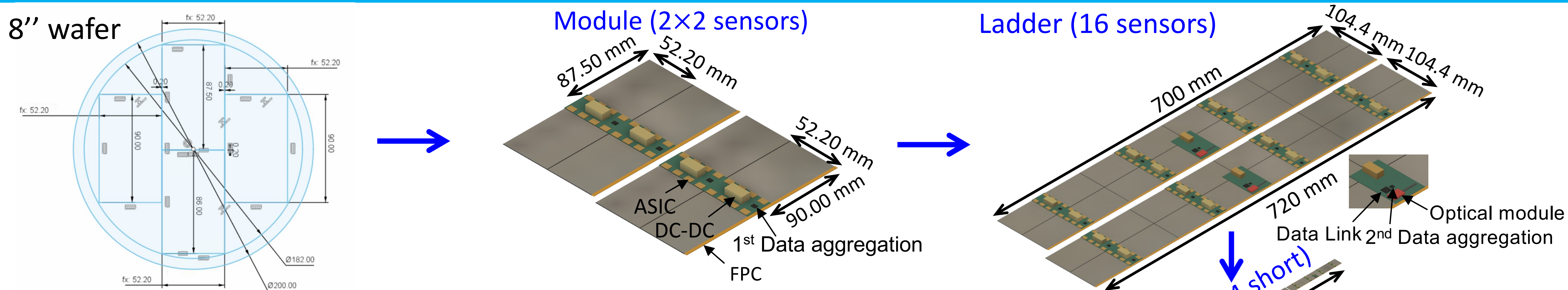
CEPC ITK Mechanics and Installation Design



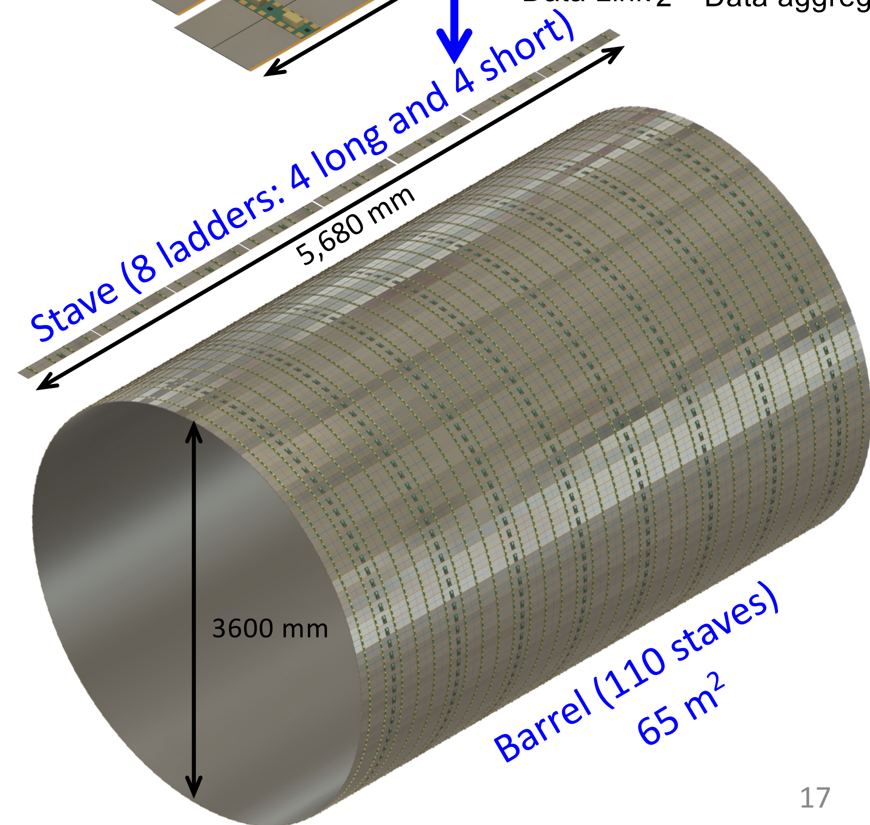
	Sensors	Sensor area
Barrels		
ITKB1	3,920	1.6 m^2
ITKB2	7,840	3.1 m^2
ITKB3	18,032	7.2 m^2
Total	29,792	11.9 m^2

Endcaps		
ITKE1	1,536	0.74 m^2
ITKE2	3,136	1.51 m^2
ITKE3	8,288	4.00 m^2
ITKE4	7,520	3.63 m^2
Total	20,480	9.89 m^2

CEPC OTK Barrel Design (AC-LGAD Strips)



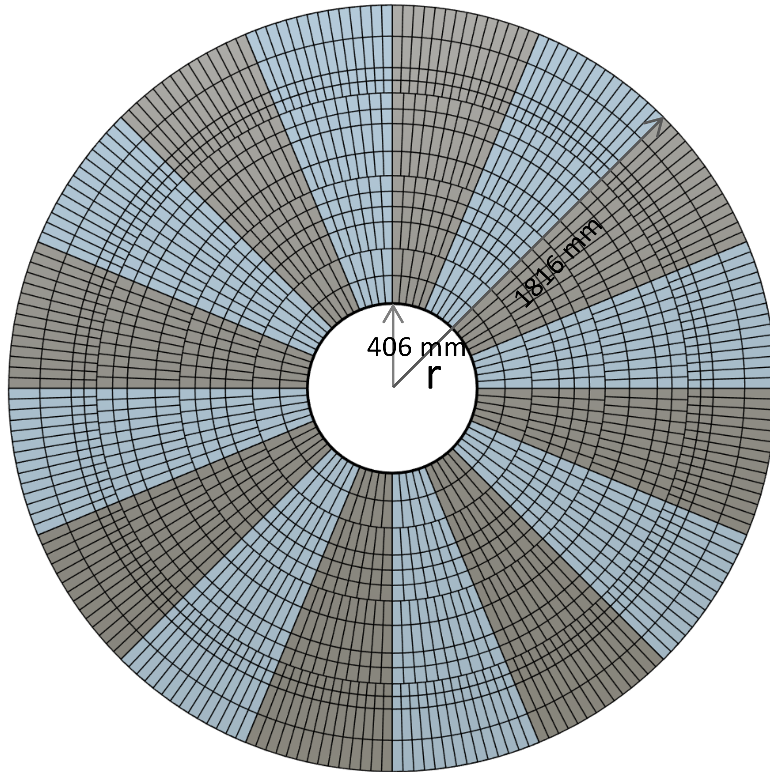
- CEPC outer silicon tracker (OTK) utilizes AC-LGAD (Low Gain Avalanche Detector) developed by IHEP-IME:
  - Sensor size: 8.75 cm × 5.22 cm
9.00 cm × 5.22 cm
  - Strip number per sensor: 512
  - Strip pitch size: 100 μm
  - Spatial resolution: 10 μm
  - Time resolution: 50 ps
  - Power consumption: ~300 mW/cm^2



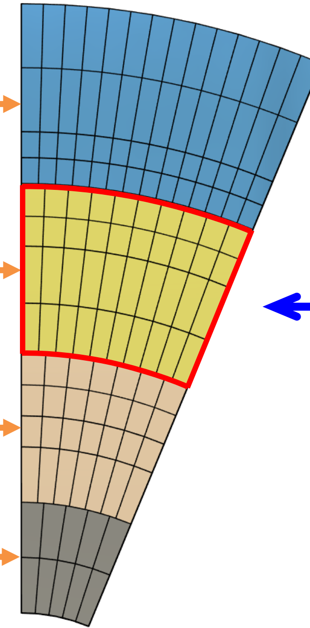
Maximum usage of silicon wafers for OTK barrel: a total 3,520 wafers, with 15% higher efficiency compared to a conventional single-piece sensor cut from a wafer.

CEPC OTK Endcap Design (AC-LGAD Strips)

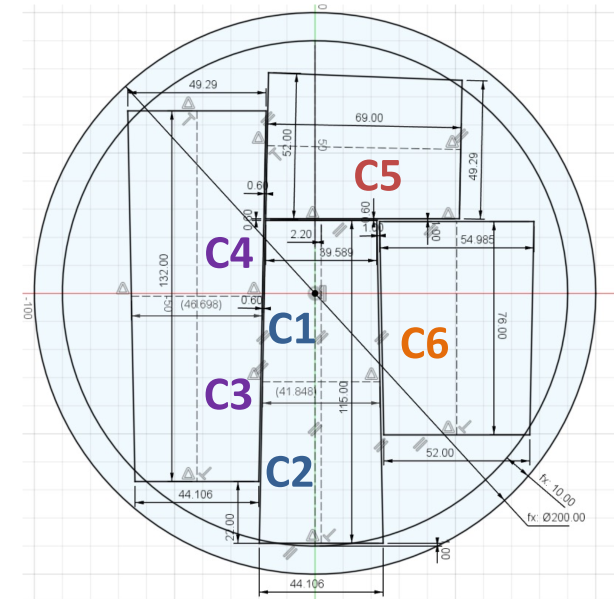
Endcap (16 sectors, 10 m^2):



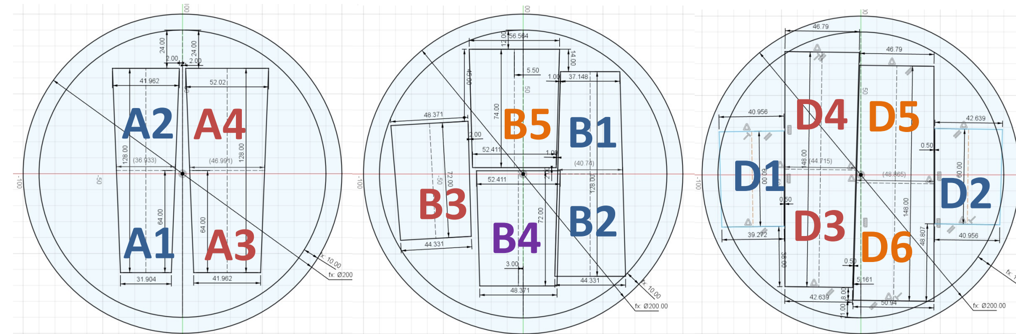
1/16 Sector:



Sensor: 8'' wafer (group C sensors)



8'' wafer (group A, B, D sensors)

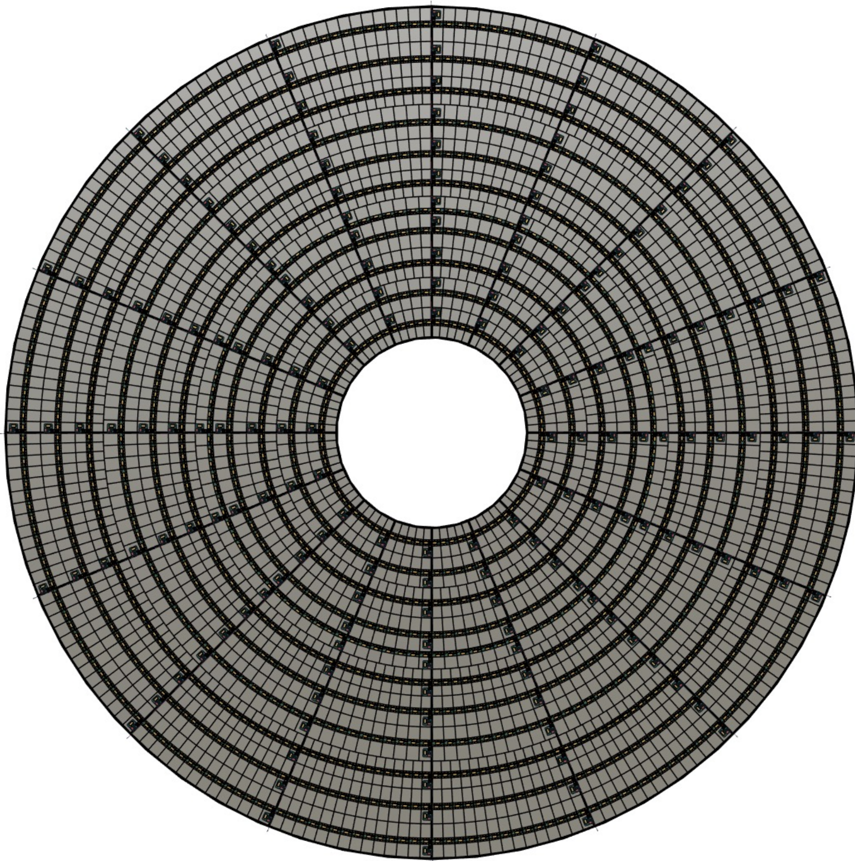


- OTK endcap consists of 14 rings, arranged into 4 groups.
- Each group contains 2-4 types of trapezoid sensors, which can be fitted to one 8'' silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
- The long sensor contains 2 sets of short-strip sensors.

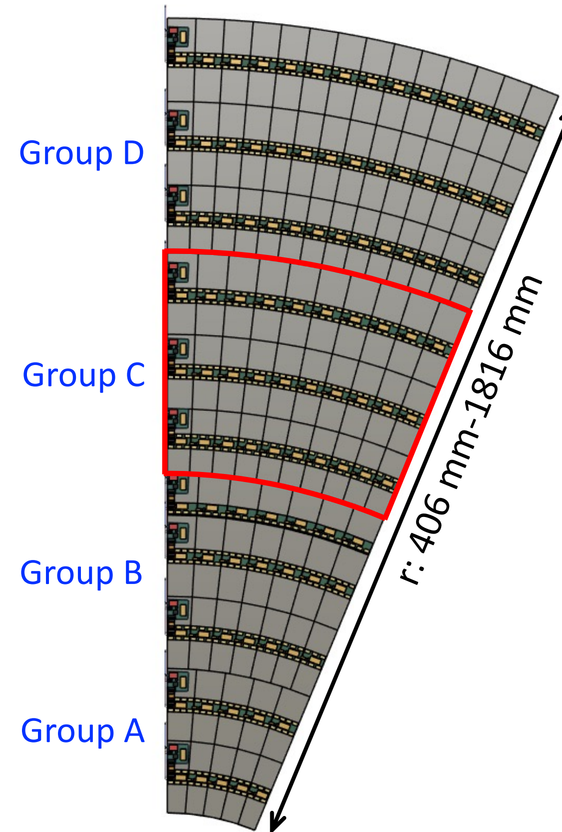
Maximize the use of silicon wafers and facilitate detector assembly.

CEPC OTK Endcap with Electronic Components

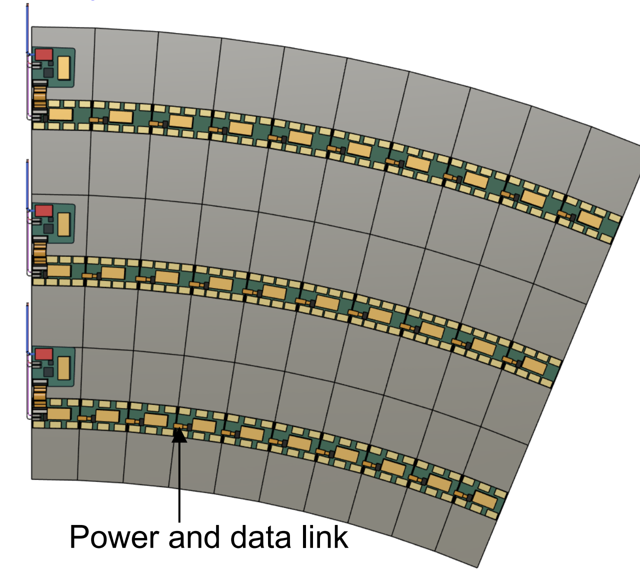
Endcap (16 sectors, 10 m^2):



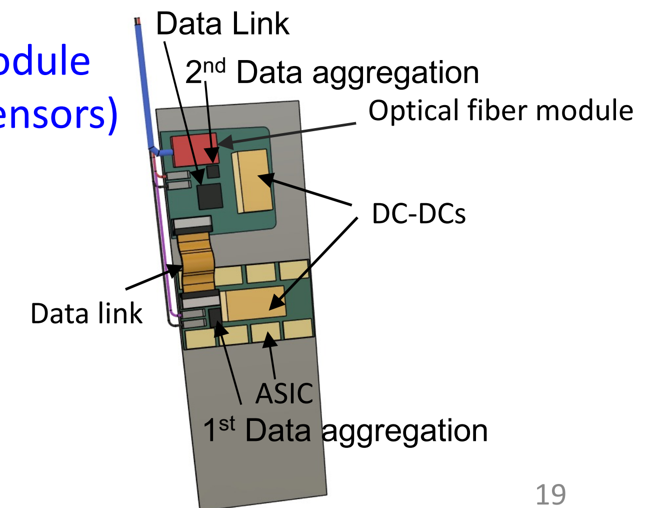
1/16 Sector:



Group C sensors:

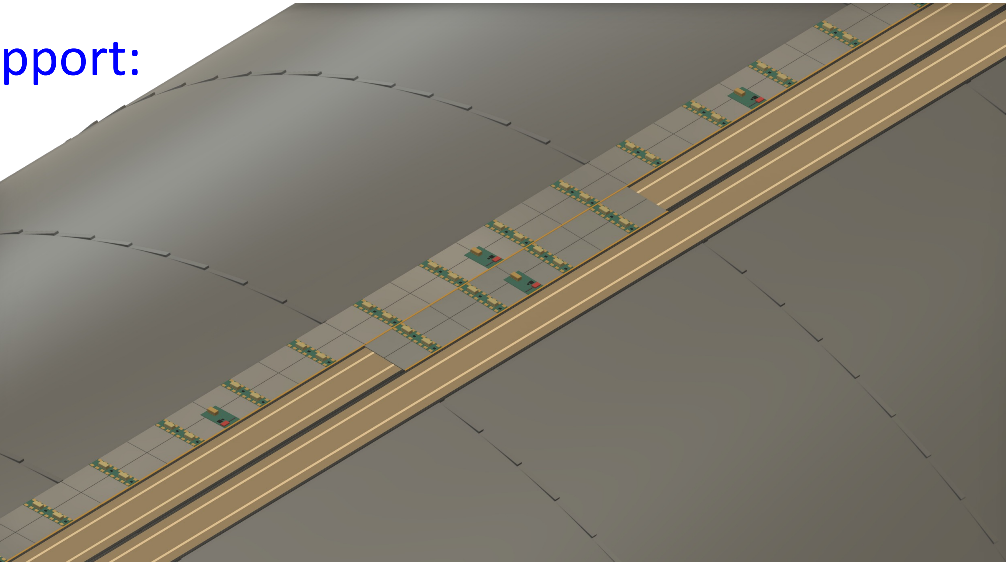


Module (2 sensors)



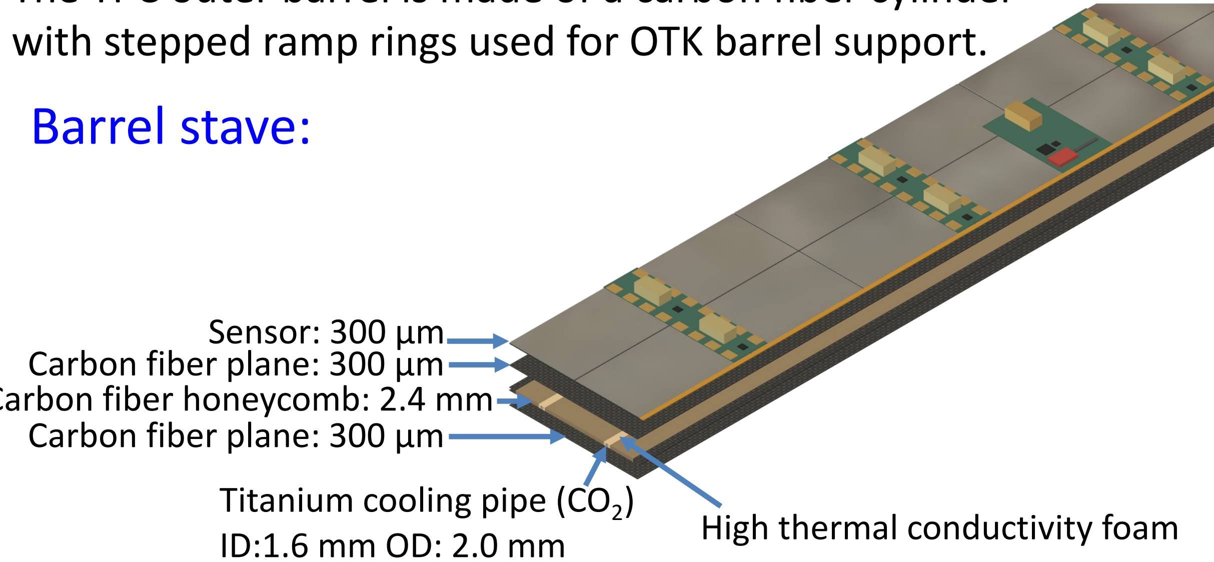
OTK Mechanical and Cooling Structure

Barrel support:

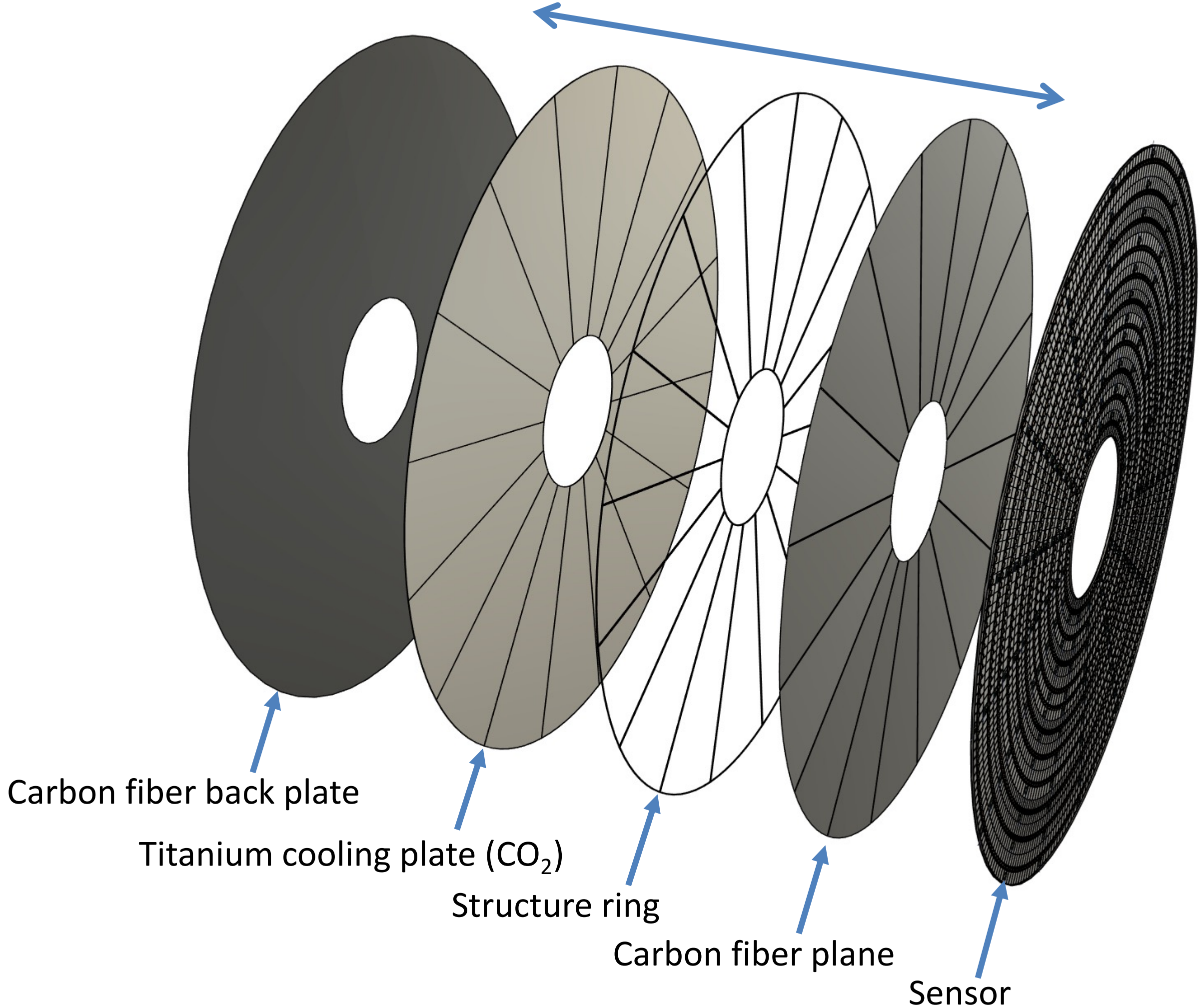


The TPC outer barrel is made of a carbon fiber cylinder with stepped ramp rings used for OTK barrel support.

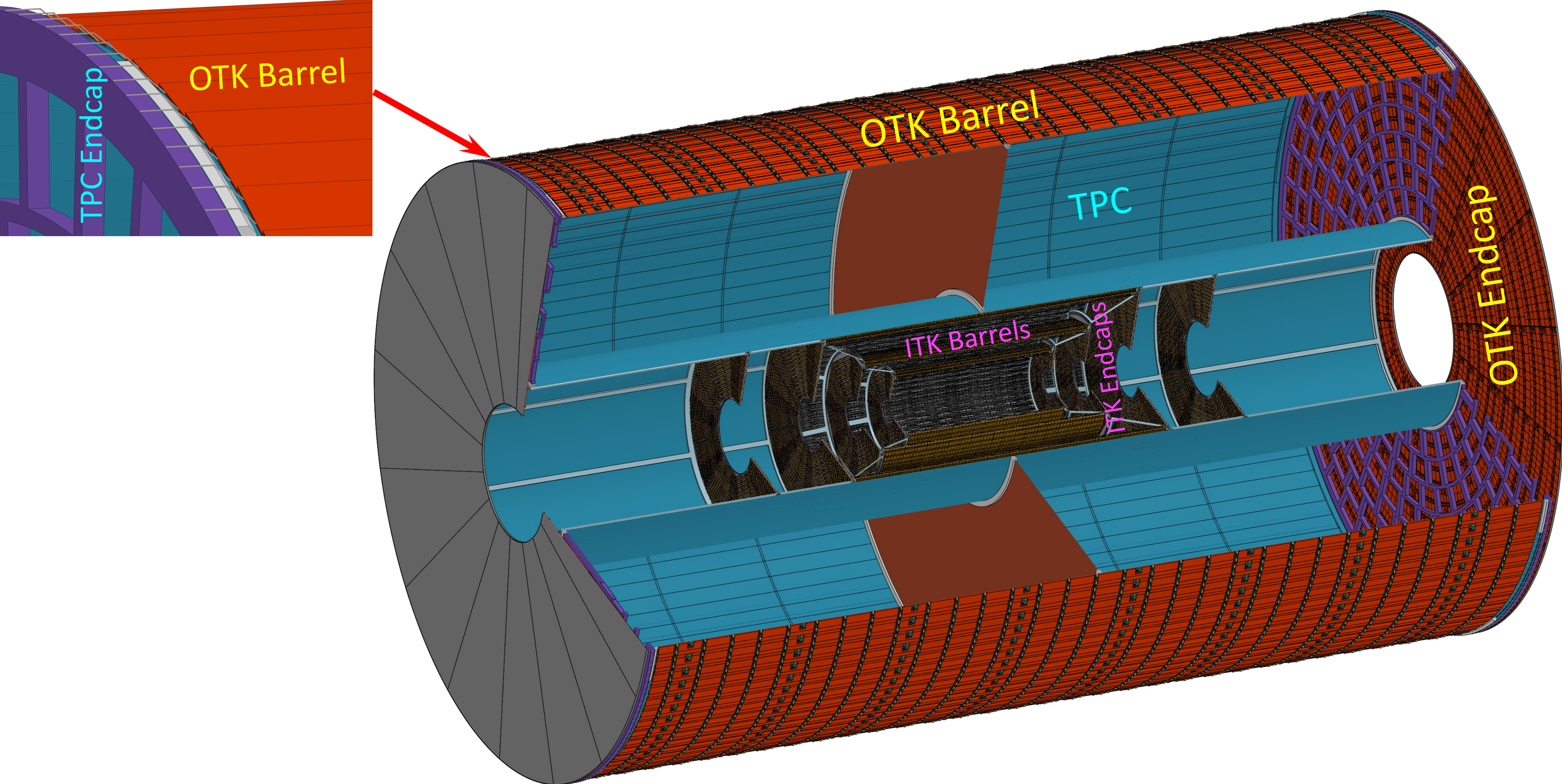
Barrel stave:



Endcap layout:



CEPC OTK Mechanics and Installation Design



Front-End Readout: CMOS Circuit or AC-LGAD ASIC

Pixels

Pixel matrix:
- 512 rows
- 64 double columns

Periphery & IOs

Schematic of a HV pixel sensor

Double column schematics: two pixels

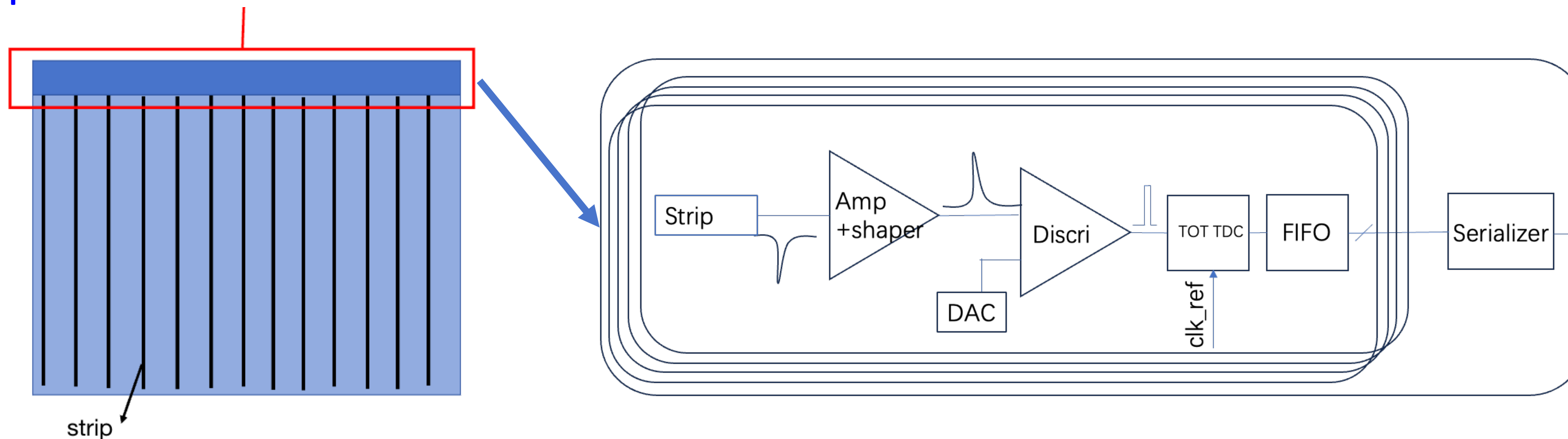
Pixel readout logic
sensor
Amp
Comparator
Tune DAC
Threshold
-HV
Addr
LE
TE
Fine time stamp logic
BCID
Token
DATA BUS
Read
Freeze

LE: Leading edge
TE: Tailing edge

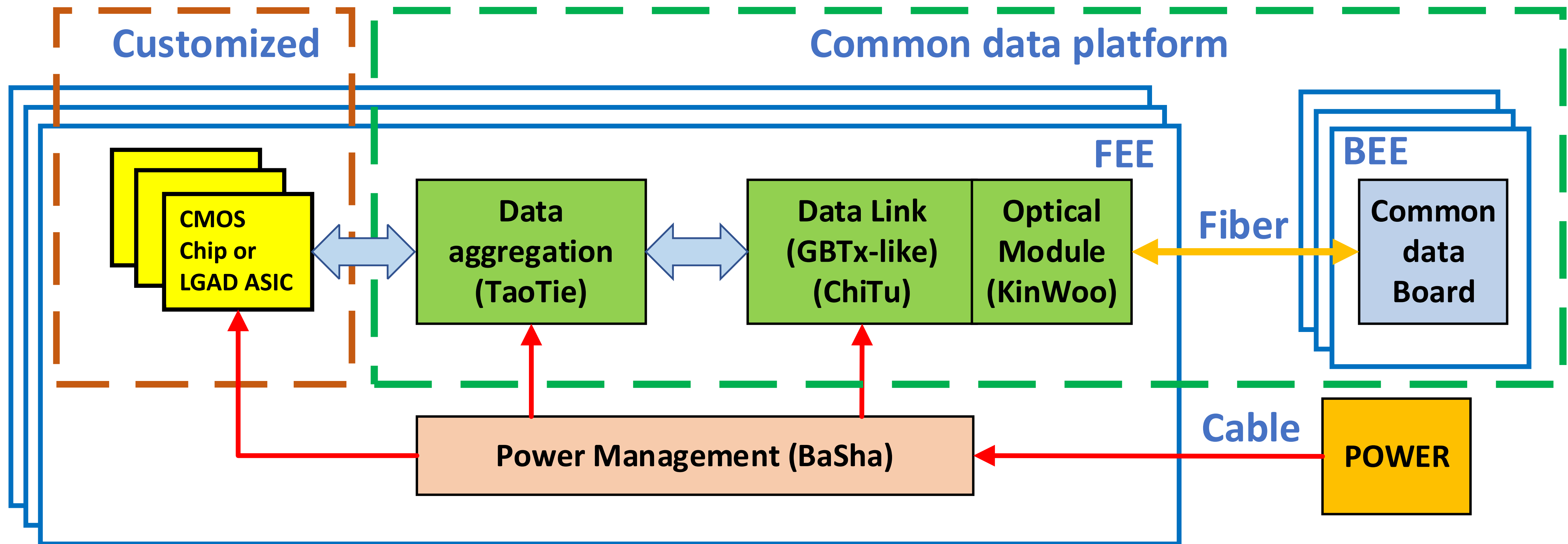
DACs for biasing
Digital process & data formation
R/O controller
......
R/O controller
40 MHz
PLL
FIFO and FSM
640 MHz
serializer
I^2C slow control
LVDS
Up to 1.28Gbps

Strips

CMOS Circuit or AC-LGAD ASIC



Silicon Tracker Common Electronics



- Data transmission: common data platform
- Trigger mode: triggerless

CEPC Tracker Performance from Simulation:
Momentum Resolution

$\sigma(P_t) / P_t\ [10^{-3}]$

10

1

OTK (+TOF)

TPC

ITK

Vertex

R [mm]

Z [mm]

1750
1500
1250
1000
750
500
250
0

0
500
1000
1500
2000
2500
3000

cos(theta)=0.85
cos(theta)=0.90
cos(theta)=0.95
cos(theta)=0.98
cos(theta)=0.99

Silicon Tracker

TPC

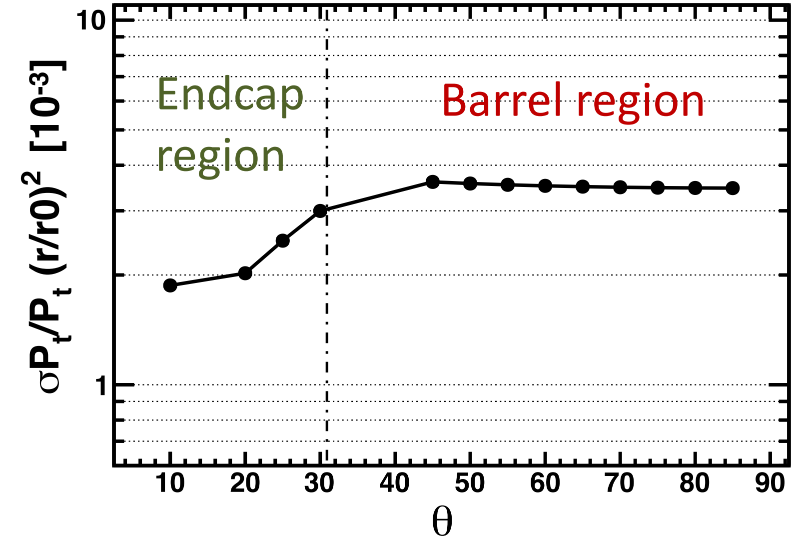
Silicon Tracker+TPC (Barrel)

10

100

P_t[GeV/c]

Silicon Tracker momentum resolution angular dependence (100 GeV/c)



r: the radius of OTK hit

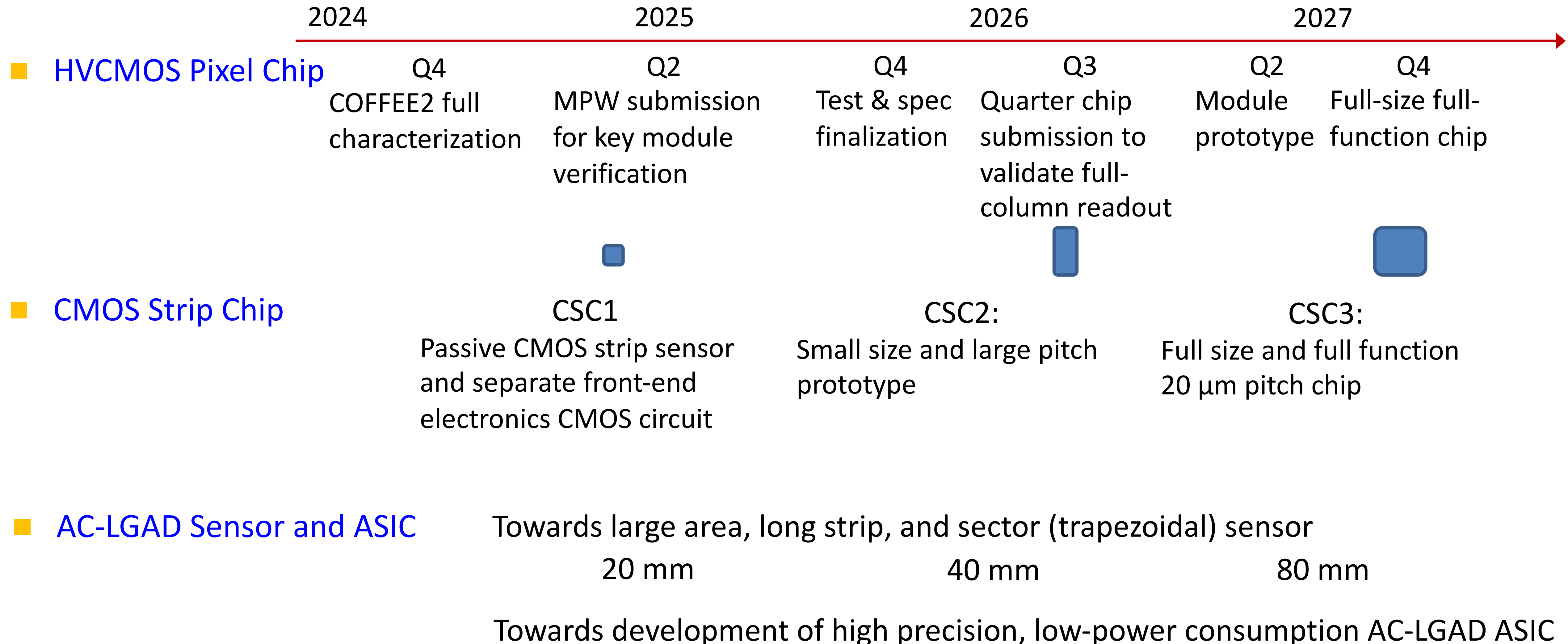
r_0: the radius of OTK barrel

Our Research Team

- ITK CMOS detector currently active: 18 institutes, 25 staff, 20+ postdocs & students

- OTK (+TOF) AC-LGAD currently active: 8 domestic and 2 international institutes, 18 staff, ~22 postdocs & students

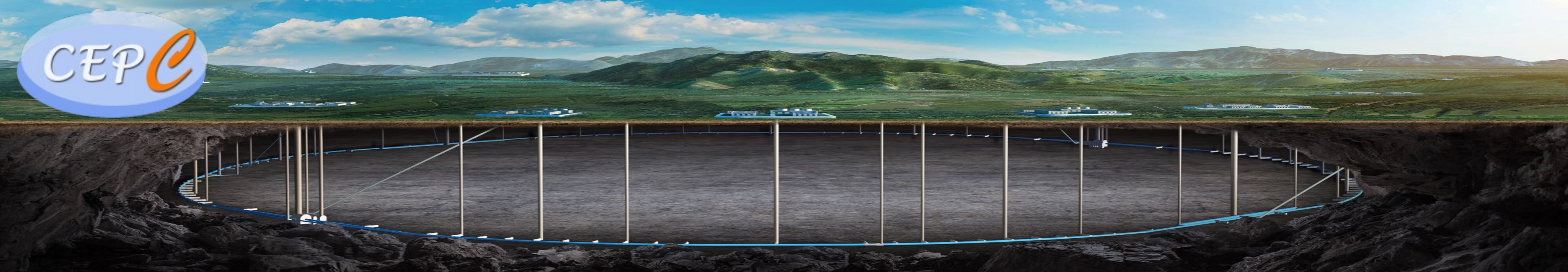
Working Plan



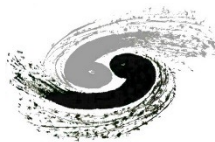
Summary

- CEPC incorporates the most advanced detector technologies while also having backup plan for construction.

- With the unique opportunity provided by CEPC to advance HEP semiconductor technology in China, we are steadily progressing in the development of forefront CEPC silicon tracker detector.

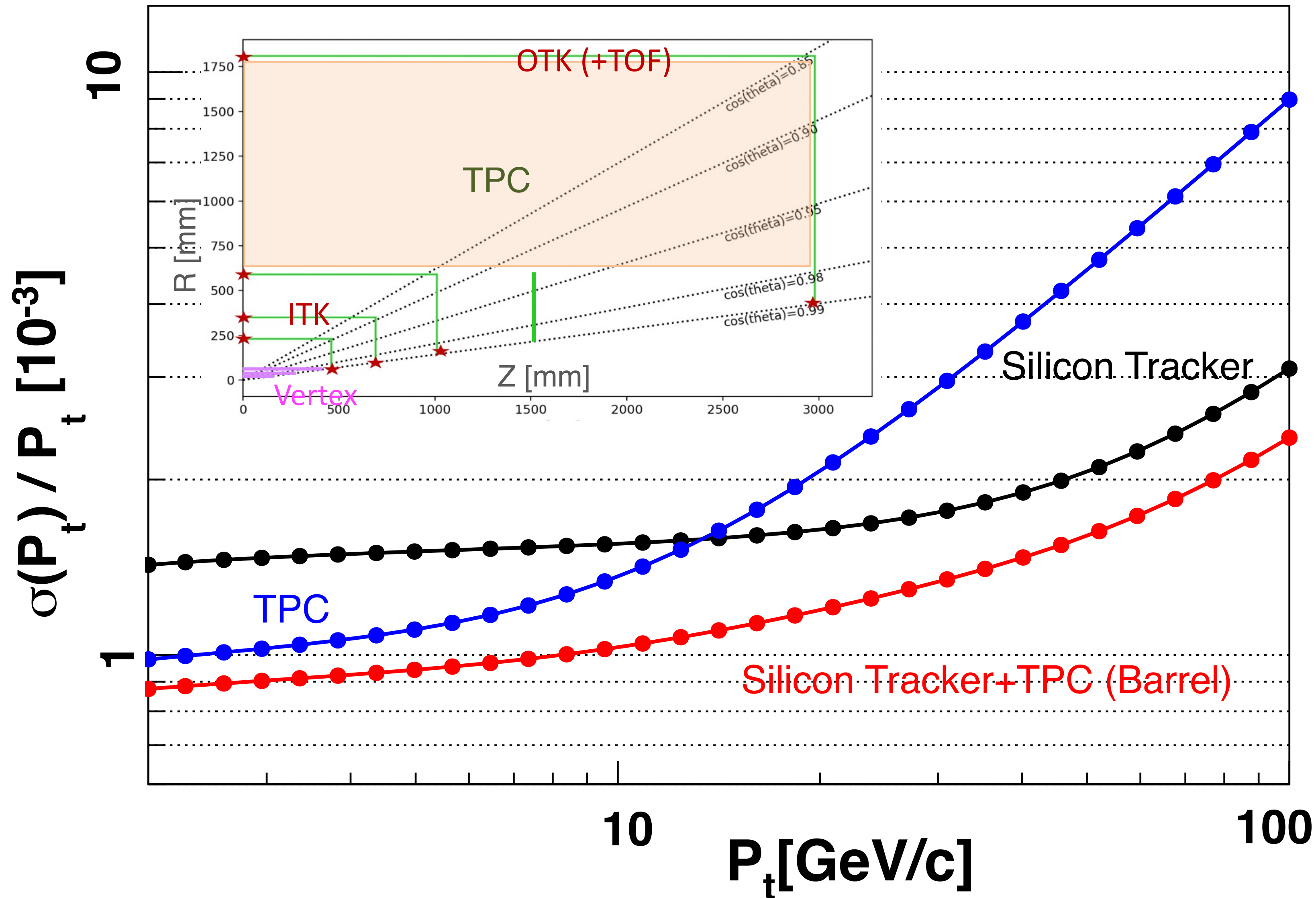


Thank you for your attention!



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

CEPC Tracker Performance from Simulation: Momentum Resolution

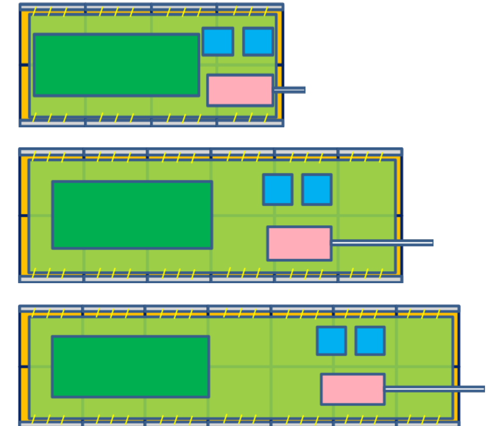


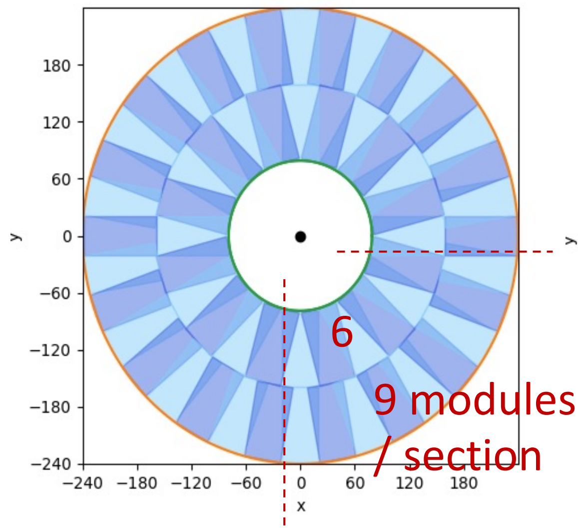
preliminary endcap design using pixels

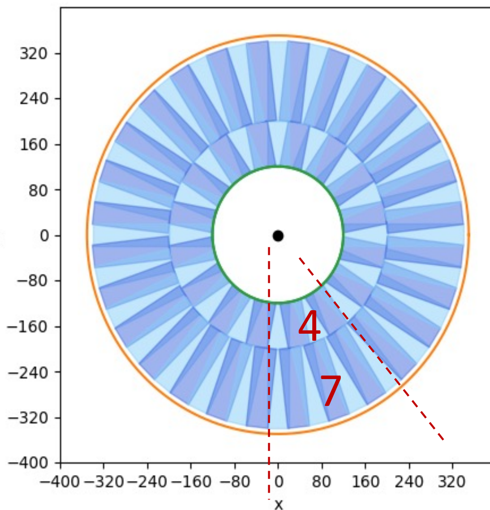
ring1 + ring2 (+ring3)	4+4	4+7	6+7+7	4+7+7
R-innermost [mm]	79	114.4	158	219
R-outermost [mm]	240	350	564	564
# modules in ring1	24	32	48	48
# modules in ring2	36	56	72	72
# modules in ring3			88	88

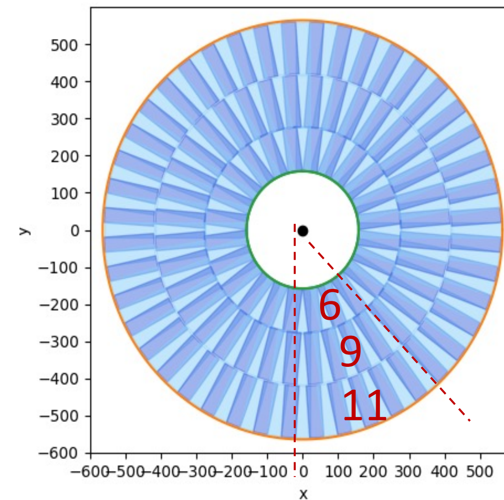
Module type	Count
"4" : 40.1 * 80.3 mm^2	92
"6" : 40.1 * 120.5 mm^2	48
"7": 40.1 * 140.6 mm^2	376

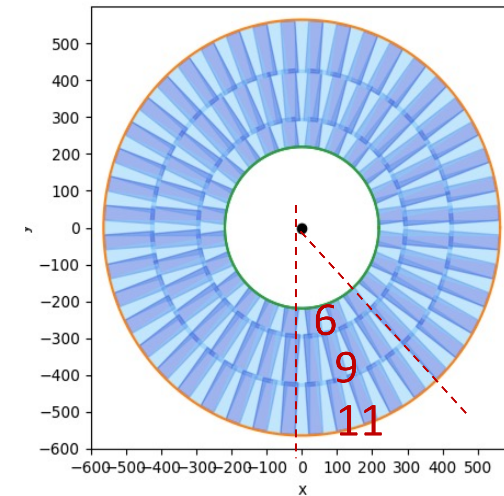
3 types of modules, one of which shared with the barrel;
516 modules, 6576 chips in total

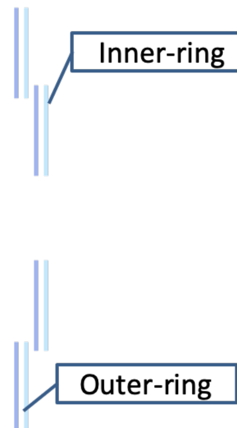








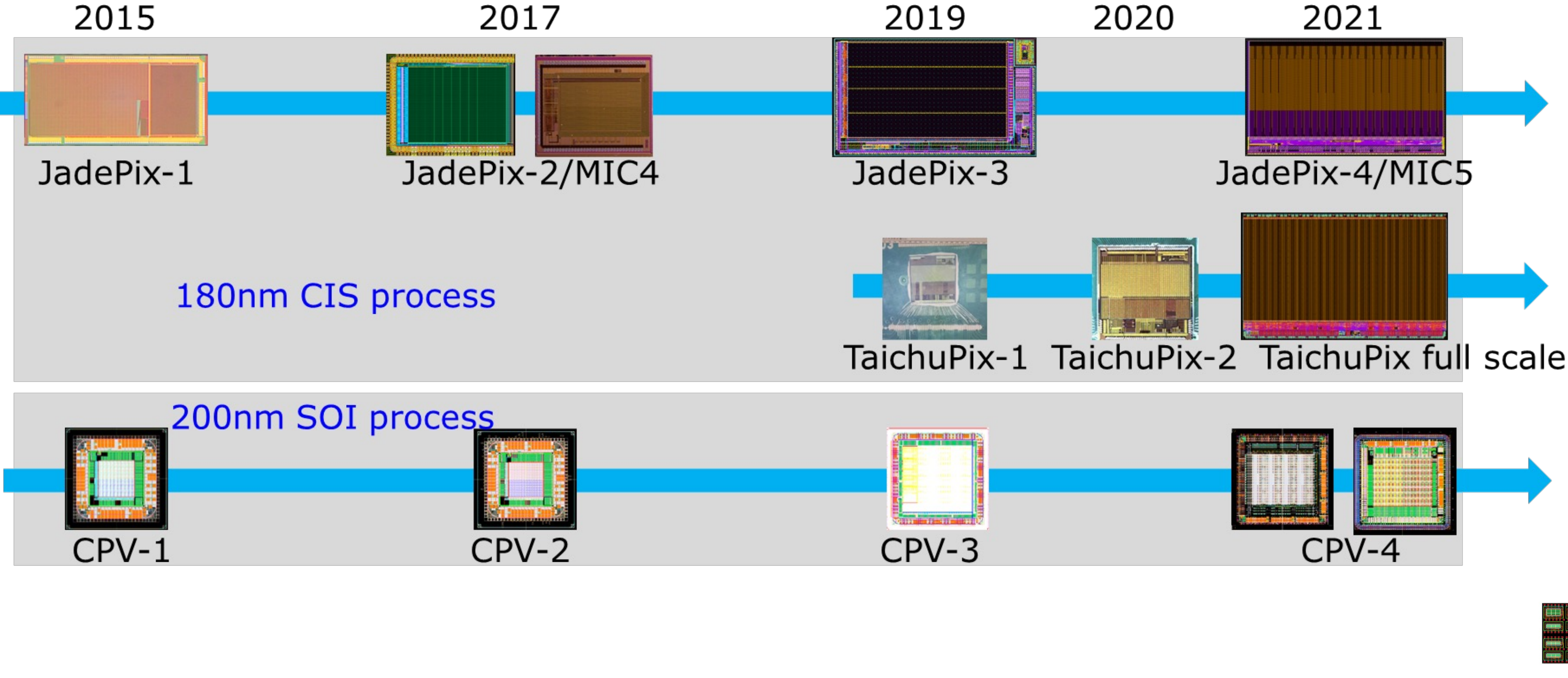




Front-side module   Back-side module

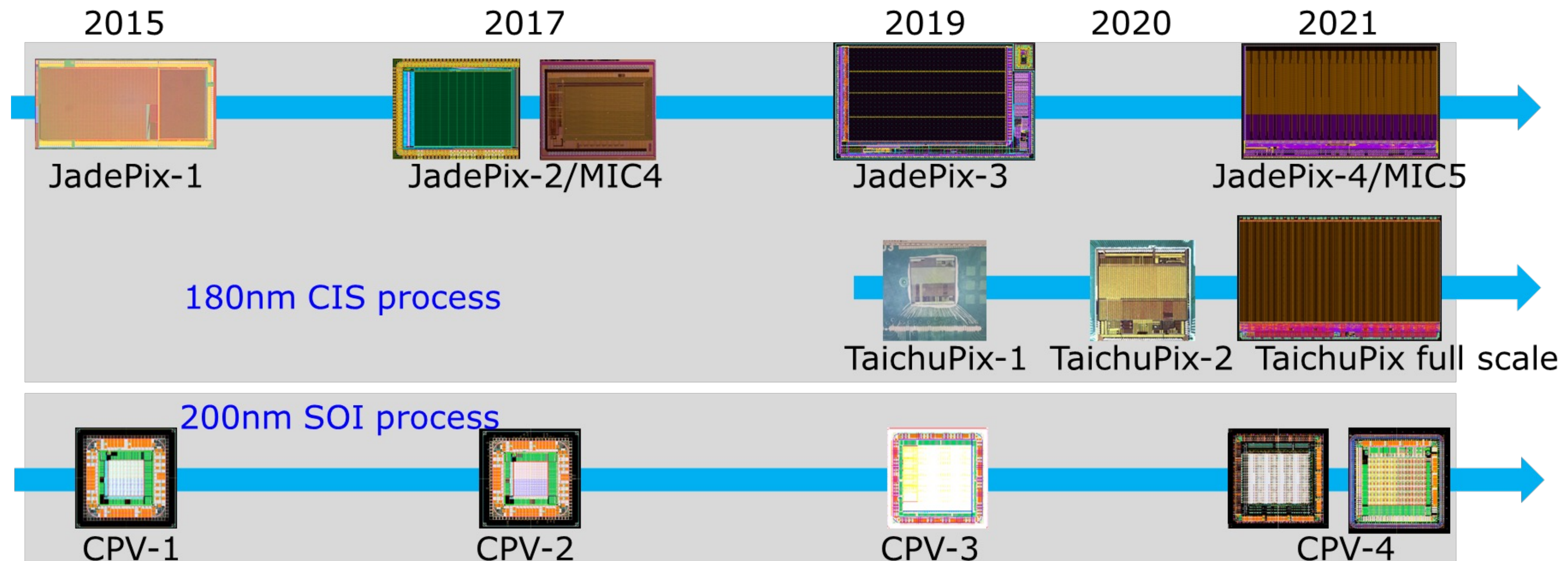
Division into 8 or 4 sections possible

CMOS Chip Development in China



Overview of pixel sensors in China for CEPC VTX

- **Development of pixel sensors for CEPC VTX supported by**
  - Ministry of Science and Technology of China (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



Ref: "Status report on MAPS in China", 2021 CEPC workshop, Yunpeng Lu