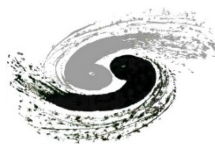
CEPC Electronics System

Wei Wei

On behalf of the CEPC Elec-TDAQ study team



中国科学院高能物理研究所

Institute of High Energy Physics

Chinese Academy of Sciences

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- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Global framework of the electronics system
- Detailed design for common electronics
- Research team and working plan
- Summary

Introduction

Chapter 11 General electronics

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11.2 Detector requirements
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- This talk is about the consideration of the general framework of the electronics system for the Ref-TDR of CEPC.
- This talk relates to the Ref-TDR Ch 11.
- Main contents will be introduced:
  - Main readout framework on Elec-TDAQ
  - General electronics blocks:
    - Data Link: aggregation, transmission & optical
    - FEE Powering
    - Common BEE board
  - Backup schemes
    - Wireless communication

Requirement from Sub Detectors (@Higgs)

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit	42bit	32bit	40~48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg： 2.9Mbps/chip Max： 3.85Mbps/chip	Avg： 38.8Mbps/chip Max： 452.7Mbps/chip	~70Mbps/ module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)	Needs detector finalization	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	Needs detector finalization	Needs detector finalization
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	Needs detector finalization
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization

Consideration on global framework of Elec-TDAQ

- Two main stream frameworks for the electronics-TDAQ can be simply categorized as FEE-triggerless readout & readout with conventional trigger
- Comparison on main aspects

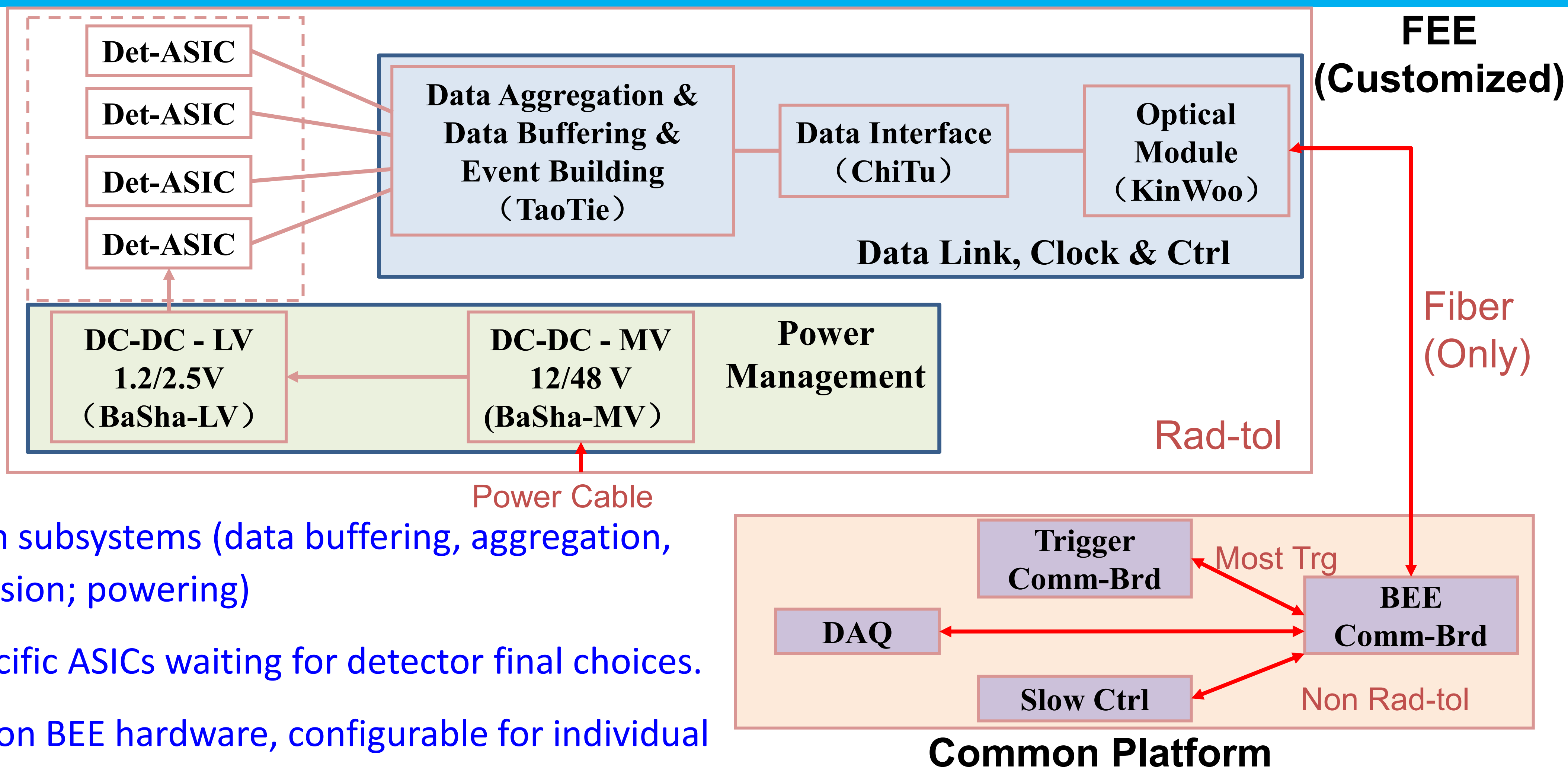
	FEE-Triggerless	Conventional Trigger	Superiority
Where to acquire trigger info	On BEE	On FEE	FEE-Triggerless
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	Conventional Trigger
Maturity	Mature but relatively new	Very mature	
Resources needed for calculation	High	Low	
Representative experiments	CMS, LHCb, …	ATLAS, BELLE2, BESIII, …	

Our choice on global framework

- We choose **FEE-triggerless readout (Backend Trigger) as our baseline global framework, while keep conventional trigger readout as the backup**, for the Elec-TDAQ system:

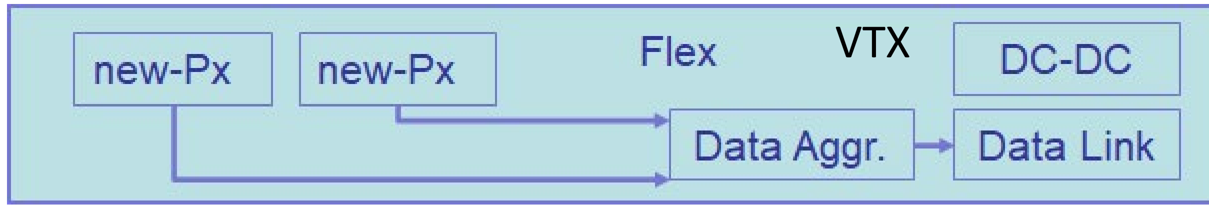
1. Keep the max possibility for new physics and future upgrade
   - readout all the information w/o pre-assumed trigger condition.
2. Speed-up the FEE-ASIC iteration & finalization process
   - w/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
3. Make it possible for a common platform design for all Sub-Det
   - Common BEE Brd, common Trg Brd, common data interface…
   - Scalable based on the detector volume
4. Sufficient headroom for FEE data transmission based on current MDI background rate
   - 10Gbps per link on FEE (max by ×4 links)

Global framework of the CEPC Elec system

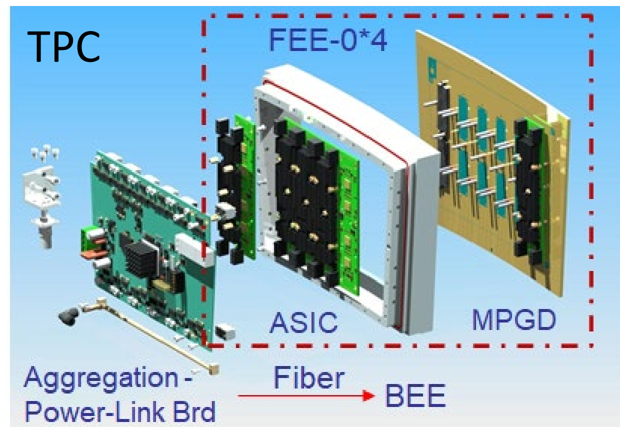


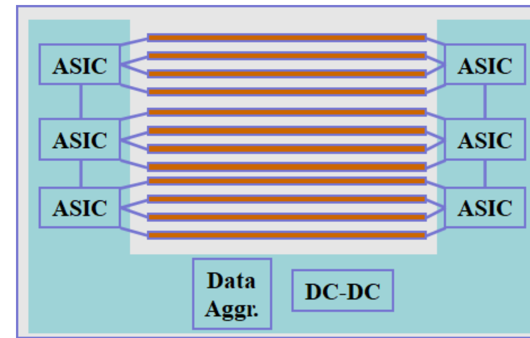
- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choices.
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

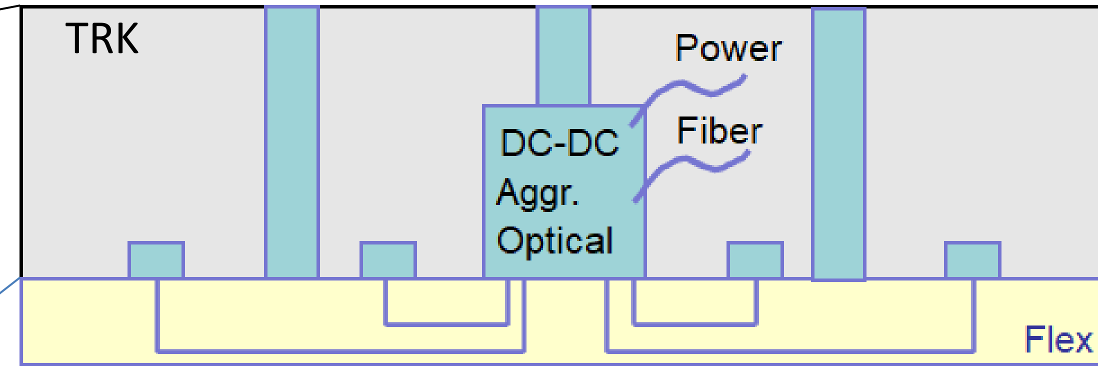
An overview of the Sub-Det readout Elec.

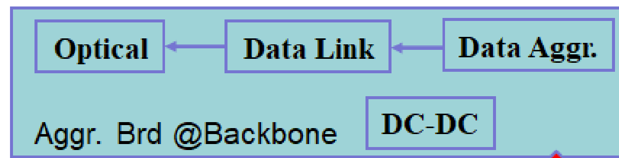


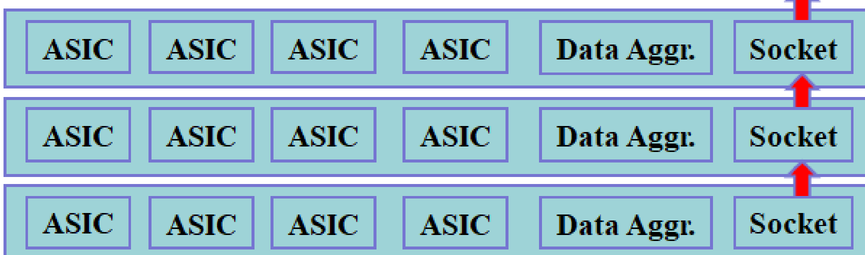
- All sub-det readout electronics were proposed based on this unified framework, maximizing possibility of common design usage.

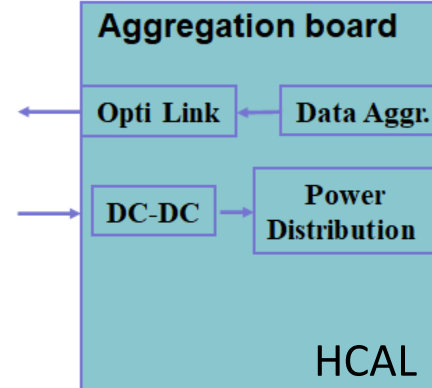


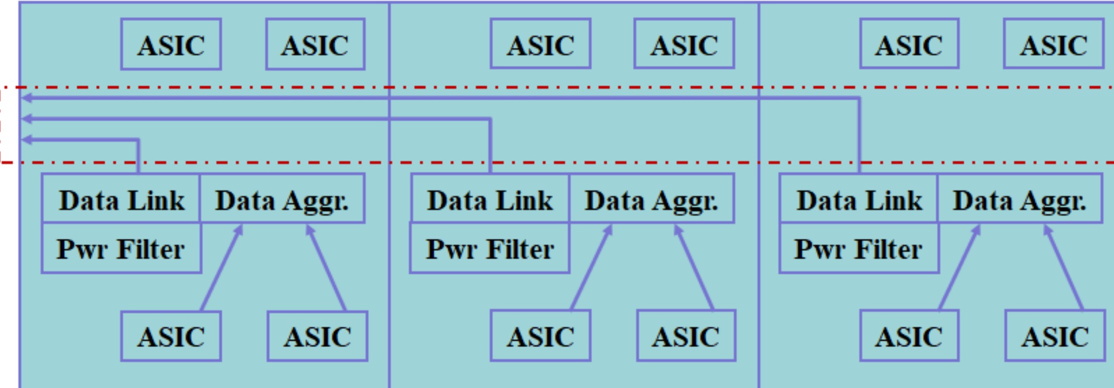




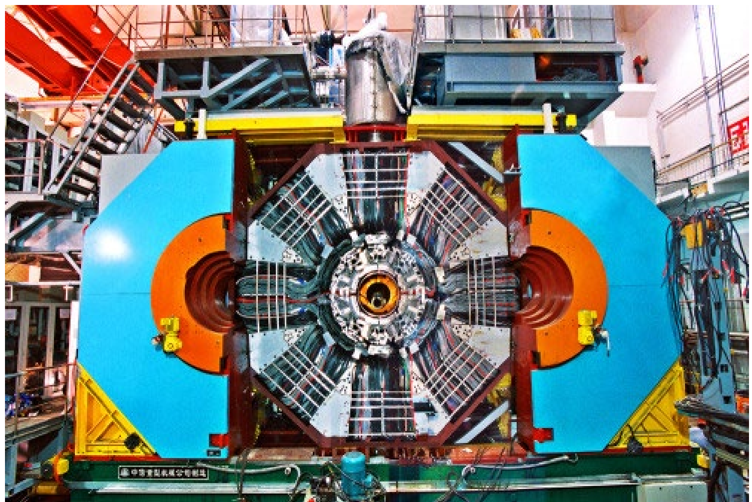




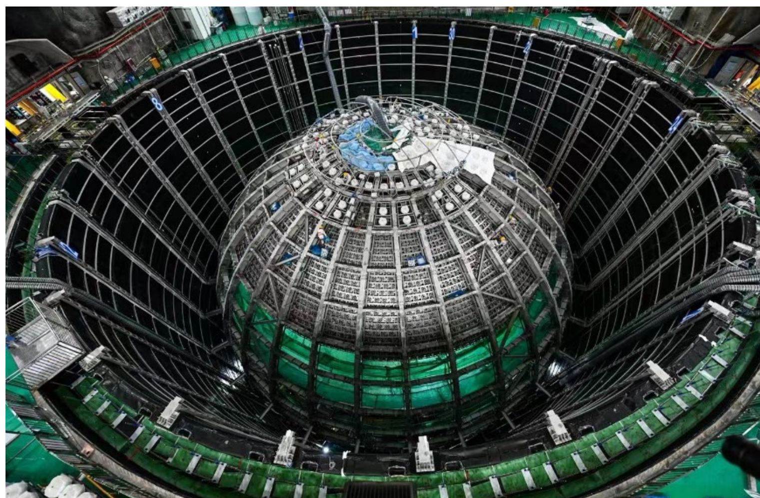




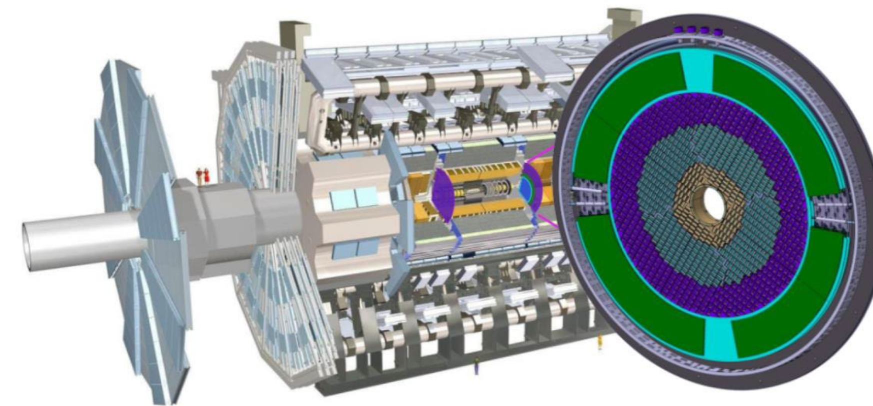
Previous experience on electronics system



BESIII

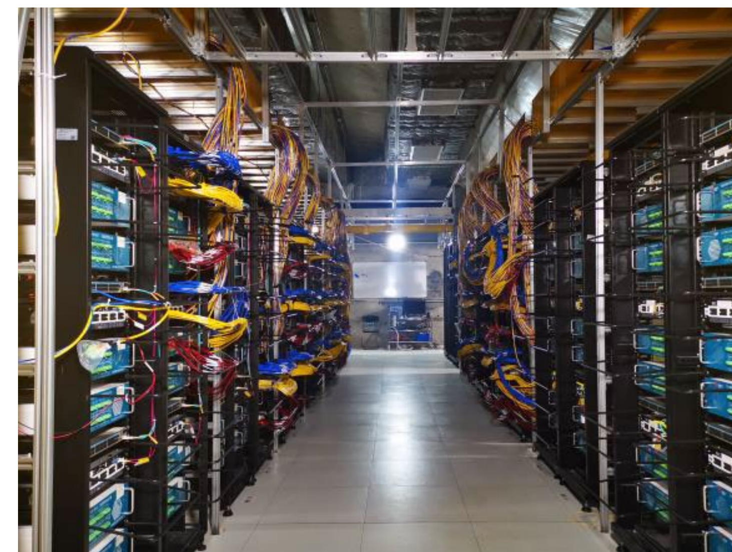


JUNO experiment



ATLAS HGTD

- Our team have developed the electronics systems of most of the major particle physics experiments in China, including BESIII, Dayabay, JUNO, LHAASO…
- Also in international collaborations as ATLAS HGTD…
- We have extensive experience in typical electronics system design from the FEE to BEE

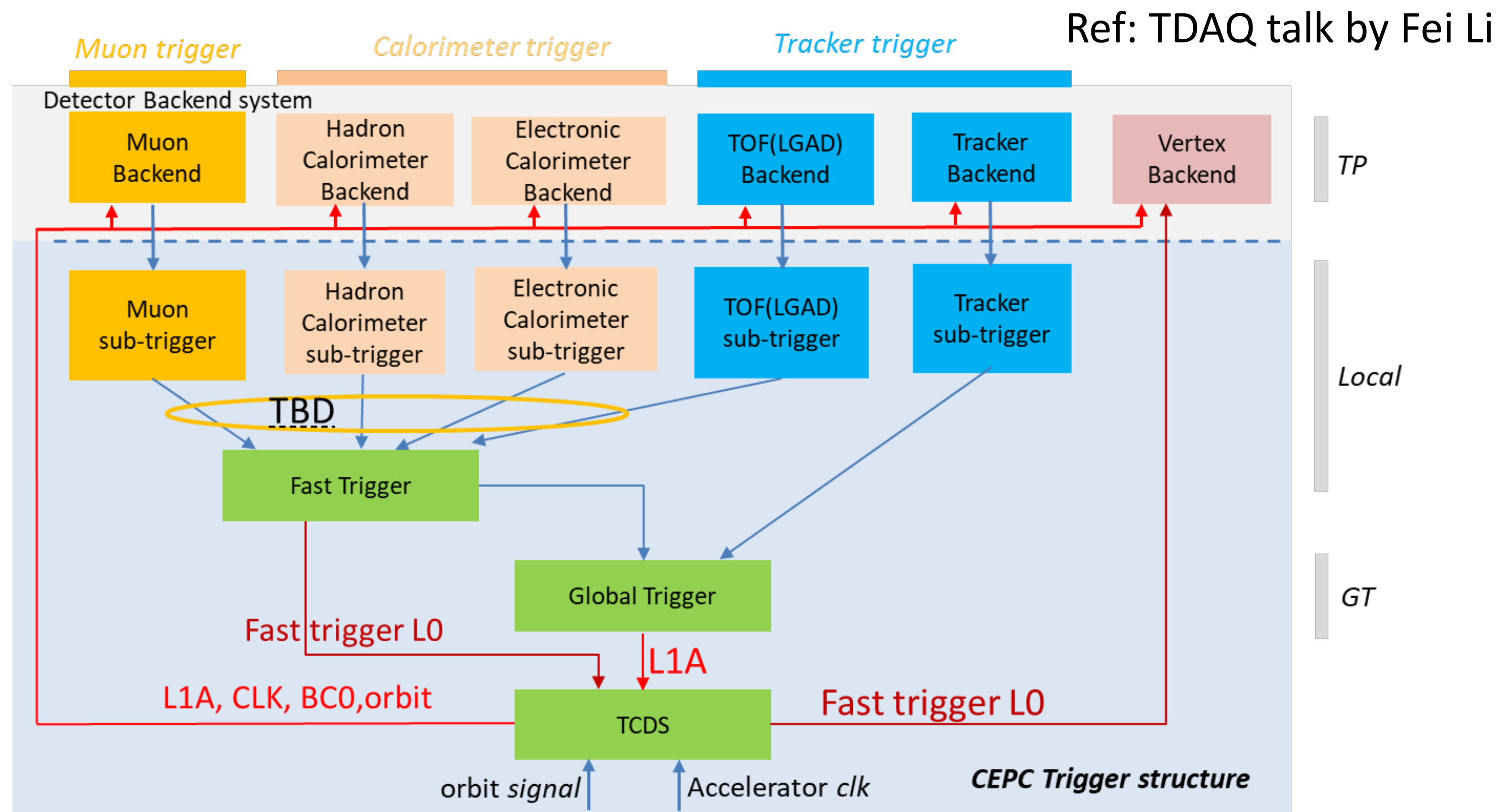


Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- In case of under-estimation or unexpected condition:

1. Additional optical links can be allocated to the hottest module.
2. In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.

Ref: TDAQ talk by Fei Li



The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

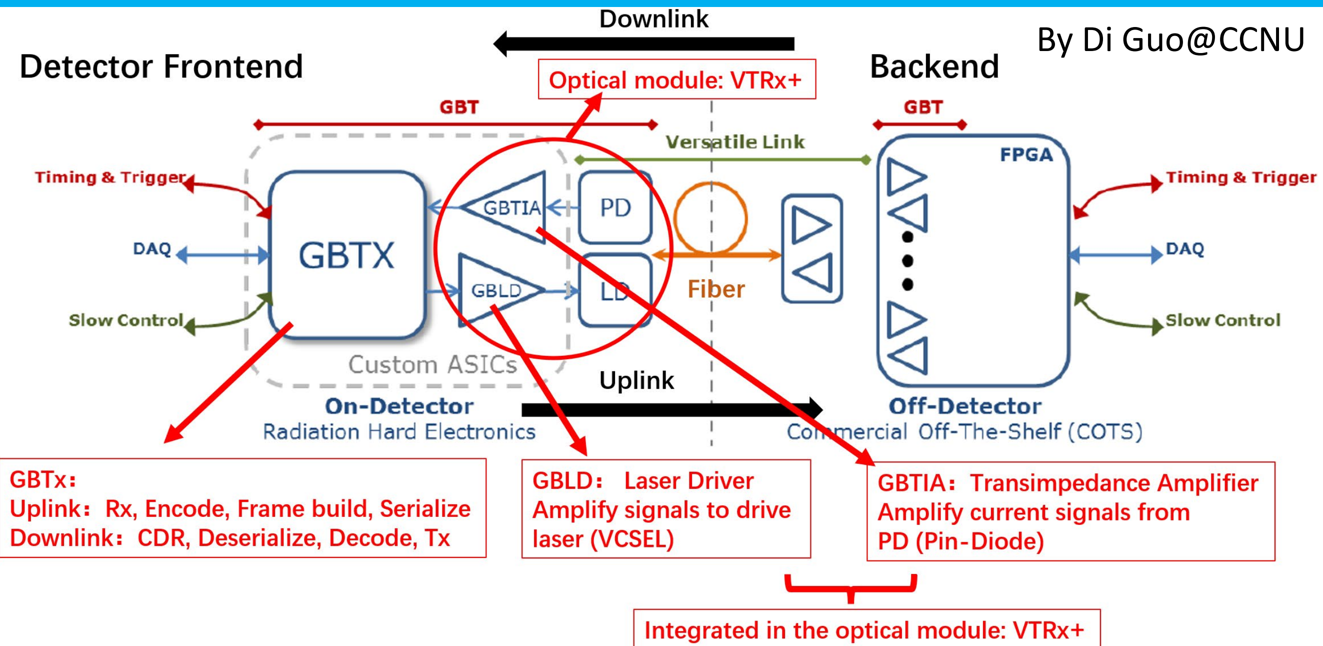
Common Electronics Components

- Common Data Link
- Common Powering
- Common Backend Electronics
- Backup Scheme based on Wireless Communication

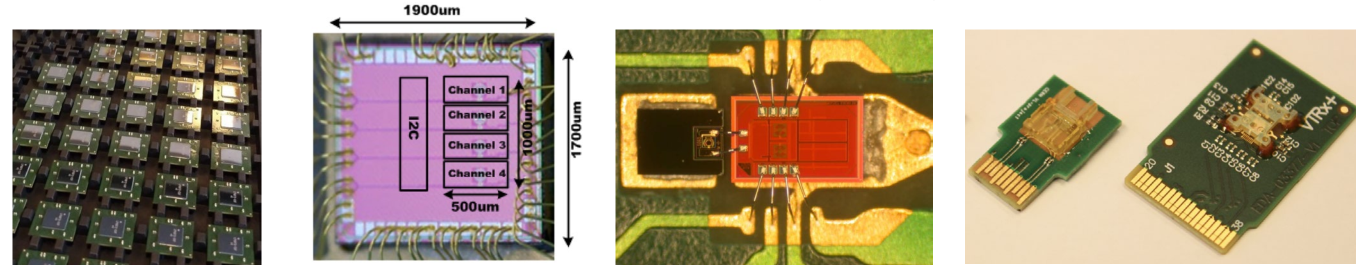
Technical Survey on Data Transmission System

- **GBT Project:**
  - The lpGBT & VTRx chip series, developed by CERN, are widely used by LHC experiments, as a common project
  - Core components:
    - GBTx: Bidirectional Serdes ASIC
    - GBLD: Laser driver
    - GBTIA: Transimpedance amplifier
    - Customized Optical Module
- **Our choice:**
  - Build a GBT-like universal bidirectional data transmission system
  - Take the lpGBT as a reference, the protocol can be a minimum & necessary set for the readout, clocking & control

By Di Guo@CCNU



GBT Architecture Developed by CERN



lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps

GBLD (LDQ10)
10.24 Gbps x 4ch

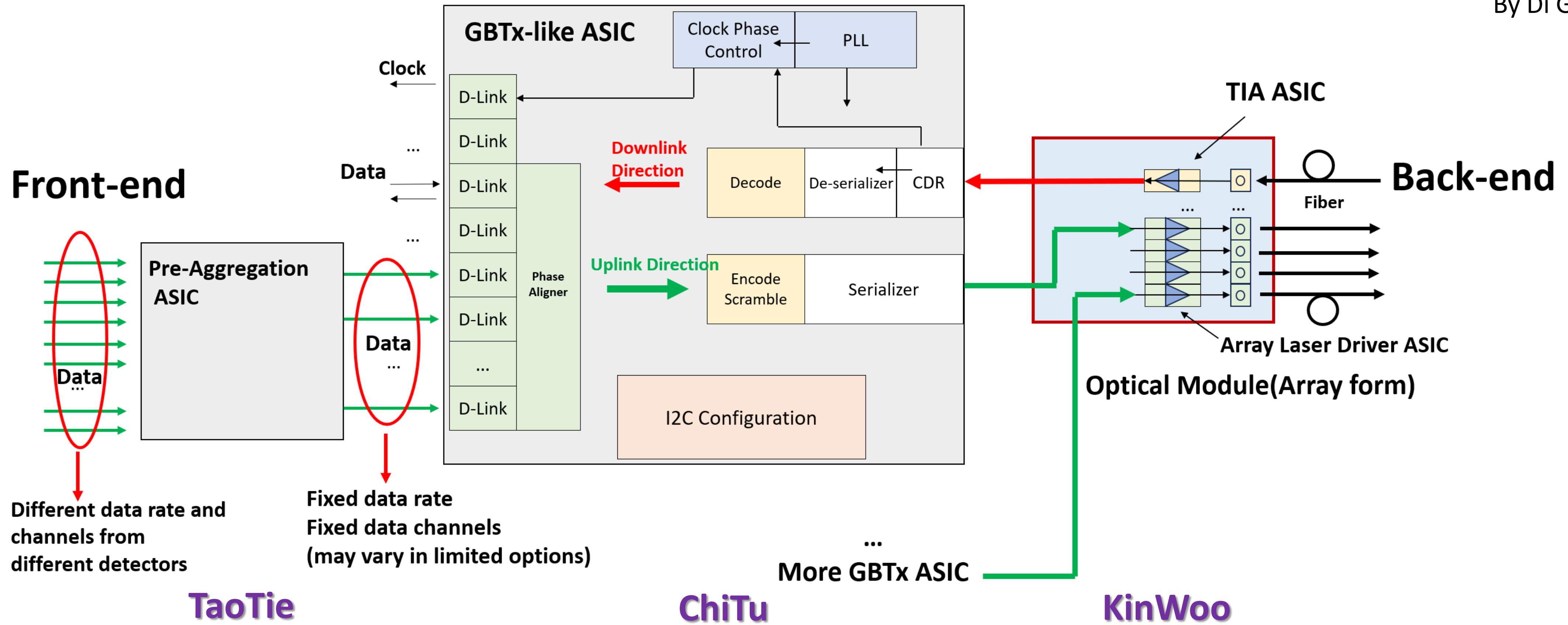
GBTIA
2.56 Gbps

VTRx+
4Tx + 1Rx
Array Optical Module

GBT Series ASICs and optical module

Detailed design on Data Transmission Structure

By Di Guo@CCNU

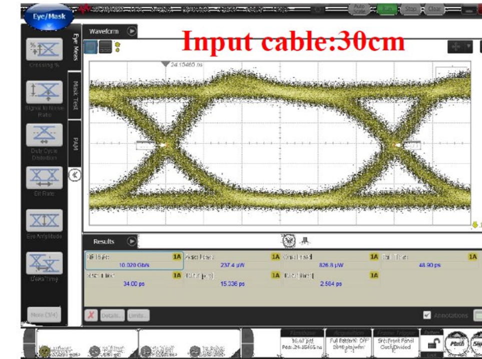


- Pre-Aggregation ASIC (TaoTie): Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like ASIC (ChiTu): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode ...
- Array Laser Driver ASIC + TIA ASIC + Customized Optical module (KinWoo)

R&D efforts and results on Data Link

- Self-developed GBT-like prototypes verified:
  - 5.12 GHz PLL + 10.24 Gbps Serializer verified√
  - 2.56 Gbps CDR + 2.56 Gbps Deserializer verified√
  - Phase aligner under test
- 10 Gbps Laser Driver Verified √
- Customized optical module prototype Done √
- The rad-tol fiber will be investigated together with the accelerator clocking system

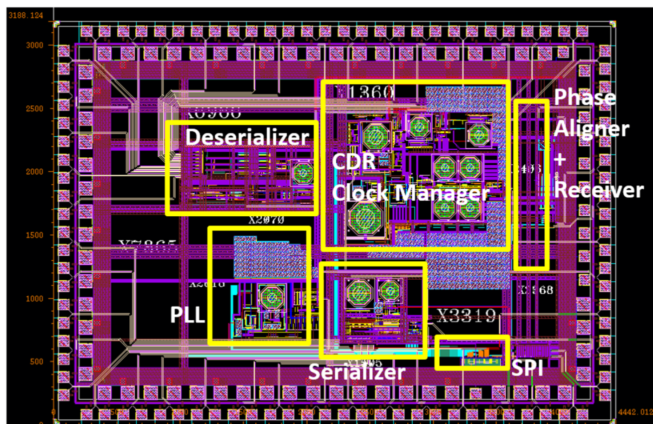
By Di Guo@CCNU



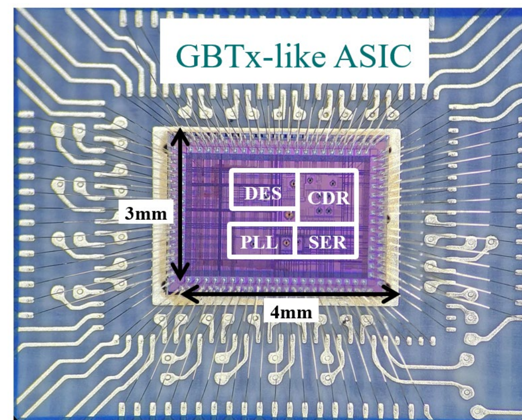
10 Gbps optical eye

Bit Rate	10Gbps	RMSJ	2.6ps
Rise Time	34.0ps	PPJ	15.3ps
Fall Time	48.9ps	Amp	589.4μW

10 Gbps optical eye diagram

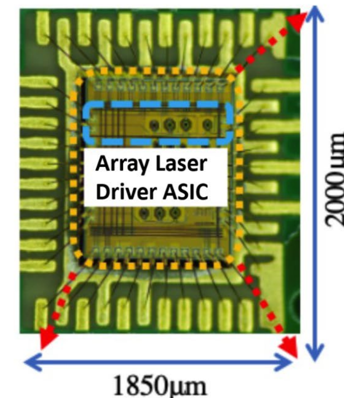


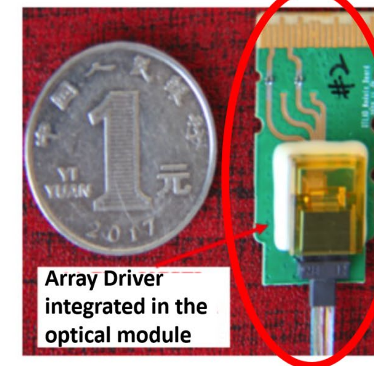
GBT-like ASIC prototype layout

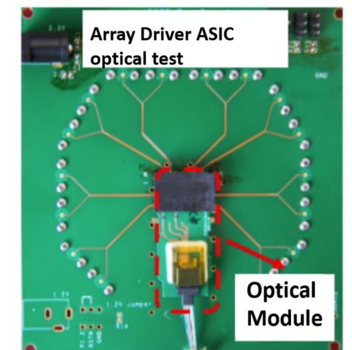


GBT-like ASIC wire-bonding picture

Customized Optical module

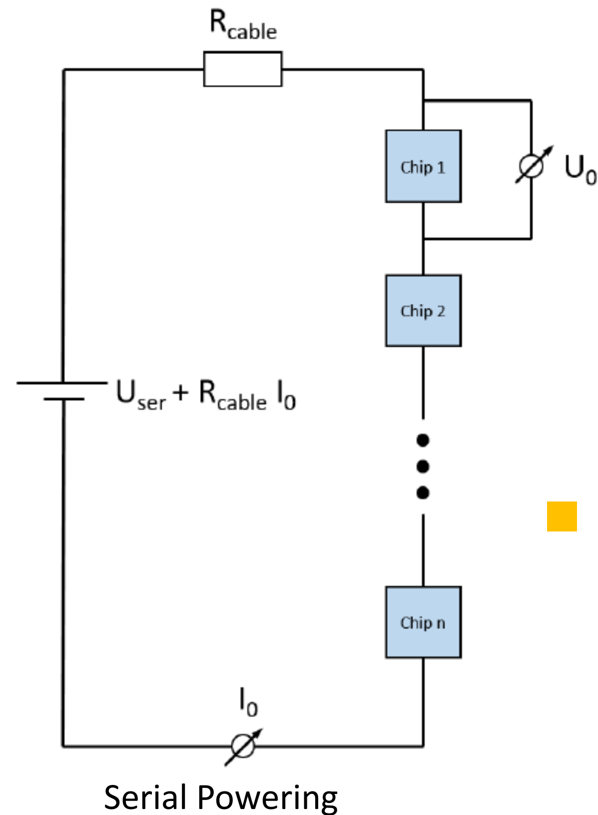




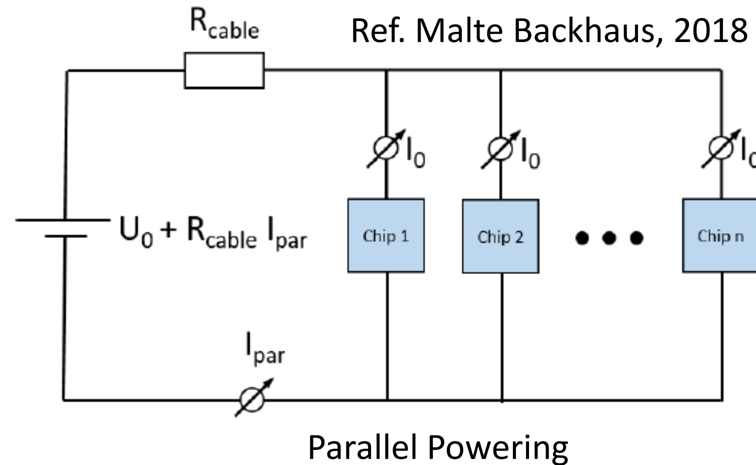


4 x 10 Gbps/ch VCSEL Array Driver with customized optical module

Technology survey and our choice on Powering



Serial Powering

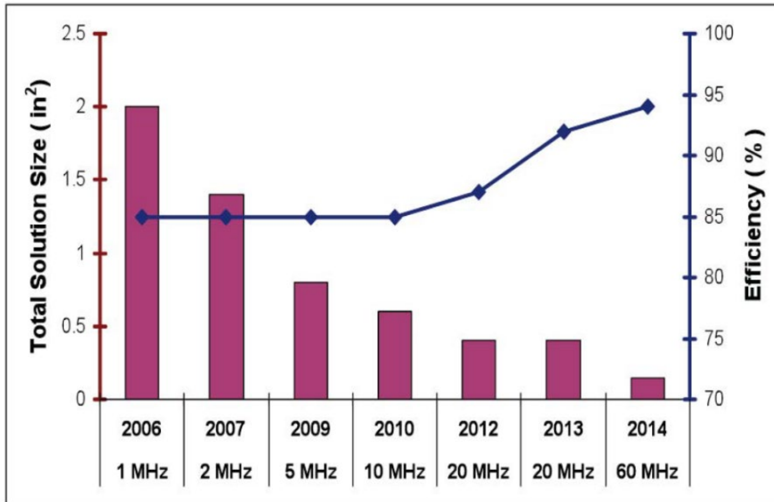


Parallel Powering

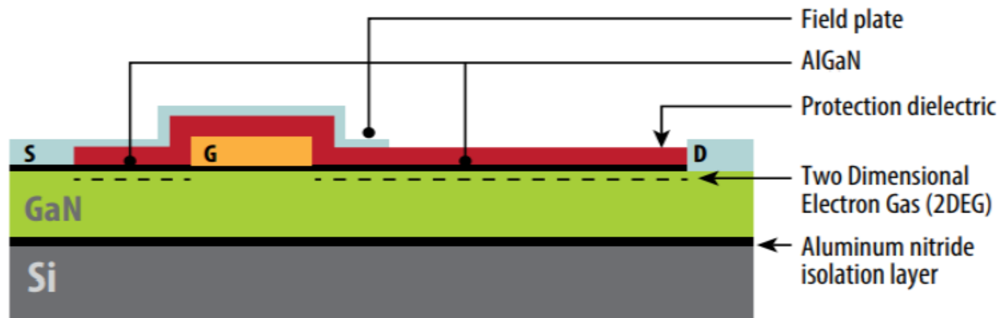
	Serial Pwr	Parallel Pwr
Material	Much less	
Cabling	Much less	
Installation	Much easier	
Maturity	New	Very mature
System Reliability	Potential issue	Very robust

- On powering distribution
  - Serial Powering is superior on many aspects (material, cabling and installation…) than Parallel Powering, especially on VTX & TRK
  - It is also a hot area with lot of focused R&D
  - However, due to the common substrate at negative voltage for the stitching sensor in VTX, serial powering is not feasible
- Our choice
  - As a general platform, we chose (conventional) Parallel Powering as the baseline scheme, while keep pace on R&D of Serial Powering as the backup scheme

Technology survey and our choice on Powering

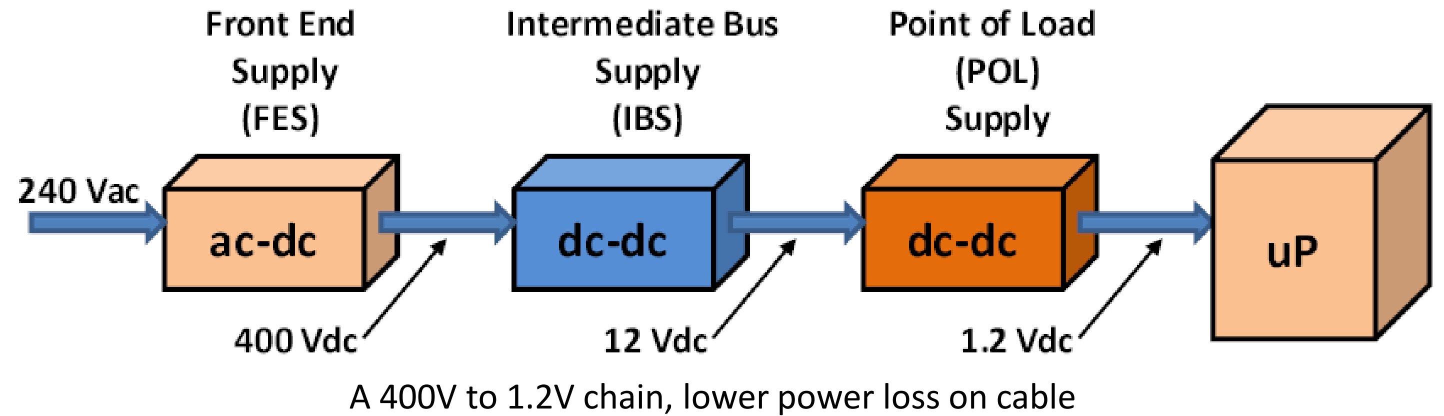


Higher switching Freq, smaller size, higher efficiency, lower on-resistance



Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency



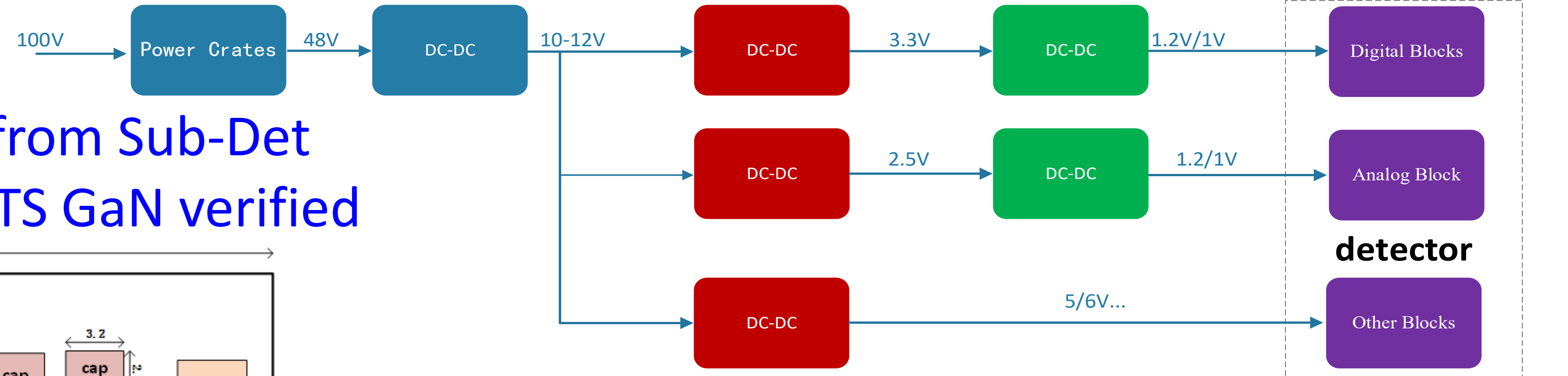
A 400V to 1.2V chain, lower power loss on cable

- Investigation was also conducted to compare the key component schemes of the power module, esp on LDO & DC-DC convertor.
- The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.
- We choose a GaN-based DC-DC as the baseline power module scheme. This also enables high voltage power distribution, for low cable material and low power loss.

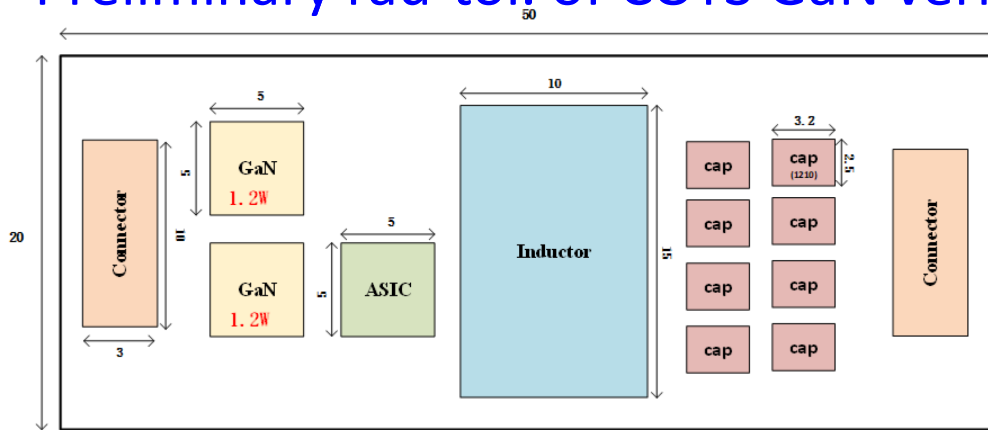
R&D efforts preliminary design on powering

- Structure of power distribution systems

By Jia Wang@NPU

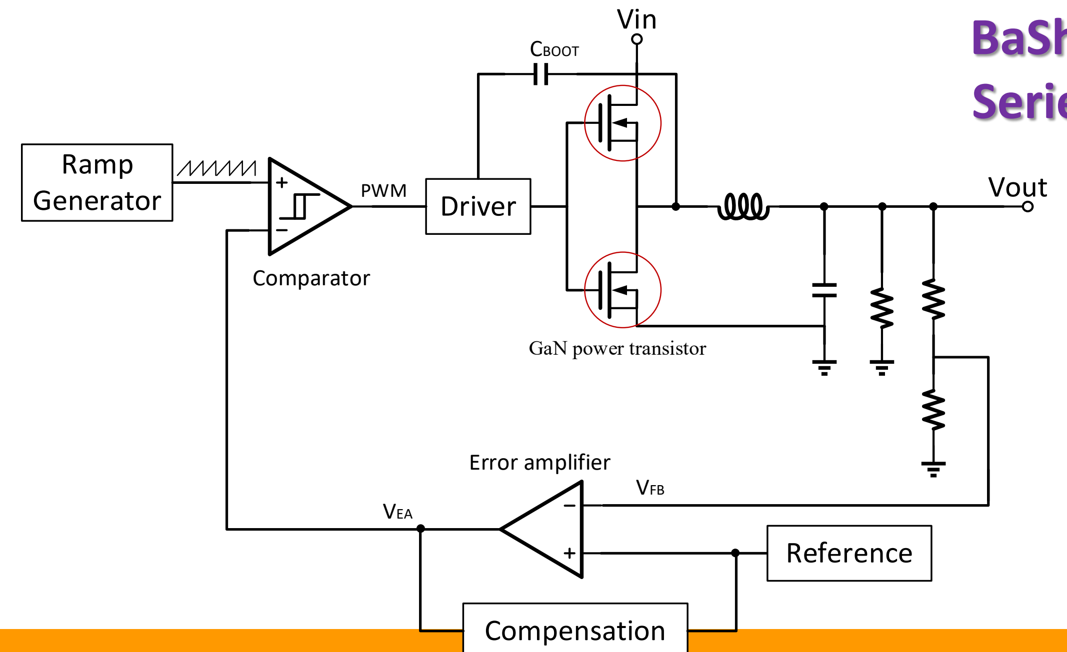


- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified



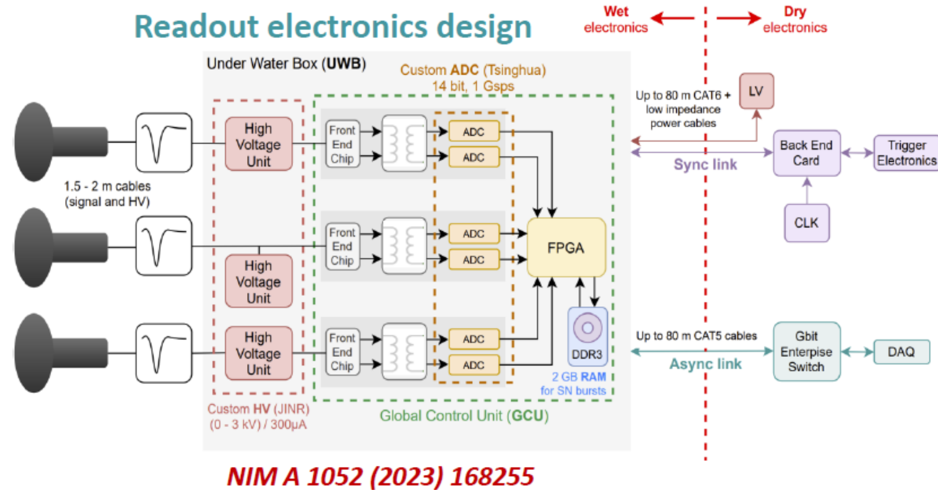
	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、2.5V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

- Proposed design of BUCK DC-DC converter



Related R&D and experience on BEE

By Jun Hu@IHEP



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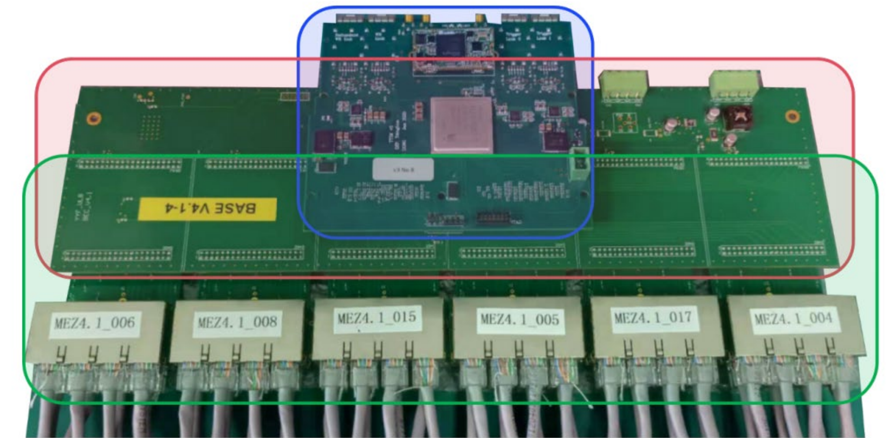
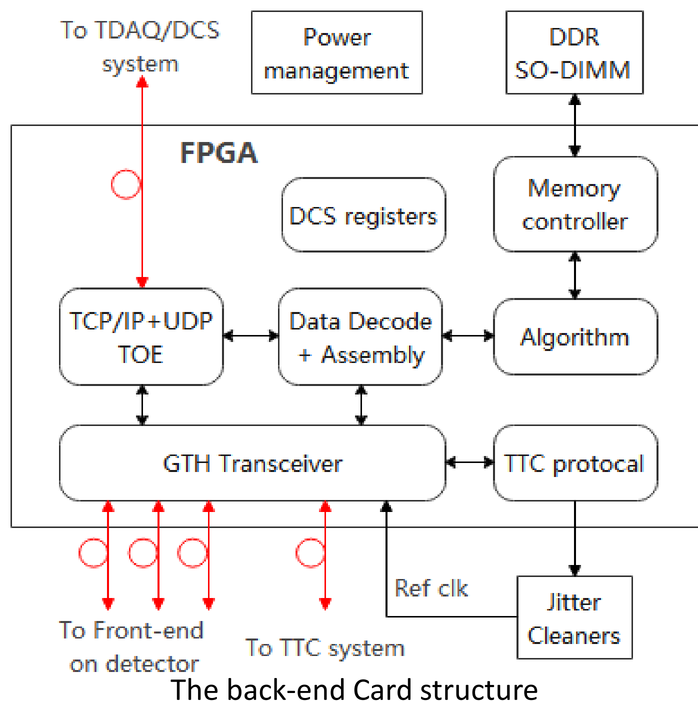


The back-end box for the JUNO experiment

- located between trigger system and front-end electronics,
- Collects the incoming trigger request for trigger system,
- Fanout the synchronized clock and the trigger decisions to front-end electronics.

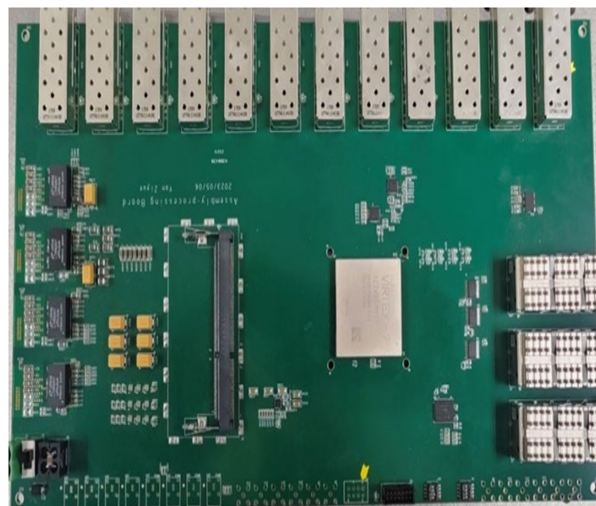
- Red box: The base board provides the power supply,
- Blue box: Trigger and Time Interface Mezzanine (TTIM) with WR node,
- Green box: The extenders interface with ethernet cables coming from underwater front-end boxes.

Detailed design on common BEE



The back-end Card structure

By Jun Hu@IHEP



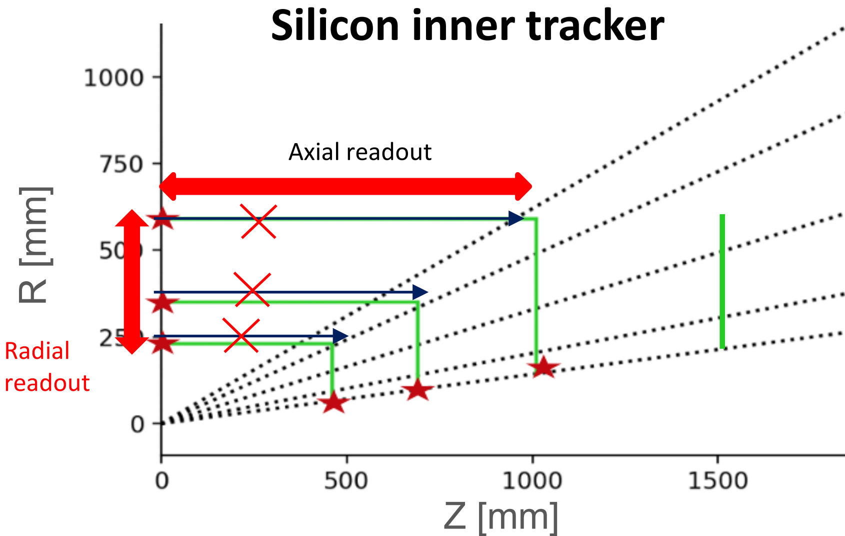
Data aggregation and processing board Prototype for Vertex detector

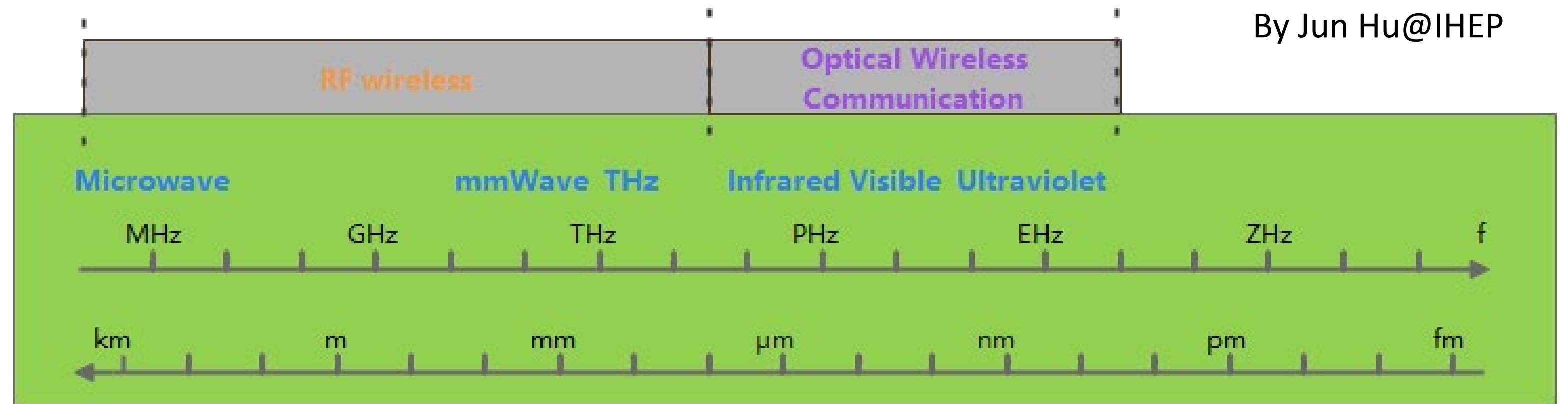
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- A cost-driven device selection: FPGA XC7VX690T
- Interface： SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Backup scheme based on wireless communication





By Jun Hu@IHEP

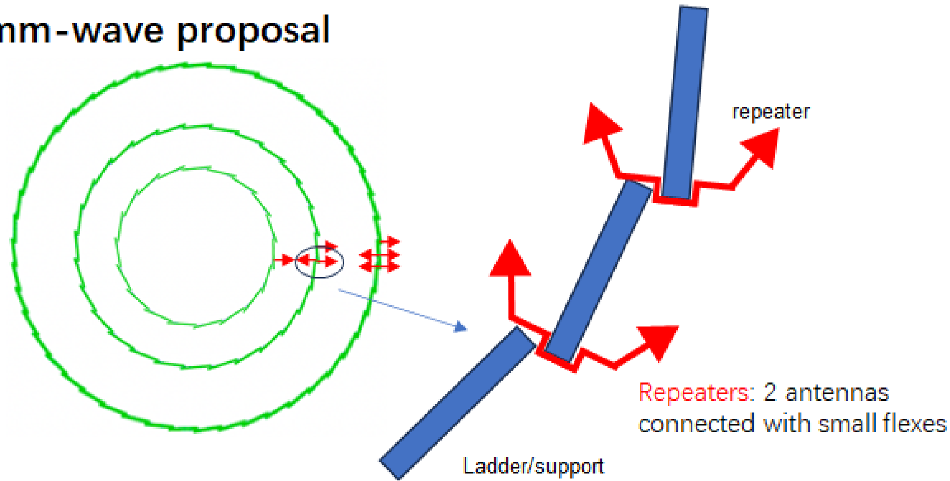
- Radial readout with mm-wave
  - 12- 24 cm transmission distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

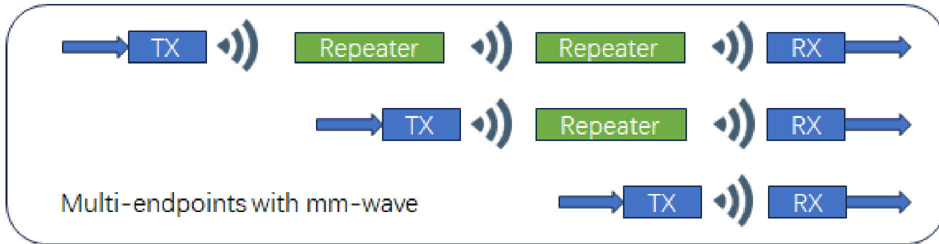
- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz， 45GHz， 60GHz， 77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

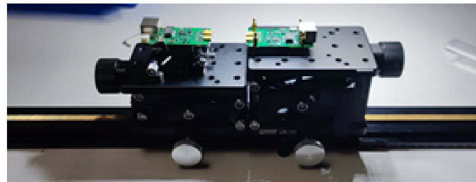
- Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme
- Three major solutions were investigated through R&D, two were selected with corresponding schemes

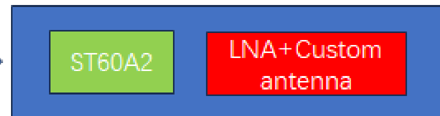
R&D efforts and results on WLess Comm

mm-wave proposal







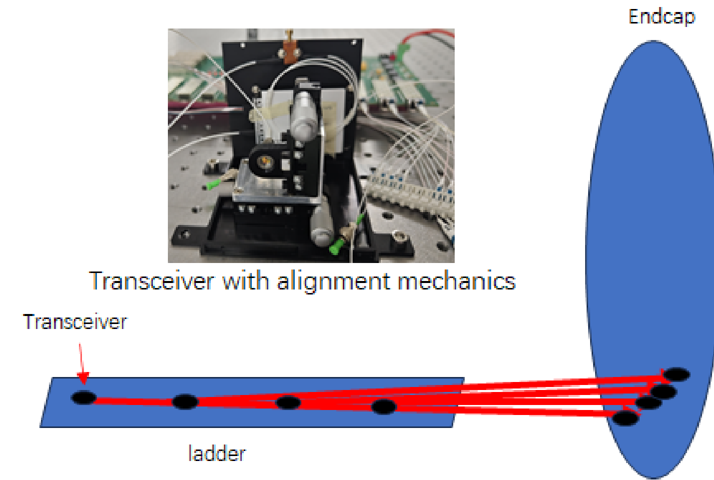


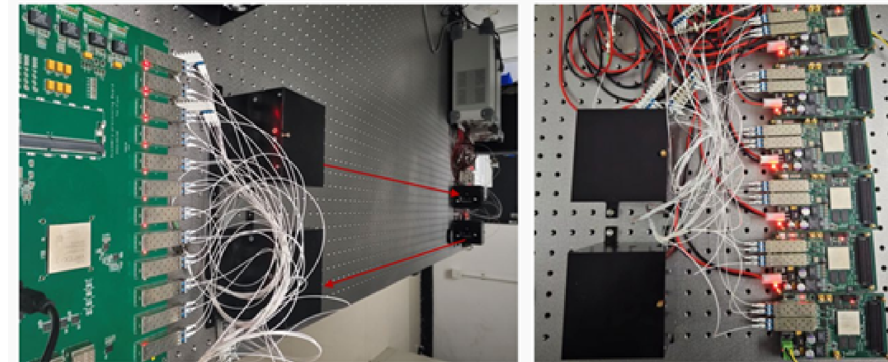
Test with evaluation boards – SK202
- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

Optical wireless proposal

By Jun Hu@IHEP

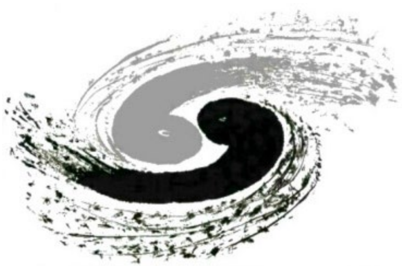




DWDM transceivers +AWG + lens
- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

Research Team

- A wide collaboration was built involving most of the affiliations in the HEP field in China (~50 people involved in different areas).
- We are working to expand the collaboration, including attracting international colleagues. We are also trying to join in the DRD7.

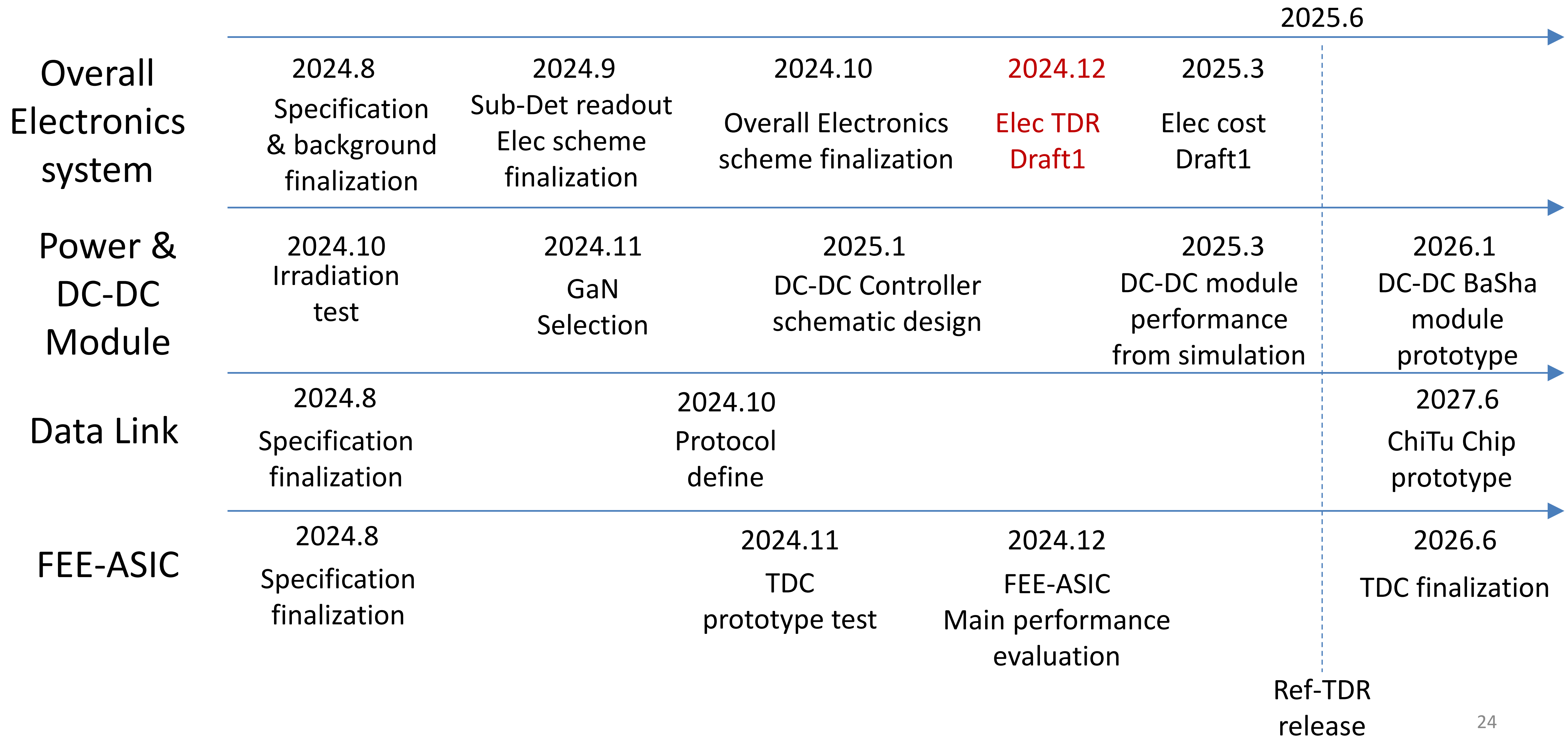


- Overall electronics and BEE: IHEP(5)
- Sub-detector readout electronics: IHEP(11), Tsinghua(5), CCNU(3), NPU(7), SDU(4), NJU(3)
- Data link: CCNU(3), IHEP(3), USTC(2)
- Powering: NPU(3), IHEP(2), USTC(2)

Working plan on key R&Ds

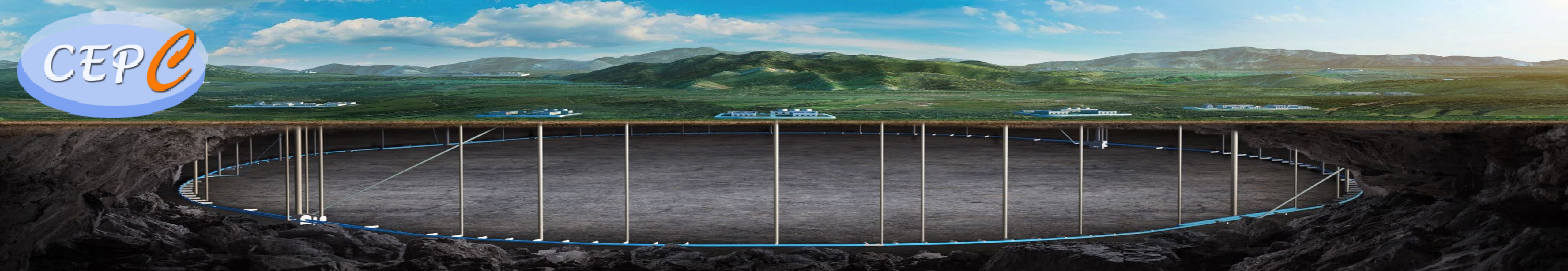
- Key R&D left to do towards & beyond the Ref-TDR
  - An lpGBT-like chip series (TaoTie + ChiTu + KinWoo) should be developed as the common data link platform
    - Transmission protocol, including up(typically 8b10b) and down(typically I2C & fast commander), is a key component according the current tech stage
  - GaN based DC-DC module (BaSha Series) is also critical for FEE modules in high radiation environment
    - Further radiation tests should be performed, including TID, SEE, and NIEL
  - A prototype based on wireless communication scheme will be demonstrated to show the feasibility
    - Customized antennas, adapters, and repeaters are being coordinated with the industrial sector in China for a more compact design

Working plan on schedule for the Ref-TDR

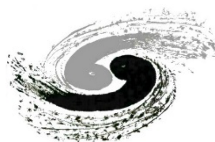


Summary

- A global framework for the CEPC electronics system based on FEE-Triggerless readout (Backend Trigger) was chosen to be baseline, while readout schemes for each sub-detector were defined accordingly.
- Previous R&D has shown promising technical feasibility for key components, including data links, common BEEs, and powering. No show stopper is found for the electronics framework & the Sub-Det readout.
  - Future R&D is scheduled to demonstrate prototypes of each key technology soon
- Backup schemes based on conventional triggers and innovative schemes based on wireless communication were also considered for more conservative and aggressive approaches, respectively.



Thank you for your attention!



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Naming of the common ASICs

ChiTu & Guan Yu

KinWoo in the sun

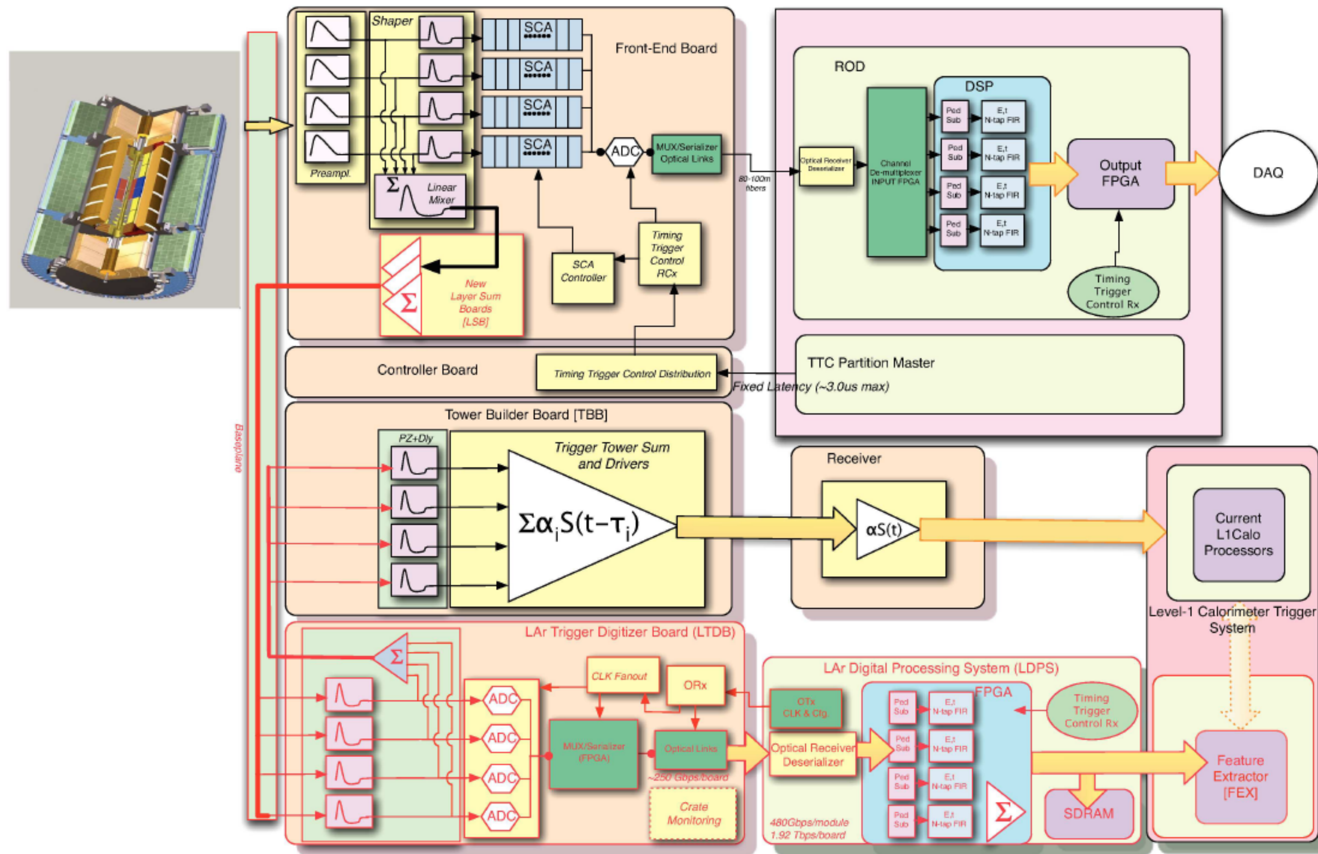
TaoTie

BaSha carrying a monument

- GBTx-like: ChiTu (赤兔）， the most famous horse in Chinese tales, ridden by the Chinese God of War Guan Yu. It is in charge of transportation with ultra fast speed, just as GBTx-like chip is doing.
- VTRx: KinWoo (金乌）， the bird who lives in the sun in Chinese tales, an avatar of the sun and in charge of the light, just as the VTRx chip does, to convert electronic signal to/from optical.
- Data aggregation: TaoTie (饕餮）， a mythical animal in Chinese tales, who can swallow anything, just as the chip does, to collect all the input data streams.
- DC-DC module: BaSha (霸下）， one of the nine sons of the Chinese Loong, who is famous for its strongness and always to bear a monument. Just like the powering system which is the basement and support of all electronics.

Technology survey on global framework

ATL-CAL-PROC-2017-001

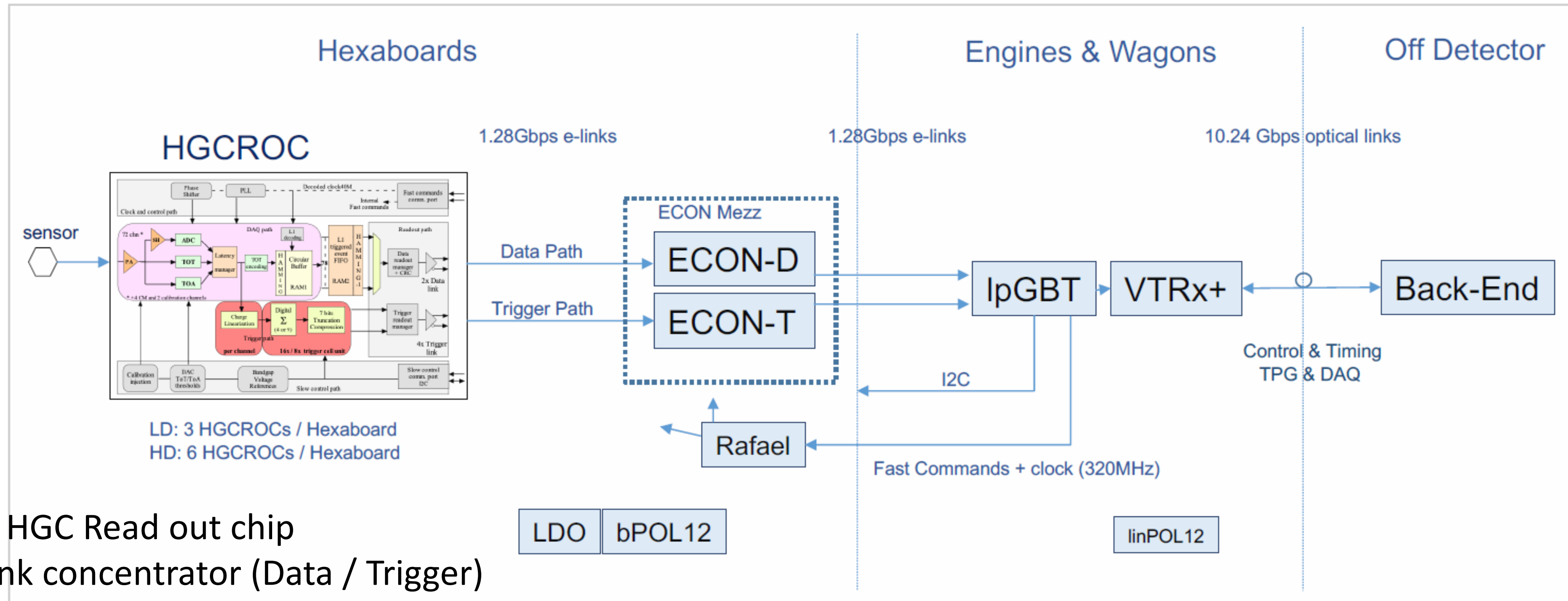


Upgraded LAr readout schemes for Phase-I

- A typical readout framework can be referred to ATLAS detector system(e.g. LAr CAL)
- It can be noted the FEE not only has to generate and send out trigger info.(e.g. SUM), but also store data for trigger latency and accept the trigger decision.

Technology survey on global framework

From Paul Aspell, CMS HGCAL An Electronics Perspective



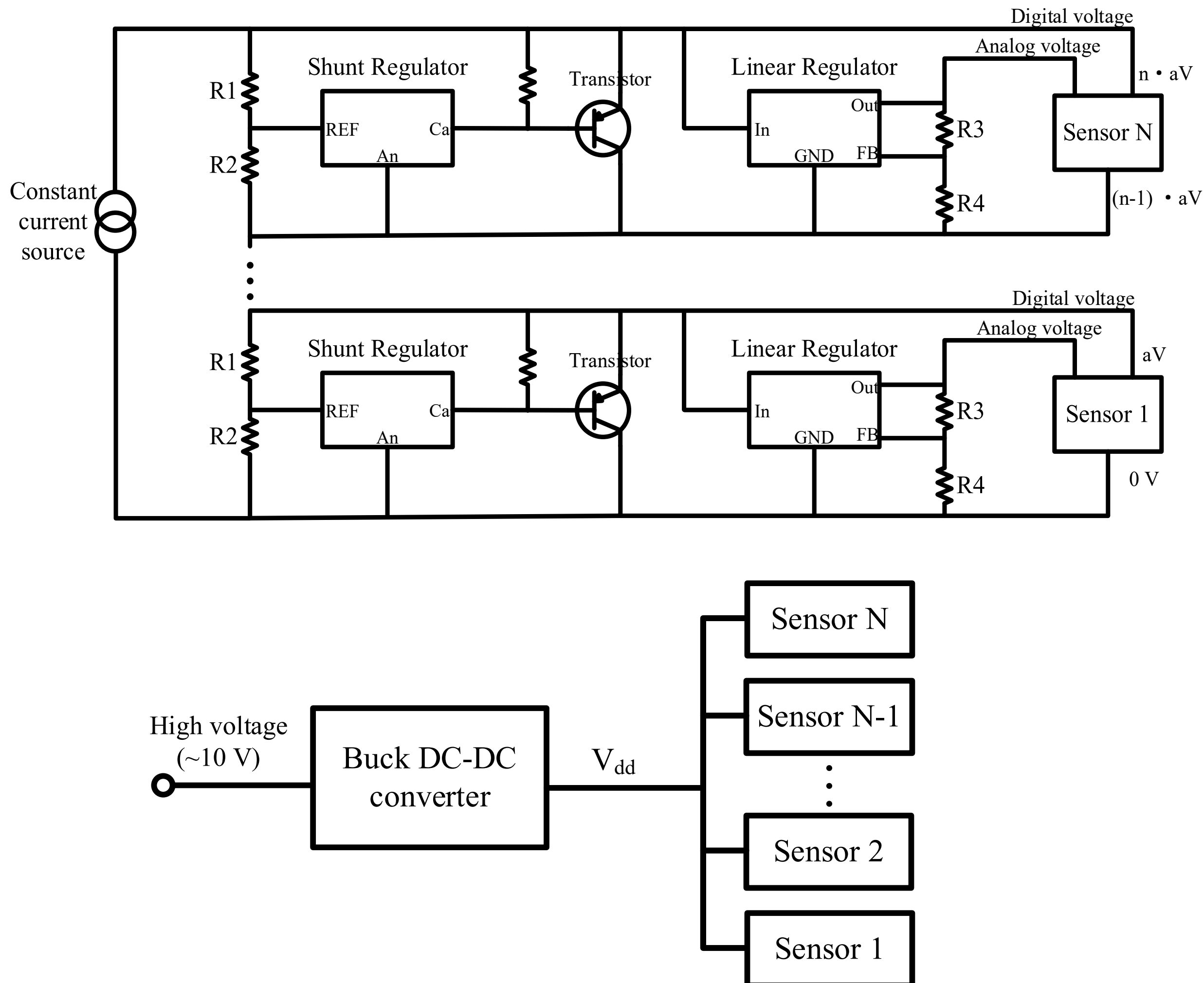
HGCROC: HGC Read out chip

ECON: elink concentrator (Data / Trigger)

- The electronics readout framework can also be inspired by CMS detector system(e.g. HGCAL).
- It can be observed that the data stream is mostly in a single direction to the BEE, and the electronics system architecture is relatively compact.

Technology survey and our choices on Powering

Serial powering VS Parallel powering with DC-DC converter



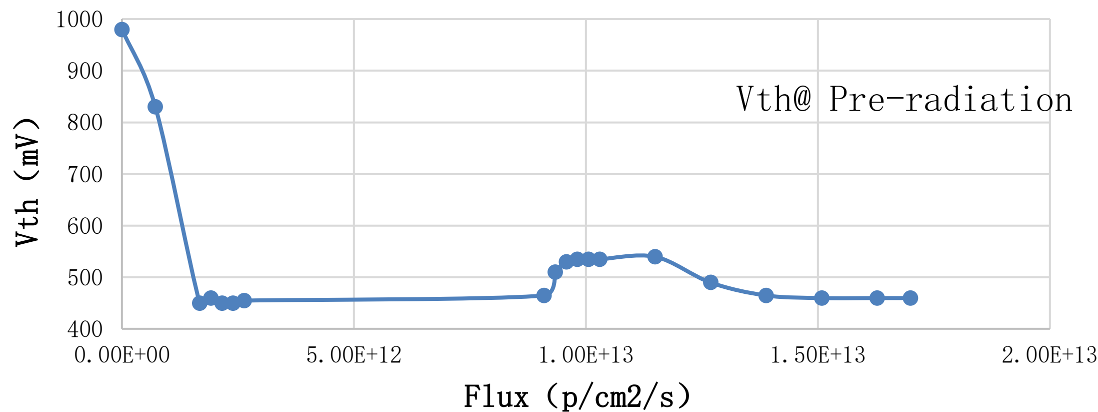
Performance comparasion of the two power distribution system

	Serial powering	Parallel powering (DC-DC converter)
Power efficiency	60-80%	60-80%
Power cable number	Reduction by factor 2n	Reduction by factor 2n
System ground potential	Different for every module	One ground level
Noise	Noiseless, even better	More noise due to the switching.
Compatibility with the old power system	Many changes are needed due to the virtual ground.	A few changes
Reliability	Not good. Bypass circuits are required for the faulty modules.	Good

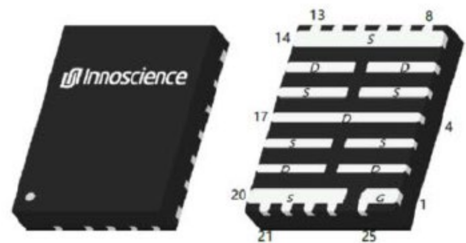
Requirement of the powering system

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 336mW/chip	20mW/chn 2.56W/chip		280μW/chn 35mW/chip	15mW/chn 240mW/chip				
Max chips@module	29	14	22	22	3	1115	64	Needs detector finalization	8~30	92~365	Needs detector finalization
Power@module (W)	5.8	11.2	7.39	56.3	58.9	39.7	30	Needs detector finalization	9~36	21.9~87.5	Needs detector finalization

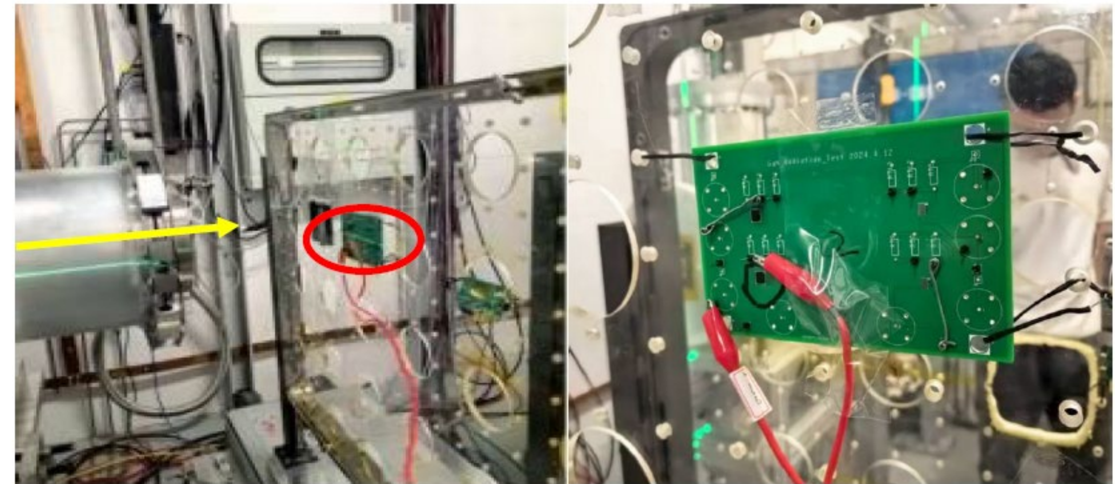
Update on common Power module



- Power requirements summarized according to the current readout schemes of each SubD
- Rad-test of COTS samples initiated, preliminary proved the GaN transistor can survive in the CEPC rad environment
- Recent plan:
  - Key component evaluation



测试仪器：源表、电源、万用表

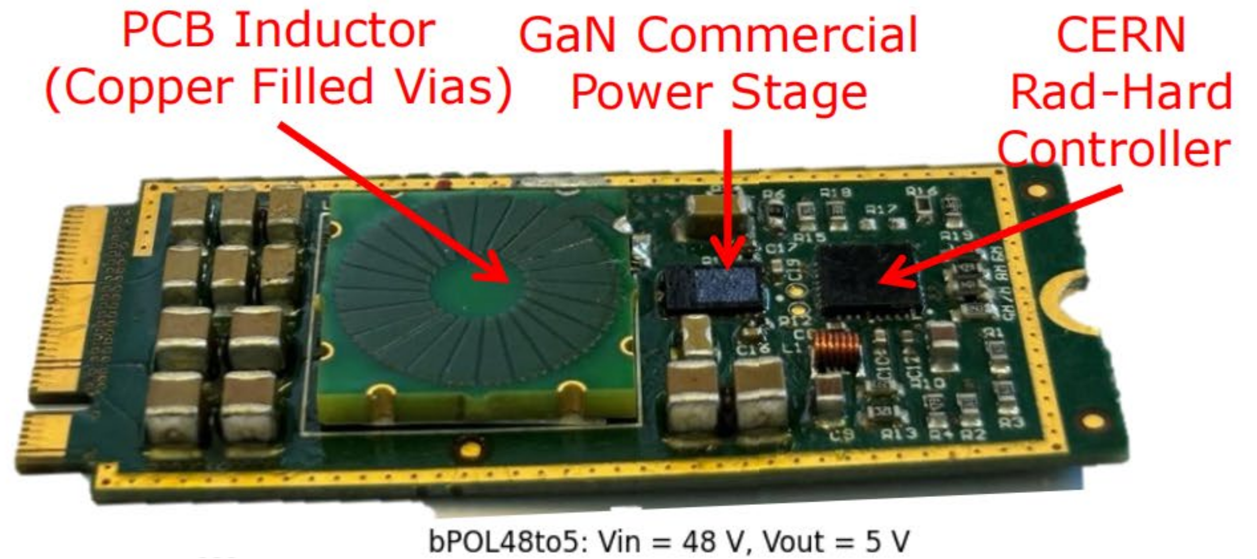


测试PCB固定到样品台上的实物照片(左图中黄色箭头为束流方向)

Using available stock of bPOL48V (~70K dies)

Volume optimized bPOL48 modules:

- bPOL48to12 (EPC2152): 48V to 12V with 6A out
- Dimensions: 24 x 55 x 4 mm



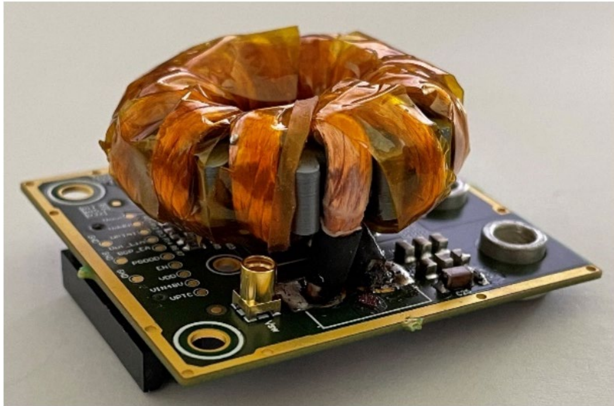


Figure 14: bPOL48V with air-core 220nH inductor.

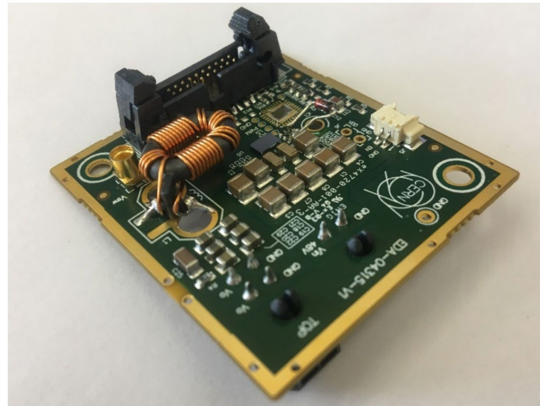
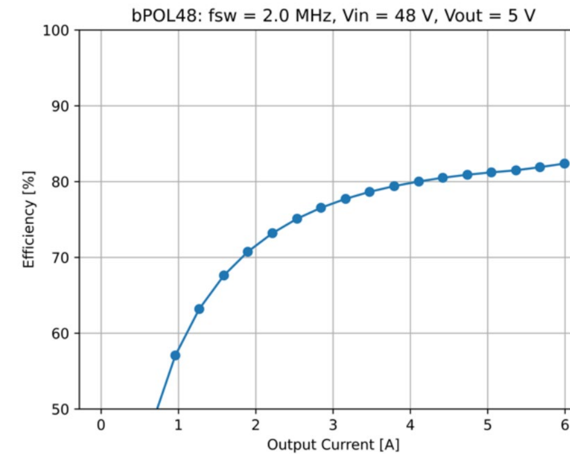
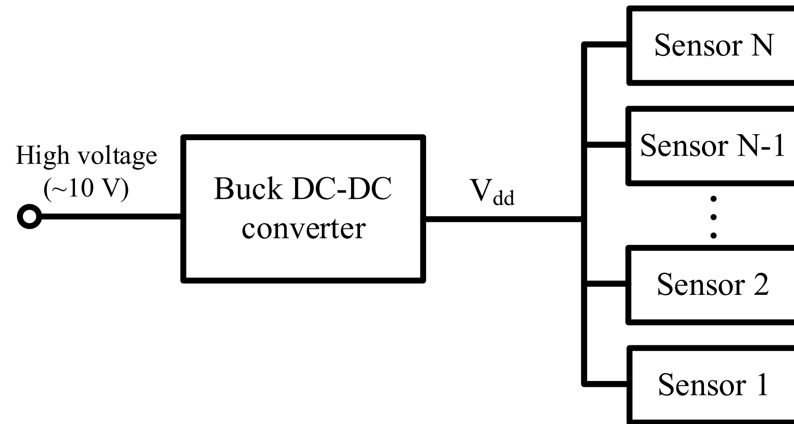


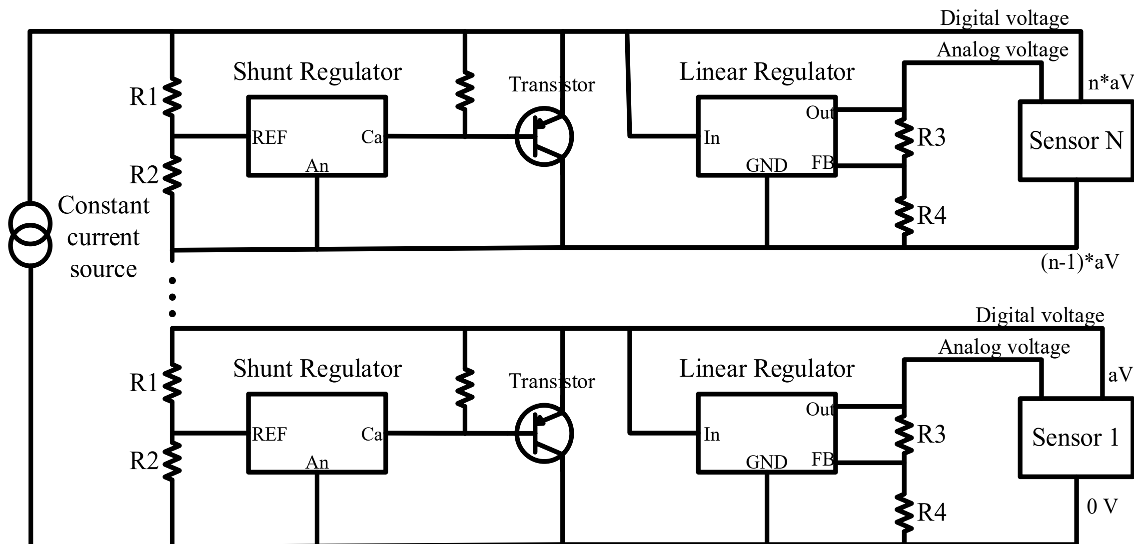
Figure 17. bPOL48V using the FEASTMP inductor.



Technology survey and our choices

Parallel powering with DC-DC converter VS Serial powering





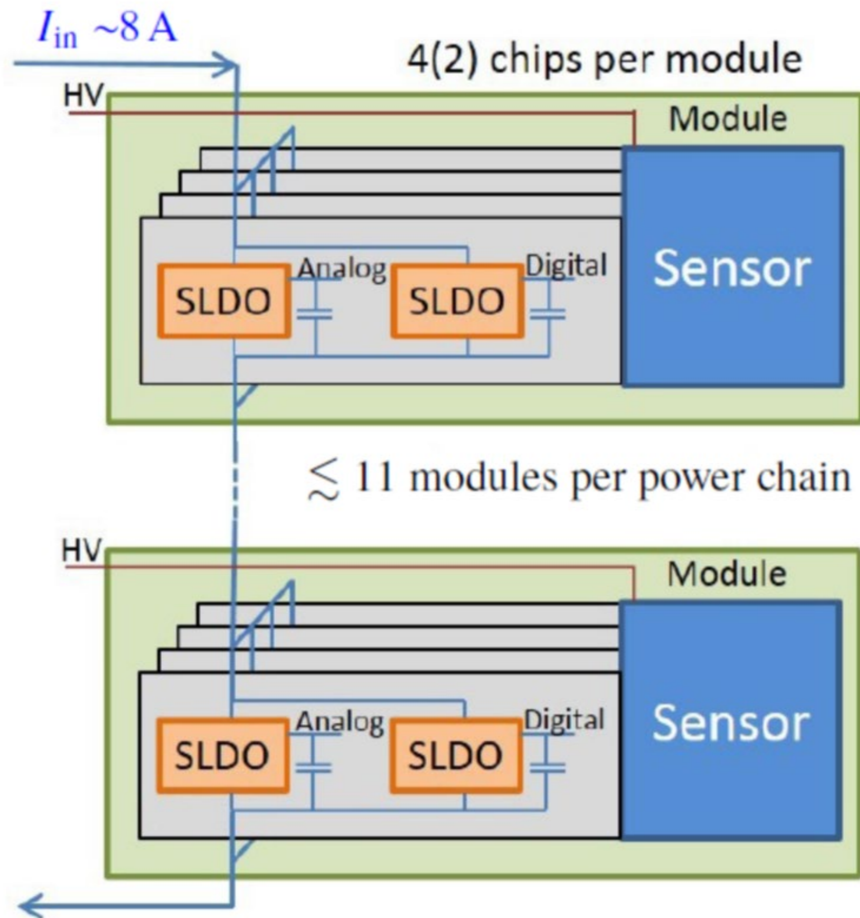
Parallel powering

- ✓ Compatible with the conventional power system
- ✓ Few changes of readout circuit or sensor required
- ✓ High reliability
- ✓ Unecessary on-chip regulator-> less die area
- ✗ Noisy ripple voltage
- ✗ Large-area air-core inductor
- ✗ EMI

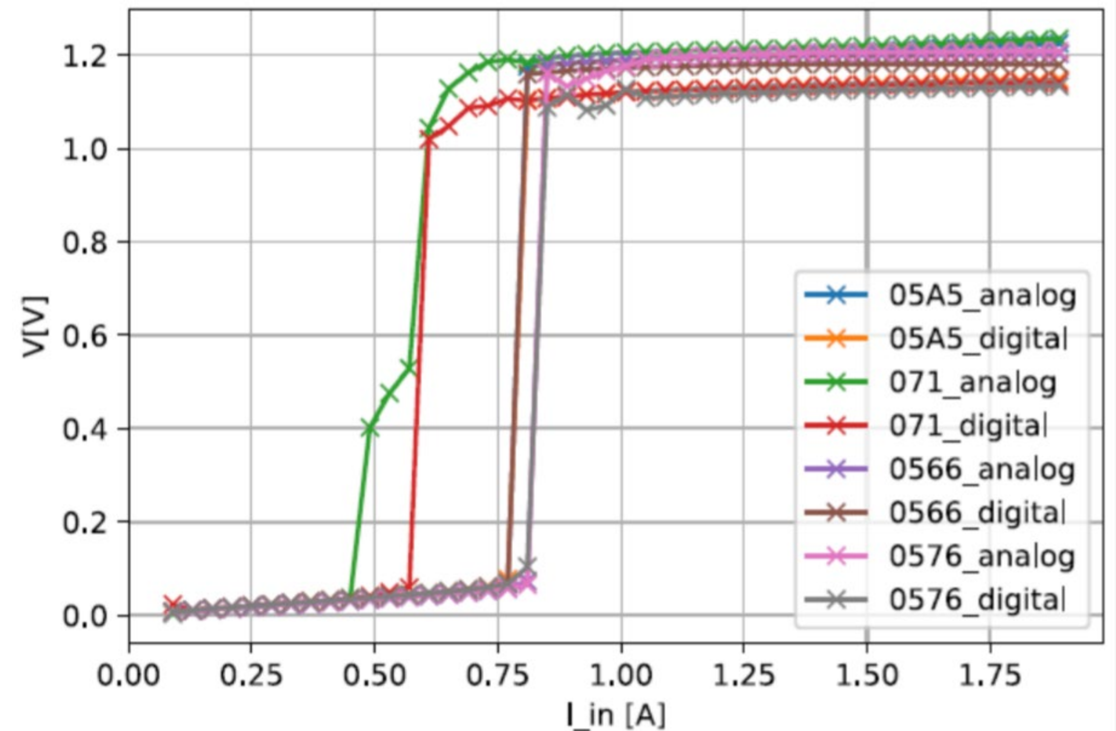
Serial powering

- ✓ Less cable mass
- ✓ Higher power efficiency, more suitable for large current load
- ✓ Low noise
- ✓ Unrequired Magnetic components
- ✗ Many changes with the old power system
- ✗ Lower reliablity
- ✗ Different groud potential -> AC-coupled output, no suitable for stiching chips, very high bias voltage of sensors
- ✗ “Larger” threshold current required to switch on shunt regulator
- ✗ Consistency of shunt regulator and LDO

Backup------Serial powering



Structure of serial powering for CMS pixel detector

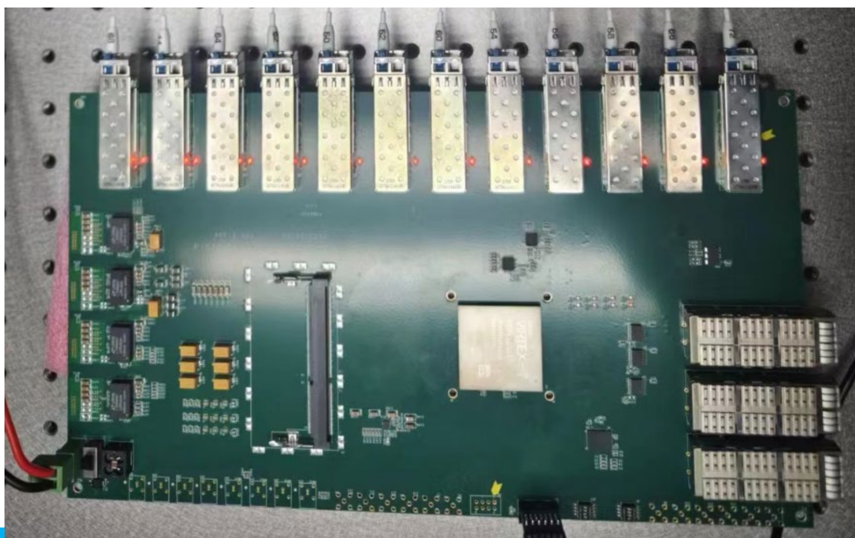


Regulated voltage for four single chips with different switching on current

[Vasilije Perovic, Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector, NIMA, Volume 978,2020,164436,]

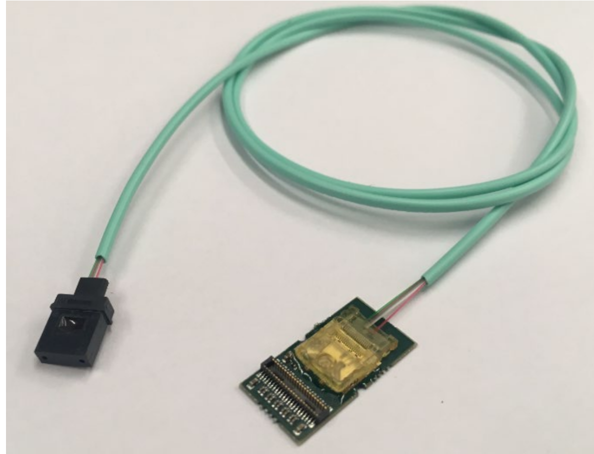
Preliminary consideration on common BEE

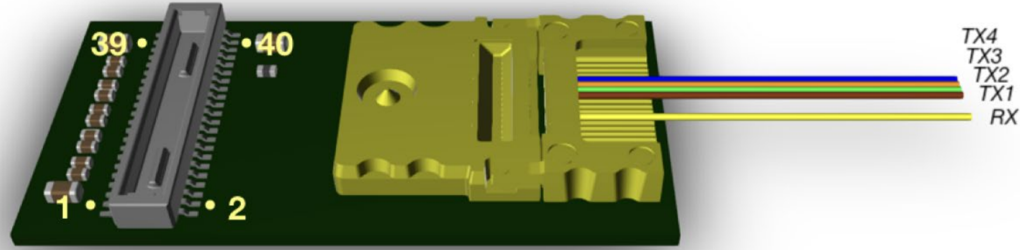
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory(Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

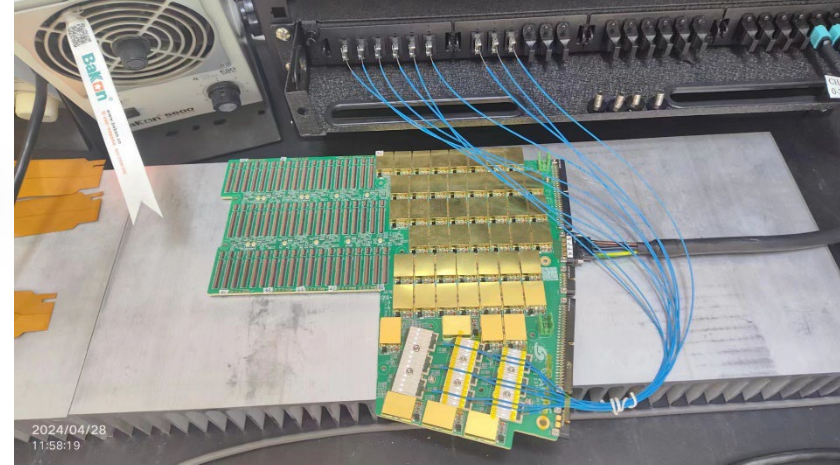


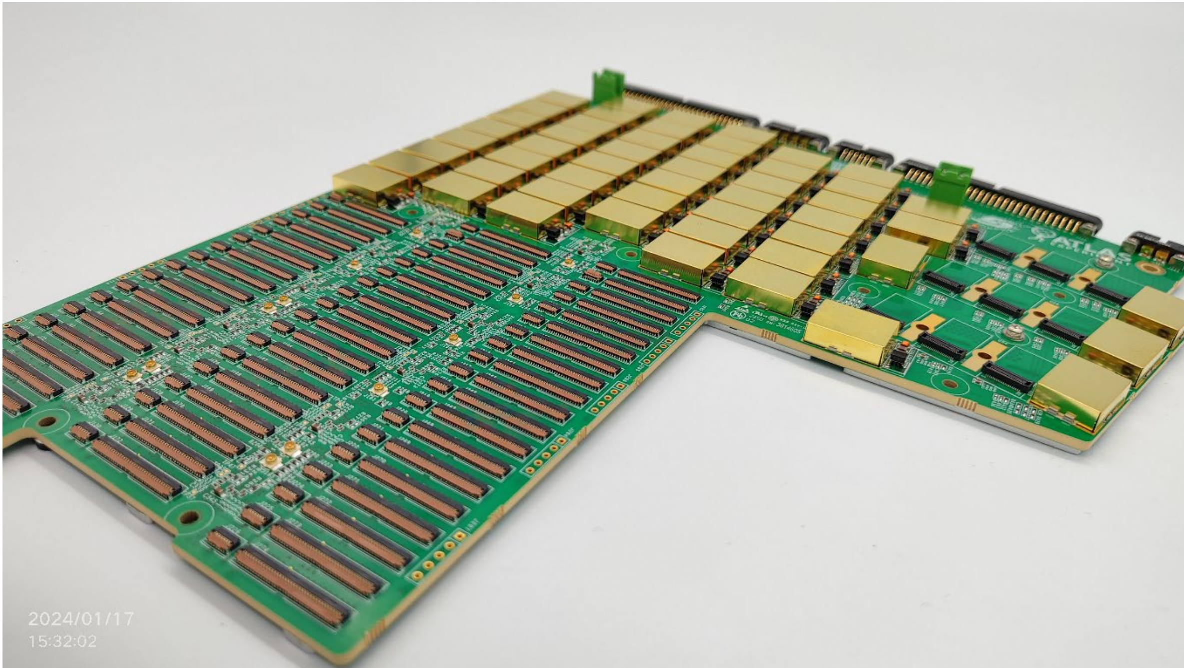
- A common station for fibers from FEE
- Providing data buffers till trigger comes
- Possible calculation resource needed for trigger algorithm
- Number of IOs, port rate & the cost are the major concerns

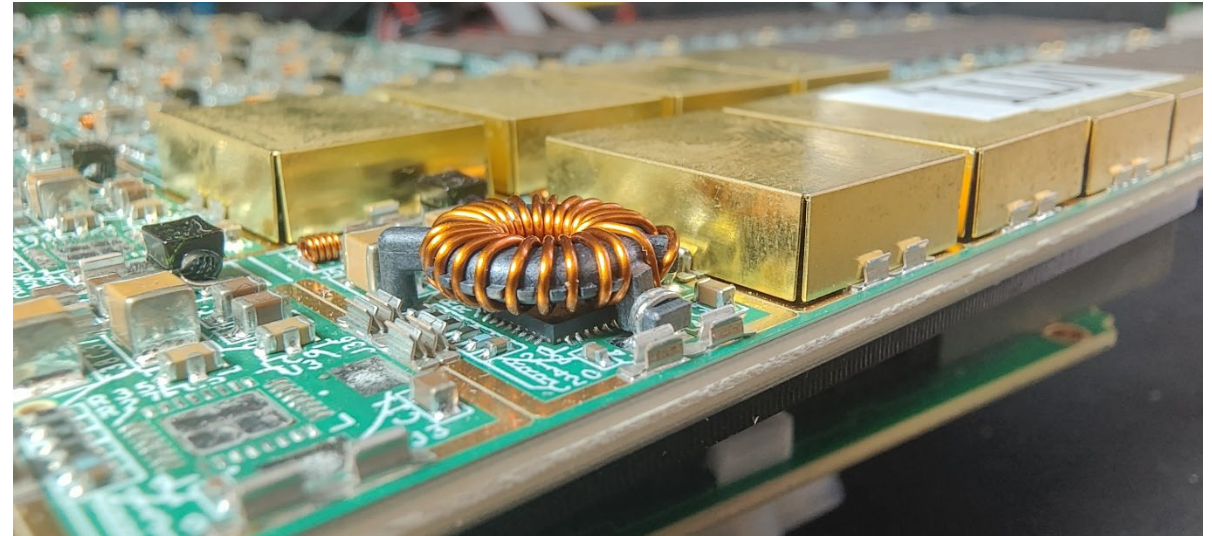
Size of bPol & GBT



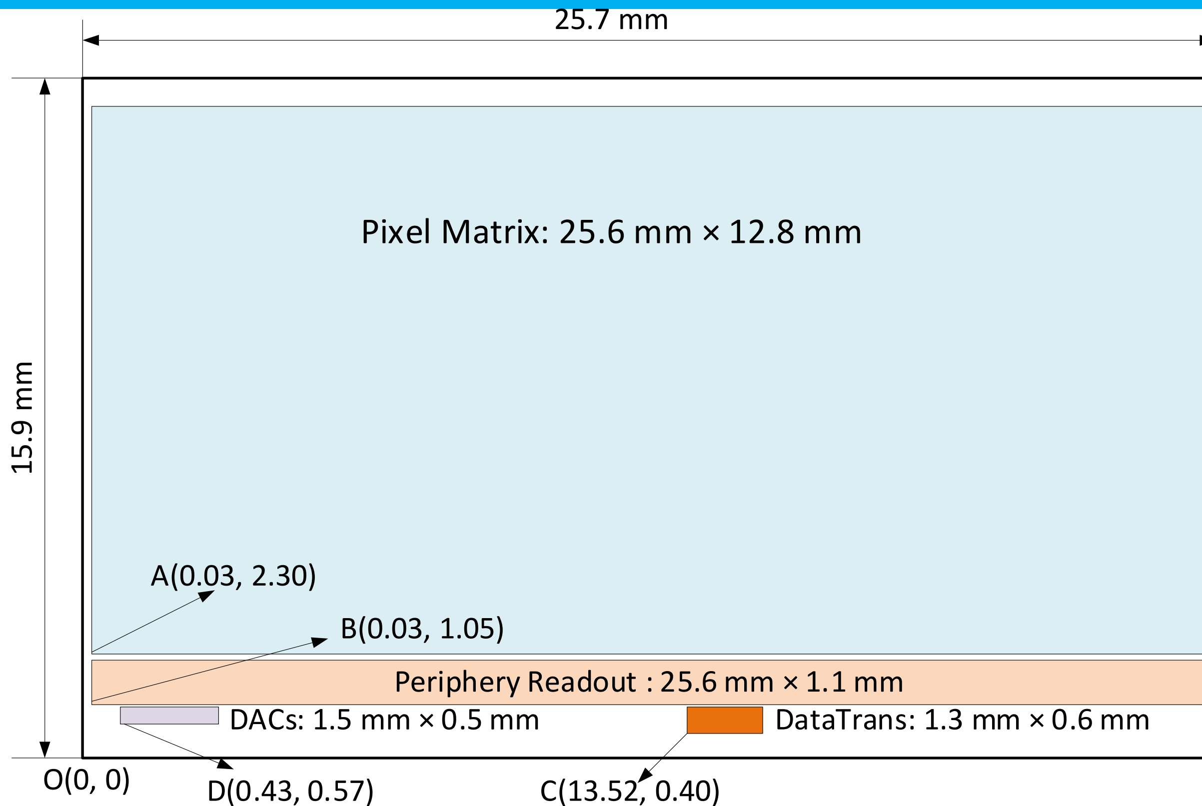








VTX像素芯片功耗分布估算

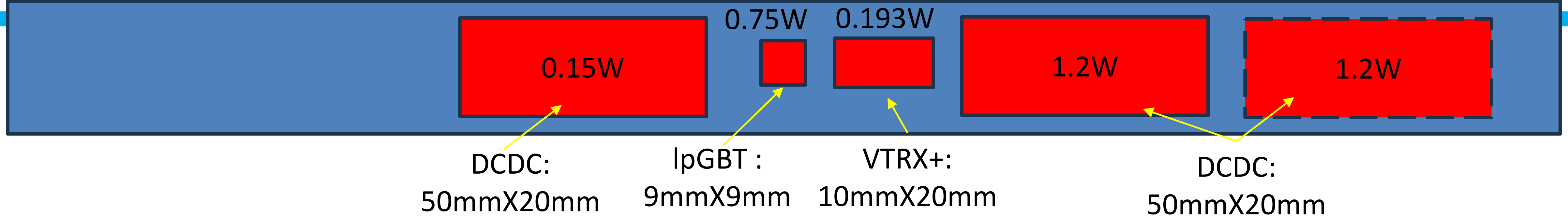


估算说明：

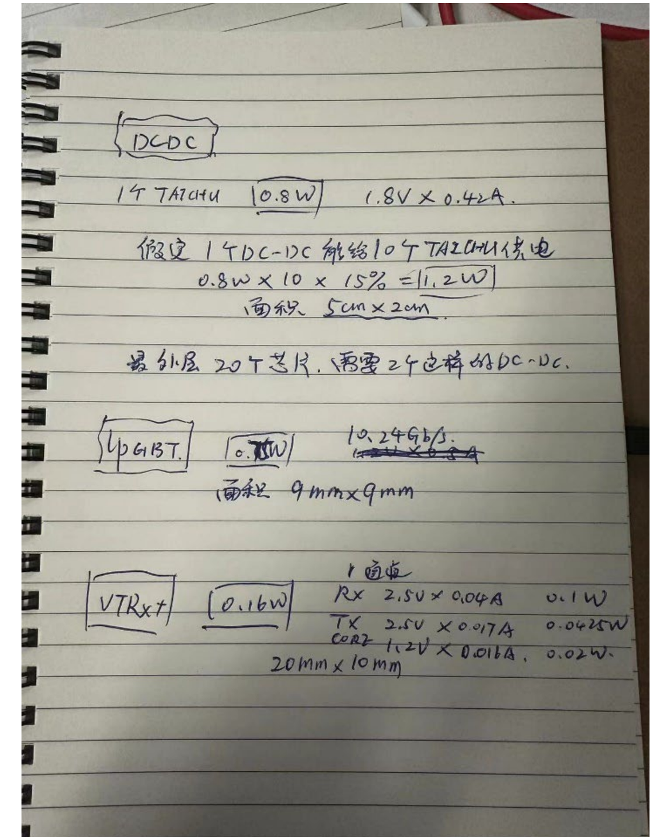
- 太初芯片：180 nm工艺，电源1.8 V;
- 65 nm芯片：电源1.2 V;
- Data rate @Triggless-CDR: 4.48 Gbps /chip
  bunch spacing (min.): 25 ns需要快前沿前端
- Data rate @Triggless-TDR (Low Lumi):
  1 Gbps/chip
- Low Lumi@TDR: bunch spacing ~几百ns，像素前端不需要快前沿，Matrix功耗可降低
- 图中芯片坐下角标为坐标原点，标注4个功耗模块的左下角坐标(X,Y)，单位为毫米

	Matrix	Periphery	DataTrans.	DACs	Total Power
太初芯片 @ triggerless (CDR)	304 mW	135 mW	206 mW	10 mW	655 mW
65nm 芯片 @ 1 Gbps/chip (TDR LowLumi)	60 mW	80 mW	36 mW	10 mW	186 mW

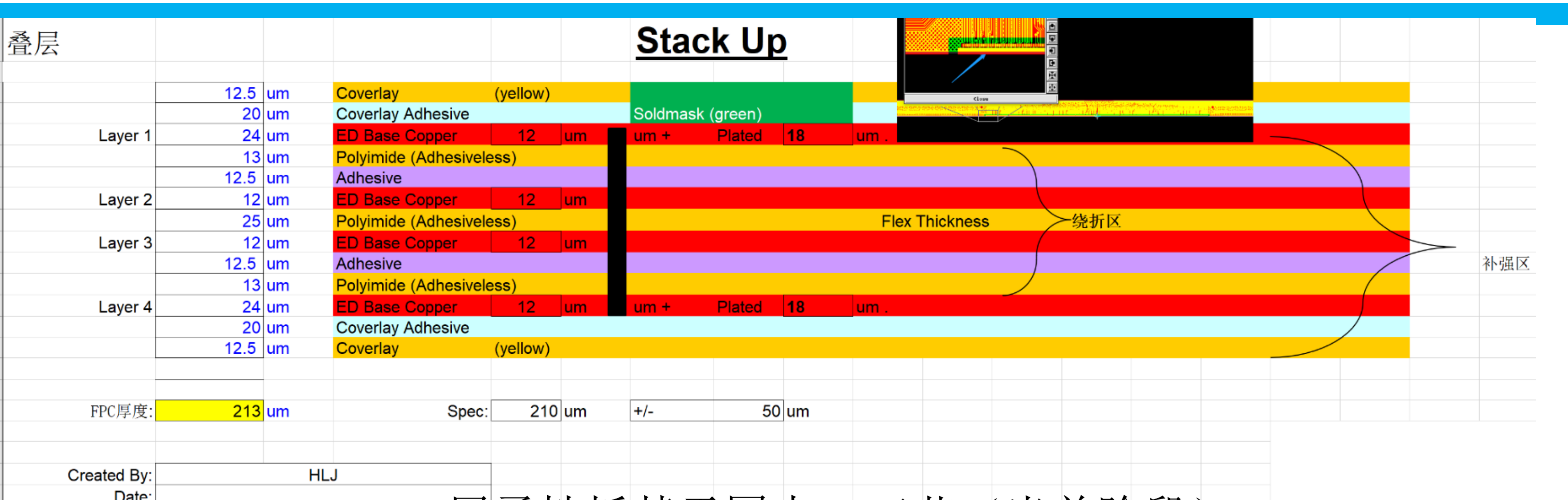
Ladder端部热功耗分布



- **DCDC：电源管理芯片**
  - TAICHU功耗0.8W（1.8V*0.42A）
  - 单个DCDC最多为10个TAICHU提供电源，效率按85%计算
  - DCDC功耗为0.8*10*15% = 1.2W
  - 如果最外层需要20个芯片则需要2个DCDC
  - lpGBT和VTRX+需要其他种类电源（1.2V，2.5V），总体功耗不高，~1W，则DCDC功耗为0.15W
- **lpGBT：数据汇总芯片**
  - 0.75W@10.24Gb/s
- **VTRX+：光电转化芯片**
  - 1发1收：0.193W（RX：2.5V*0.05A，TX：2.5V*0.02A，core：1.2V*0.015A）
- **说明：1：图中仅展示ladder一端一面，底面及ladder另一端有同样的配置**
- **2：lpGBT及VTRX+的参数为CERN对应芯片手册得到，CEPC最终参数可能有所不同。**
- **Ladder长度及端部器件位置，需结合机械及安装设计来调整**



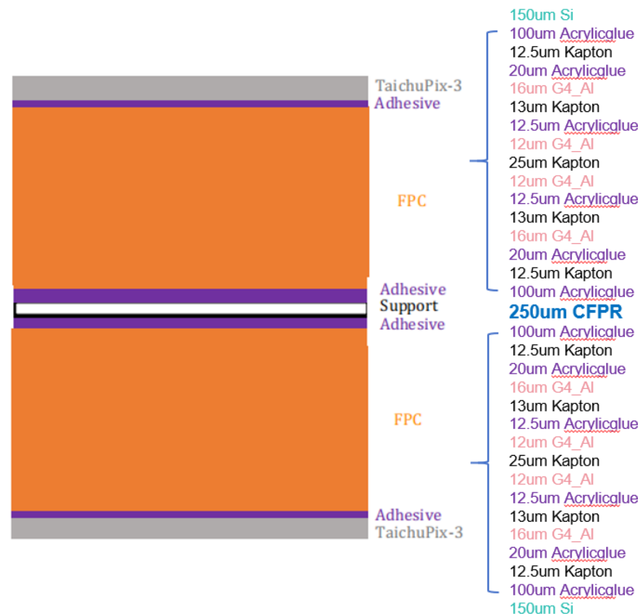
Flex厚度和物质分布



4层柔性板基于国内Cu工艺（当前阶段）

	12.5	um	Coverlay
	20	um	Coverlay adhesive
layer1	24	um	ED Base Copper
	13	um	Polymide(Adhesiveless)
	12.5	um	Adhesive
layer2	12	um	ED Base Copper
	13	um	Polymide(Adhesiveless)
	12.5	um	Adhesive
layer3	12	um	ED Base Copper
	25	um	Polymide(Adhesiveless)
layer4	12	um	ED Base Copper
	12.5	um	Adhesive
	13	um	Polymide(Adhesiveless)
layer5	12	um	ED Base Copper
	12.5	um	Adhesive
	13	um	Polymide(Adhesiveless)
layer6	24	um	ED Base Copper
	20	um	Coverlay adhesive
	12.5	um	Coverlay
厚度	288	um	

6层柔性板基于国内Cu工艺（当前阶段）



Proposed Double-sided ladder based on 铝

- 国内工艺当前只能实现基于铜的PCB，如需采用铝材料，需要委托CERN进行加工（accessibility？）
- Long barrel方案，同ladder芯片更多，需要更多层的PCB
  - For Innermost：4层Flex（now：Cu based，proposed：Al based）
  - For Middle & Outer：6层Flex（now：Cu based，proposed：Al based）

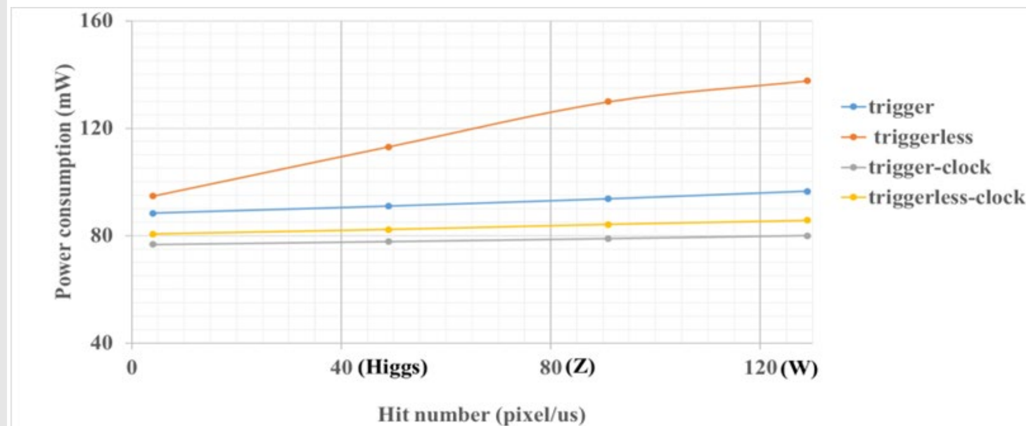
Backup

Specification calculation- from hit density

		Hit density (Hits/cm²/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm²)	Hit Pix rate (M Px/cm²)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	213.9?
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	213.9?
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

- TDR raw hit density: Higgs 0.54， Z 0.3; Safety factor: TDR 1.5, CDR 10;
- Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)
- Area: 1.28cm*2.56cm=3.27cm² (@pixel size 25um*25um)
- Word length: 32bit/event (@Taichu's scale, 512*1024 array)
- Trigger rate: 20kHz@CDR, 120kHz@TDR estimated
  - Trigger latency: 3us(very likely not enough), Error window: 7 bins
  - FIFO depth: @3us * hit rate/chip
  - Data rate=pixel/bunch*trigger rate*32bit*error window

2



仅外围电路功耗vs计数率

	能力		
	160Mbps	2.56Gbps	4.48Gbps
PLL	20	34	34
MUX	8	27.8	44.2
CMLdriver		36.5	36.5
LVDS_TX	5	7.5	10
	33	98.3	114.7

数据接口功耗vs数据率