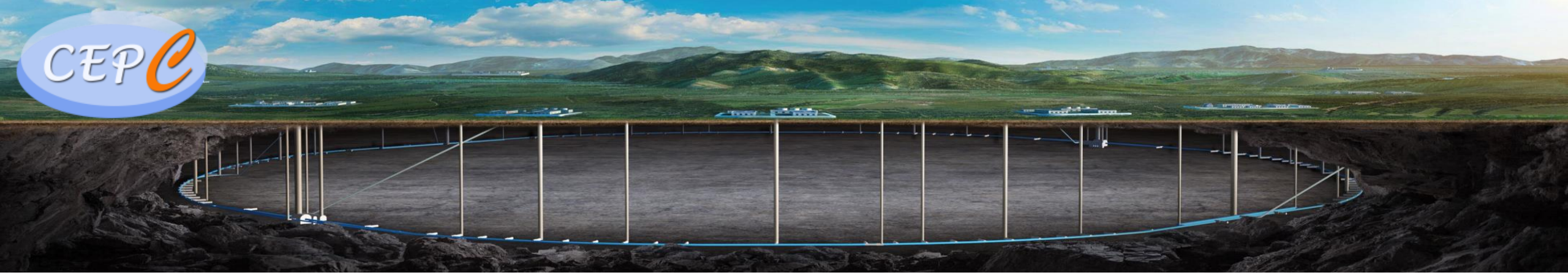

Progress of CEPC ref-TDR TDAQ

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Institute of High Energy Physics
Chinese Academy of Sciences

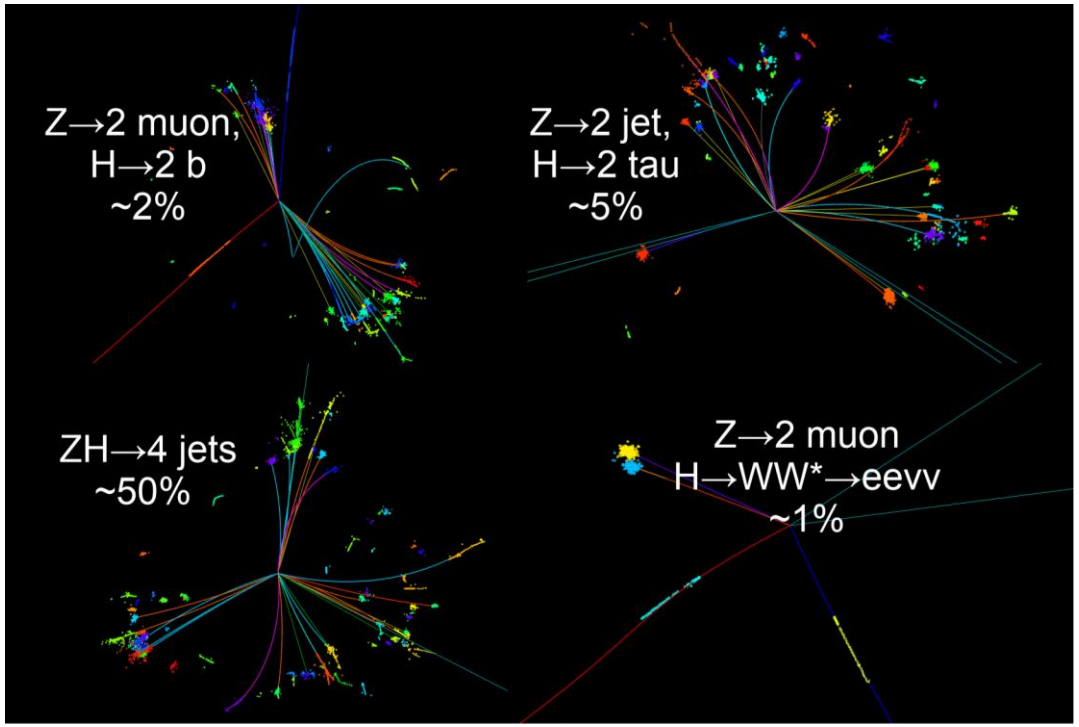
Progress of TDAQ

- Ref TDR meeting
  - Oct. 11th (Fri. morning)
  - Review talk and TDR discussion
    - Merge HW option 1 and 3 together
    - Cancelling software trigger option
  - Boping Chen
    - Trigger simulation progress
  - Confirmed schedule for workshop

Requirements: Physical Event Rate

- 8 Hz @ Higgs 240GeV(50MW)
  - Bunch crossing rate: 2.889 MHz
  - Higgs: ~0.02Hz
- 82 kHz @ Z pole 91GeV(50MW)
  - Bunch crossing rate: 43.3 MHz
- Physical event rates are sufficiently low relative to the bunch crossing rate.
- Keep as more physical events as possible
  - Through a rough selection of the relevant objects (jet, e, muon, tau,v, ...) and combinations.
  - Detailed signal feature extraction and simulation studies are required.

	Higgs	Z	W	$t\bar{t}$
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 (×15)	23.1 (×1)	138.5 (×6)	2700.0 (×117)
Train gap (%)	54	9	10	53
Luminosity per IP (10^{34} cm^{-2} s^{-1})	8.3	192	26.7	0.8



Ref: CEPC Physics at a glance, Lomonosov Conference 2021, by Manqi Ruan

Requirements: Data Rate

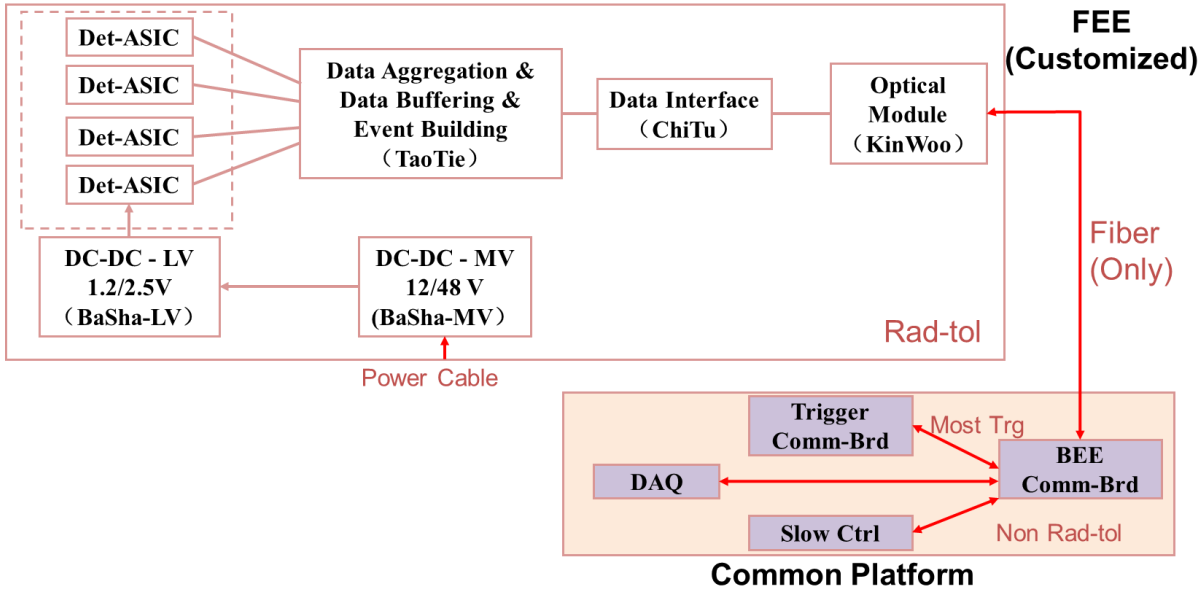
- Data rate before trigger
  - < 1 TB/s @ Higgs
  - Several TB/s @Z
- Expect event rate after HLT
  - O(1k) Hz @ Higgs
  - O(100k) Hz @ Z
- Event size < 2 MB
- Data storage rate
  - Higgs: 2 GB/s
  - Z: 200 GB/s

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024	512*128	1024	128		128	8~16				
Data Width /hit	32bit	42bit	32bit	48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip	Avg. 3.53Mbps/chip	Avg. 21.5Mbps/chip	Avg: 2.9Mbps/chip	Avg: 38.8Mbps/chip	~70Mbps/module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	Needs detector finalization
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1 Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs finalization	Needs finalization	Needs finalization	Needs finalization
Occupancy	0.22e-4	2.5e-4				2.8e-4	0.58e-2			1.95e-5	
Sum	5.8Tbps										

Preliminary background and data rate estimation

Our choices

- Fewer physical processes and lower backgrounds @CEPC
- Electronics framework schema
  - Readout full data from Front-end Elec.
  - Back-end Elec. connect with trigger
- Trigger solutions
  - Hardware trigger(L1) + HLT
    - Common hardware trigger board
      - Collect trigger primitives from BEE(Back-end electronics)
      - Send back trigger accept signal to BEE
    - Provide fast and normal trigger menu
    - Network readout

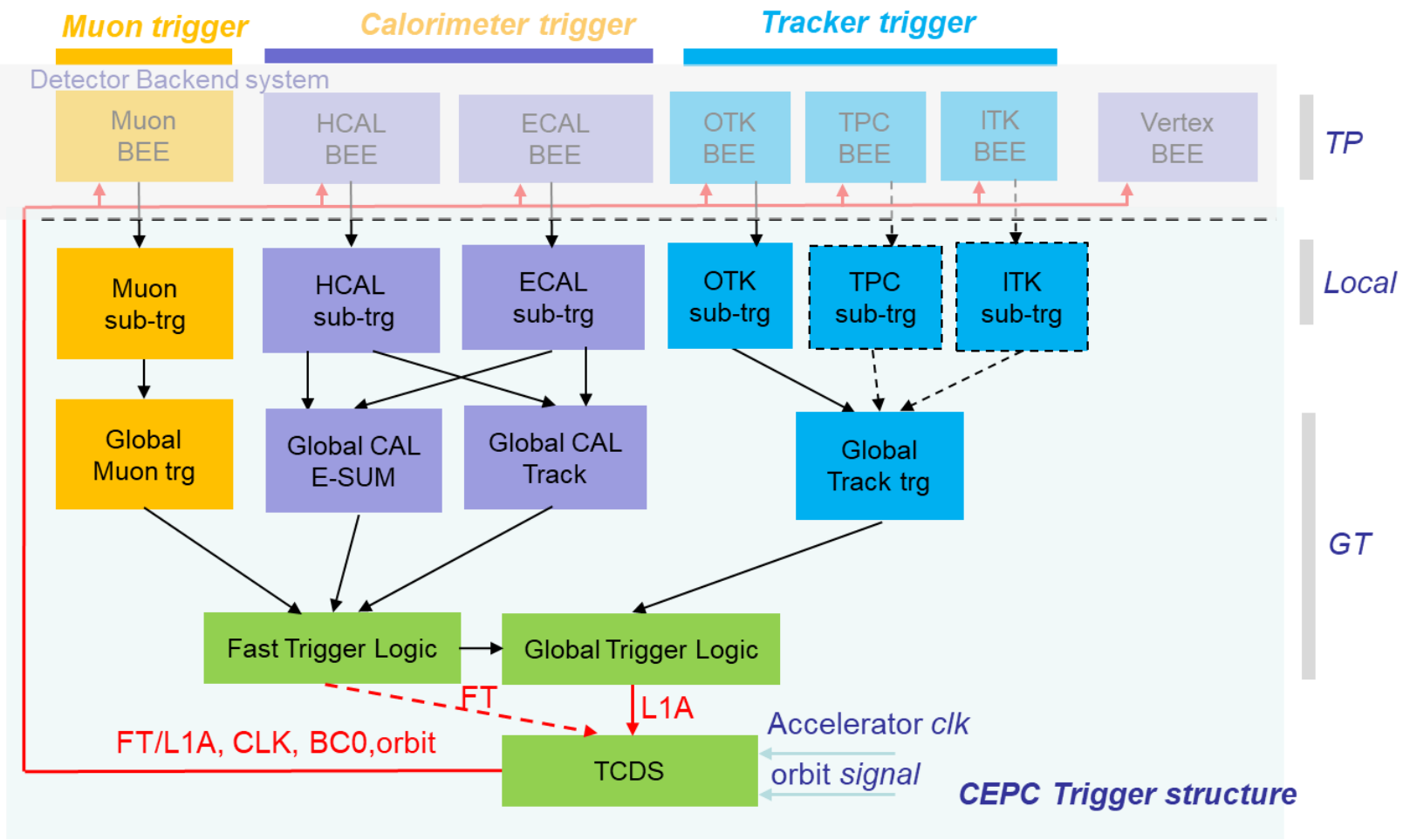


Main Technical Challenges

- High efficiency in trigger and background compression
  - 2.887MHz->O(100)Hz @Higgs
  - 43.3MHz->O(100k)Hz @Z
- Trigger primitive synchronization control with asynchronous data readout from electronics
  - Manage data disorder due to data transfer queuing and delay
  - Align sub-detector data of each bunch crossing within limited time and resource

Design of Hardware Trigger Structure

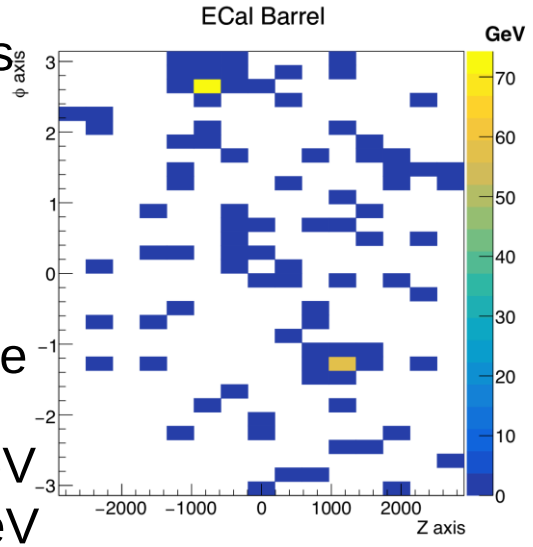
- Trigger primitive(TP)
  - Generated by BEE
- Local detector trigger information(energy, track…)
  - Generated by sub-trigger
- Fast trigger(FT) and L1A
  - Generated by global trigger according to physical requirement
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied

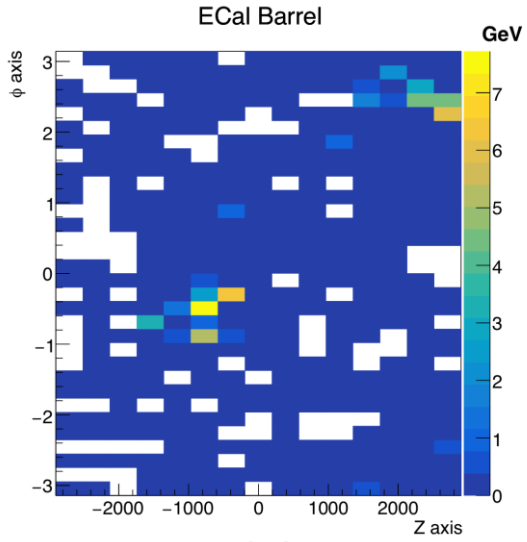


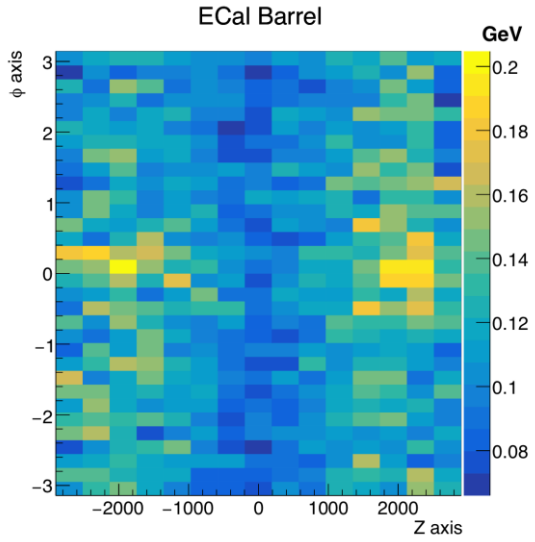
Designing a single type of common trigger board

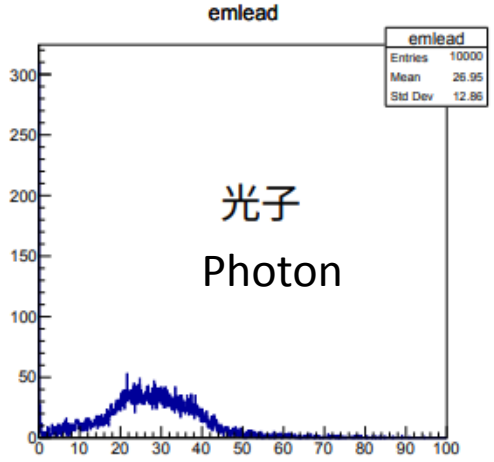
Preliminary Trigger Simulation with ECal

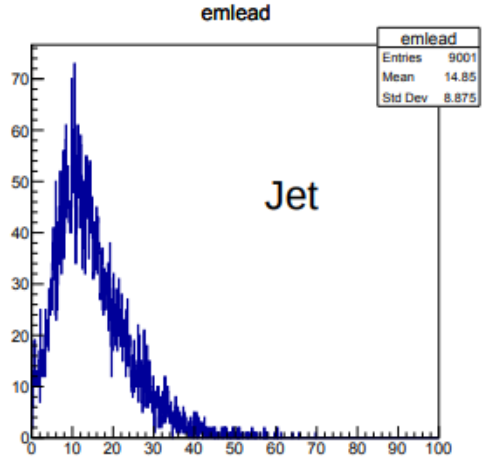
- Physical events signature at Ecal
  - Energy deposition is relatively large and concentrated
- Trigger primitive and condition
  - Two clusters with the highest energy
  - ECal energy>0.5GeV
  - HCal energy>0.5GeV
- Trigger efficiency
  - nnaa:100%
  - nnbb:100%
  - nnaZ:99.7%
  - nntautau:96.7%
  - nnWW:99.1%
  - nnZZ:95.8%
  - nnZZ:95.8%
  - Beambkg:4.8%

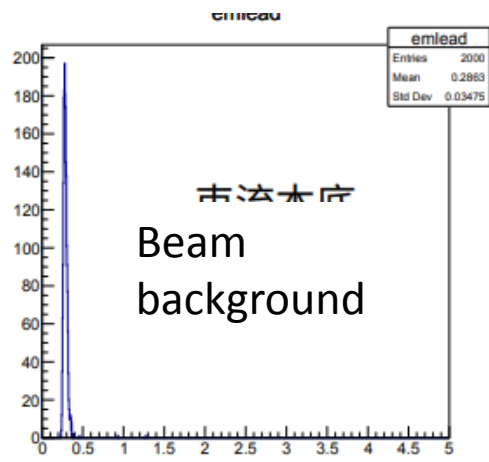








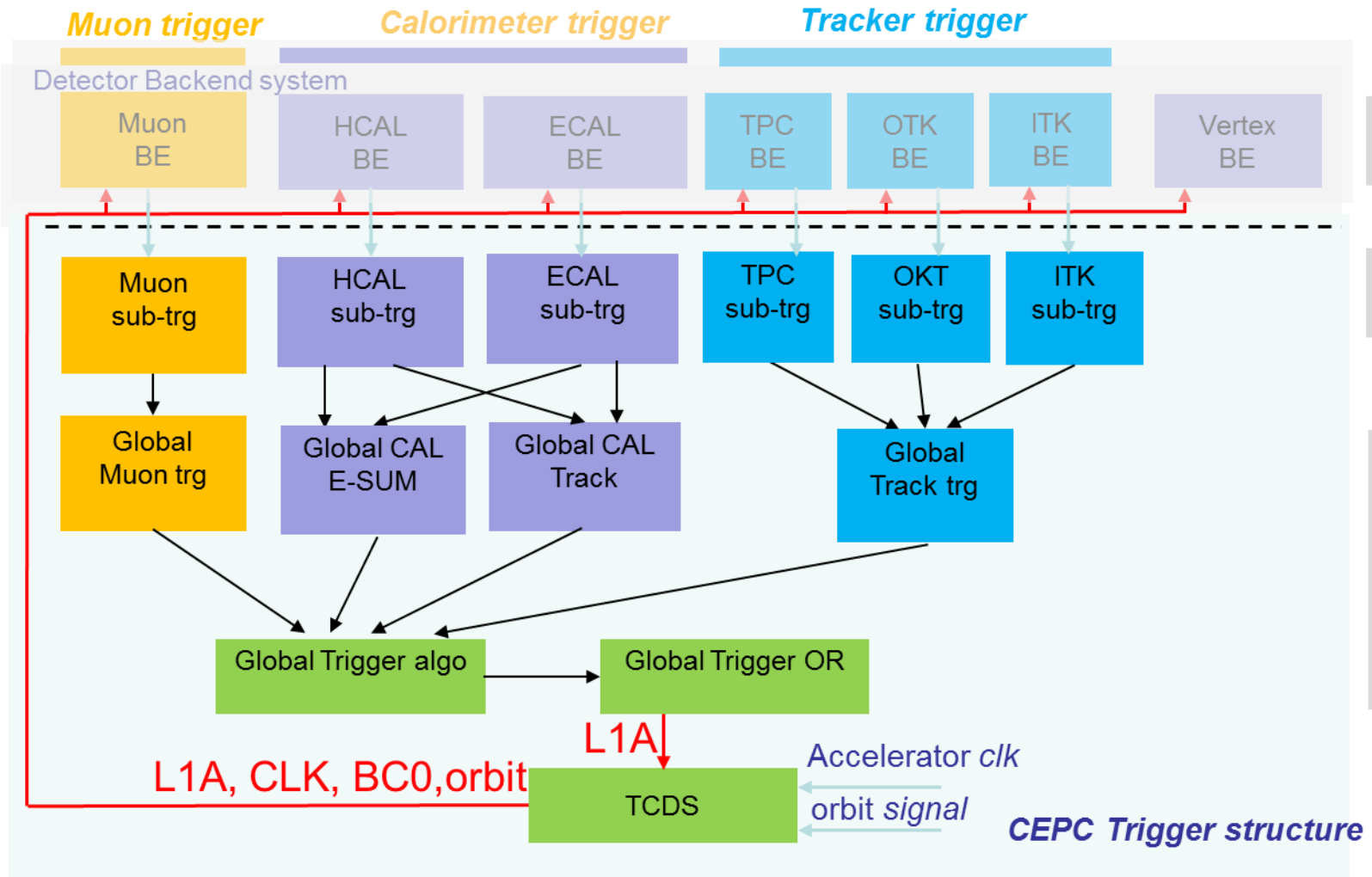




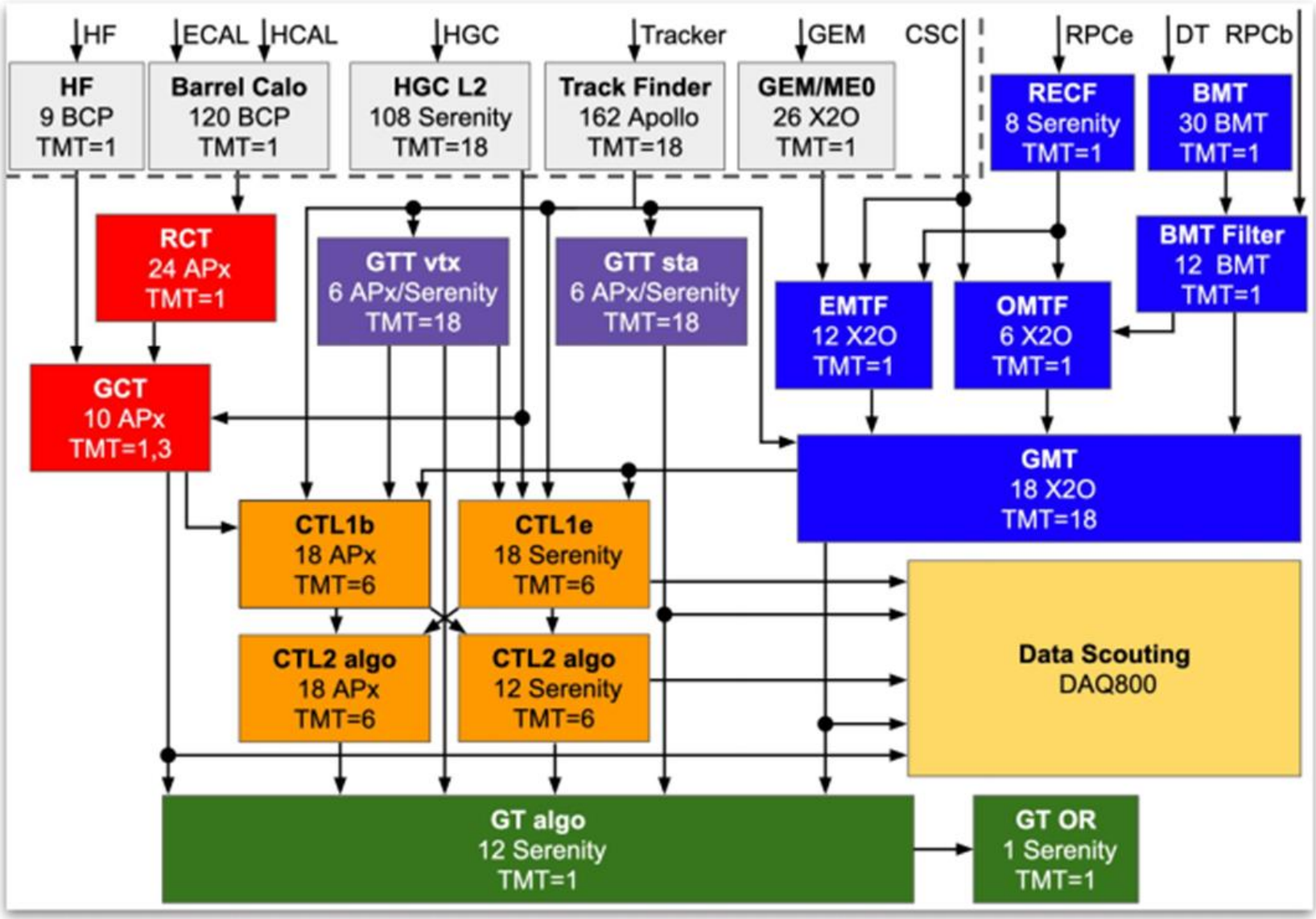
Backup

触发系统结构设计与规模估算

- 触发三层结构设计
  - 分区、探测器、全局
- 触发板数量计算因素
  - 触发板input：16x10Gb
  - BEE连接数
    - 920 BEE/16=58
  - 传输数据量
    - 未定
    - 35@Higgs
      - 4.42Tbps/8Gbps/16
    - 35*5=173@Z
  - 算法复杂度
    - 未知
    - CMS 210块触发板
- 初步估算：触发板160块，ATCA机箱20个，机柜10个

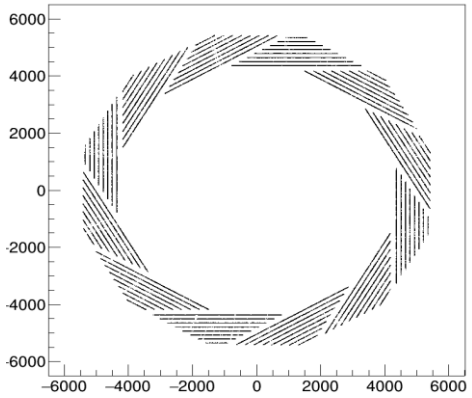


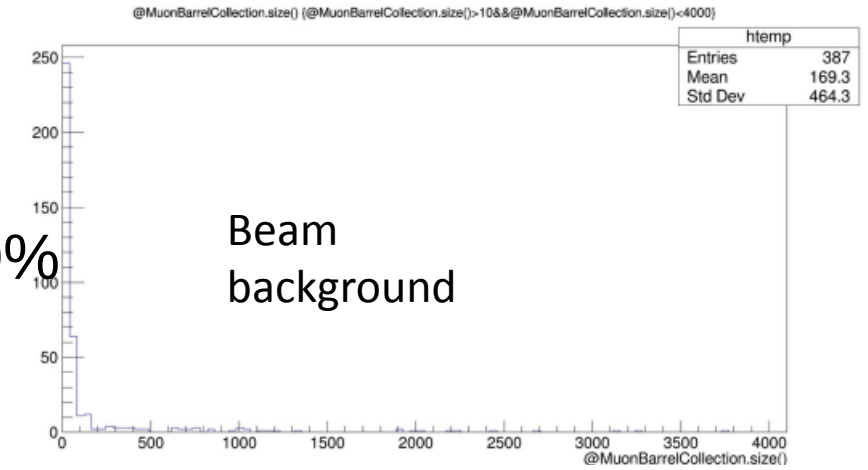
CMS二期触发板数

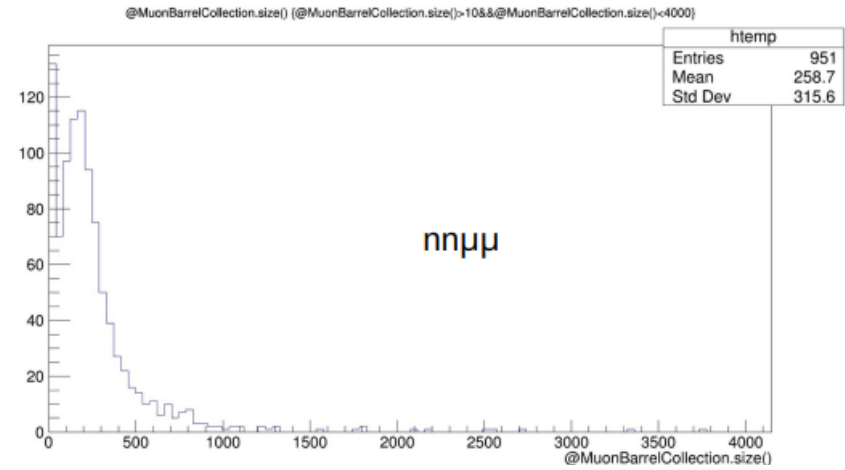

HF
ECAL
HCAL
HGC
Tracker
GEM
CSC
RPCe
DT
RPCb
HF
9 BCP
TMT=1
Barrel Calo
120 BCP
TMT=1
HGC L2
108 Serenity
TMT=18
Track Finder
162 Apollo
TMT=18
GEM/ME0
26 X2O
TMT=1
RECF
8 Serenity
TMT=1
BMT
30 BMT
TMT=1
RCT
24 APx
TMT=1
GTT vtx
6 APx/Serenity
TMT=18
GTT sta
6 APx/Serenity
TMT=18
EMTF
12 X2O
TMT=1
OMTF
6 X2O
TMT=1
BMT Filter
12 BMT
TMT=1
GCT
10 APx
TMT=1,3
GMT
18 X2O
TMT=18
CTL1b
18 APx
TMT=6
CTL1e
18 Serenity
TMT=6
CTL2 algo
18 APx
TMT=6
CTL2 algo
12 Serenity
TMT=6
Data Scouting
DAQ800
GT algo
12 Serenity
TMT=1
GT OR
1 Serenity
TMT=1

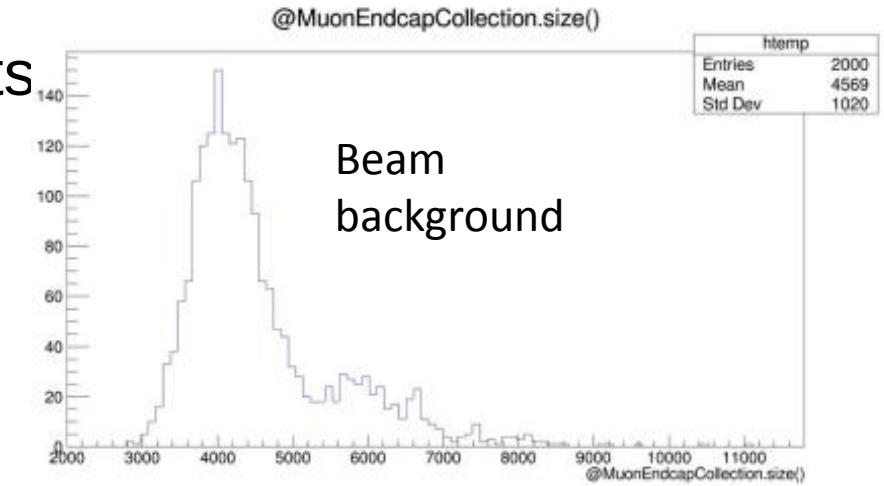
Preliminary Trigger Simulation with Muon

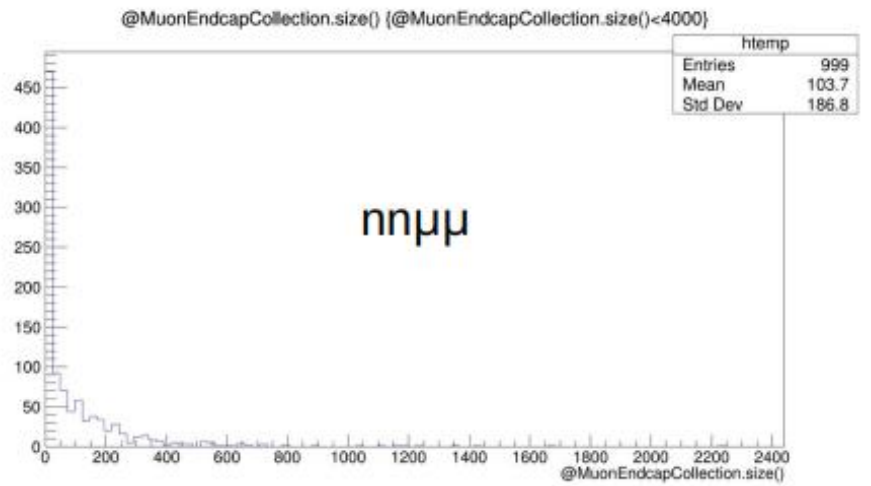
- Left： 2000 background events(10BX)；Right： 1000 ZH→nnμμ events
- Up：Barrel
  - N(Barrel)>10
  - nnμμ efficiency: 100%
  - Background: 19%
- Down：Endcap
  - High background hits





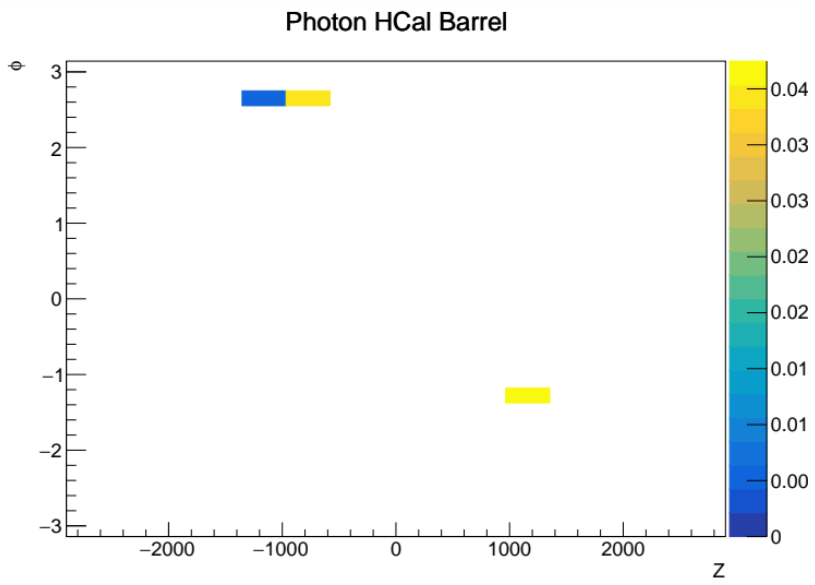


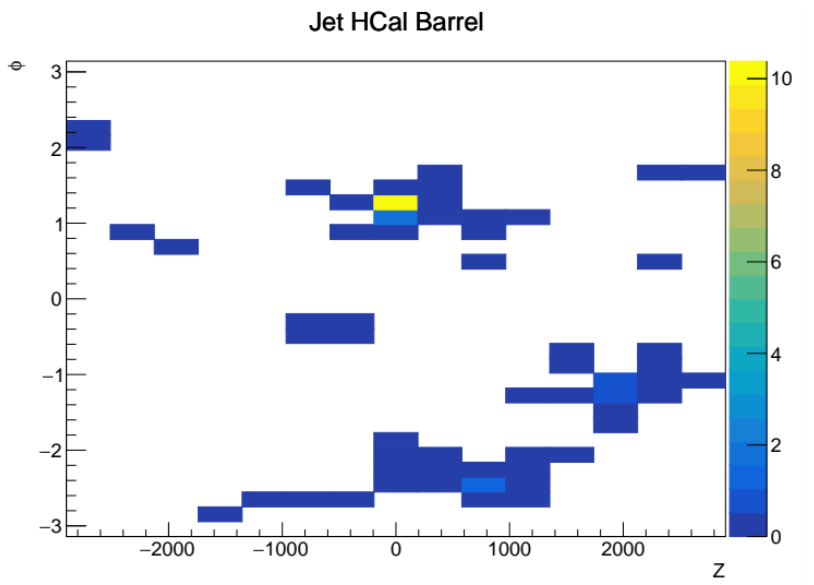


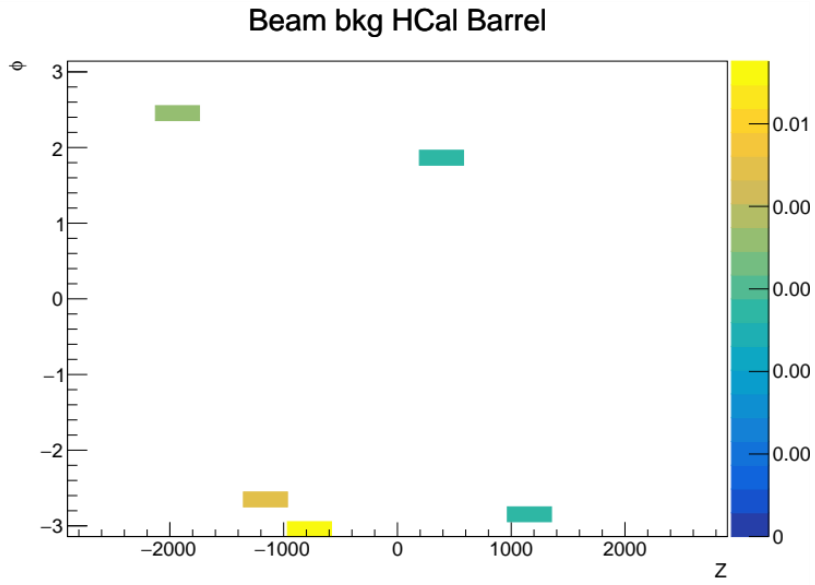


HCal barrel 能量分布

- 左：nnɣɣ；中：nnbb；右：束流本底

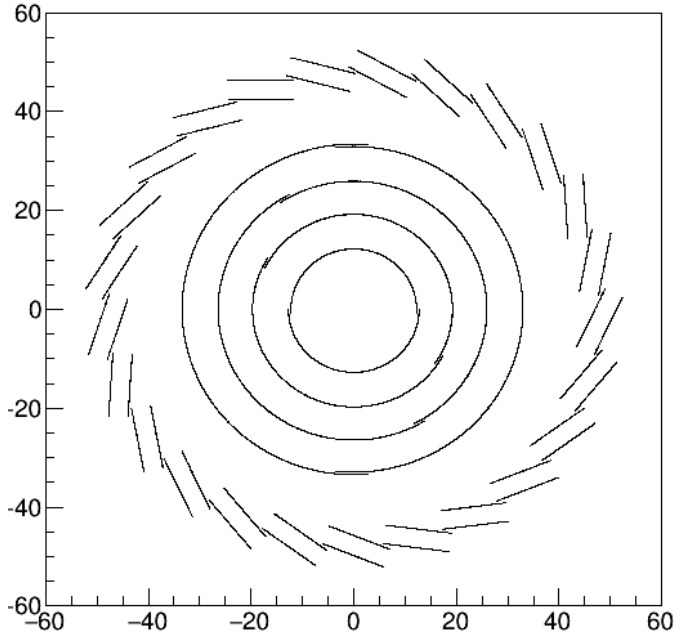


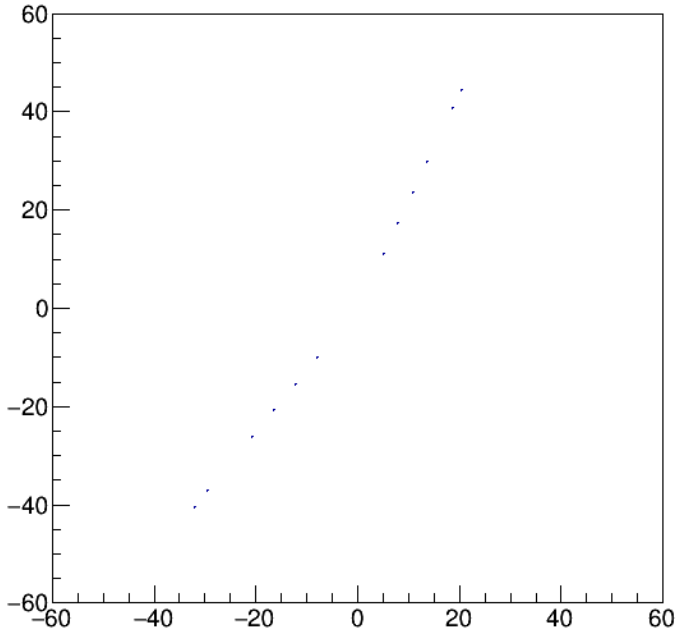


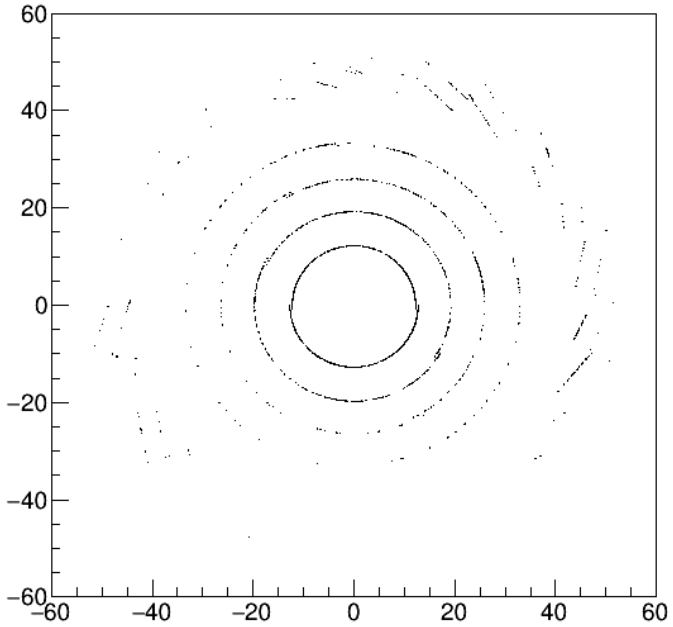


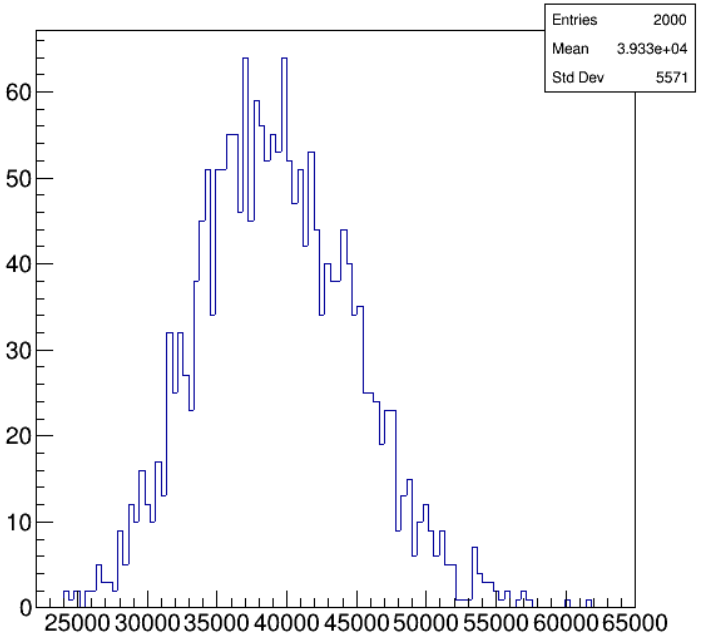
Vertex

- 左：单个ZH→nnμμ事例
- 中：单个束流本底事例
- 右：束流本底Vertex hit数量分布



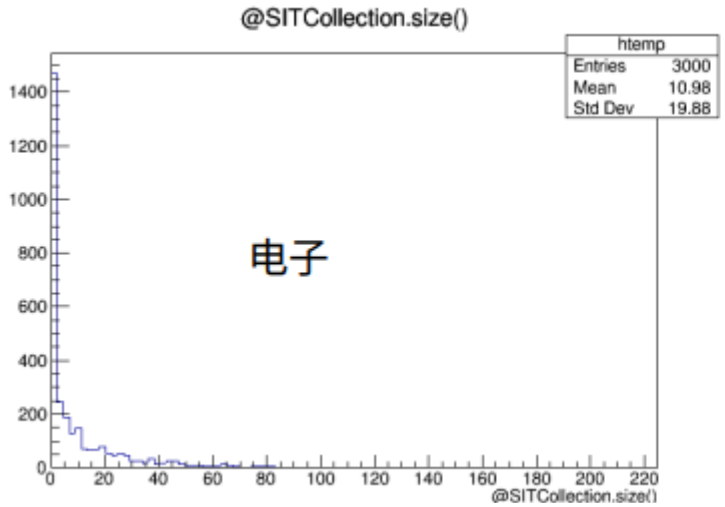


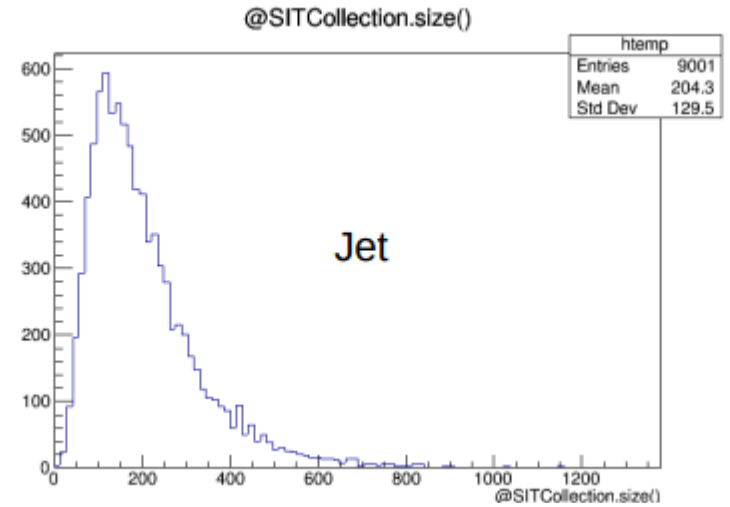


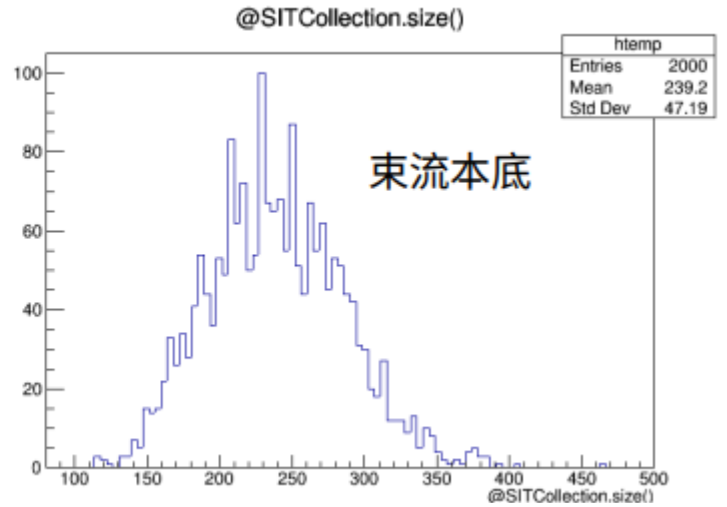


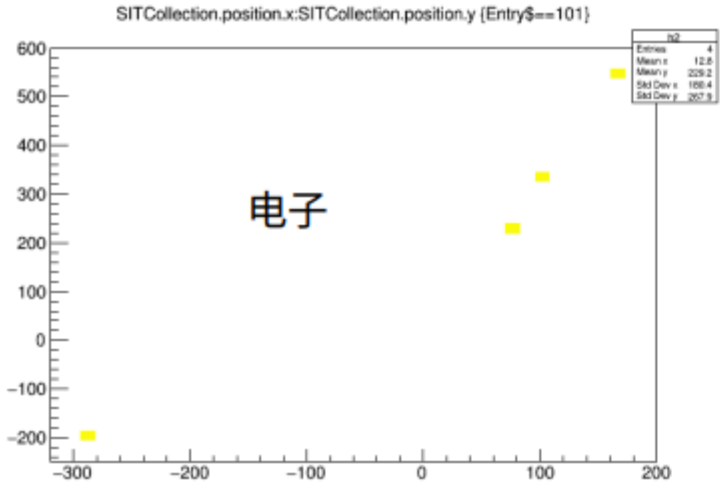
ITK Hit 个数分布

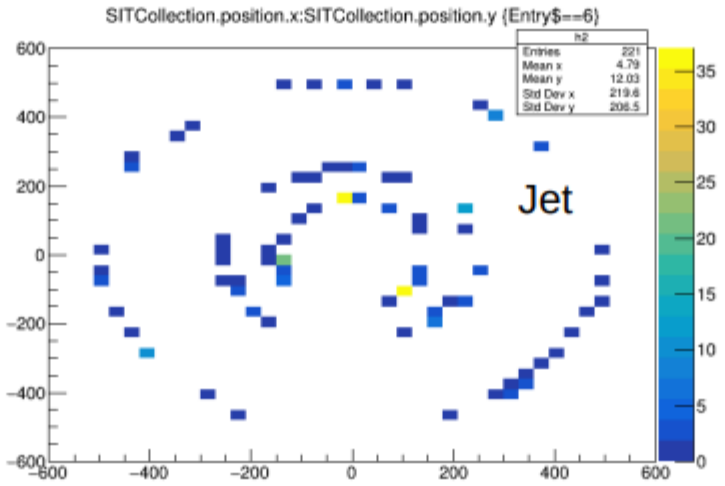
- 左： bhabha ；中： nnbb ；右：束流本底（ 10BX ）

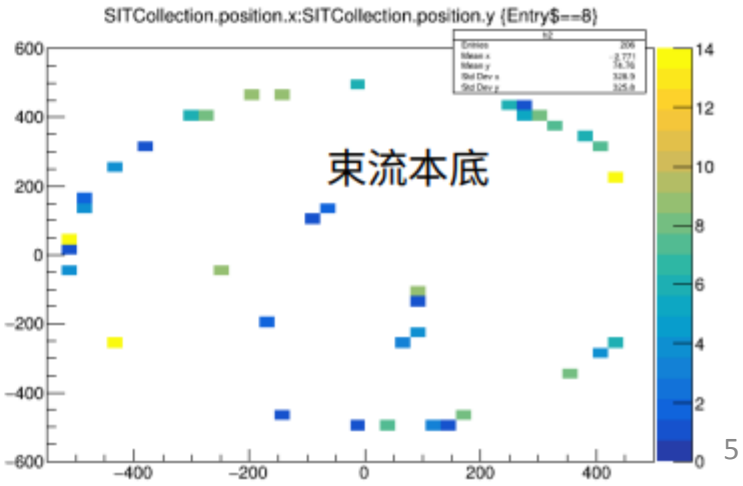






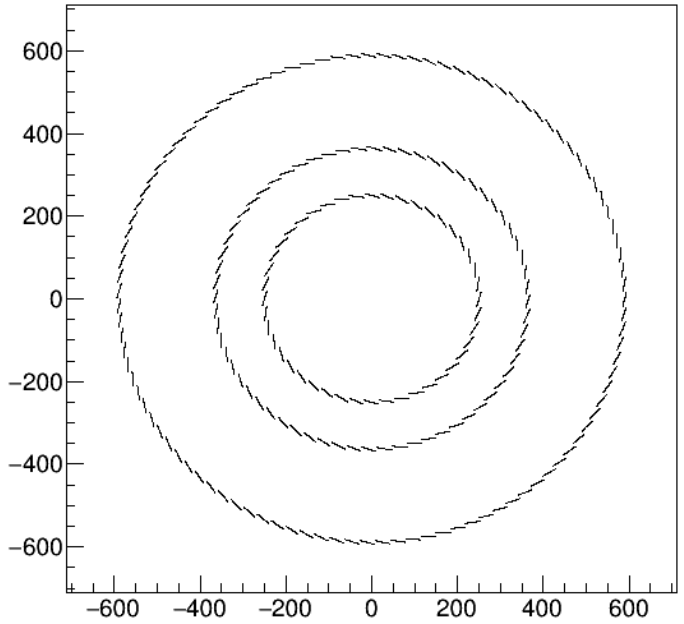


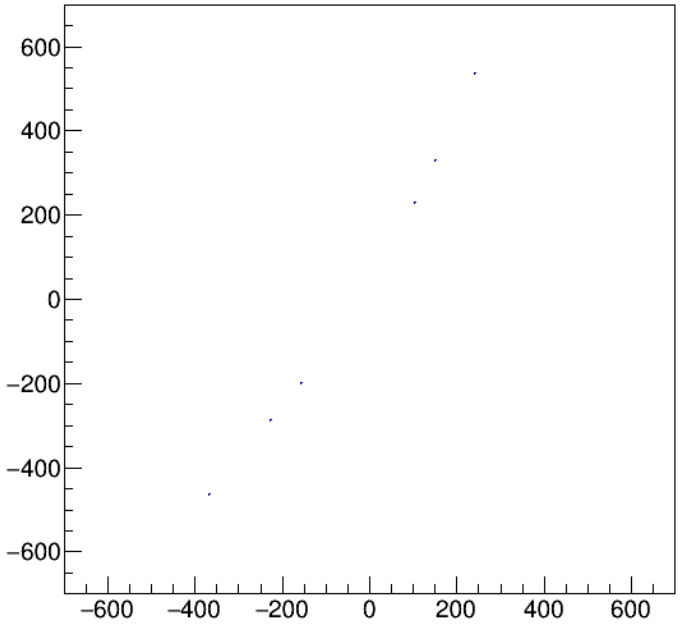


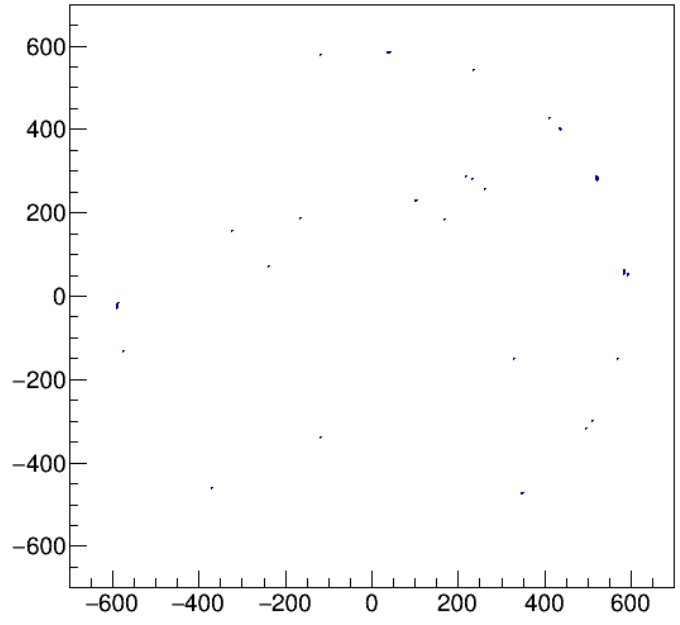


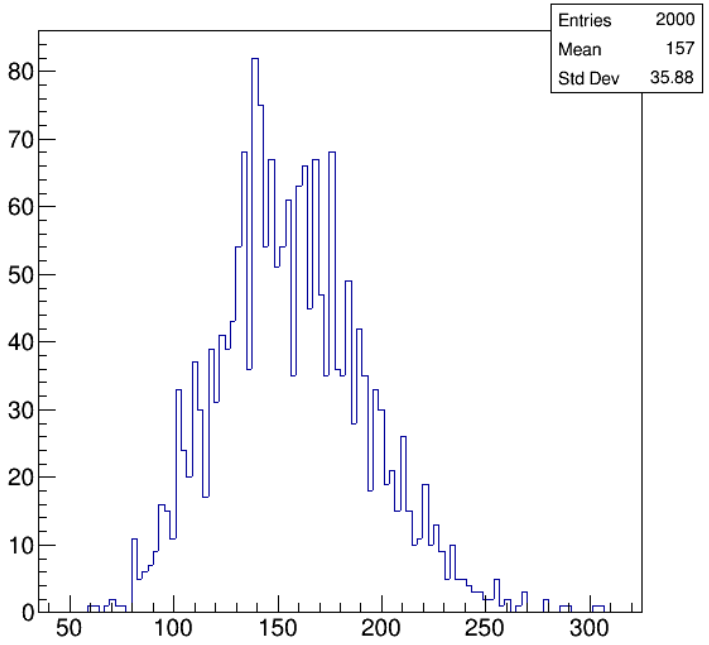
ITK

- 左：单个ZH→nn μ μ 事例
- 中：单个束流本底事例
- 右：束流本底Vertex hit数量分布



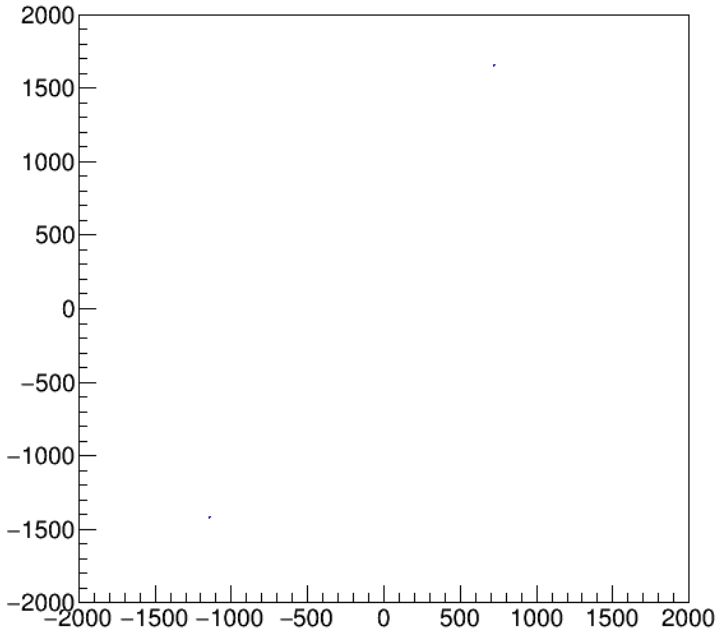


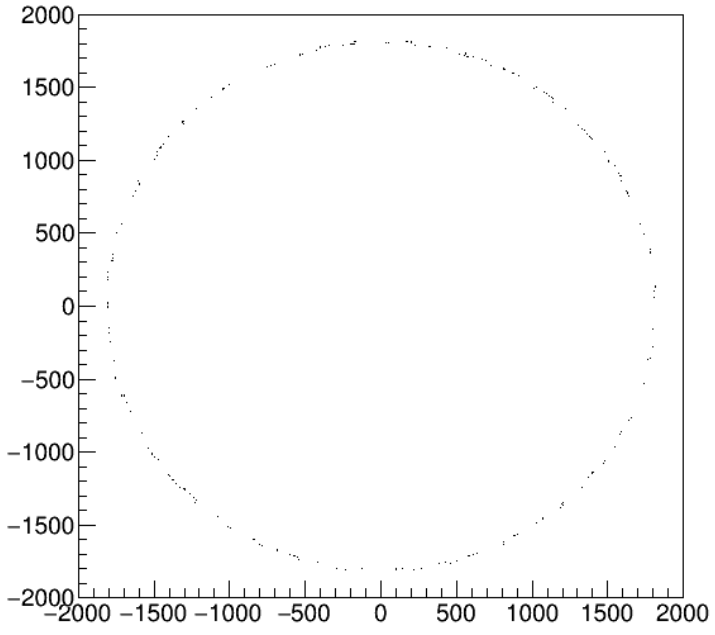


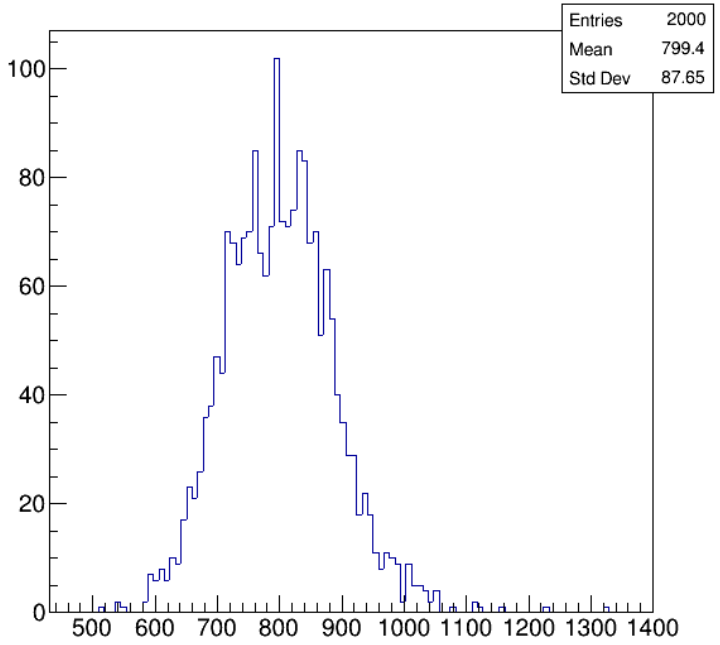


OTK

- 左：单个ZH→nnμμ事例
- 中：单个束流本底事例
- 右：束流本底Vertex hit数量分布







TPC

- 左：单个ZH→nn μ μ 事例
- 中：单个束流本底事例
- 右：束流本底Vertex hit数量分布