UT commissioning and performance

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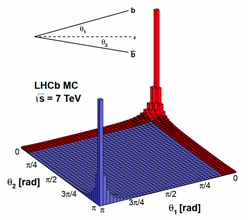
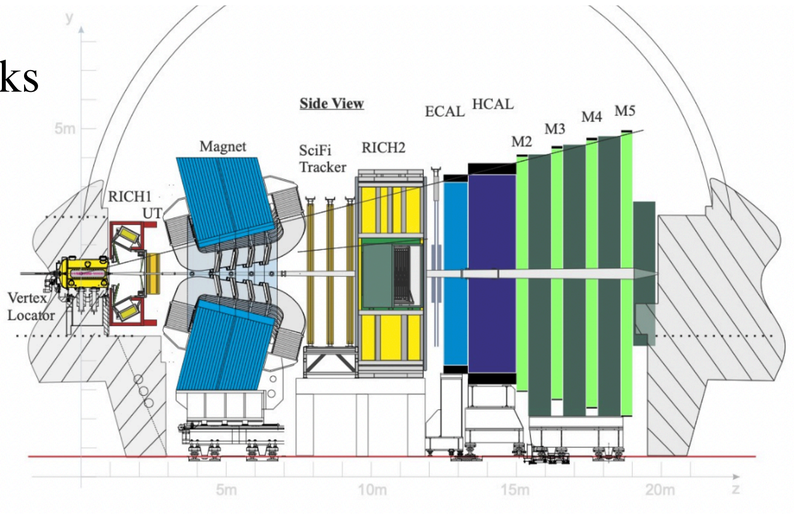
13-17, November, Qingdao

LHCb Detector

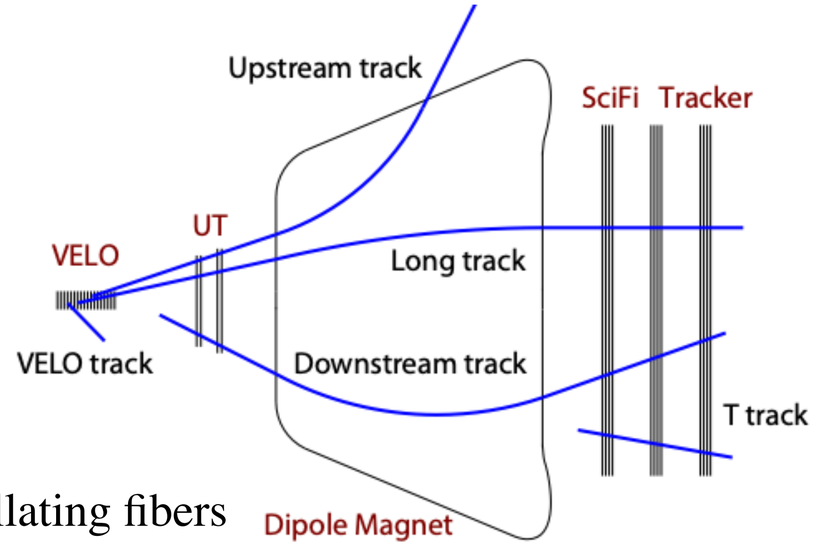
- Single arm forward spectrometer ($2<\eta<5$)
  - Designed to study CP violation and rare decays in hadrons containing b- and c-quarks





- LHCb data-taking phases
  - Run1(2010 - 2012) and Run2 (2015 - 2018)
    - Running with luminosity leveling at $4 \times 10^{32} cm^{-2} s^{-1}$
    - Total of $9\, fb^{-1}$ (3+6) collected
  - **Run3 (2023 -) — LHCb Upgrade**
    - Luminosity increased by a factor of 5 → $\mathscr{L} = 2 \times 10^{33} cm^{-2} s^{-1}$
    - Software-only trigger to 40 MHz readout
    - Sub-detector upgrade

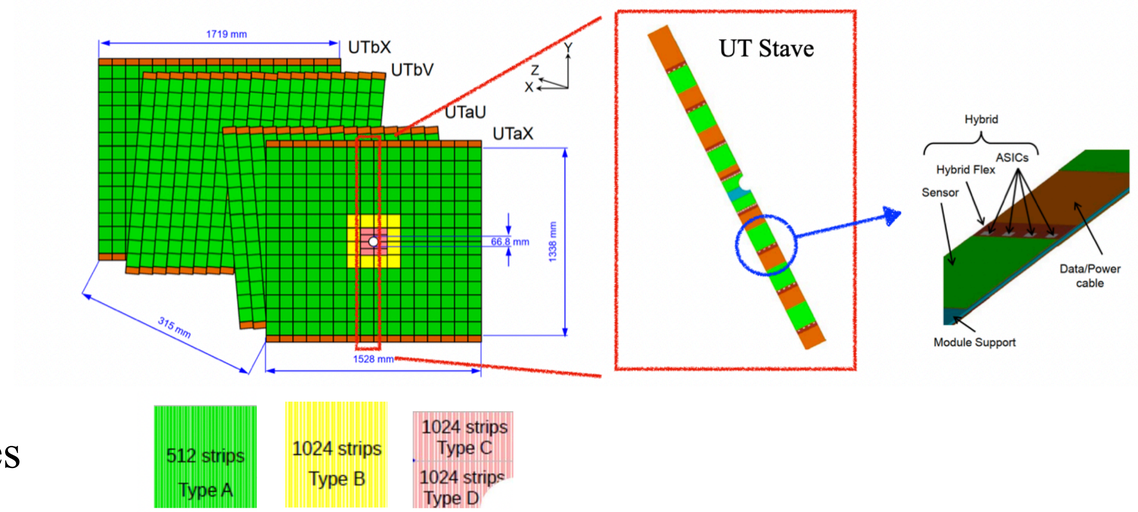
- LHCb Tracking System (all sub-detector upgraded after LS2)
  - Vertex Locator (Velo): Silicon strips → Silicon pixel
  - Upstream Tracker (UT): Silicon strips (Tracker Turicensis, TT) → Silicon strips
  - Scintillating Fiber Tracker (SciFi): Silicon strips + straw tubes (IT + OT) → Scintillating fibers



UT Detector

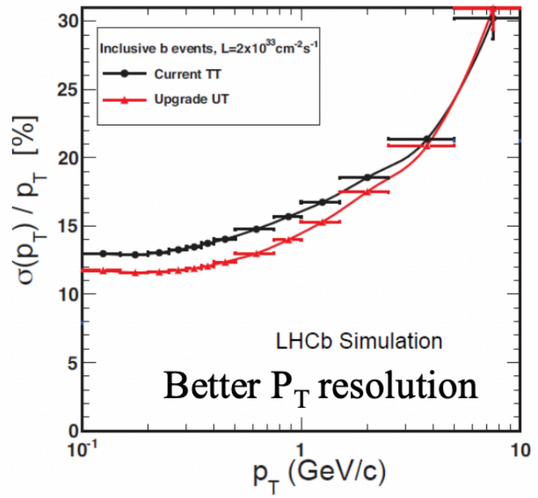
The Upstream Tracker (UT)

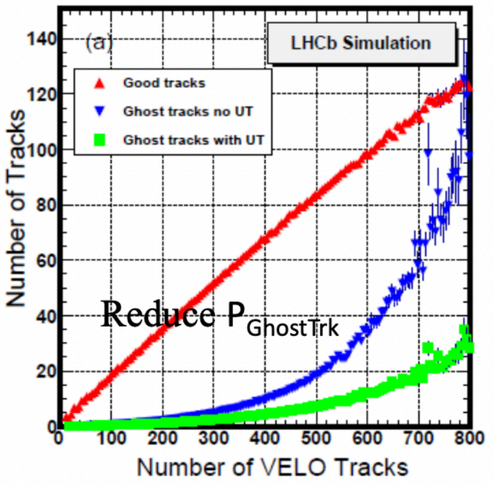
- Replace TT, located upstream of the LHCb bending magnet
- Silicon strip detector with four layers
  - 4 types of modules with different silicon strip densities
  - 4192 ASICs of 128 channels each, with a total of 536,576 strips
- Full angular coverage
- Higher segmentation sensors in the region surrounding the beam pipes
- 40MHz readout with SALT (Silicon ASIC for LHCb Tracker) chip



An important component of LHCb track system

- Provide fast estimates of momentum in the software trigger
- Improve momentum resolution
- Reduce ghost rate in long tracks
- Increase reconstruction efficiency of long lived particles

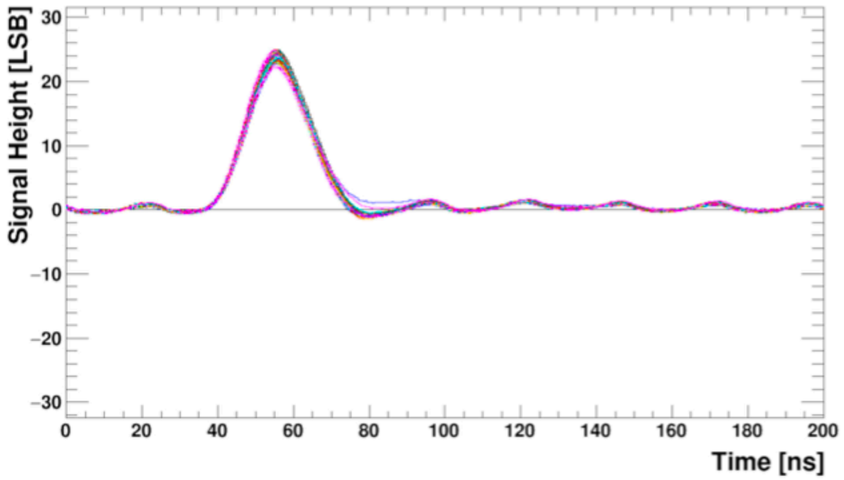




SALT chip and UT commissioning

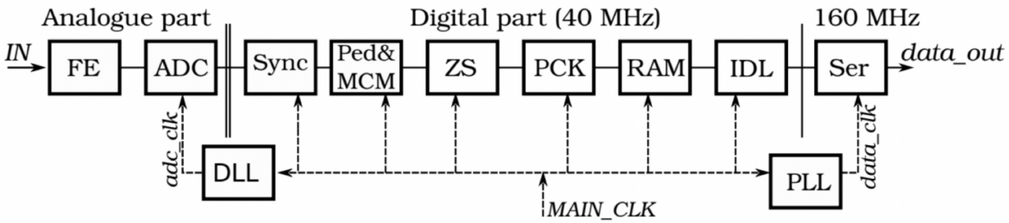
UT front-end readout, SALT (Silicon ASIC for LHCb Tracker)

- 128 Channels with 6-bit ADC, 40MHz readout
- CMOS 130nm technology
- Fast shaping time: Tpeak < 25ns
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression



UT Commissioning

- UT was the last detector to be installed in the LHCb, leaving very limited time for commissioning
  - Tune Delay-Locked Loop (DLL) / Phase-Locked Loops (PLL)
  - TrimDAC scan
  - Pedestals and Mean Common Mode (MCM) thresholds subtraction
  - Tune Zero Suppression (ZS) threshold
  - Pulse-shape scan
  - Time alignment



UT Calibration steps:

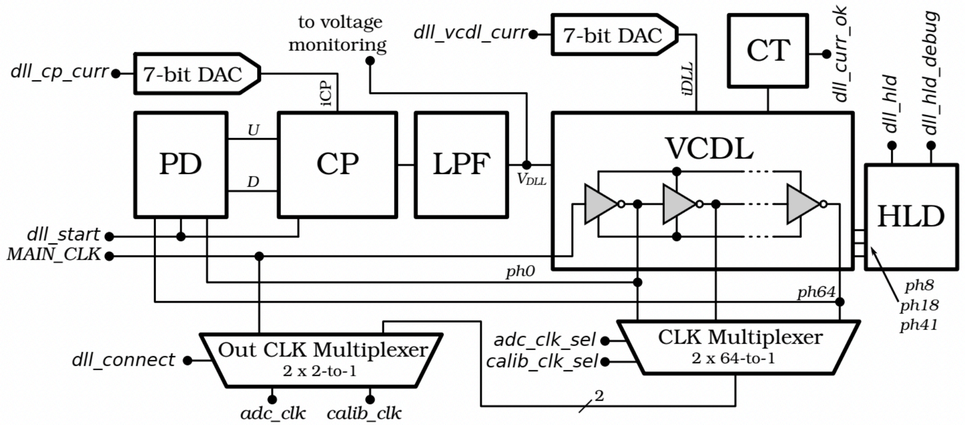
Tune DLL/PLL, Scan serializer delay, Tune e-link phase on GBTx, Tune ADC, Tune deserializer, TrimDAC scan, Pedestals, Tune ZS threshold, Tune MCM thresholds, Pulse-shape scan, Gain scan, Run DAQ with random triggers @ 30MHz

Tune DLL

Details for Tune DLL/PLL can be found in Mark Tobin's talk

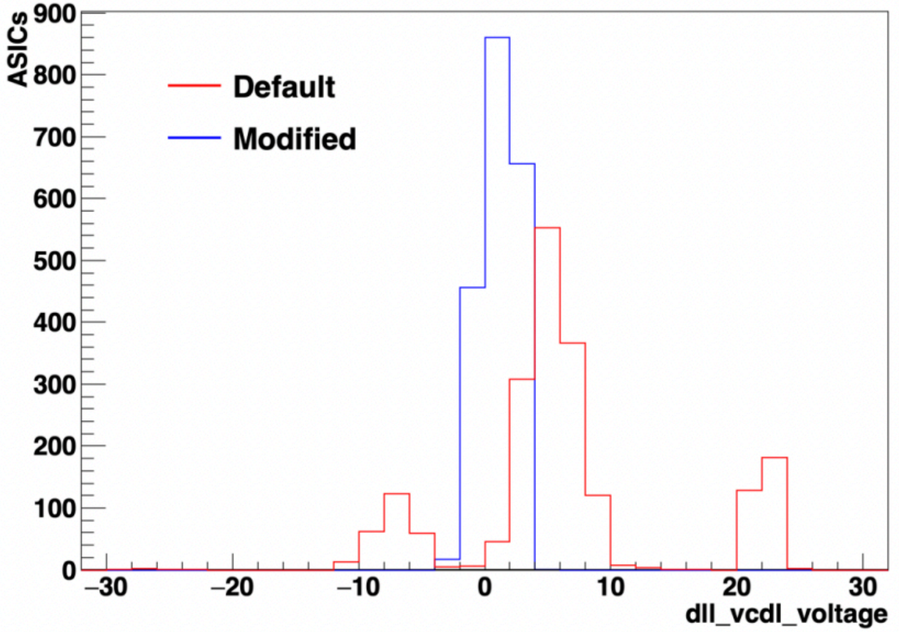
DLL in SALT

- Input frequency 40 MHz
- Provide 64 independent clock phases selection



Tune DLL

- The dll_vcdl_voltage means the difference between V_{DLL} and $V_{vdd/2}$
  - **Best setting when dll_vcdl_voltage around 0**
- The dll_vcdl_cfg register sets the Voltage Controlled Delay Line (VCDL) bias current
- Adjust dll_vcdl_cfg since the default settings are not optimal

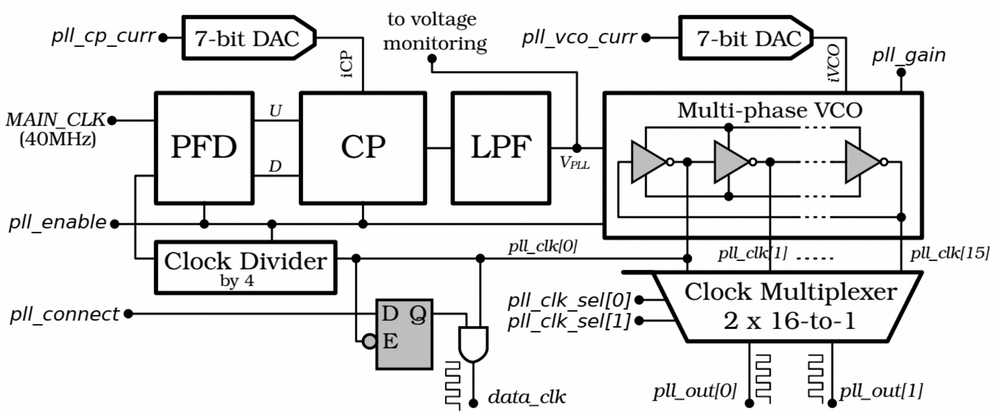


Tune PLL

Details for Tune DLL/PLL can be found in Mark Tobin's talk

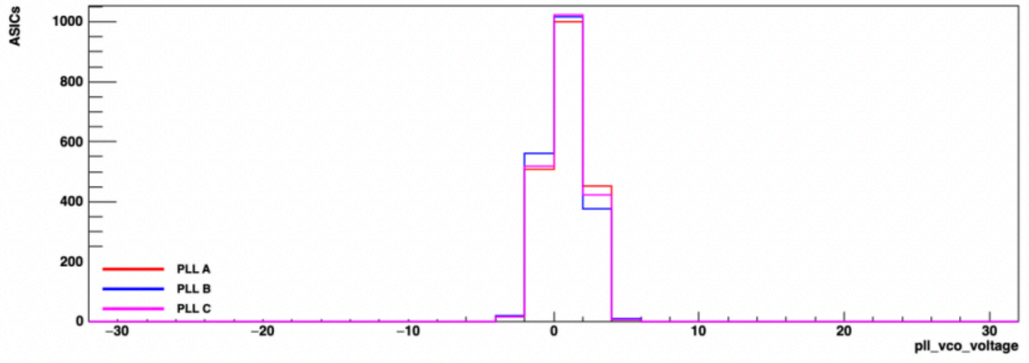
PLL in SALT

- Input frequency 40 MHz
- Generates a stable high-frequency (160 MHz) clock signal for the Double Data Rate (DDR) serializer
- Triple Modular redundancy (TMR) design enhances reliability against Single Event Upsets (SEUs) — **Three PLLs in the SALT**



Tune PLL

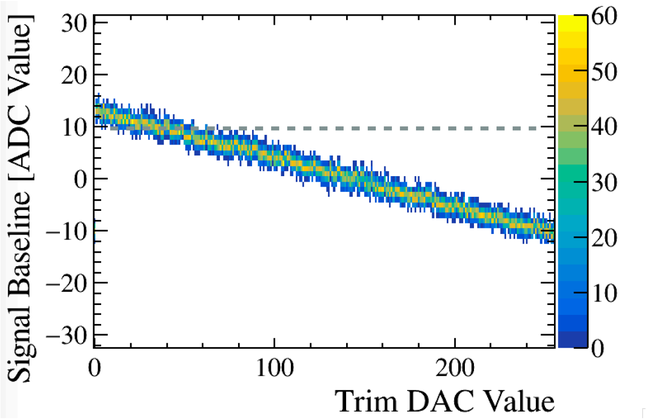
- Check the Voltage Controlled Oscillator (VCO) for all three PLLs
- The pll_vco_voltage means the difference between V_{PLL} and $V_{vdd/2}$
  - **Best setting when pll_vco_voltage in all three PLLs are around 0**
- The pll_vco_cfg register allows to change the VCO bias current which is directly related to the output frequency



TrimDAC scan

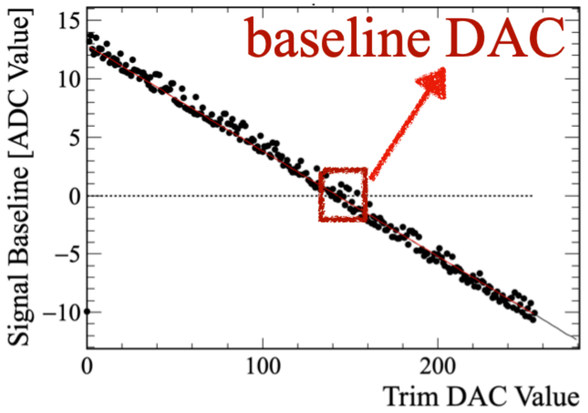
Each ASIC channel contains an 8-bit trimming DAC for a precise baseline setting

- Scan the TrimDAC from 0-255 with step of 1. Each step took 100 events
  - the ADC value = 0 → Baseline DAC

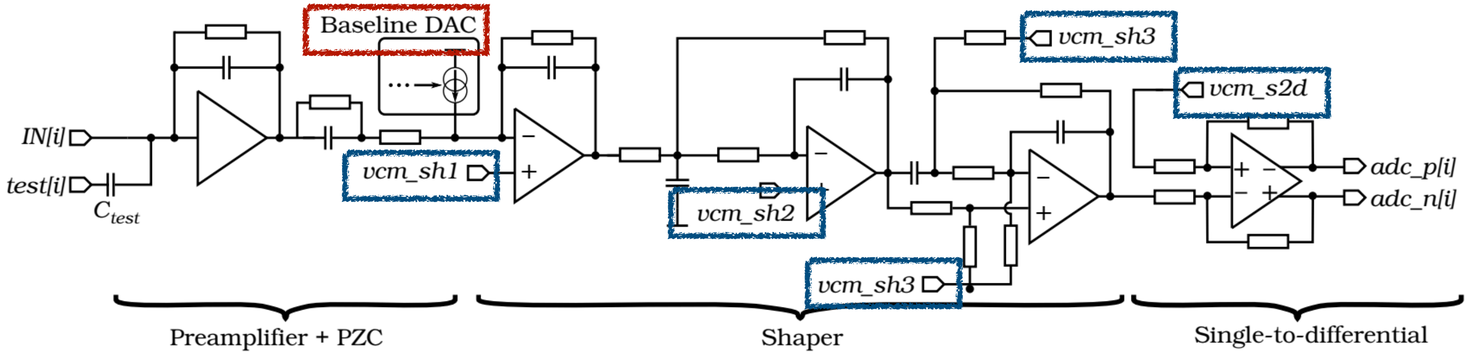


Each ASIC contains 6-bit DAC setting the I_{vcm} for generation of common voltages

- The single common mode voltage setting couldn't cover all cases, TrimDAC scans at 4 different common mode voltages allow almost all channels to be compensated



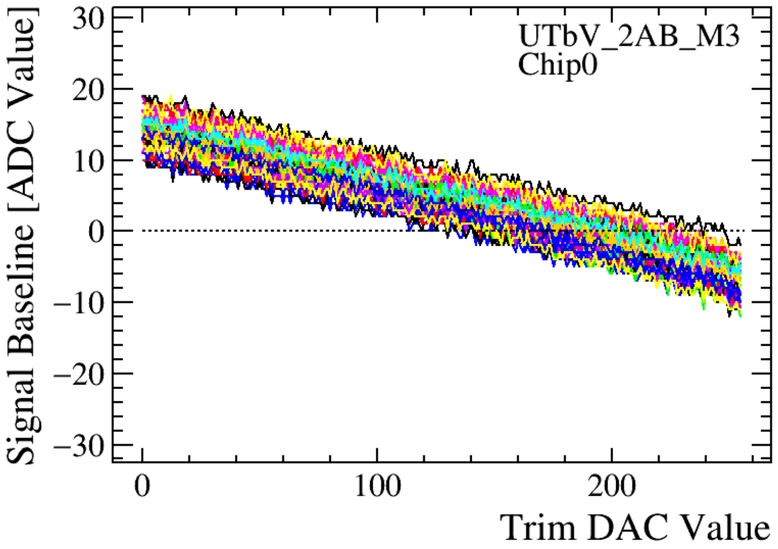
8-bit trimming DAC



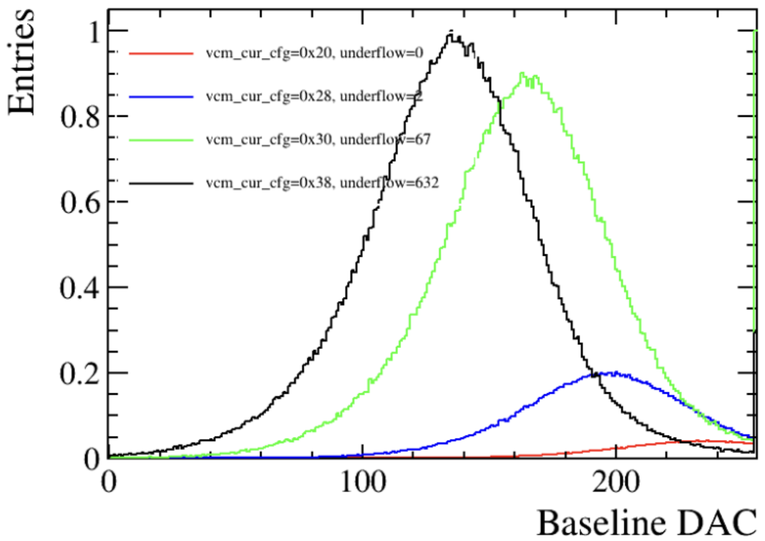
6-bit DAC setting the reference current I_{vcm}

TrimDAC scan

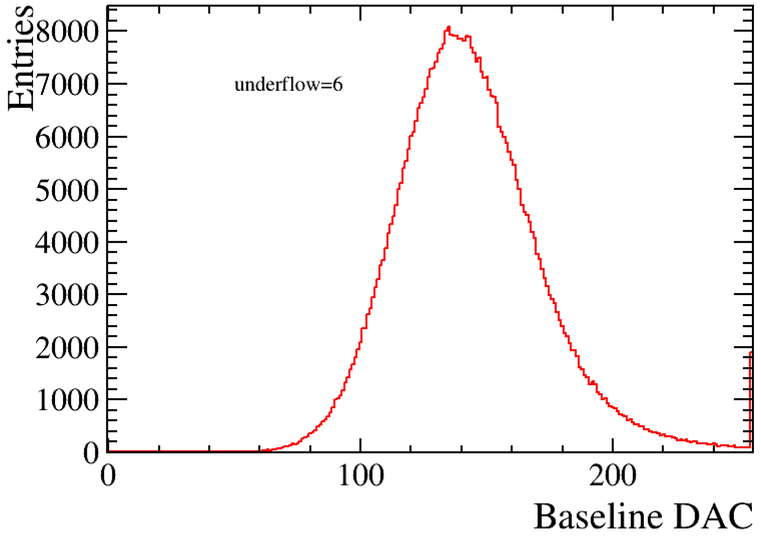
TrimDAC scan for UTbV_2AB_M3 chip0



TrimDAC scan with 4 common mode voltage settings



Final resulte



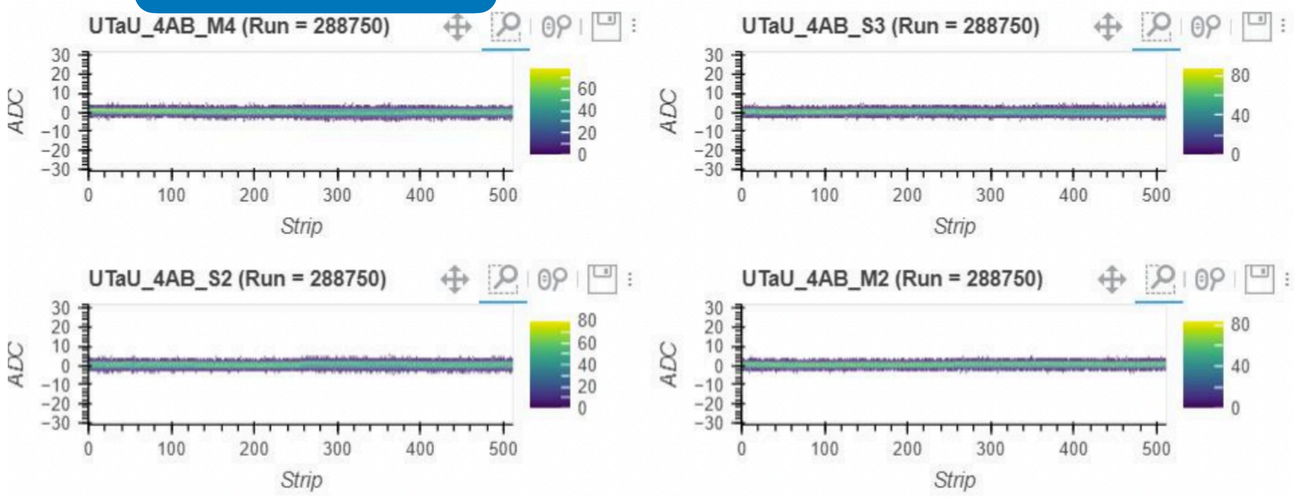
99.97% channels work properly at the TrimDAC scan stage!

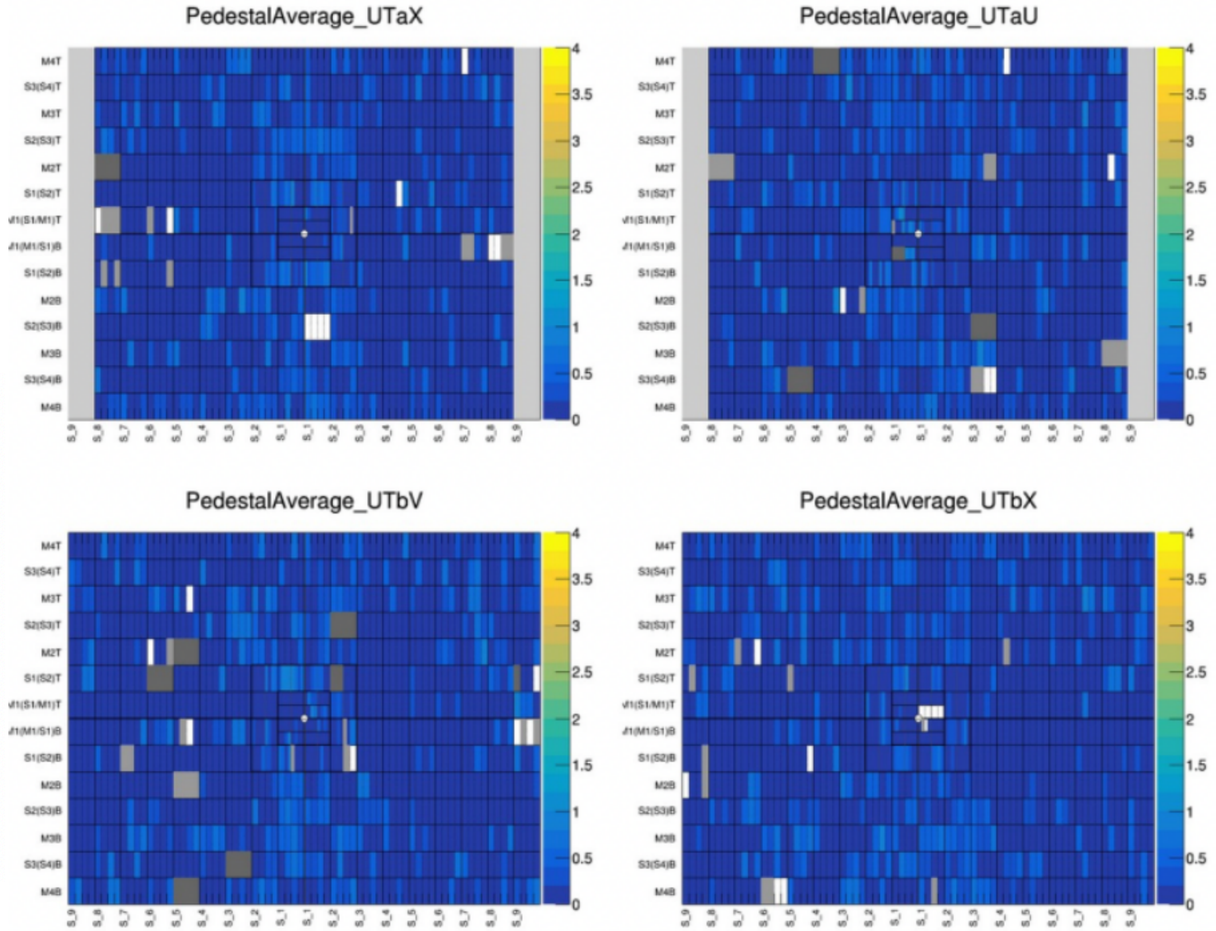
Pedestals subtraction

Details for Pedestals subtraction can be found in Wojciech Krupa's talk

- Performed after TrimDAC scans
- After TrimDAC calibration the pedestal values close to 0
- Subtraction in each channel

Raw ADC per channel

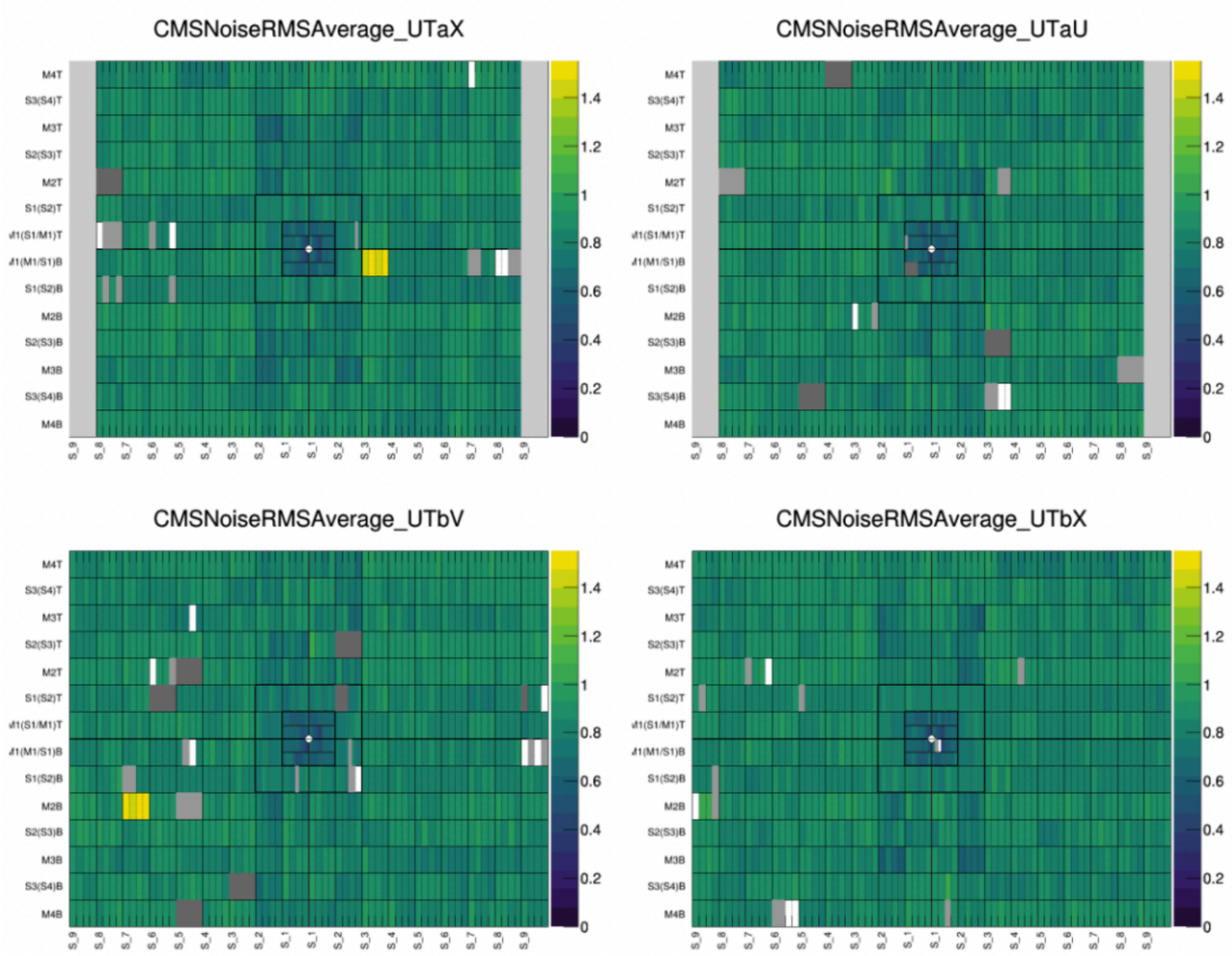




MCM thresholds subtraction

Details for Tune MCMS can be found in Wojciech Krupa's talk

- Calculate an average value of all channels without a hit and subtract this value from all channels
- MCMS run (after pedestal subtraction and MCMS in the chip)
- Very uniform distribution of CMS noise

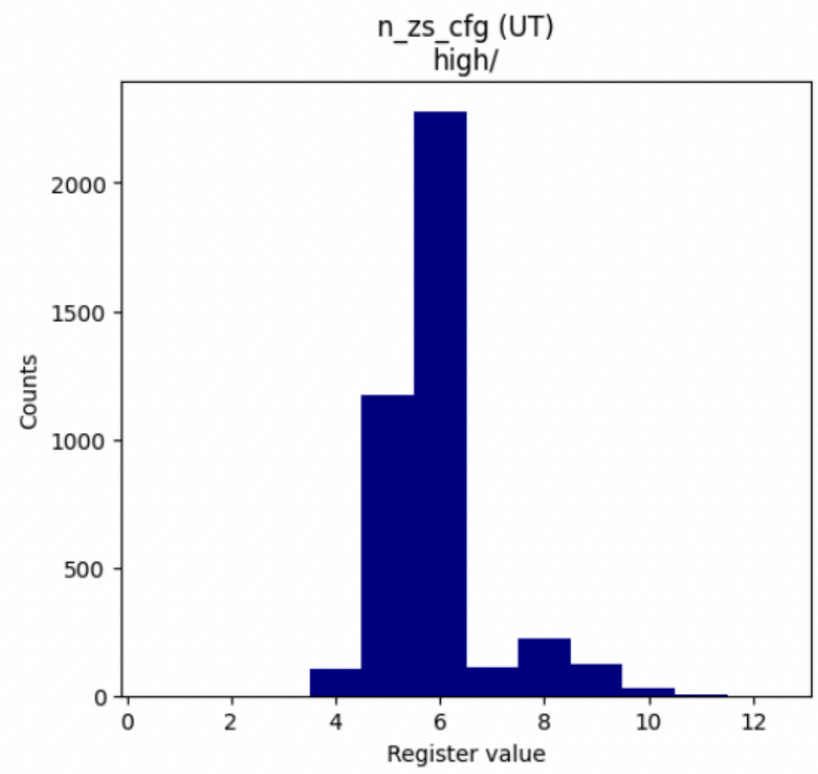


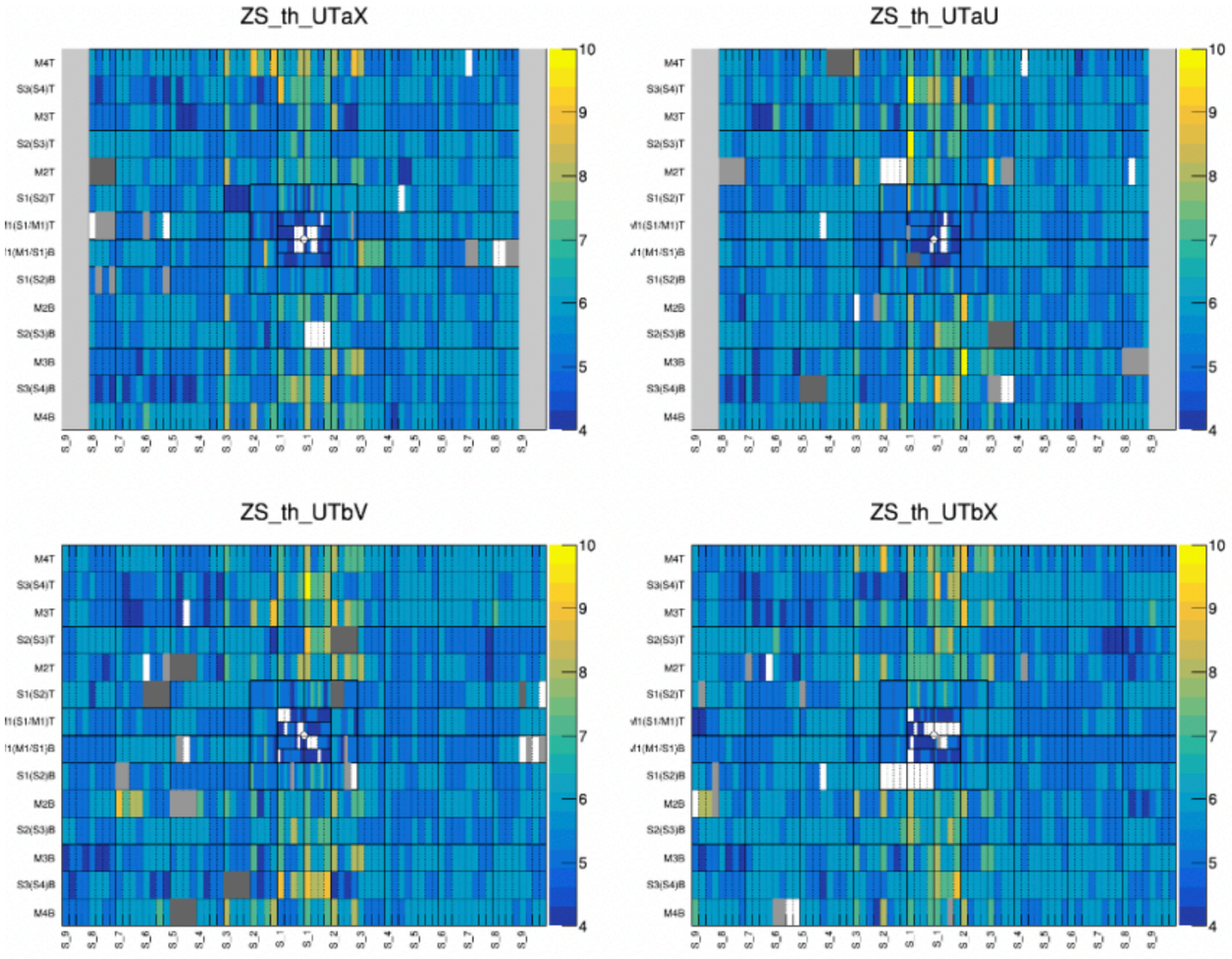
Tune ZS threshold

Details for Tune ZS threshold can be found in Wojciech Krupa's talk

Calculation of ZS thresholds based on CMS-noise

$$z_{s_{th}} = \begin{cases} 5 \cdot \sigma_{ADC}(\text{mcms}) \\ 5 \cdot \sigma_{ADC}(\text{mcms}) + \max(\mu_{ADC}(\text{mcms})) \end{cases} \quad \text{if } \max(\mu_{ADC}(\text{mcms})) = 0{,}1$$





Pulse scan

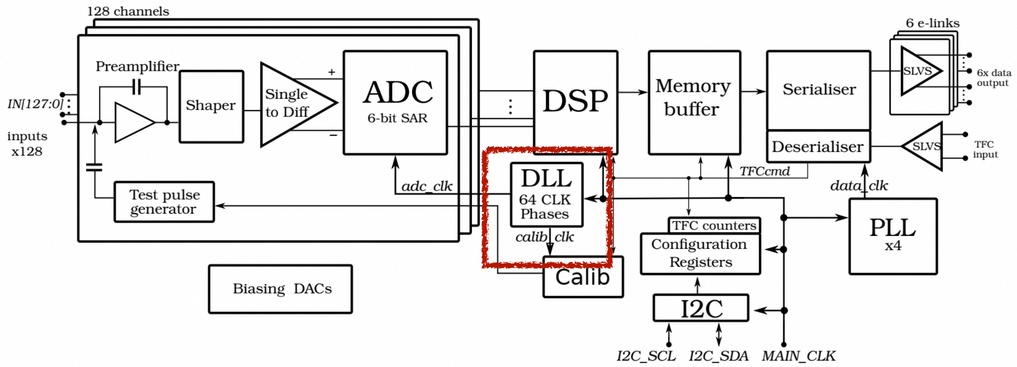
Using test pulse to check the whole processing chain in the SALT chip

SALT contains a dedicated internal DLL block to provide 64 independent clock phases selection

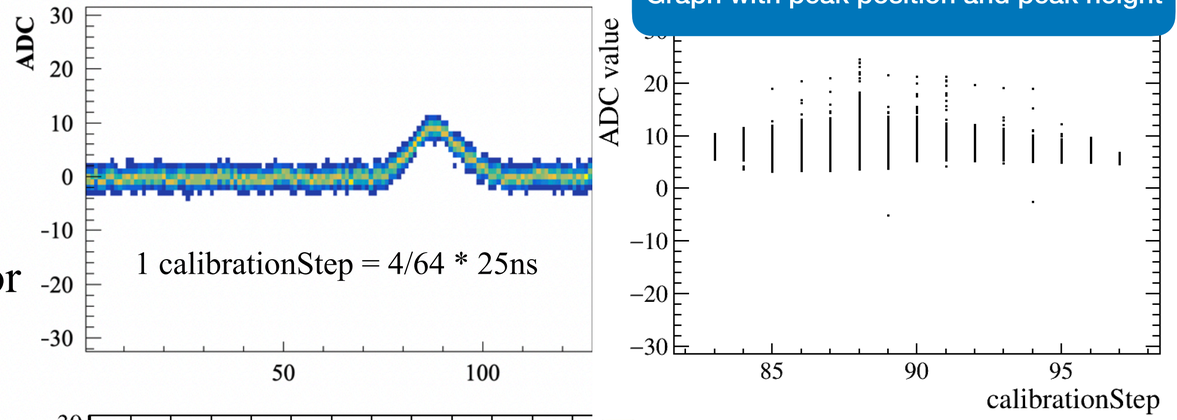
- We generate test pulse and take data with different clock phase (**adc_clk_sel**)

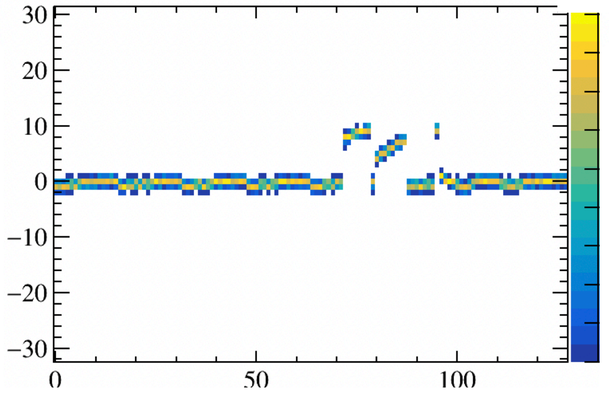
Most of ASICs have the correct pulse shape

- 32 (4192 in total) ASICs need to recorrect adc_sync_sel bit setting for different DLL delays



Graph with peak position and peak height





adc_clk_sel	*adc_sync_sel*	time shift [ns]
0 – 7	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64} + 25$
8 – 39	0 (rising edge)	$adc\_clk\_sel \cdot \frac{25}{64}$
40 – 63	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64}$

Default setting

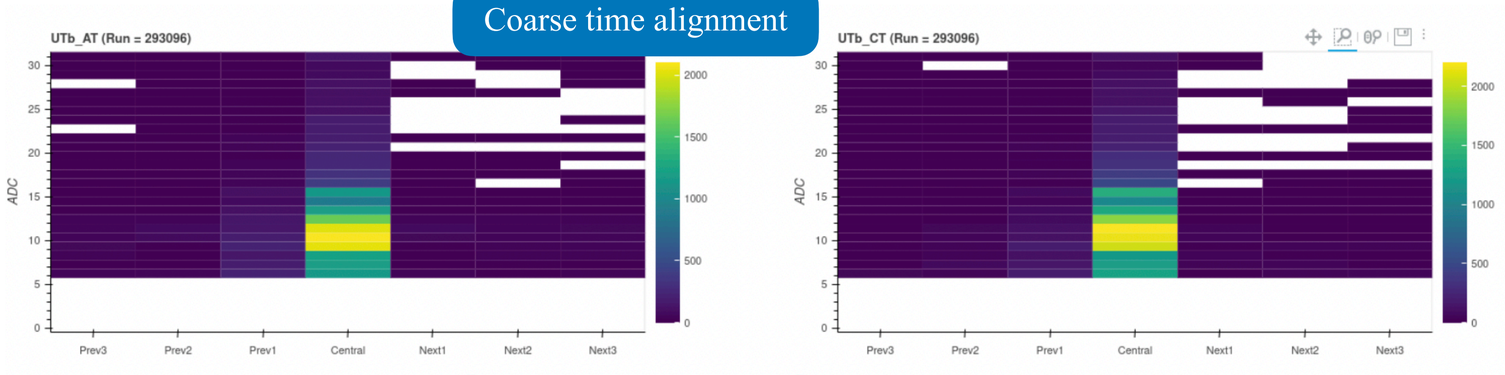
Time alignment

Details for UT fine time alignment can be found in Christos Hadjivasiliou's talk

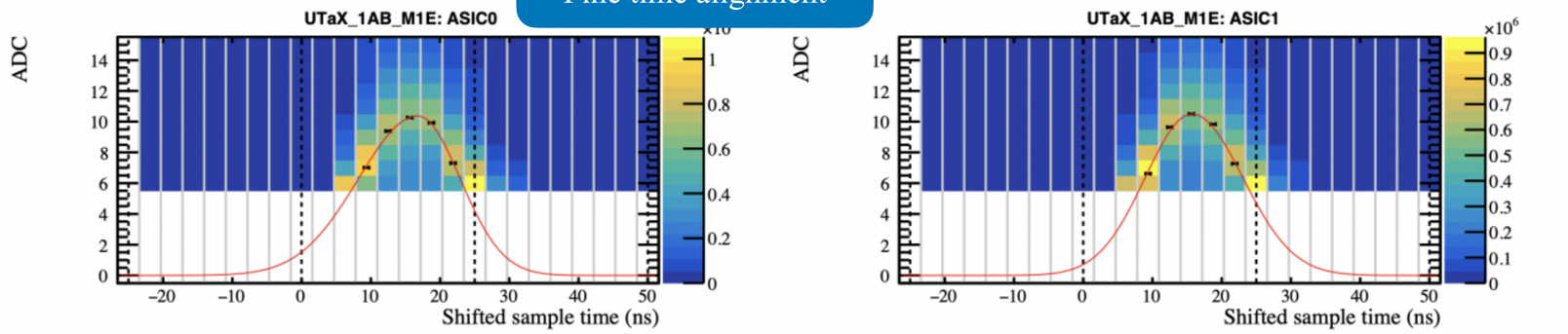
Time alignment was done using the TAE events produced by the LHC during its 2024 luminosity ramp-up

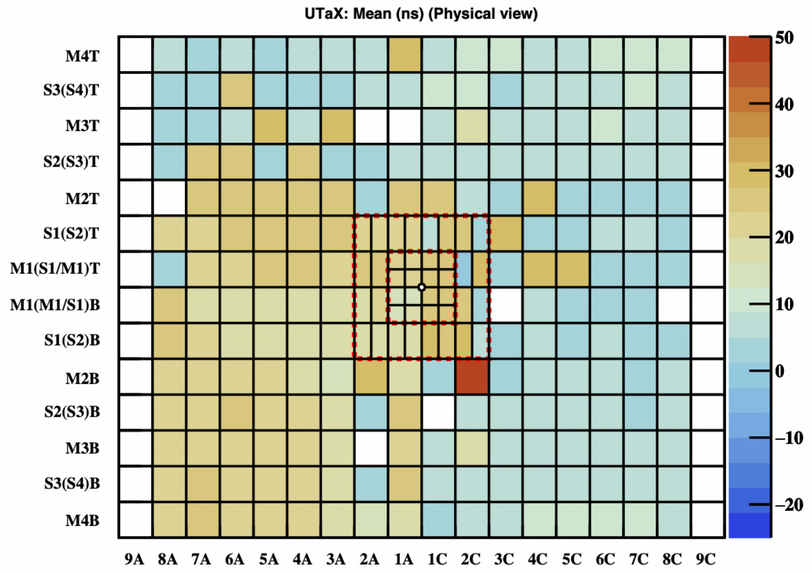
- **Coarse time alignment**
  - Done per DCB (Data Control Boards), it makes sure that all ASICs correctly identify a bunch crossing with its corresponding bunch crossing ID within the LHC orbit
- **Fine time alignment**
  - Done per module, done by scanning the ADC sampling phase, which adjusting the delay for each ASIC by fitting a known signal shape to the actual detector signals, resulting in precise time synchronization across the detector

Coarse time alignment



Fine time alignment





Time alignment

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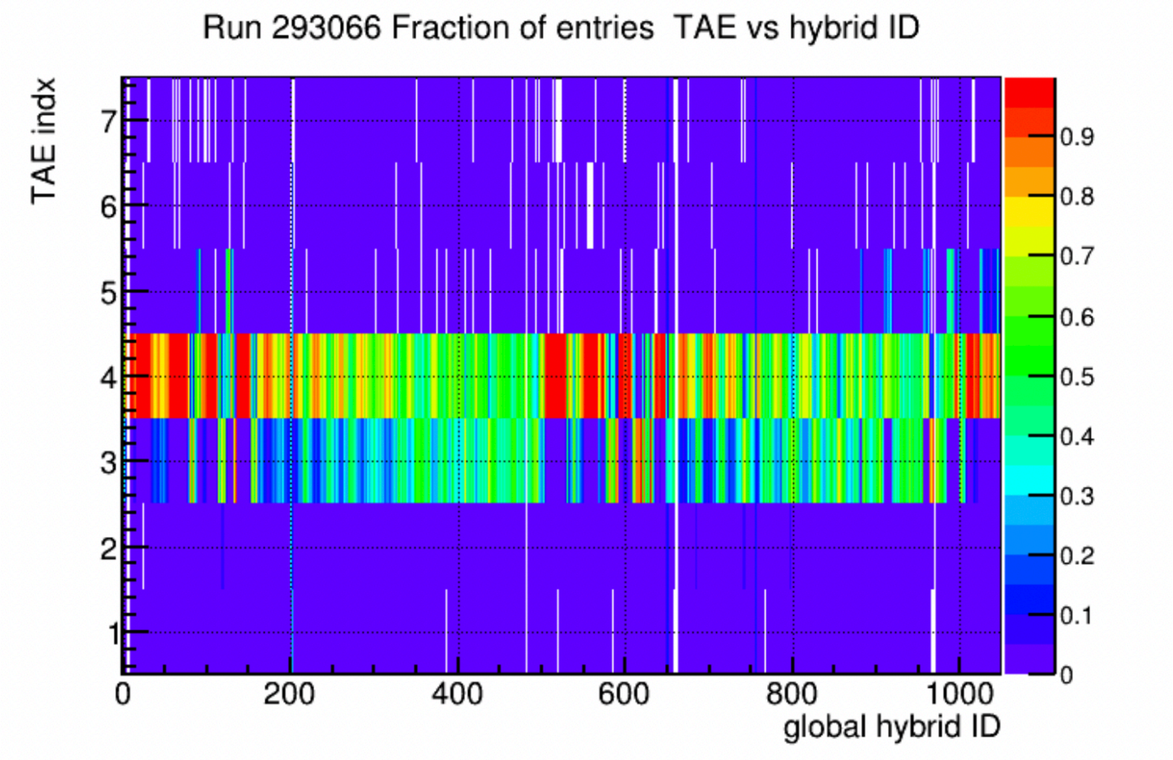
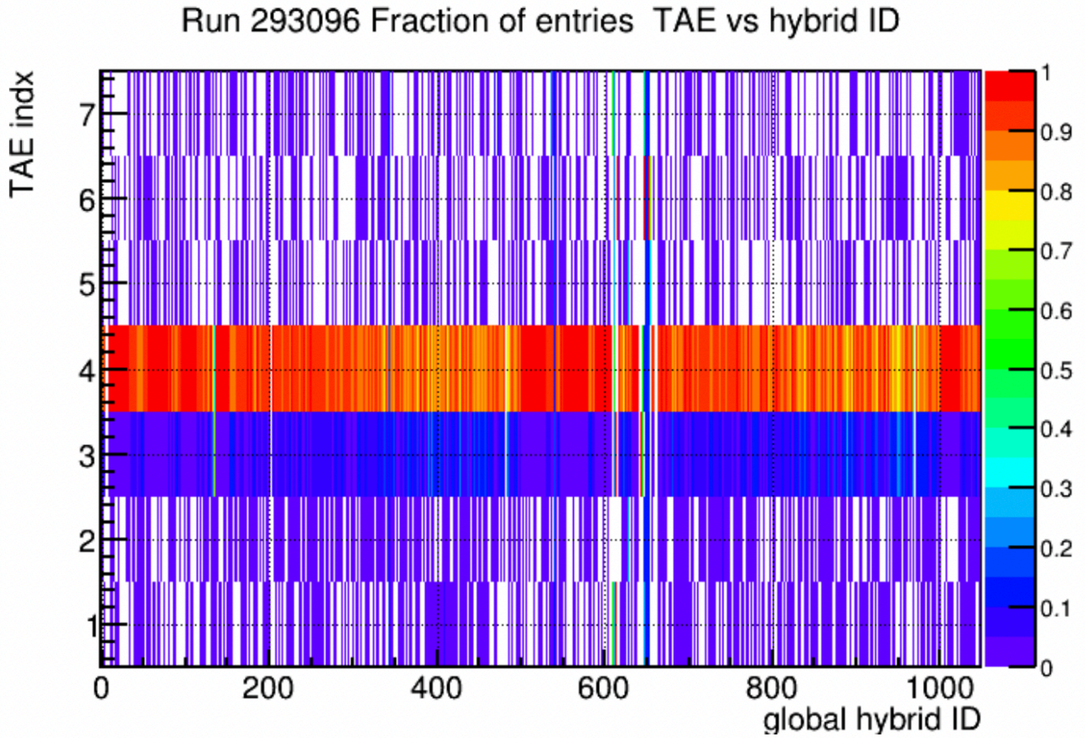


Before fine time alignment



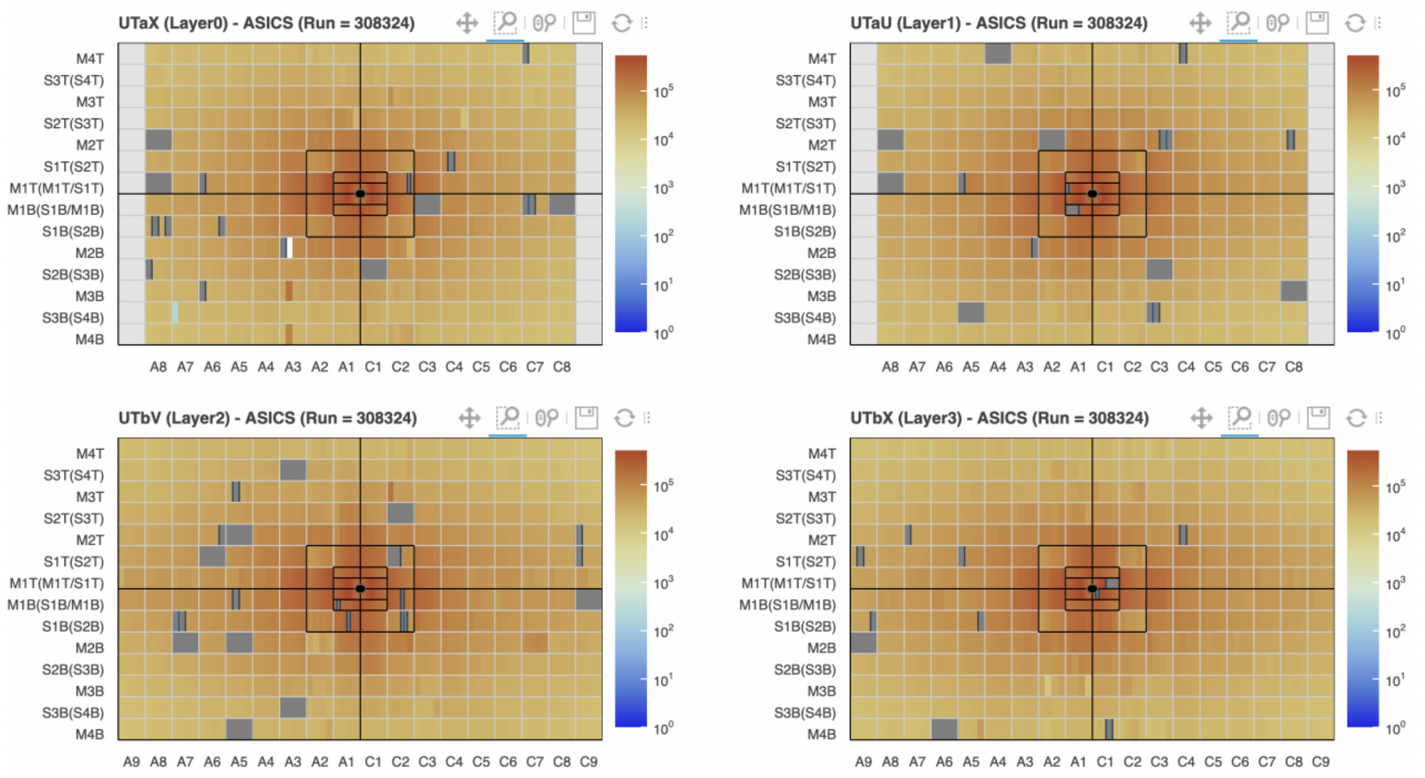
After fine time alignment

Working in global

The UT is already taking data smoothly at nominal rates with the rest of LHCb

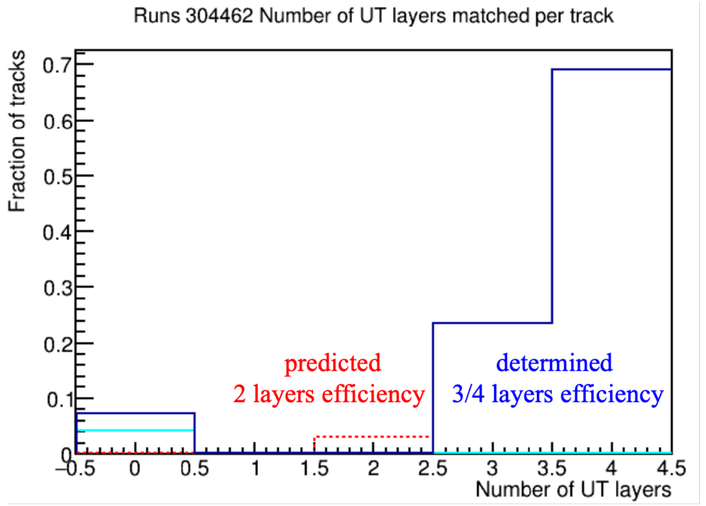
Most of the ASICs work properly, and the hit distribution is consistent with expectations!

A typical fill of proton-proton collisions at nominal luminosity



Number of hits in each UT chip

White gray: not occupied slot
Gray and dark gray: disabled



- The determined efficiency of UT layers (3+4) that match the long track ~ 96.9%
- The predicted UT layers (2+3+4) efficiency ~ 99.8%

Summary

- LHCb has completed the upgrade I and currently in the Run3 data-taking phase
  - Luminosity increased by a factor of 5
  - Software-only trigger to 40 MHz readout
  - All sub-detector of LHCb tracking system was upgraded
- The commissioning of UT has completed
  - Improve calibration of detector
  - Test detector in local and global
- The UT is already taking data smoothly with the rest of LHCb

Thank you!

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