CMOS R&D for LHCb UT in Upgrade II

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On behalf of COFFEE team

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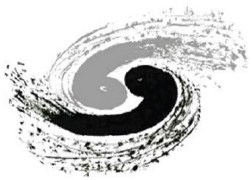
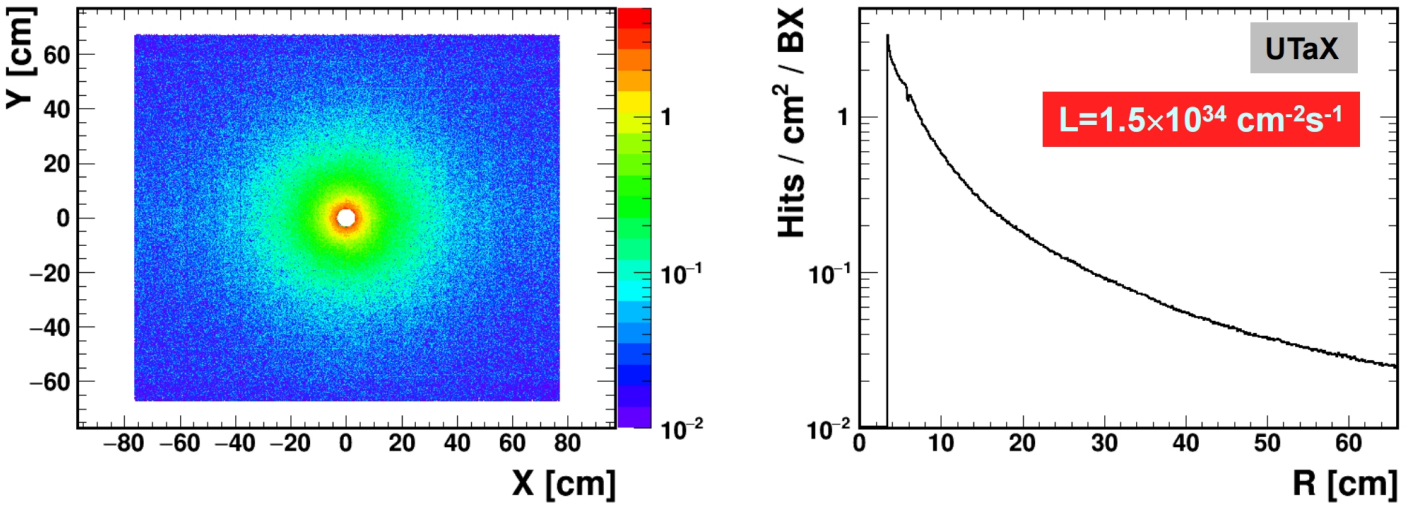
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS



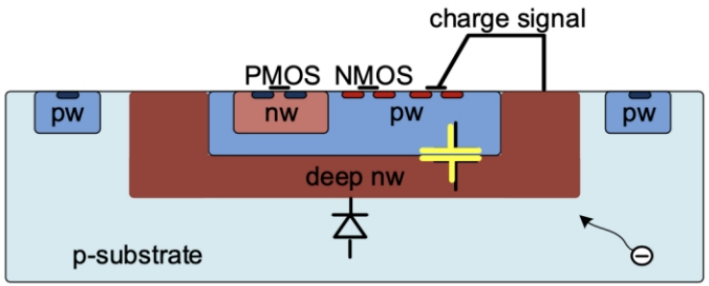
UT @ Upgrade II

- The future of LHCb, Run5, will evolve into high-luminosity. Increased multiplicity require a finer grained and more radiation-hard Tracker
- For Upstream Tracker (UT), the max hit density is at the inner-most area (5.92 Hits/cm2/BX), or 4.0 averaged over all bunch crossings
  - The occupancy (max $\sim$ 10%) will significantly comprise the performance of UT
- A new UT for the Upgrade II is mandatory: Si-strip $\rightarrow$ Si-pixel



CMOS MAPS as Possible Solutions

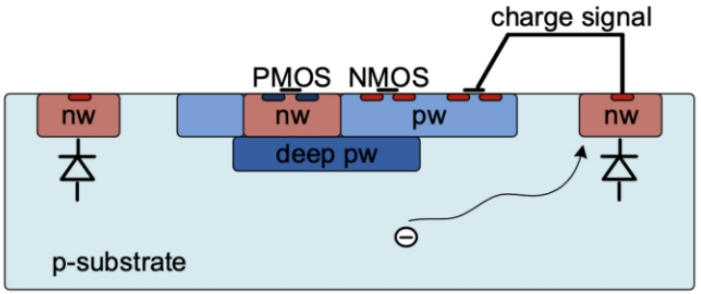
HV-CMOS



Large collection electrode

- Typical pixel size: $50 \times 100 \mu\mathrm{m}^2$
- Circuitry inside the charge collection well
- Large uniform electric field
- On average shorter drift path
- High radiation tolerance (less trapping)
- Very large sensor capacitance (both pw and dnw)

LV-CMOS

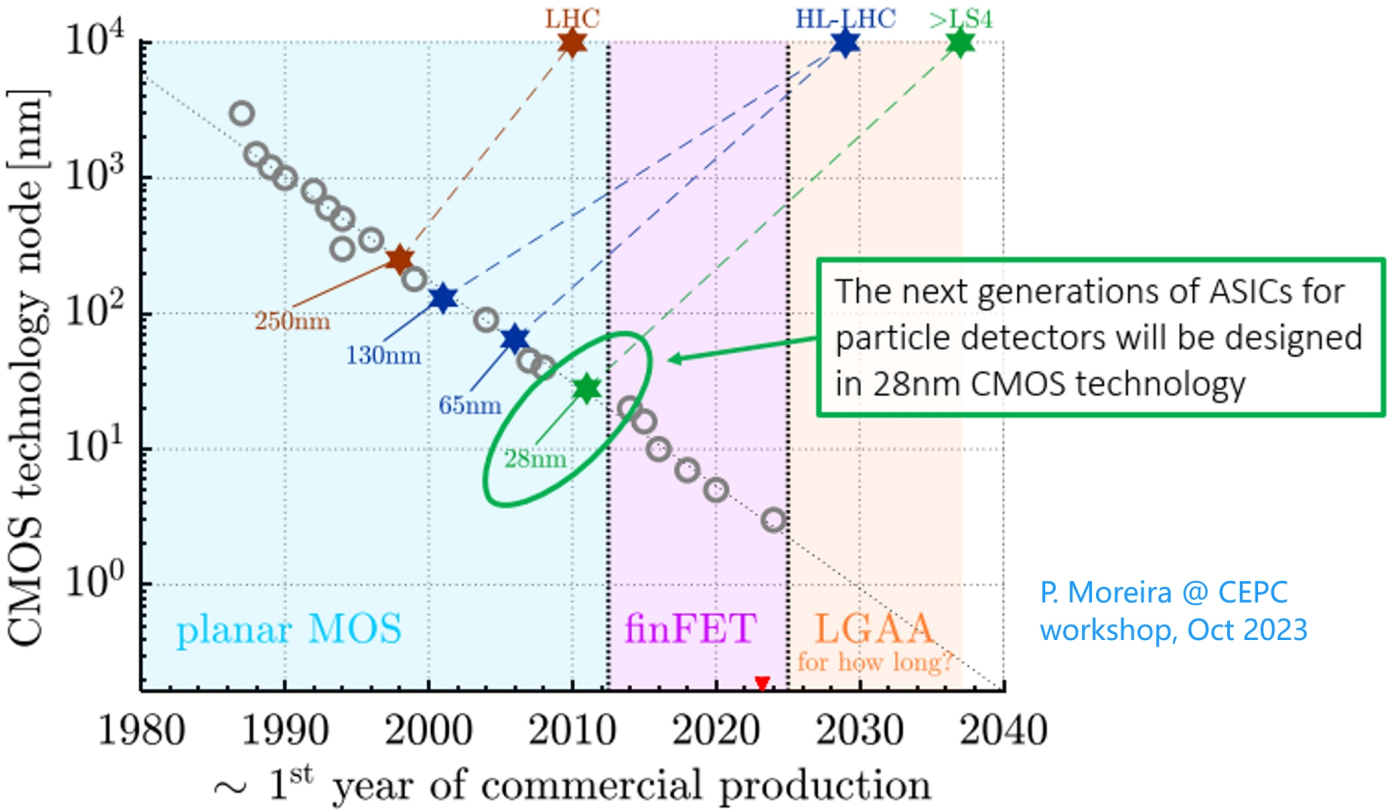


Small collection electrode

- Typical pixel size: $30 \times 30 \mu\mathrm{m}^2$
- Circuitry outside the charge collection well
- Optimization of little low-field regions
- On average longer drift path
- Radiation hardness needs process modifications
- Very small sensor capacitance

Choice of HVCMOS with 55nm process

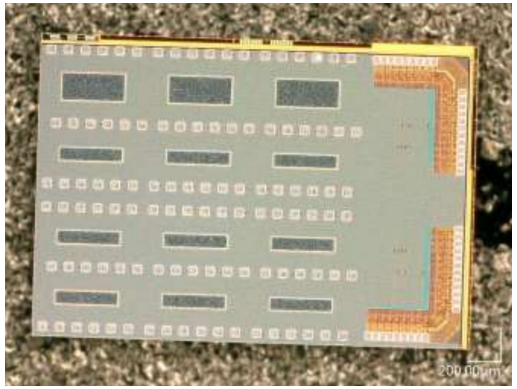
- The international mainstream technology is 180/150 nm process. HV-CMOS pixel sensor has been applied to Mu3e experiment
- Chip research and development determined with 55nm process in domestic factory
  - Safety concern: 55nm process should provide stable support for mass production in next 10 years
  - Technological benefits: lower power, higher speed, higher TID...



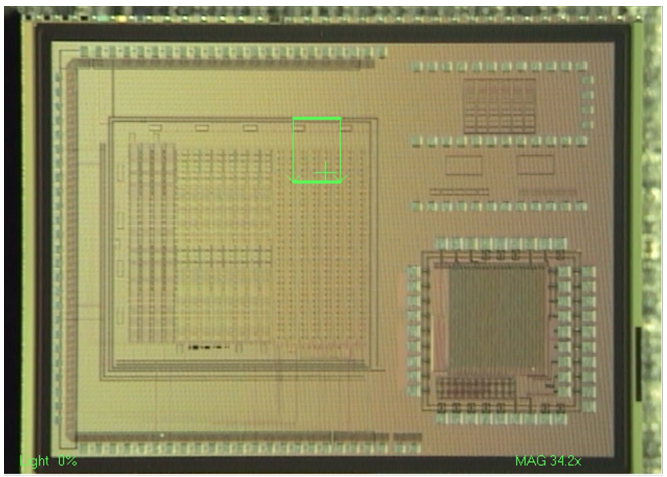
P. Moreira @ CEPC workshop, Oct 2023

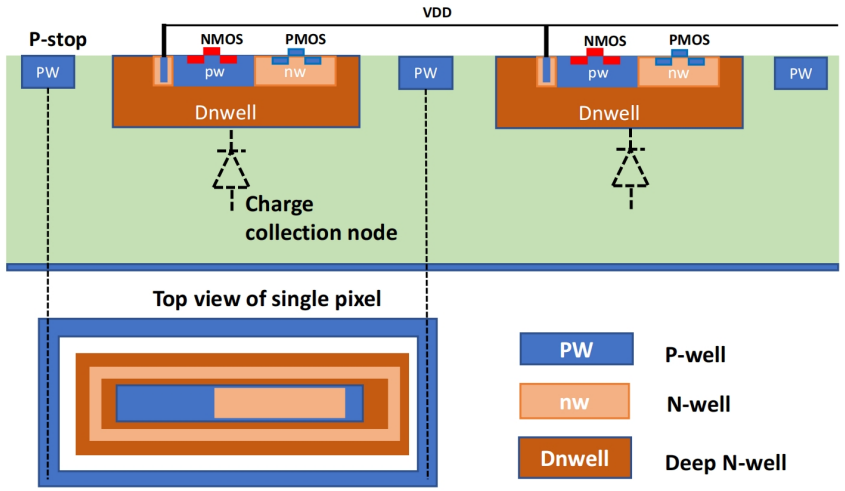
CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

- COFFEE1 chip ($3 \times 2\mathrm{mm}^2$):
  - Similar deep N well
  - pixel size: $25 \times 150\mu\mathrm{m}^2$
  - Variation of passive diode arrays
  - Simple amplifiers added



- COFFEE2 chip ($4 \times 3\mathrm{mm}^2$): (test results shown today)
  - Real validation of the sensor structures with electronics included
  - Variation of passive diode arrays
  - Integral analog amplifier and switch circuit to select certain pixel
  - Discriminator and DAC unit added

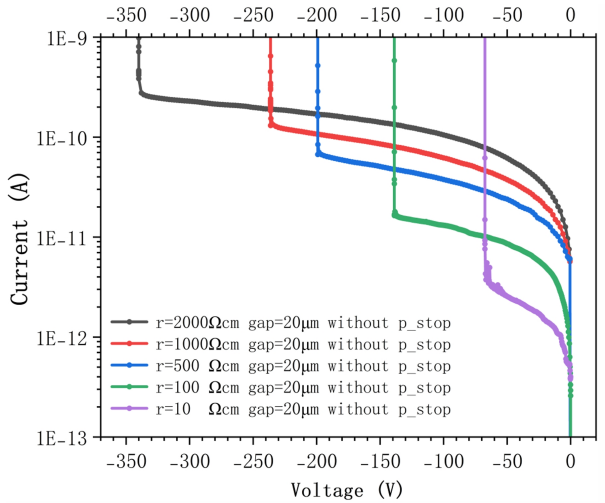


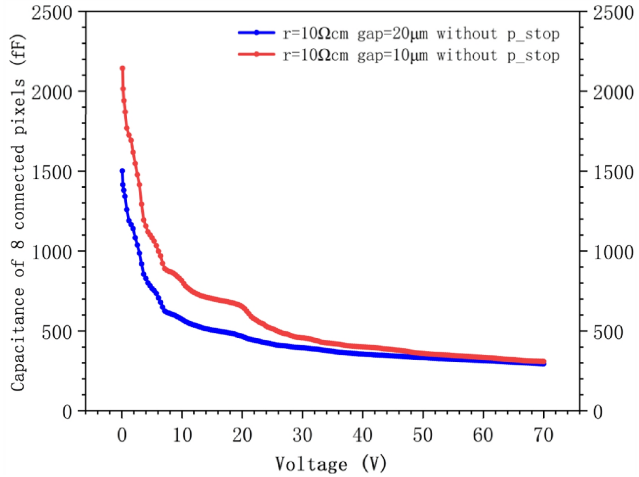


NIMA Volume 1069 P169905 (2024)

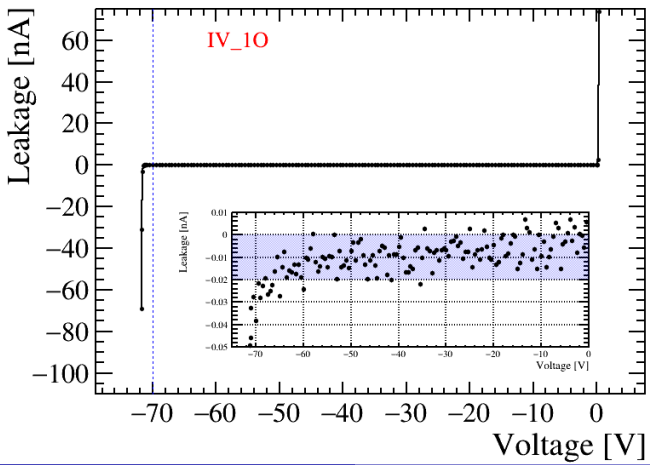
Typical IV/CV, simulation v.s. test

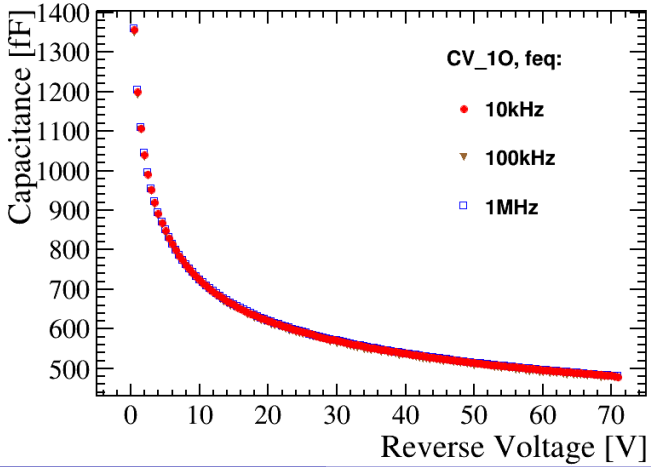
- TCAD simulation results are confirmed through testing
- Current substrate resistivity ($10\Omega \cdot \mathrm{cm}$) limits the break down voltage





- Breakdown voltage $>$ 70V, leakage $\sim$ 10pA (mainly edge breakdown)
- At 70V, the capacitance of single pixel due to depletion $\sim 30 - 50\mathrm{fF}$

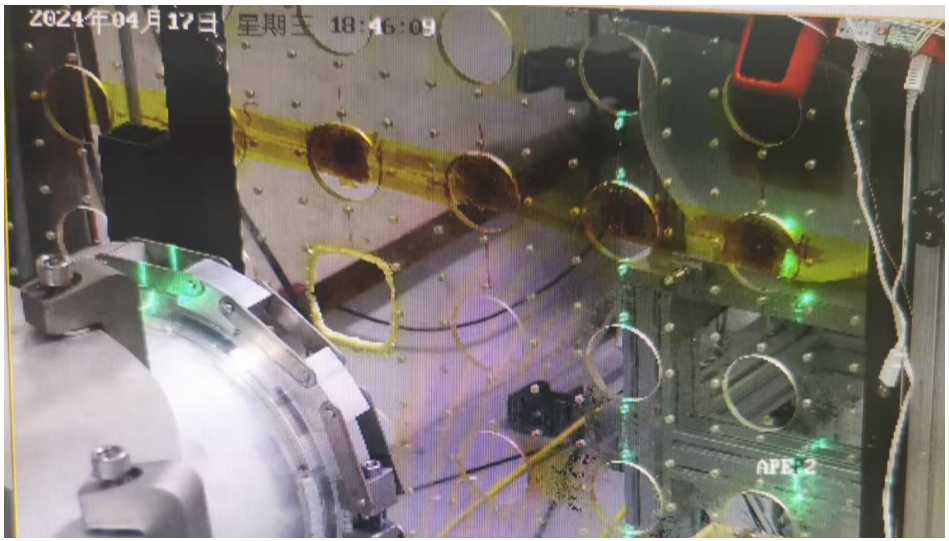


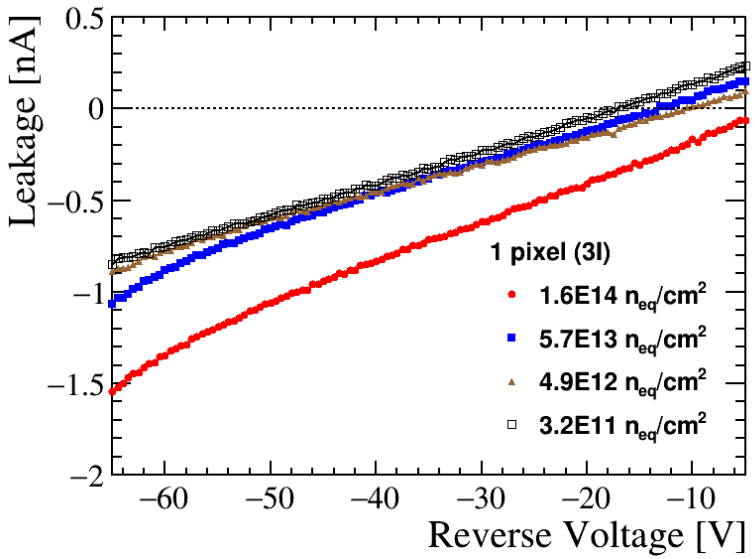


Irradiated leakage change

- Tested with proton beam @80MeV in Spallation Neutron Source
- 4 gradient doses were irradiated at room temperature
- Magnitude of leakage current proportional to the irradiation dose

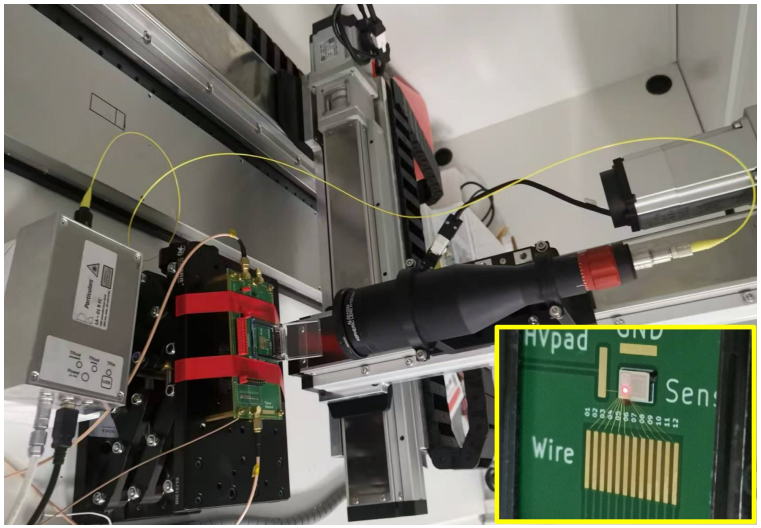
Dose $[\mathrm{n_{eq}/cm^2}]$	3.2×10^{11}	4.9×10^{12}	5.7×10^{13}	1.6×10^{14}
Leakage I [nA]	0.57	0.59	0.65	1.06

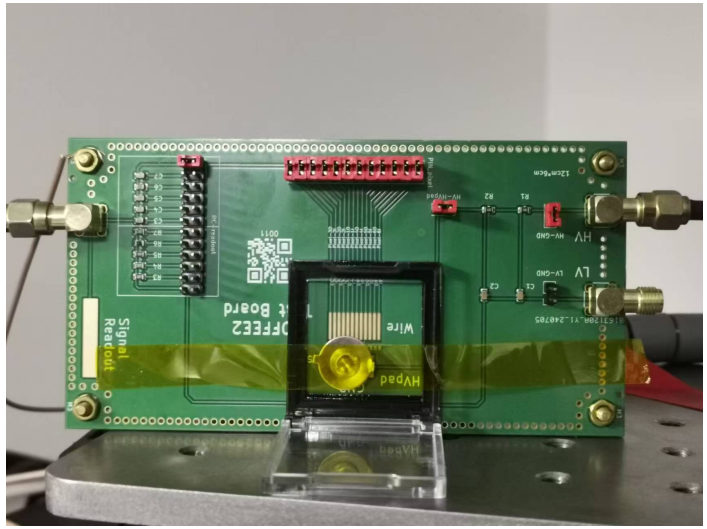


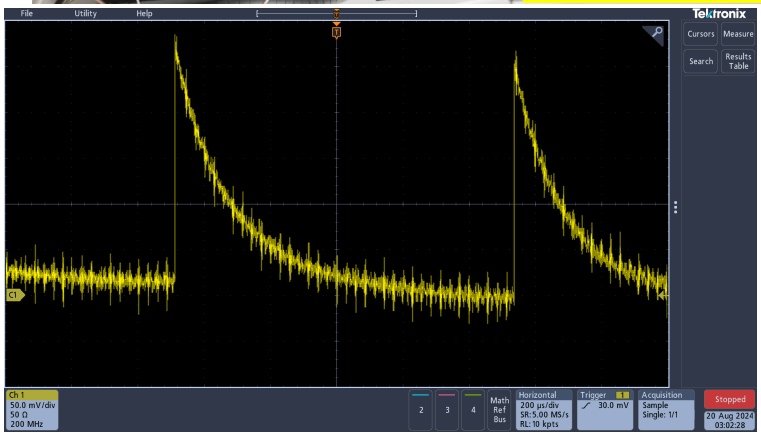


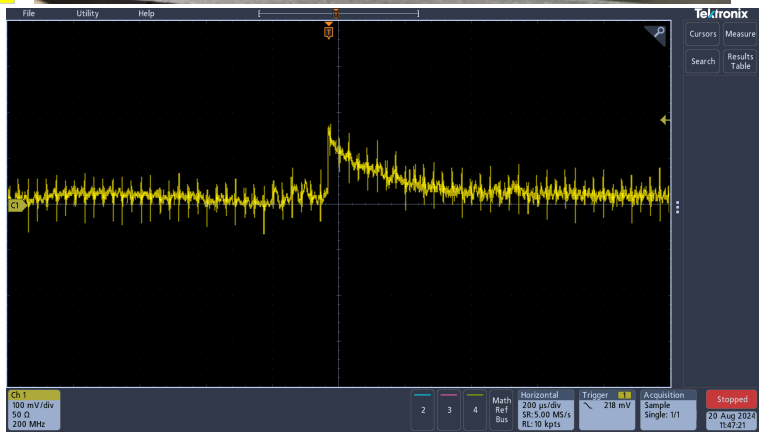
Passive pixel signal test

- 54 pixels read out at a time, via external Charge Sensitive Amplifier
- Clear response to both laser ($\lambda \sim 650\text{nm}$) and α radioactive source



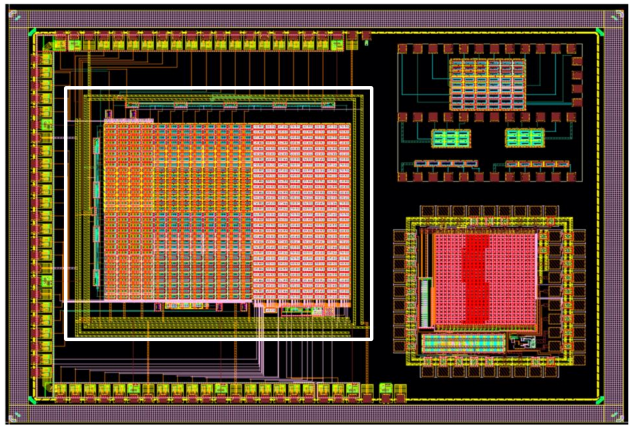




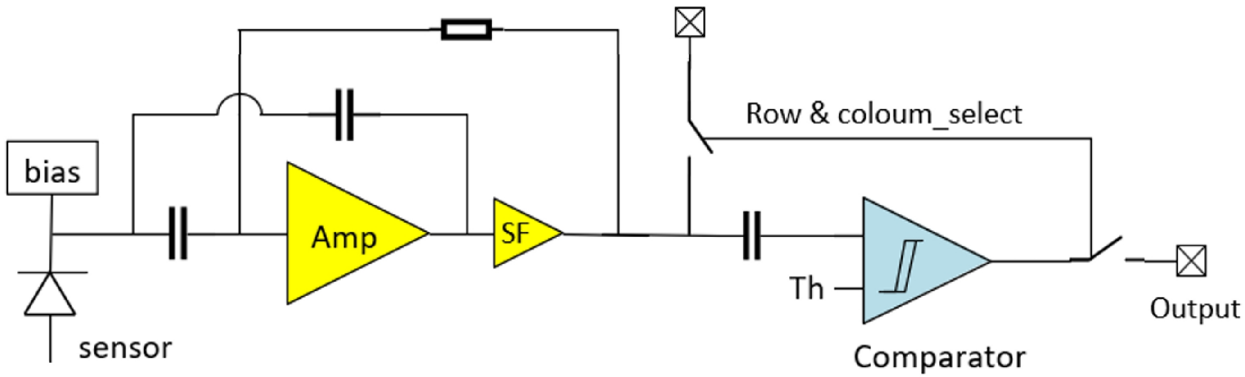


Active pixel matrix

- 32×20 active pixel matrix, peripheral modules including bandgap, analogue buffer, DACs and row/column gating
- Vary with CSA + Comparator combination to evaluate the X-talk issue



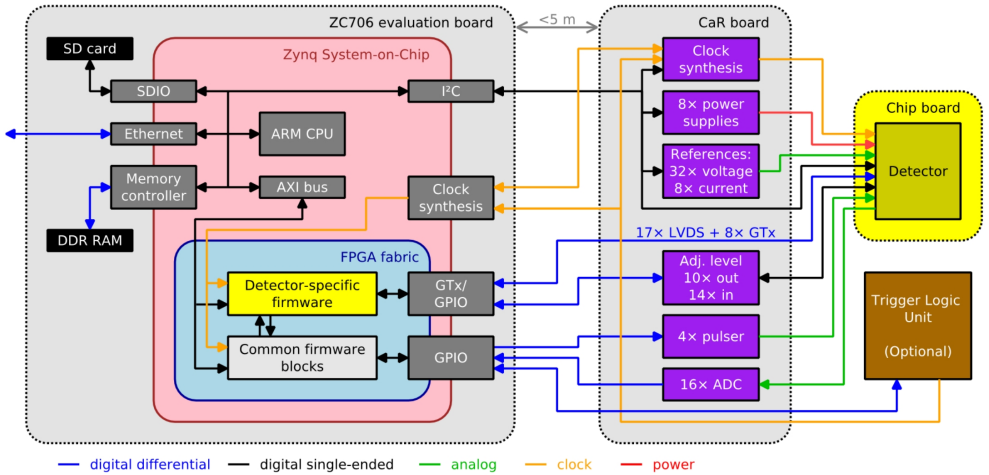
- Circuit simulation performance
  - CSA: ~140e ENC, gain $\sim 57\mu\mathrm{V/e}$
  - CMOS comparator: Time walk $\sim 2\mathrm{ns}$; Time over threshold $\sim 5\mu\mathrm{s}$
  - NMOS comparator: Time walk $\sim 9\mathrm{ns}$; Time over threshold $\sim 5\mu\mathrm{s}$

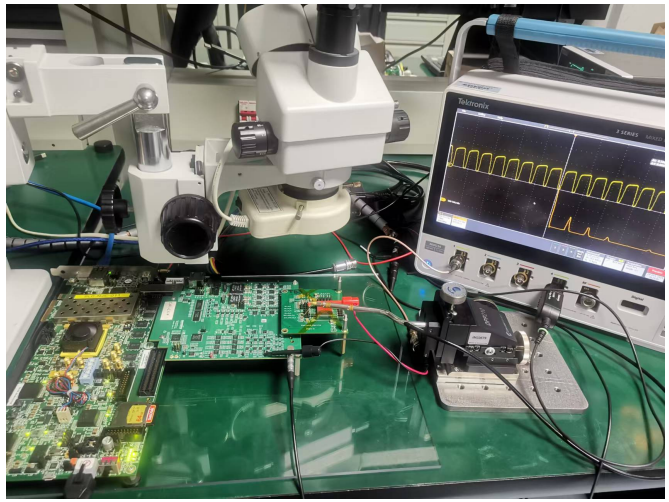


Active pixel matrix test system

PC + ZC706 + Caribou board + specific carrier board

Caribou system architecture



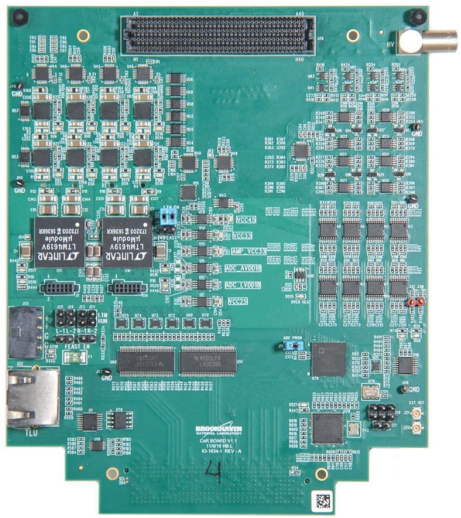


Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications

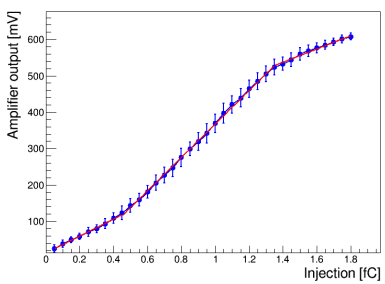
20 CaR boards v1.4 produced and distributed within RD50 common project

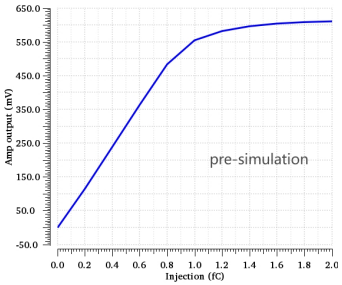


https://gitlab.cern.ch/Caribou/hardware/carboard

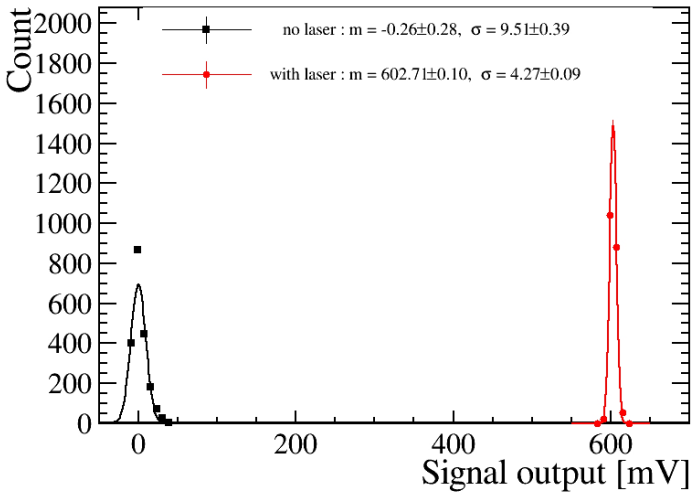
Active pixel matrix test results

- CSA output calibrated with charge injection. Response curve similar as pre-simulation

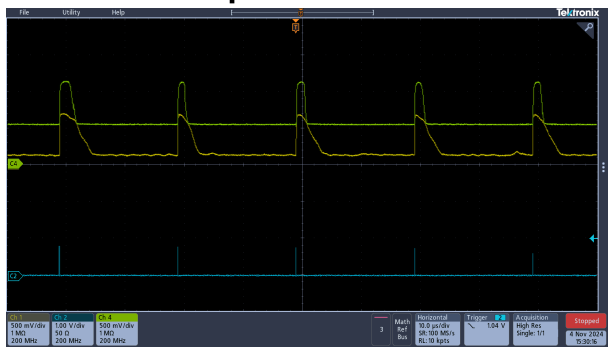




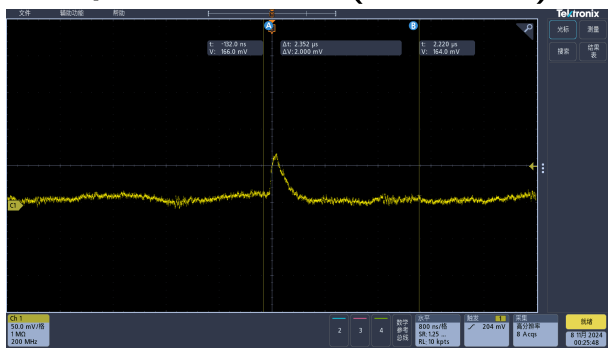
- Clear response to laser with low noise. 2000 injections @70V



- Discriminator works well, as shown in green while yellow for amplifier output



- Clear response to $^{55}\mathrm{Fe}$ source observed. Charge deposit estimated $\sim 1500e-$ consistent with expectation (1640e-)



Summary & future

- HVCMOS chip in 55nm process has developing for UT@Upgrade II
- Test results for first prototype, COFFEE2 chip, show good diode properties (breakdown$> 70\mathrm{V}$, leakage $\sim 10\mathrm{pA}$)
- Promising results from test with laser and radioactive source (α, X-ray). Digital circuit also works well
- Opportunities are being sought for MPW on high resistivity substrate
- COFFEE3 is currently being designed to validate the pixel array readout architecture and fully functional chip