The reference detector includes four tracking systems: the vertex detector, the Inner tracker (ITk), the TPC, and the outer tracker. These systems provide excellent position and momentum resolution. They are also crucial for Particle Identification.

The design and choice of technologies for Vertex detector, ITK and OT are very ambitious. The latest advances in Silicon detector technologies were implemented. This puts the detector design at the forefront of technological developments but also means that a much larger community needs to be engaged to complete the prototyping phase and eventually construct the detector(s). The achievements of groups involved in the silicon tracker, given the number of institutes involved, are impressive.

Recommendations

The manpower so far engaged in the design and R&D studies should be enlarged in order to ensure the successful completion of the project.

It is critical to assess the Outer Tracker (OTK) influence on the global momentum resolution and its impact to PID. To achieve this, a realistic full simulation is needed that accounts for the following aspects:

- **Alignment between ITK and OTK:** The relative alignment of the ITK and OTK has a significant impact on the global tracking precision. The simulation must incorporate realistic alignment tolerances and errors, reflecting expected mechanical installation uncertainties.

We thank the referees for this important comment. Alignment is indeed crucial for achieving ultimate track position resolution at the micron level. Alignment involves two key steps: the optical survey (mechanical assembly precision) and track-based mathematics alignment.

The assembly of both ITK and OTK follows a hierarchical structure, starting from small modules and building to larger ones. Based on our experience, the mechanical assembly (or optical survey) precision for small modules, such as sensors on ladders (staves or sectors), should be within tens of microns. For the large modules, such as ladders (staves or sectors) on the supporting frame, precision should be within hundreds of microns. While we have extensive experience with small module assembly. For large module assembly, we plan to develop detailed mounting procedures and alignment system to achieve the required precision.

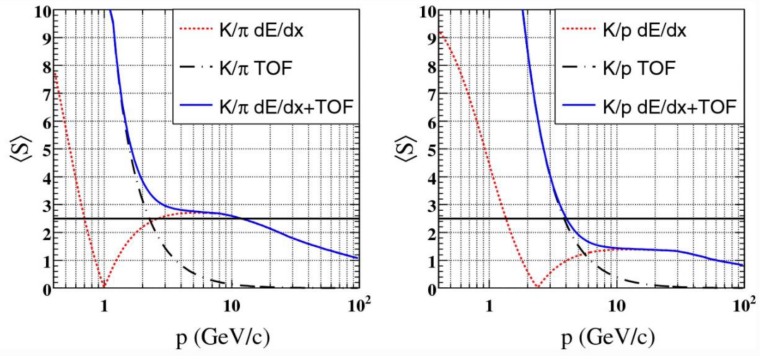
For track-based alignment, we plan to use a composite global alignment procedure, which aligns all detector modules from different hierarchy levels simultaneously, considering all correlations (*Eur. Phys. J. C* **83**, 245 (2023)). Additionally, we will simulate alignment precision under various mechanical tolerance scenarios using this approach.

● **Quantifying the Overall PID Improvement:** The simulation should ultimately demonstrate the quantitative improvement in PID when incorporating OTK-based ToF compared to using TPC dE/dX alone. This will provide a clear understanding of the role the OTK plays in broadening the detector's PID capabilities across a broader spectrum of momenta. OTK importance to PID in forward regions outside TPC coverage is particularly important.

We thank the referees for this important comment.

We provide Figure XXX for the referees, illustrating a PID study for K/pi and K/proton separation using TPC alone, Tof alone, and a combination of both. As shown, TOF offers dominant performance for K/pi separation below 2.5 GeV/c and K/proton separation below 5.5 GeV/c.... (contacted with TPC group, and this plot will be updated accordingly.)

K/pi separation **K/proton separation**



ITK

The **Inner Silicon Tracker (ITK)** uses a combination of **HV-CMOS pixels** (34 μm × 150 μm pixel size) and **CMOS strips** (2.1 cm x 2.3 cm size, 20 um pitch) to provide excellent spatial resolution, with a target of less than 10 μm in the bending plane and around 50 μm in the

longitudinal direction for the barrel region. The endcap sections are optimized for particle identification and momentum measurement, featuring strip sensors arranged with a cross angle to maximize track resolution in the bending direction. The ITK is designed to handle hit rates of up to **10^6 Hz/cm^2** in high-luminosity environments, with a total sensor area of about **20 m^2**.

The ITK HVCMOS (CAFFEE chip) utilizes a so-called large pixel CMOS sensor design and was realized in 55 nm process and standard reticle size (no stitching) and follows standard pixel module design (modules, sensor+flex, on staves). The advantages of this process are the use of high resistivity substrates (1-2 kOhm cm) which allows for higher depletion depth and also bias voltages of ~70 V assuring large depleted regions. First CAFFE tests were successful with passive CMOS diodes while active cells and active cells with periphery electronics are yet to be tested.

The Depleted Active Micro Strips sensors would use a different process (CMSC 180 nm). As sensor size is limited to reticle size, it doesn't require stitching and seems a safe design. The CMOS passive strips have already been demonstrated, however, the small strip pitch and the design of the readout part in the periphery are very challenging and have yet to be demonstrated.

Comments:

● There is no dedicated effort mentioned in the current development of the CMOS strip sensors specifically for the Inner Tracker (ITK).

We thank the referees for this important comment. As mentioned in our presentation to the IDRC, we are preparing the design for the tape-out for the first CMOS chip (CSC1) by the end of this year. In the coming month, there will be two rounds of technical reviews to discuss the design details and project plan. In the ref-TDR, we will also provide further information on the R&D progress.

● 180 nm process may not be available over the next several years and presents a risk.

We thank the referees for this important comment. We spoke with the CSMC foundry, and they preliminarily confirmed that 180 nm process will be maintained for the next 20 years. In parallel, we also have a backup plan to migrate to 65 nm or 28 nm, depending on the results of functional test of the 180 nm process with high-resistivity silicon wafers.

● Strip CMOS sensors with readout circuitry in the periphery of the sensors is novel and surprises are likely.

For now, there are no fundamental barriers to the development of readout circuits in the periphery of strip sensors. In the CSC1 mask design, we have included different sections: passive sensor only, circuitry only, and sensor with peripheral circuitry to facilitate testing. After the CSC1 tape-out, we will have further insights into the readout circuitry design.

Recommendations:

● A detailed plan for the development of the ASIC for both CMOS strips and AC-LGAD (for OTK in this case) is needed, as the R&D timescales for these ASICs technologies with low-dissipation, high-time resolution is particularly challenging, requiring careful optimization of power consumption, timing precision, and integration with the sensors. They should be developed alongside the sensors. ASIC design, fabrication, and testing are time-intensive processes, often requiring multiple iterations to meet the performance requirements, and any delays in this pipeline could have cascading effects on the overall project timeline.

OTK

The outer tracker is planned with 85 m2 of AC-LGAD strip detectors located at r=1.85, z=+/-2.35m and measuring a single coordinate in the bending plane. The sensors should have 100 um wide strips that would be 6-9 cm long and deliver around 10 um position and 50 ps time resolution. The much-needed expertise in LGAD technology comes from ATLAS HGTD detector where IME is the sole producer of conventional LGADs and the IHEP and USTC designed the sensors.

The envisaged power consumption is 300 mW/cm^2 (ASIC) and requires active CO2 cooling.

The full coverage will require ~3500 wafers with 2 different sensor designs in the barrel and 21different detectors in endcaps (wedge-shaped). The purpose of the detector is to provide a ToF point for the tracks originating at the same vertex (PID).

First prototypes on small sensors ~5x2 mm2 AC LGADs showed a time resolution of 37 ps and position resolution of around 8 um. The ASIC has not been designed yet, but it is planned to mimic the current ASICs for LGAD readout.

Comments:

● The number of different sensor designs is large in the endcap and can complicate the construction.

The dimensions of the OTK endcap are large, with a radius ranging from 406 mm to 1816 mm. In the current OTK endcap design, we require only 4 masks for OTK silicon wafers, with the silicon sensors designed in a trapezoidal shape. This approach aims to minimize the complexity in sensor production and assembly.

● The discharge of generated electrons through n+ layer may be affected by radiation damage and can change during the lifetime of the detector.

We are conducting LGAD irradiation test to assess the detector performance with regards to radiation damage affecting the n+ layer of LGAD.

● The capacitance of some sensors will be large (up to ~10 pF) which will make the noise jitter and rise time such that it will be difficult to achieve the desired time resolution.

This is one of our main concerns. In the coming years, we plan to tape out a few phototypes to study the relationship between time resolution and capacitance as related to strip length.

● Operation of AC-LGADs can be susceptible to high particle rate effects and make sure that you understand that well (also related to size of LGADs).

We acknowledge the point and will conduct studies to gain a comprehensive understanding.

● For the given pitch and thickness a charge-sharing mechanism and by that the position resolution should be carefully studied for different electrode dimensions taking possible

variations of gain layer properties across the large detector into account.

Please refer to the answer provided above.

● The localized power dissipation at the ASIC should be taken into account in the cooling design and performance evaluation.

We appreciate referees' suggestion. Localized power dissipation at the ASIC has been considered in our cooling design, such as using thermal vias in PCBs. Additionally, we are exploring other options to simplify ASIC assembly while enhancing thermal dissipation.

Recommendations:

● Reconsider the size of the AC-LGADs and take both the performance (rate effects, time resolution and achievable position resolution) and expected yield into consideration in order to reach a cost effective solution.