

# **CEPC Silicon Tracker Progress Report (10)**

#### Qi Yan On behalf of the Silicon Tracker Group Nov 5, 2024

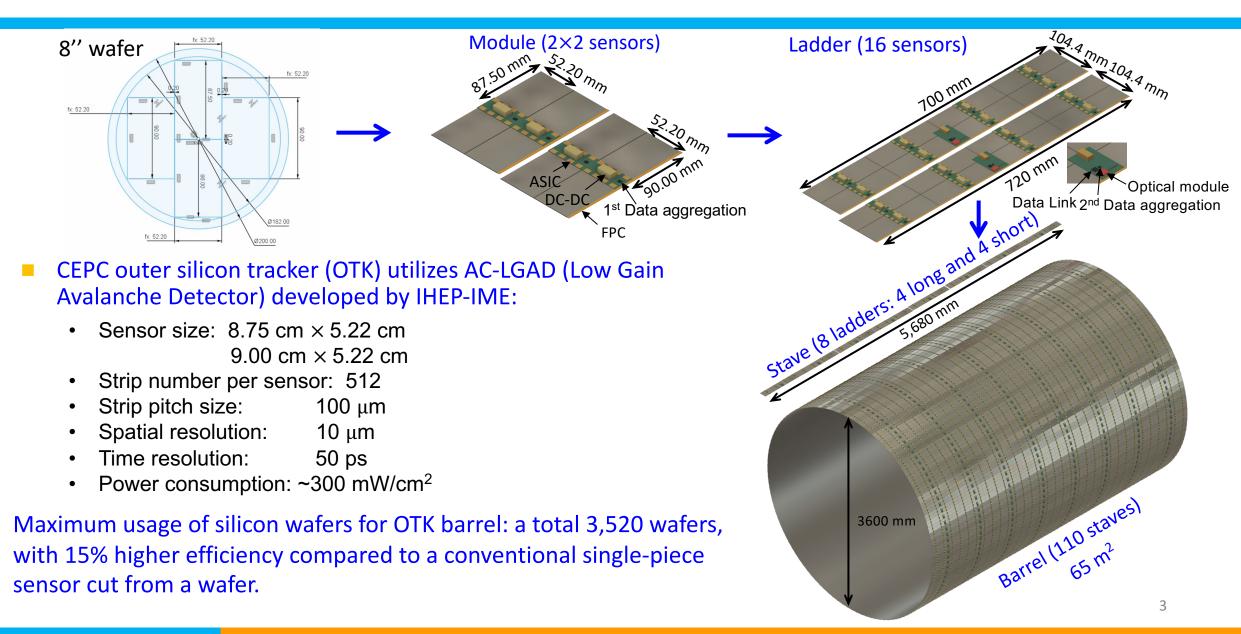


中國科學院為能物招加完施 Institute of High Energy Physics Chinese Academy of Sciences

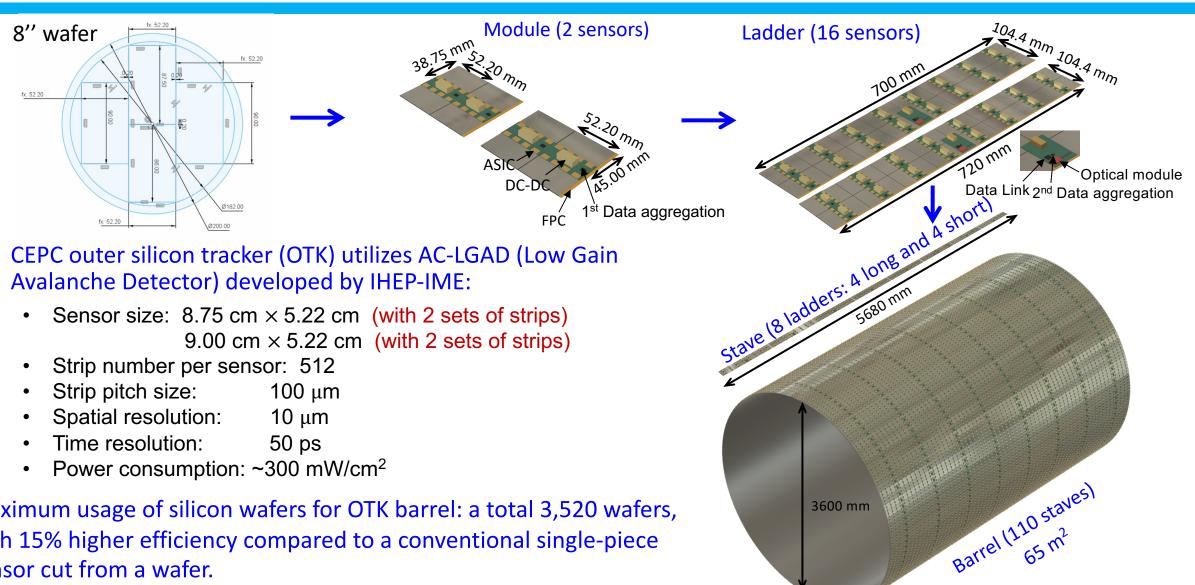
### **IDRC Review Comment (OTK LGAD)**

The capacitance of some sensors will be large (up to ~10 pF) which will make the noise jitter and rise time such that it will be difficult to achieve the desired time resolution.
This is one of our main concerns. In the coming years, we plan to tape out a few phototypes to study the relationship between time resolution and capacitance as related to strip length.

# **OTK Barrel Design with AC-LGAD Long Strips**

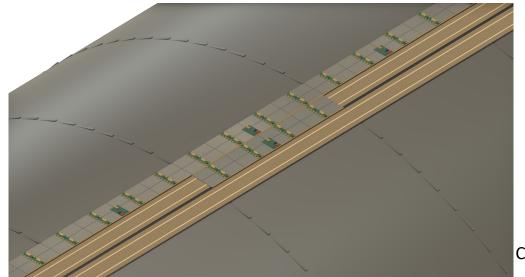


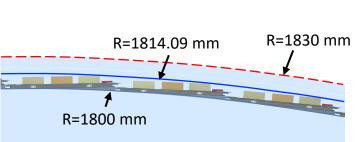
# **OTK Barrel Design with AC-LGAD Short Strips**



Maximum usage of silicon wafers for OTK barrel: a total 3,520 wafers, with 15% higher efficiency compared to a conventional single-piece sensor cut from a wafer.

#### **OTK Barrel Mechanical and Cooling with Long Strips**





Sensor: 300 μm Carbon fiber plane: 300 μm Carbon fiber honeycomb: 2.4 mm Carbon fiber plane: 300 μm

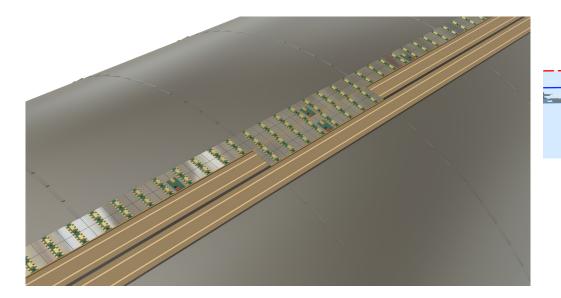
• The outer barrel of the TPC is made of a carbon fiber cylinder with stepped ramp rings used for OTK support.

- The installation of OTK stave begins with the carbon fiber honeycomb and cooling pipe (~6 m in length), along with the lower support carbon fiber plane.
- Afterwards, the OTK ladders are inserted one by one. Each ladder (~0.7 m) has its own support, consisting of 16 sensors, electronic components, and a carbon fiber plane.

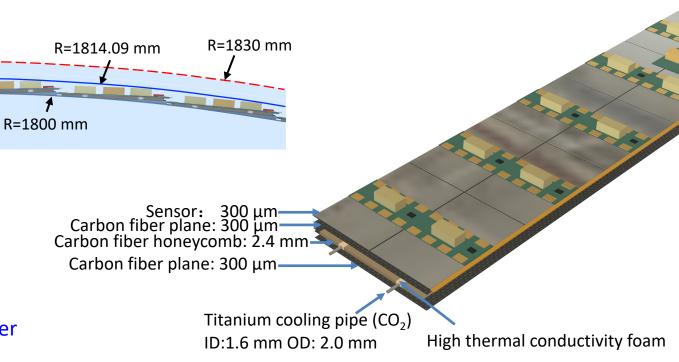
Titanium cooling pipe  $(CO_2)$ ID:1.6 mm OD: 2.0 mmHigh

High thermal conductivity foam

#### **OTK Barrel Mechanical and Cooling with Short Strips**

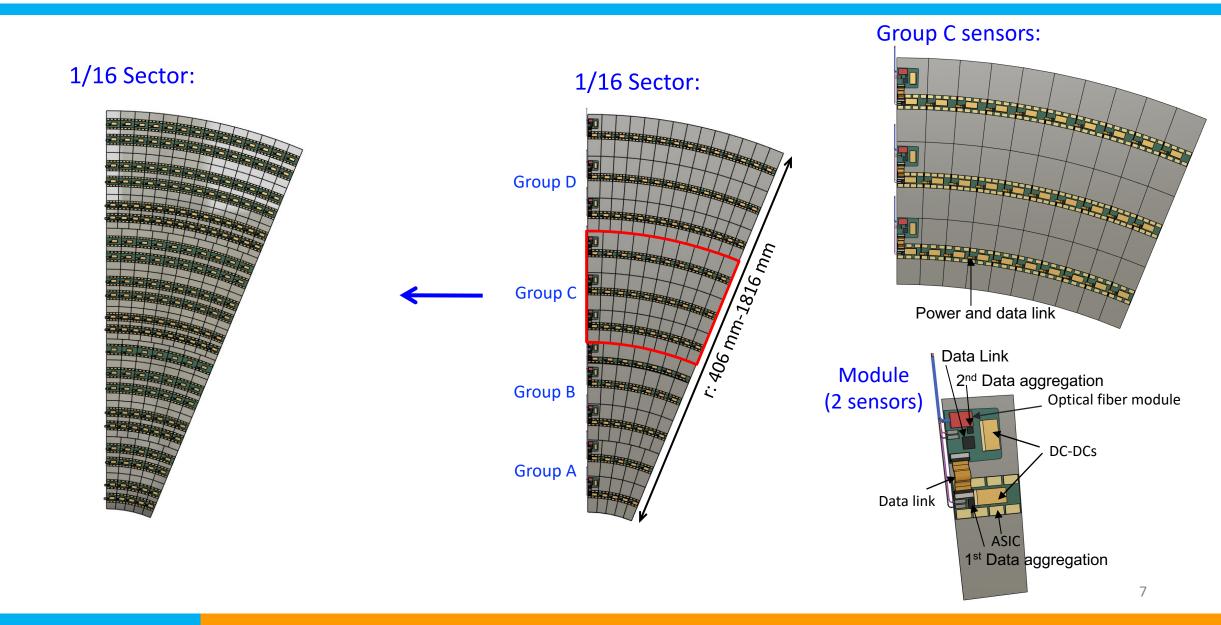


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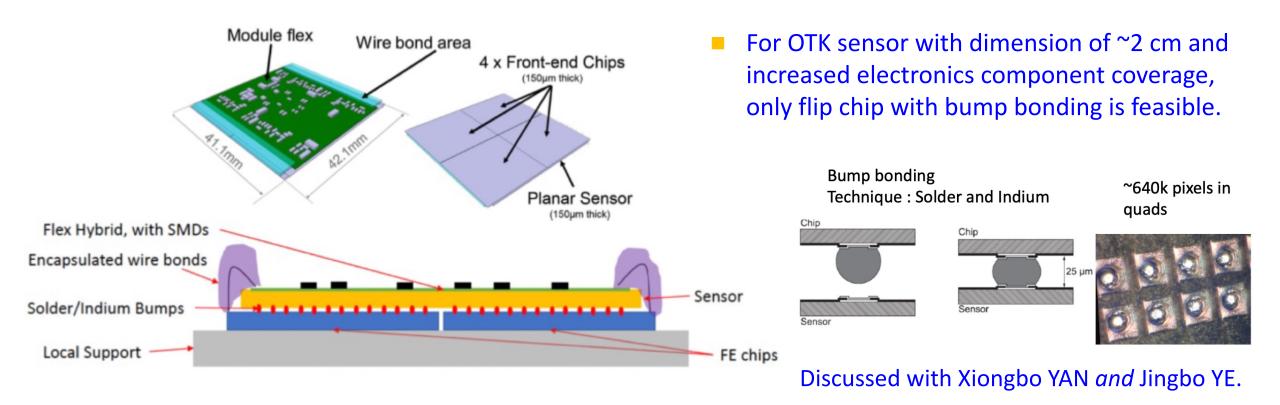


More electronic components and readout channels are introduced for the short strip sensor (~4 cm).

### **CEPC OTK Endcap Electronic Components**

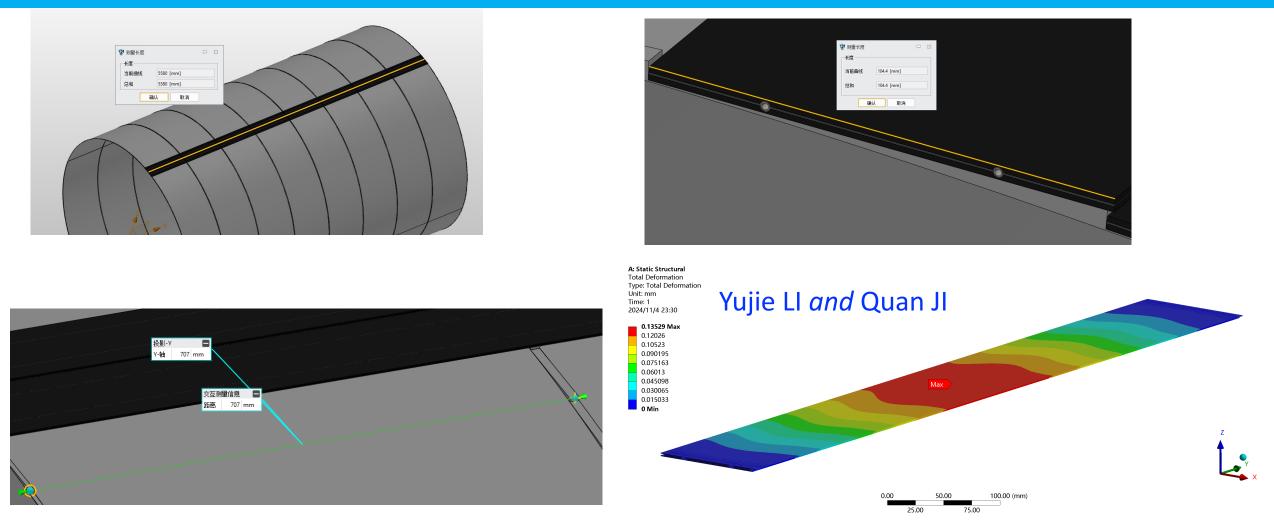


### **OTK Assembly for Sensor Dimension <2 cm**



For sensors <2 cm, assembly is even more difficult. Mei ZHAO is conducting simulation to understand the correlation between capacitance (and related performance) and sensor size.

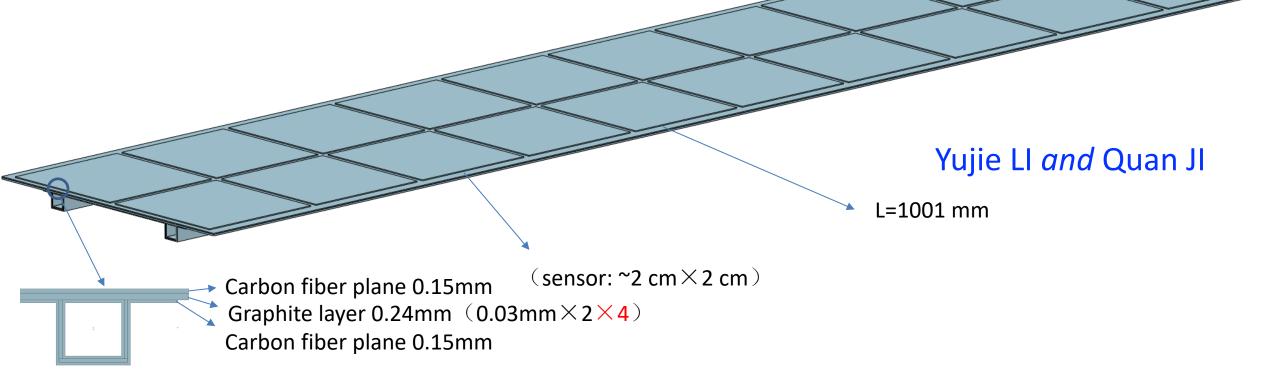
# **Study of OTK Ladder Deformation**

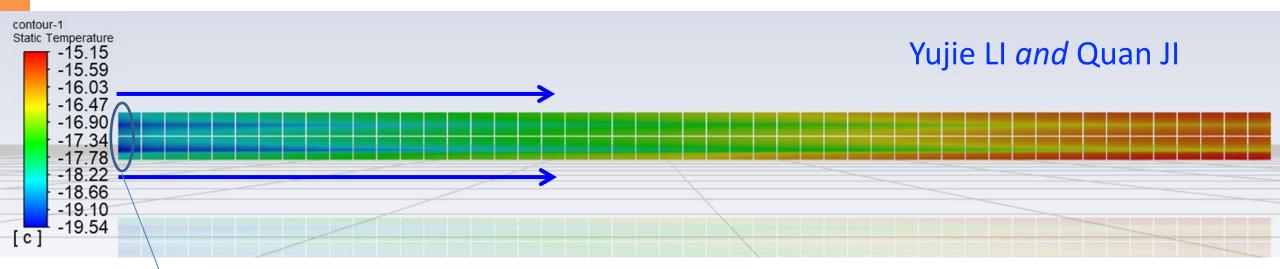


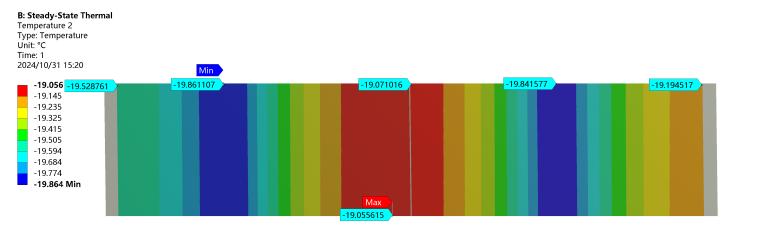
Under its own weight, including its electronics components, the maximum deformation of a single ladder (720 mm) is calculated to be ~0.135 mm.

# **Simulation of ITK Thermal Performance**

To make the model more realistic, the sensor structure and essential thermal components have been taken into account.



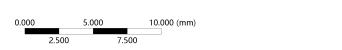


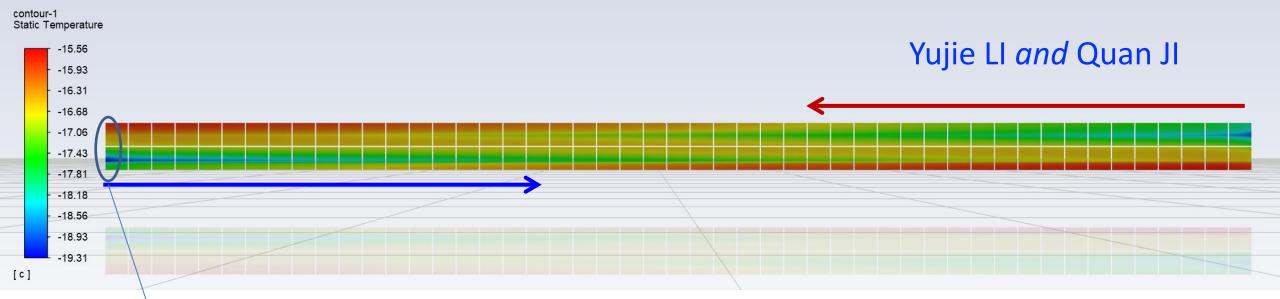


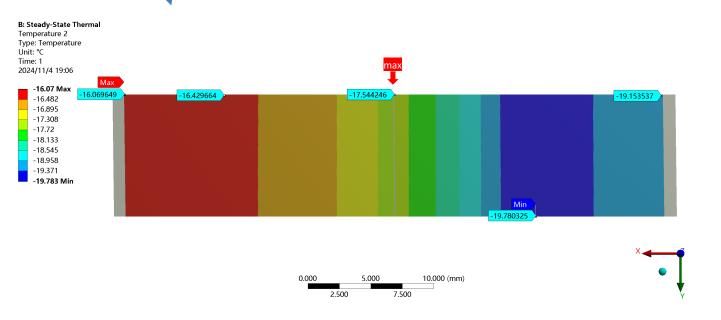
Using liquid CO<sub>2</sub> at -20°C with an inlet flow rate of 0.003 kg/s from one side:

The maximum longitudinal temperature difference on the stave: 4.39 °C

The maximum temperature difference on a single sensor: ~0.8°C







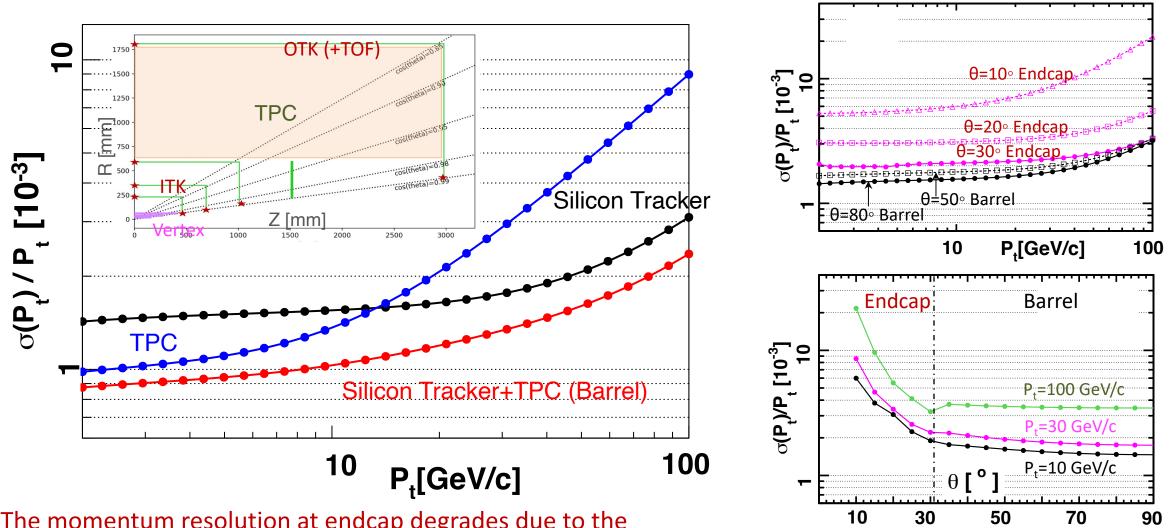
Using liquid CO<sub>2</sub> at -20°C with an inlet flow rate of 0.003 kg/s from both sides:

The maximum longitudinal temperature difference on the stave: 3.75°C

The maximum temperature difference on a single sensor: ~2.24 °C

The maximum temperature difference decreased compared to single-side inlet (4.39°C  $\rightarrow$  3.75°C), but the temperature gradient on a single sensor increased significantly (0.8°C  $\rightarrow$  2.24°C).

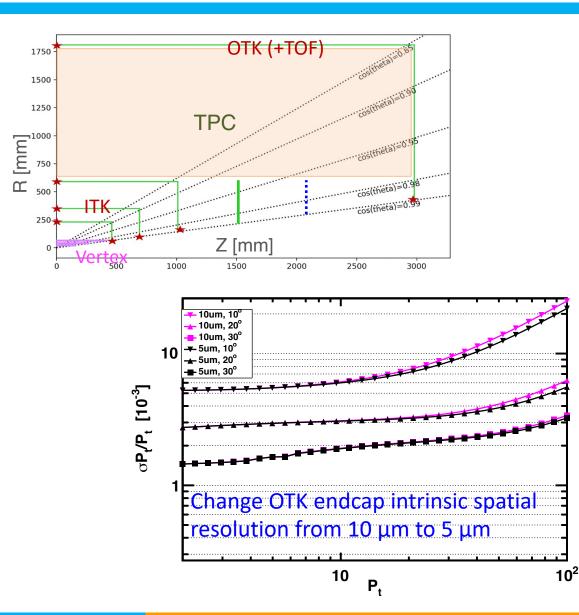
#### **CEPC Tracker Performance from Simulation:** Momentum Resolution

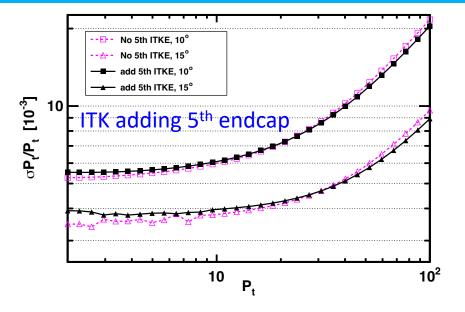


The momentum resolution at endcap degrades due to the shorter lever arm (r) as:  $\sigma(P_t)/P_t \propto 1/r^2$ . Is any way to improve?

Silicon Tracker momentum resolution angular dependence

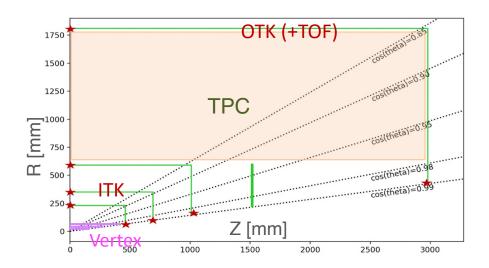
# **Sensitivity of Endcap Momentum Resolution**



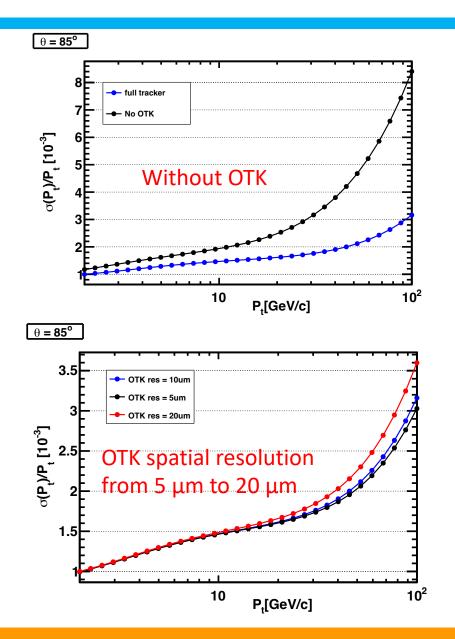


Improving intrinsic resolution is not beneficial. Compared to the intrinsic spatial resolution, multiple scattering dominates momentum resolution below 50 GeV/c.

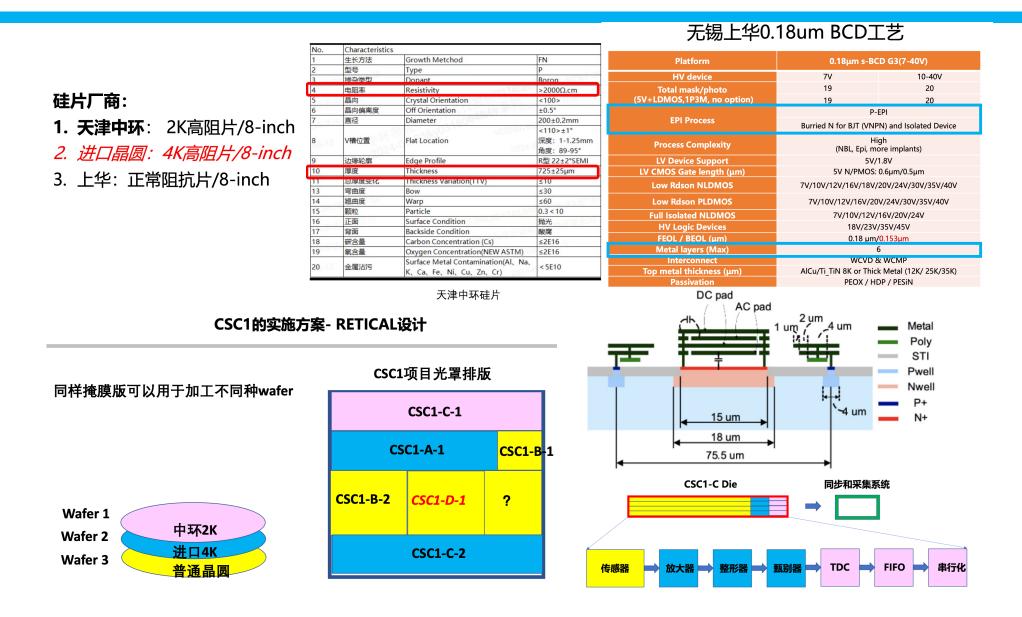
### **Sensitivity of Barrel Momentum Resolution**



An OTK spatial resolution of ~10  $\mu m$  is crucial for the overall track momentum resolution.

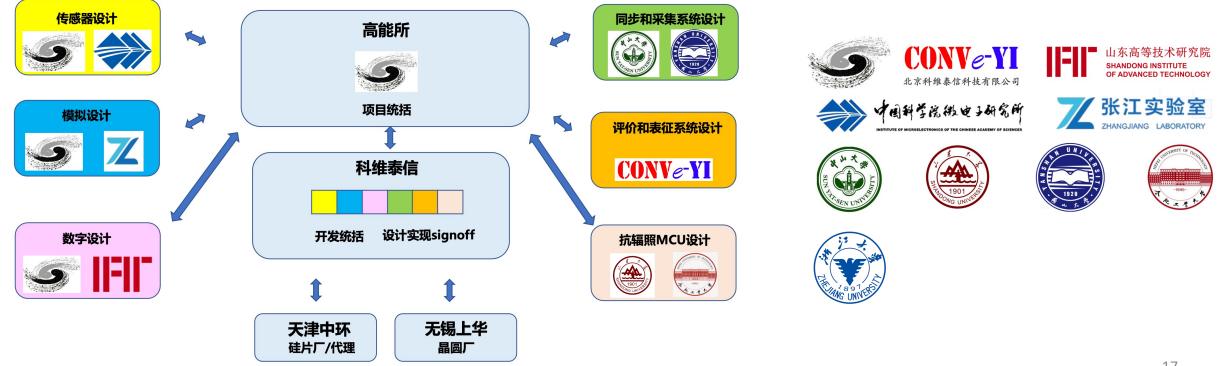


### **CMOS Strip Chip Project Introduction and Review**



The CMOS Strip Chip project (CSC) explores a different approach for developing of fully depleted monolithic CMOS detectors. It utilizes domestic high-resistivity wafers (Tianjin Zhonghuan 2K) and CMOS foundry (CSMC, Wuxi Shanghua). The project combines efforts from both research institutes and industry (9 units currently participating).

Last Friday (November 1), we conducted the first review of CMOS strip project, inviting institute's electronics group. The review was constructive and included a detailed discussion of the technical approach, development specifics, and project organization. Participants in the review included: 郭超英, 王铮, 魏微, 叶竞波, 严雄波, 赵梅, 陆卫国, 张颖, 李刚, 李一鸣, …



# **Key Discussions in the Review**

The review discussed many key technical issues and was very beneficial (~4 hours discussion). The team has recorded them thoroughly:

对于20 um间距的硅微条,不只是微条之间的串扰,ASIC之间的串扰可能也很复杂。

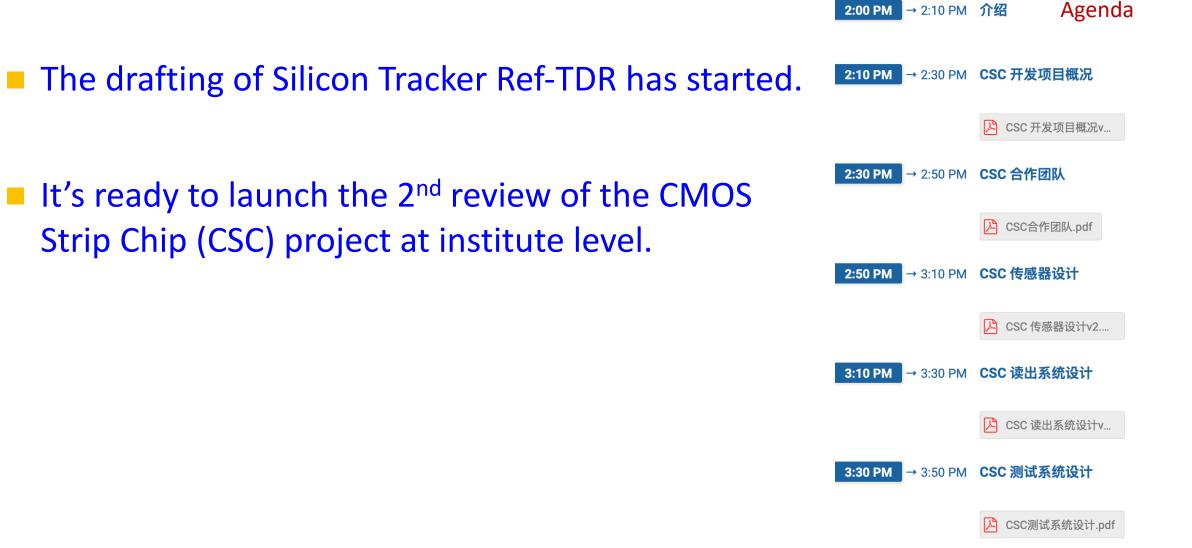
当前CSC项目需要20 μm宽,1024通路,这是非常有挑战性的工作,在实际设计过程中金属电极是有 阻抗的,对于1000多路的传感器压降问题需要考虑。

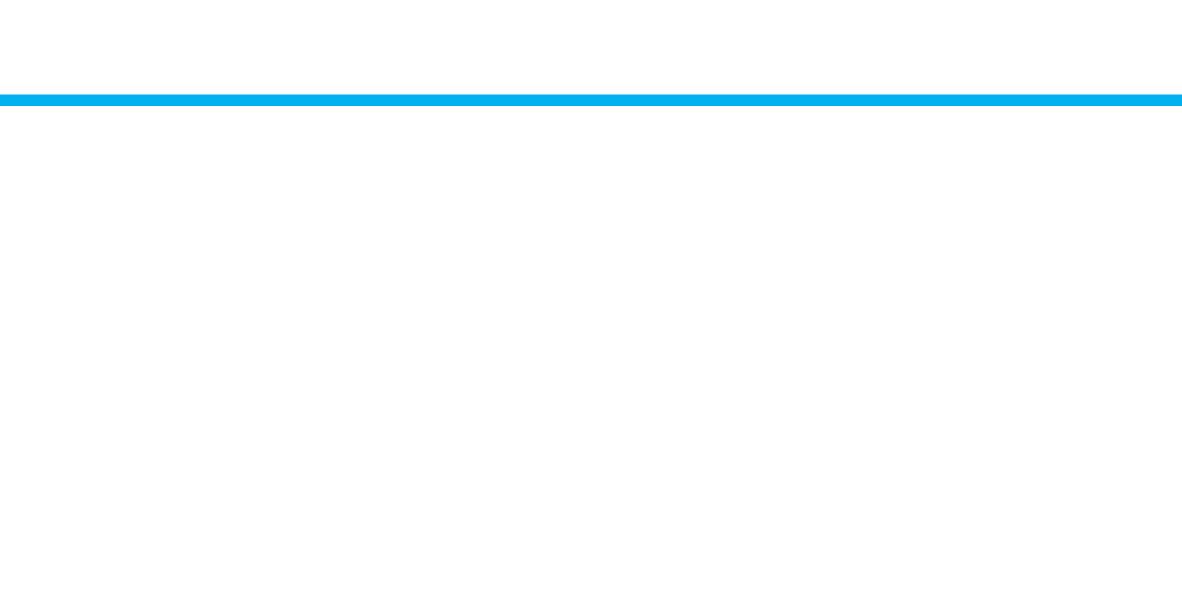
CMOS每层工艺需要填充,填充如何解决?电路和sensor的不同可能会导致凹陷,由此导致的良品率。

目前计划在电路部分挖掉衬底来实现sensor和电路的隔离,通过20 um 的DTI来实现隔离,需要仿真 验证是否能够实现。

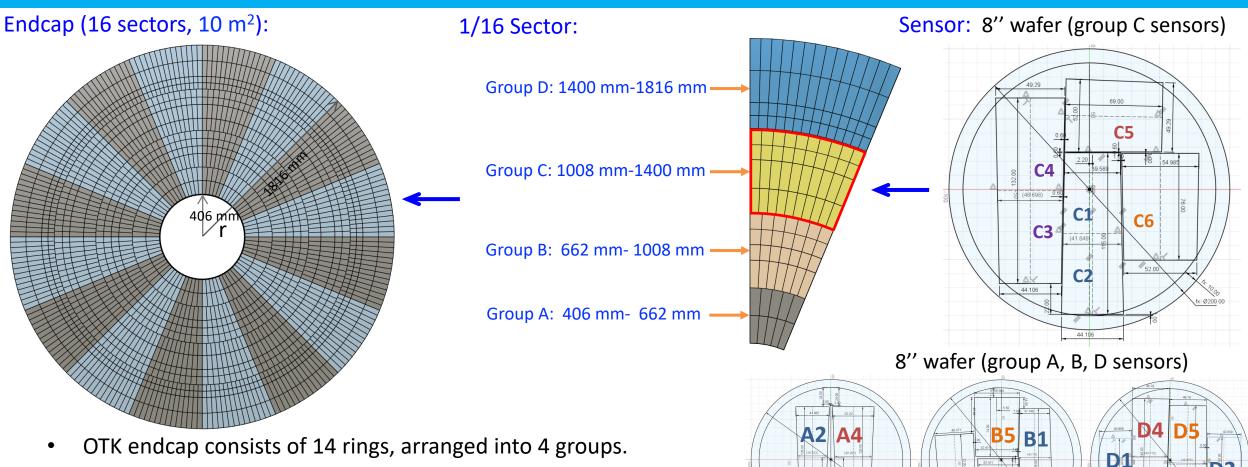
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# **Next Plan**





# **CEPC OTK Endcap Design (AC-LGAD Strips)**



- Each group contains 2-4 types of trapezoid sensors, which can be fitted to one 8" silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
- The long sensor contains 2 sets of short-strip sensors.

**B3** 

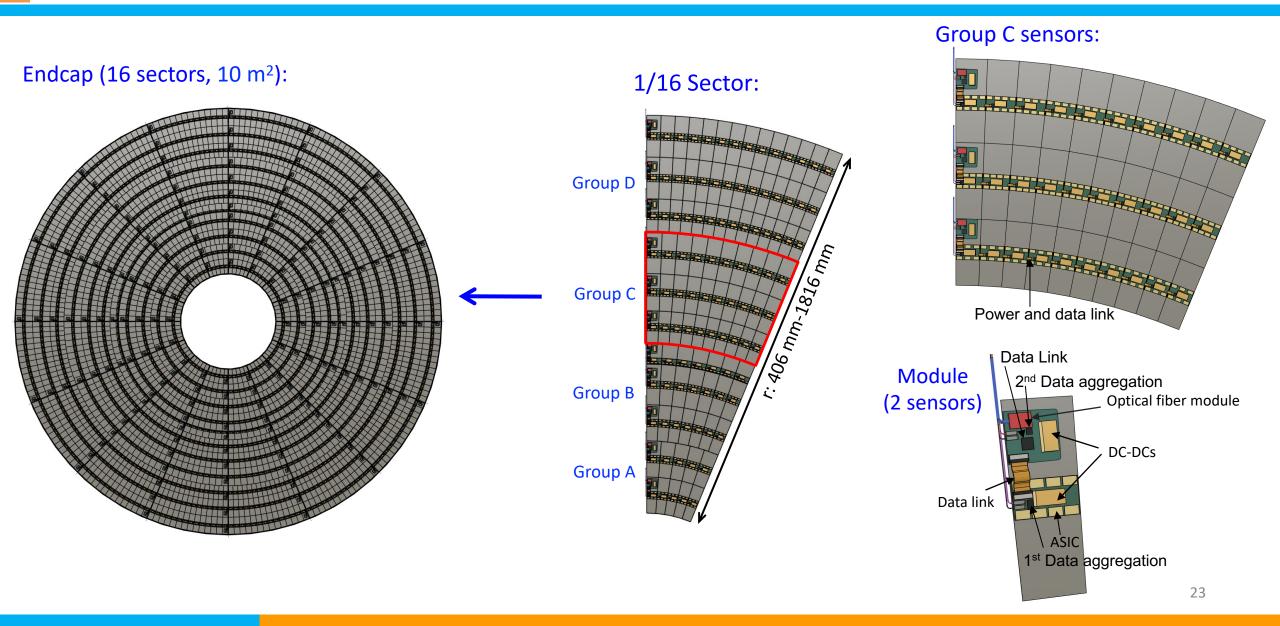
**A1** 

**B2** 

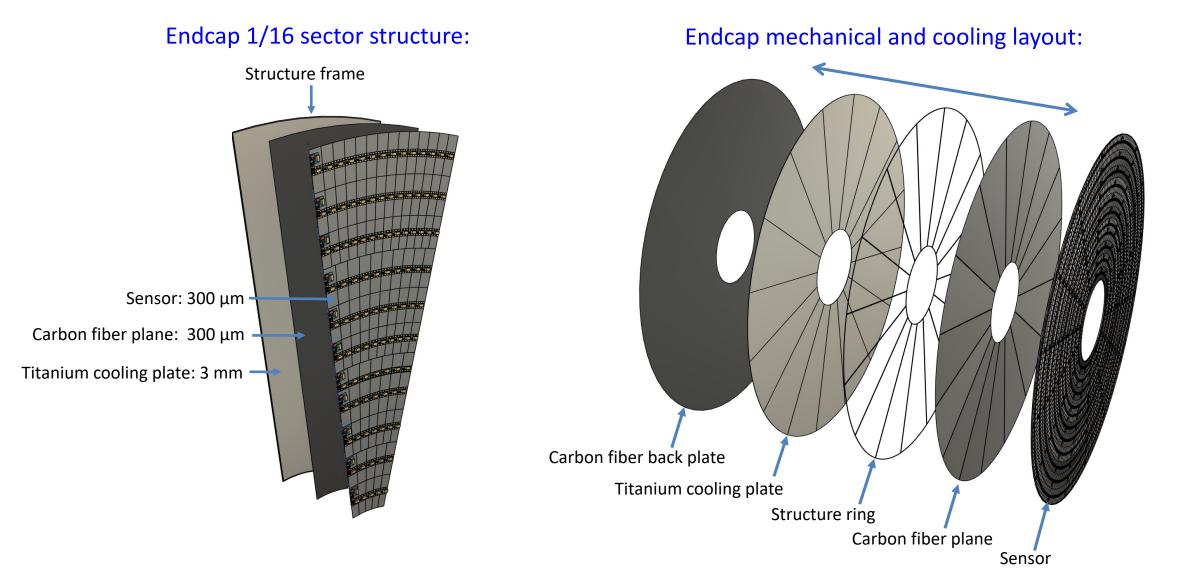
Maximum usage of silicon wafers

**B4** 

### **CEPC OTK Endcap Electronic Components**



### **OTK Endcap Mechanical and Cooling Structure**



### **CEPC OTK Mechanics and Installation Design**

