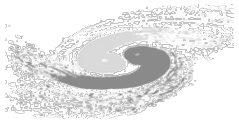
# Summary of the weekly meeting

- **Indico link: https://indico.ihep.ac.cn/event/24042/**
- **Went through again of the SiPM ASIC & OTK ASIC, on the spec & schemes**
- **Timeline of all sub-detector ASIC & common ASIC development**
- **Schedule of the TDR writing**

# Timeline for all the FE ASICs – common ASIC – recent



Ref-TDR release 2025.6

Long term

**Overall Electronics system**

- 2024.8 Specification & background
- 2024.9 Sub-Det readout Elec scheme finalization
- 2024.10 Overall Electronics scheme finalization
- 2024.12 Elec TDR Draft1
- 2025.3 Elec cost Draft1

**Power & DC-DC (BaSha霸下)**

- 2024.10 Irradiation test
- 2024.11 GaN Selection
- 2025.1 DC-DC Controller schematic design
- 2025.3 DC-DC module performance from simulation
- 2026.1 DC-DC BaSha module prototype

**Data Link (TaoTie饕餮、ChiTu 赤兔 & KinWoo金乌)**

- 2024.8 Specification finalization
- 2024.10 Protocol define
- 2027.6 ChiTu Chip prototype

**VTX STCH (Taichu太初)**

- 2024.8 Tech route define
- 2024.10 Preliminary scheme for Stitching
- 2027.12 Stitching prototype

**PIX TPC**

- 2025.6 Prototype beamtest
- 2026.12 Chip Finalization

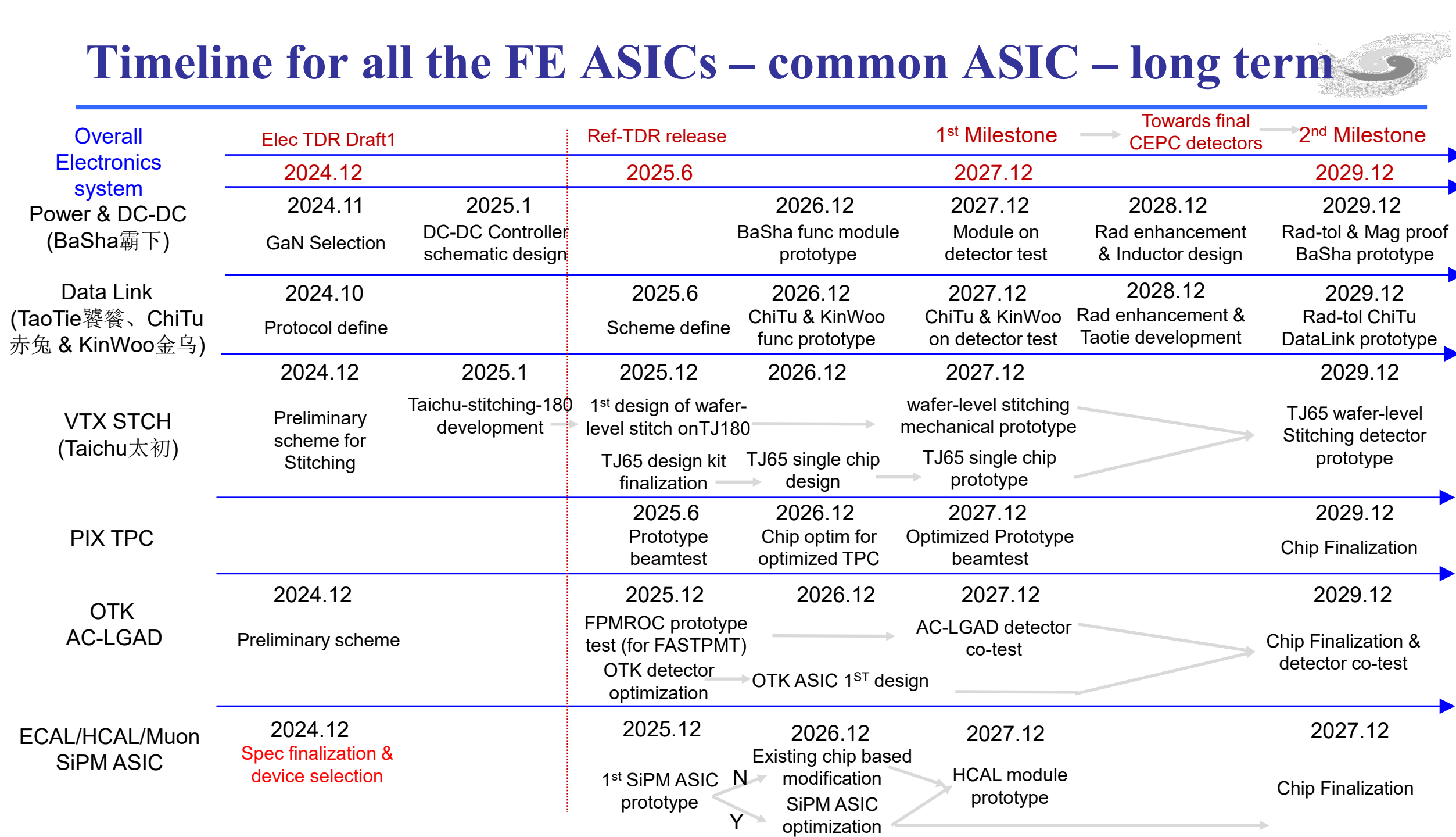
**OTK AC-LGAD**

- 2024.8 Module scheme design
- 2024.12 Detector Parameter optimization
- 2027.12 Chip prototype

**ECAL/HCAL/Muon SiPM ASIC**

- 2024.8 Preliminary scheme
- 2024.12 Spec finalization & device selection
- 2027.12 Module prototype

# Timeline for all the FE ASICs – common ASIC – long term



# SiPM requirements summary

## Crystal ECAL: specifications

| Key Parameters | Value | Remarks |
|---|---|---|
| MIP light yield | ~200 p.e./MIP | Ensure EM resolution $\sim 3\%/\sqrt{E}$ |
| Energy threshold | 0.1 MIP | Balance between S/N and dynamic range |
| Crystal non-uniformity | < 1% | Along the crystal length and between crystals |
| Dynamic range | 0.1~3000 MIPs / channel | Maximum energy deposition with 360 GeV Bhabha |
| Timing resolution | ~500 ps @ 1 MIP | Bunch Crossing ID; clustering and hadron performance |

## HCAL requirement

| | | |
|---|---|---|
| Signal Dynamic Range | 1 – 100 MIPs | 0.1 MIP as trigger threshold |
| Time Resolution (1-MIP signal) | 1 ns | Bunch crossing ID timing hadron performance |
| Power Consumption | 15 mW/ch | O(5.6M) channels |

## Muon requirement

- Readout design for ECAL and HCAL covers the requirements of Muon detector: $N_{pe} < 100, \sigma_T < 0.5ns$
- Use the ASIC scheme from ECAL or HCAL, and customize the FEE based on ASIC.
- Revise according to the constraints from cooling and mechanical structure of the detector

**Potential issue to use a common ASIC for ECAL & HCAL:**

- **pe @ MIP is different for ECAL/HCAL**
- **Charge is strongly depend on SiPM gain charge_over_pe**
  - **The real input for ASIC**

# SiPM ASIC requirements & remain issues

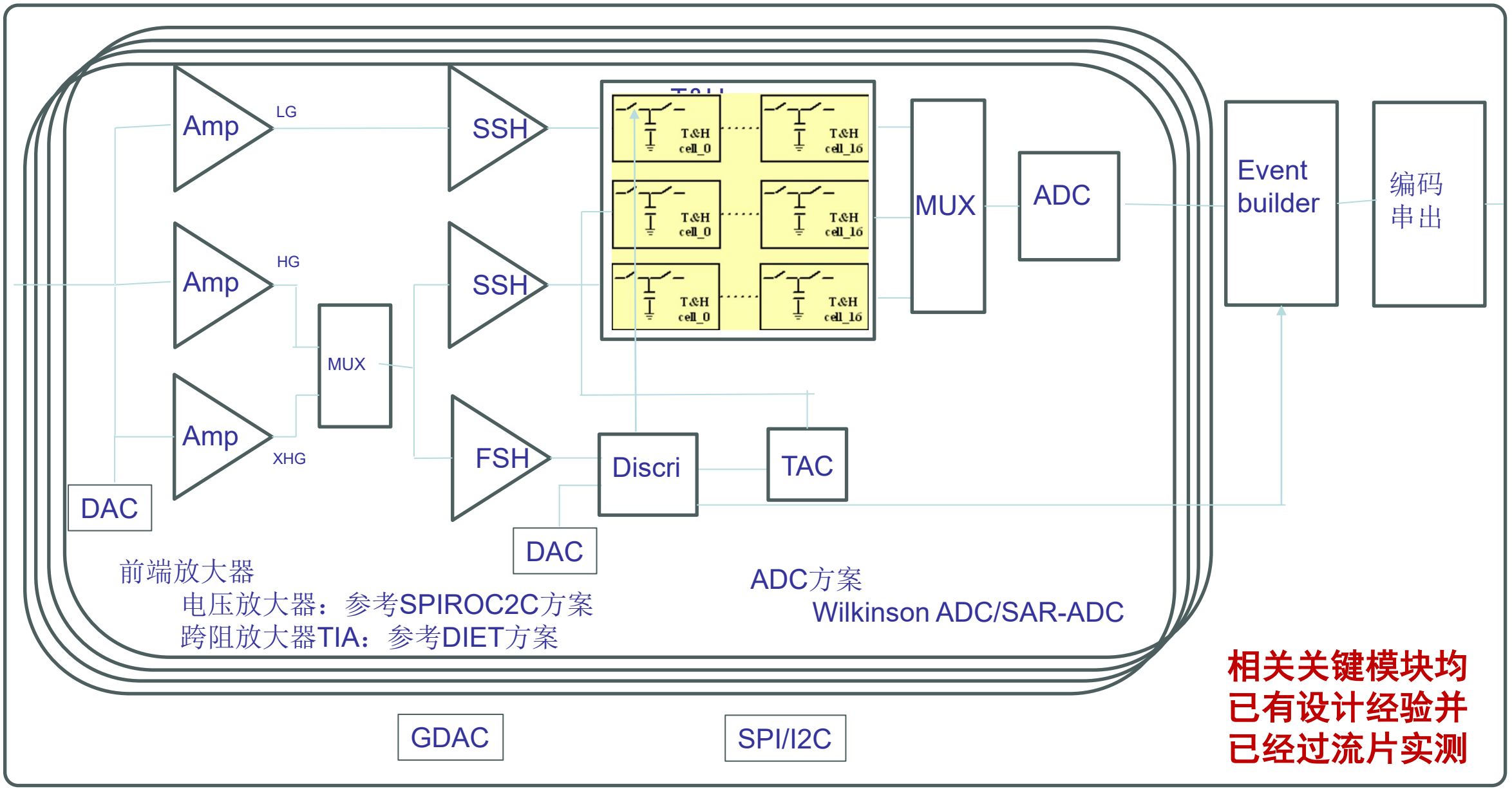
- SiPM输出信号处理方式：Q&T
- 动态范围：0.1MIP (?) ~3000MIPs
- 电荷分辨： 10% @1MIP， (?) @3000MIPs
- 时间分辨：~500ps@1MIP
- 单通道计数率：（暗计数、束流本底、物理事例）
- 功耗：~15mW/ch

待确认问题：

- SiPM的型号（增益、Cd、一致性、偏压的调节、温漂）
  - 不同器件对芯片方案有显著影响
- 信号特征（前、后沿，信号宽度）
- 刻度方案：是否需要单光子？
- 工作模式：是否需要random trigger读基线？
- 探测器本底：
  - 平均 & 最高（需最终确认） - 前放设计、数据读出能力相关
  - 分布（层间、BX间） - 读出、数据汇总相关
  - 占空比 - 片上缓存相关

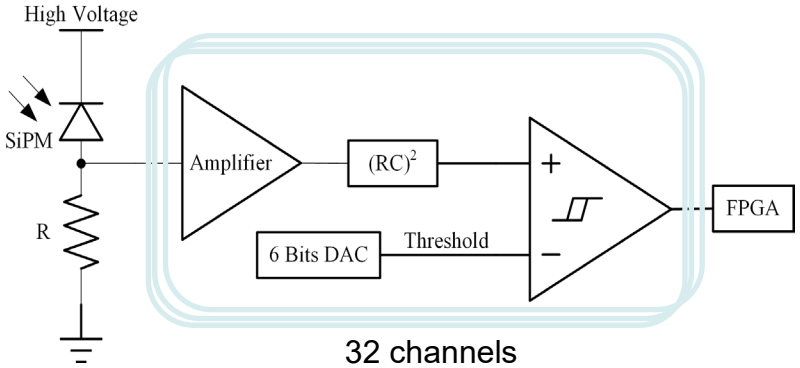
为实现3年实现7000通道小模型测目标，探测器方案和器件选型需在年底前确定

# SiPM ASIC scheme （0.1~3000MIPs）



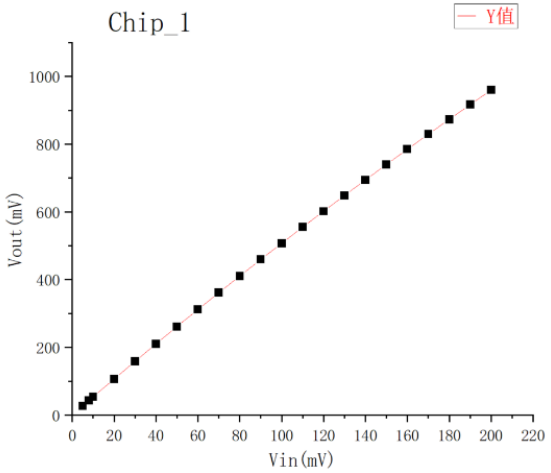

**相关关键模块均已有设计经验并已经过流片实测**

# Previous experience: Voltage Amp-Shaper-Disc. ASIC for SiPM @CSNS

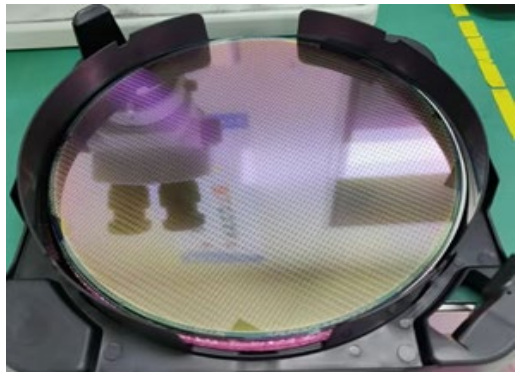



32 channels

Block diagram of the CSNS_VASD ASIC

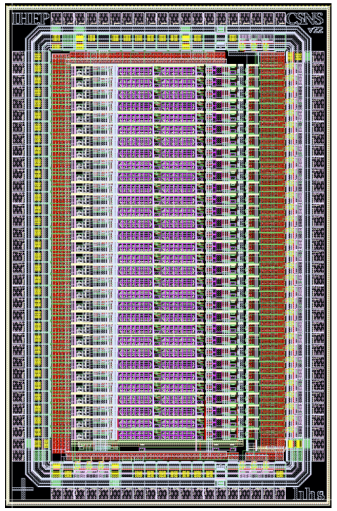



INL of the ASIC

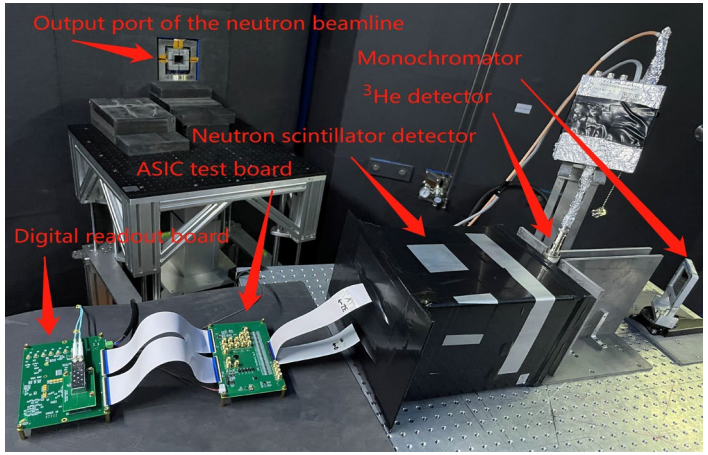


8-inch wafer

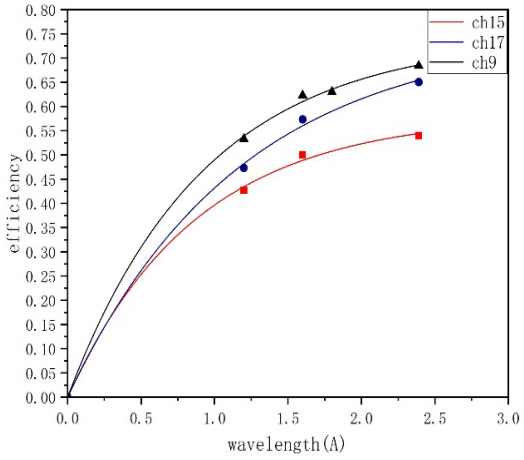
180 nm CMOS process



Layout



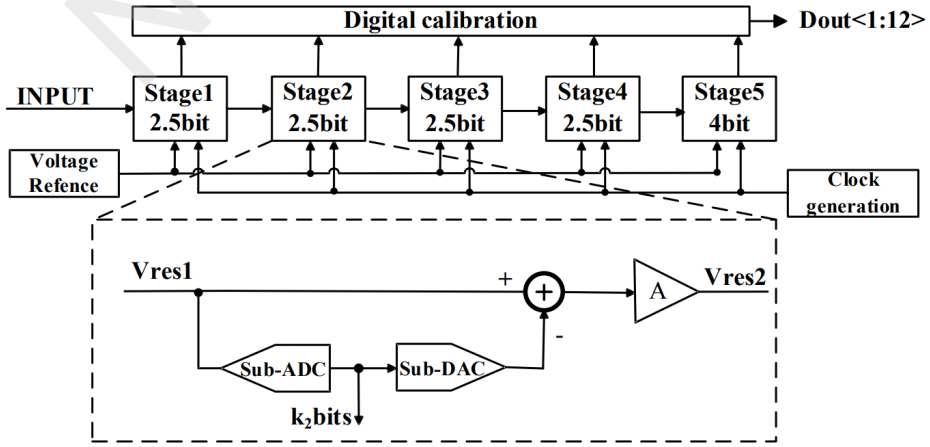

Detection efficiency test of the detector



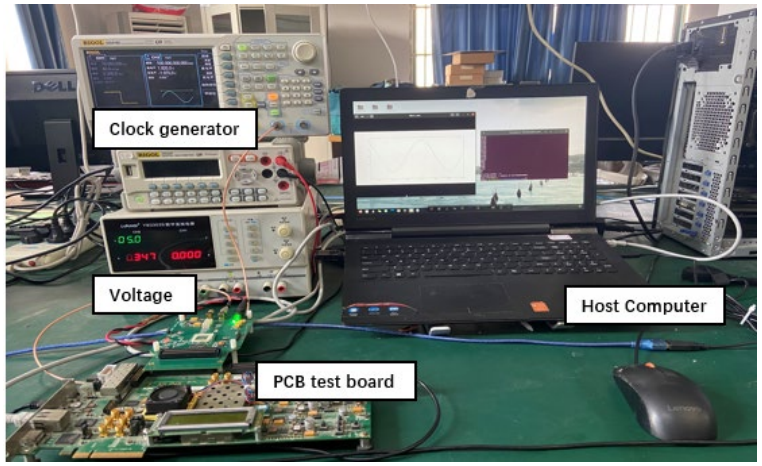

Detection Efficiency

| | Spec. |
|---|---|
| Dynamic Range | 120mV （@100Ω load） |
| Event rate | >200kHz/channel |
| ENV | <0.5mV |
| Power | <3mW/channel |

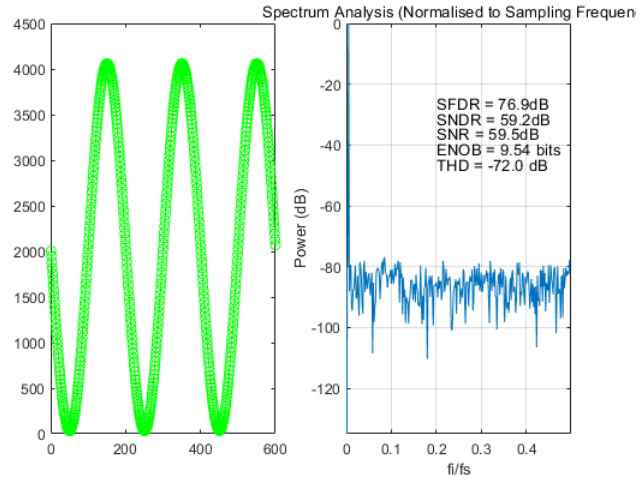
# 40Msps 12bit Pipeline ADC (tested)



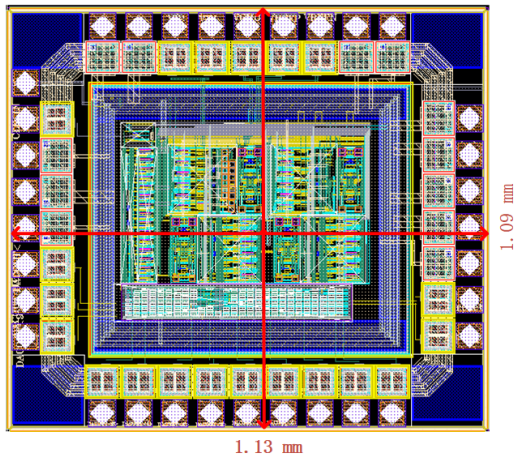

Block diagram of the Pipeline ADC



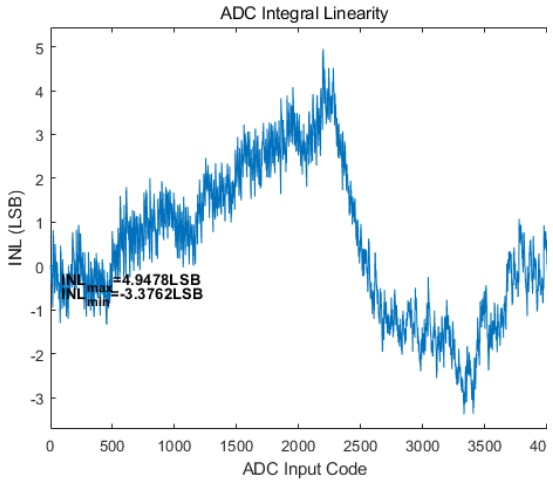

Test system of the Pipeline ADC



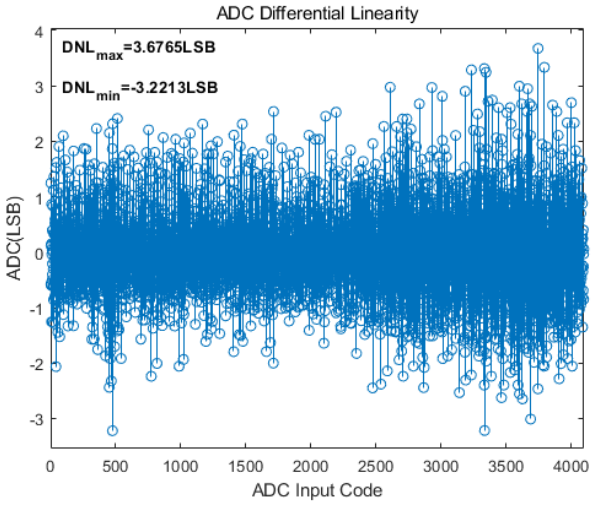

Test results of the Pipeline ADC




layout




INL of the Pipeline ADC




DNL of the Pipeline ADC

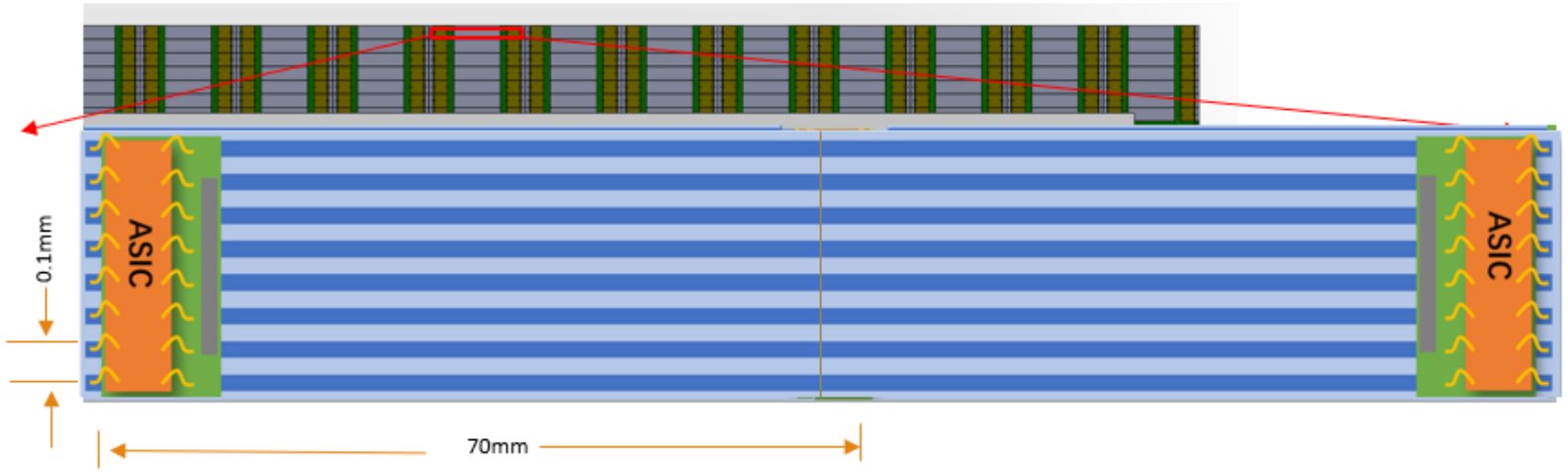
- 180 nm CMOS process
- Design: 12 bit 40MS/s
- test results: ENOB 9.54bit
- Power: ~28mW

# SiPM ASIC小结

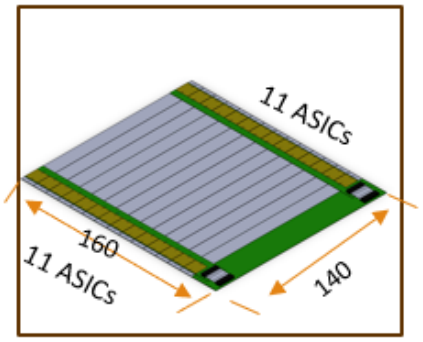
- 所有关键芯片模块均已有前期设计经验，没有明显障碍
- 主要困难：以样机为目标的3年研发周期
  - 7000chn样机必然需要工程批量产级流片（成本高）
  - 3年时间从第0版设计开始，时间非常非常紧张！
- 工作方案：
  - 第一年全力以赴实现第一版实现主要性能，和必要功能
  - 视该芯片实测结果，决定：
    - 如有明显问题： 1. 联系公司已有芯片，确保样机3年验收；自主芯片按长期路线（5年）研发。
    - 如实现基本目标：2. 自主芯片按3年实现初版工程批确保验收；继续按长期路线（5年）优化
- 必要前置条件：
  - 探测器方案、参数、需求（第一版）最终确认，在3年时间内确保不进行大调整
  - SiPM选型确认，在3年时间内确保不进行大调整

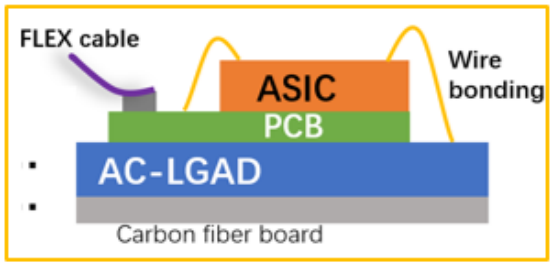
# Requirement of LGAD detector

**Ladder**



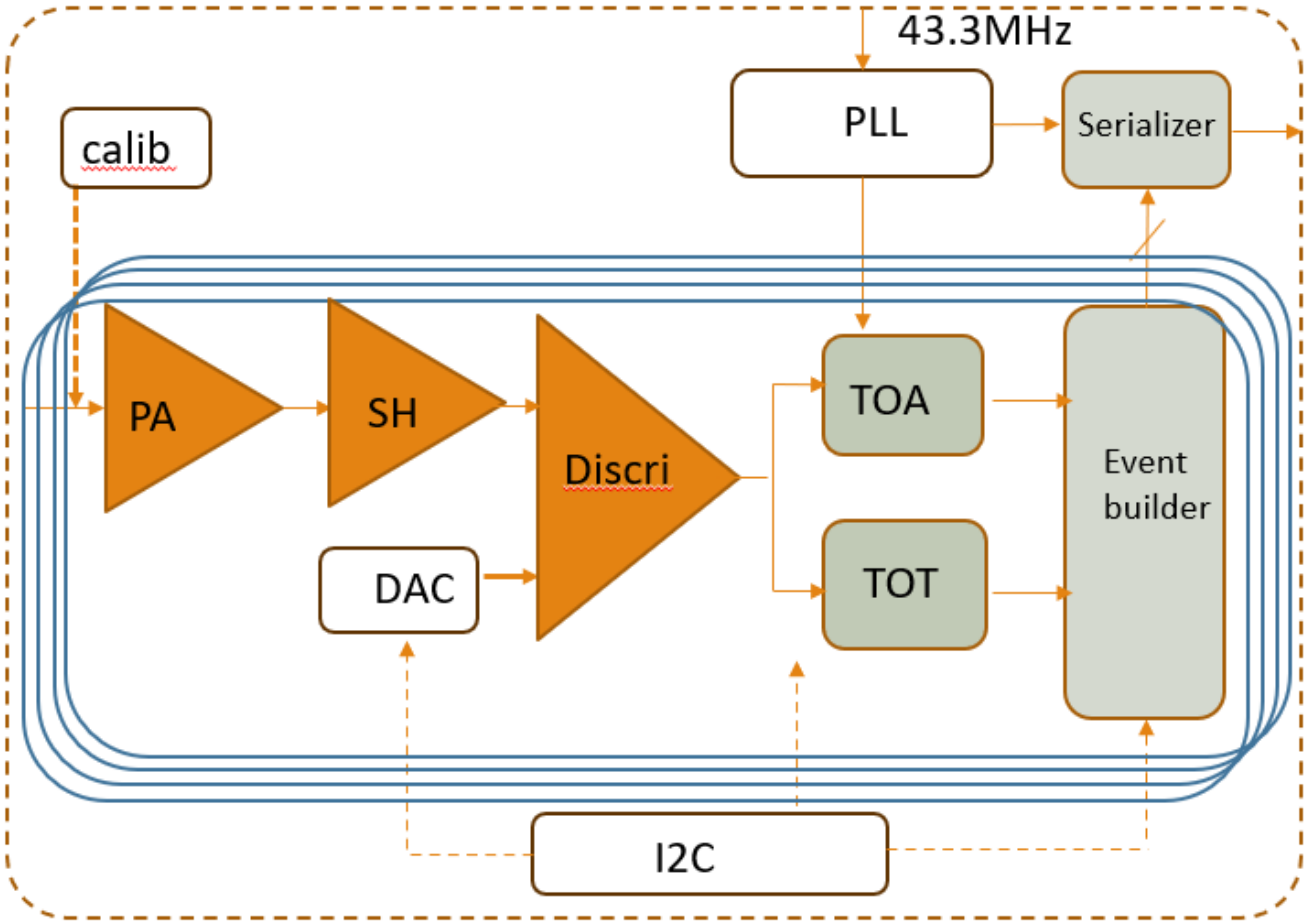

**Module**
**140mm x 160mm**




| | Barrel | Endcap |
|---|---|---|
| 信息需求 | TOA，TOT | |
| Area ($m^2$) | ~ 70 | |
| Granularity | 70mm × 0.1mm (10平方厘米，每个芯片128道) | |
| Capacitance | ~10 pF | |
| Charge | >16fC | |
| MIP Time resolution | ~50 ps | |
| Charge resolution | ? | |
| Spatial resolution | ~ 10 μm | |
| Number of Module | 3780 (14cm*14cm) | 480 |
| total NO. of chips | 83160 (128道/chip) | 11520 |
| Data size | 40-48 bits | 40-48 bits |
| Event rate | 140 Hz / cm2 | 35K Hz / cm2 |
| consumption | 20mW/ch | 20mW/ch |

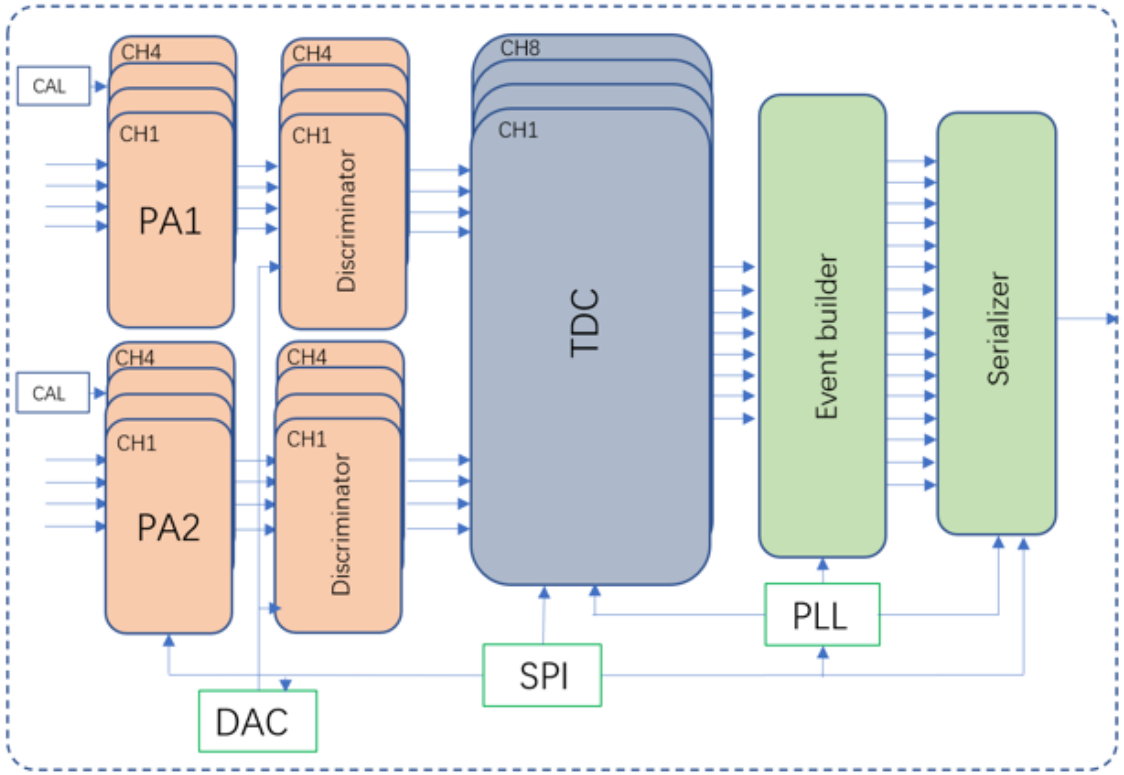
# LGAD readout Chip

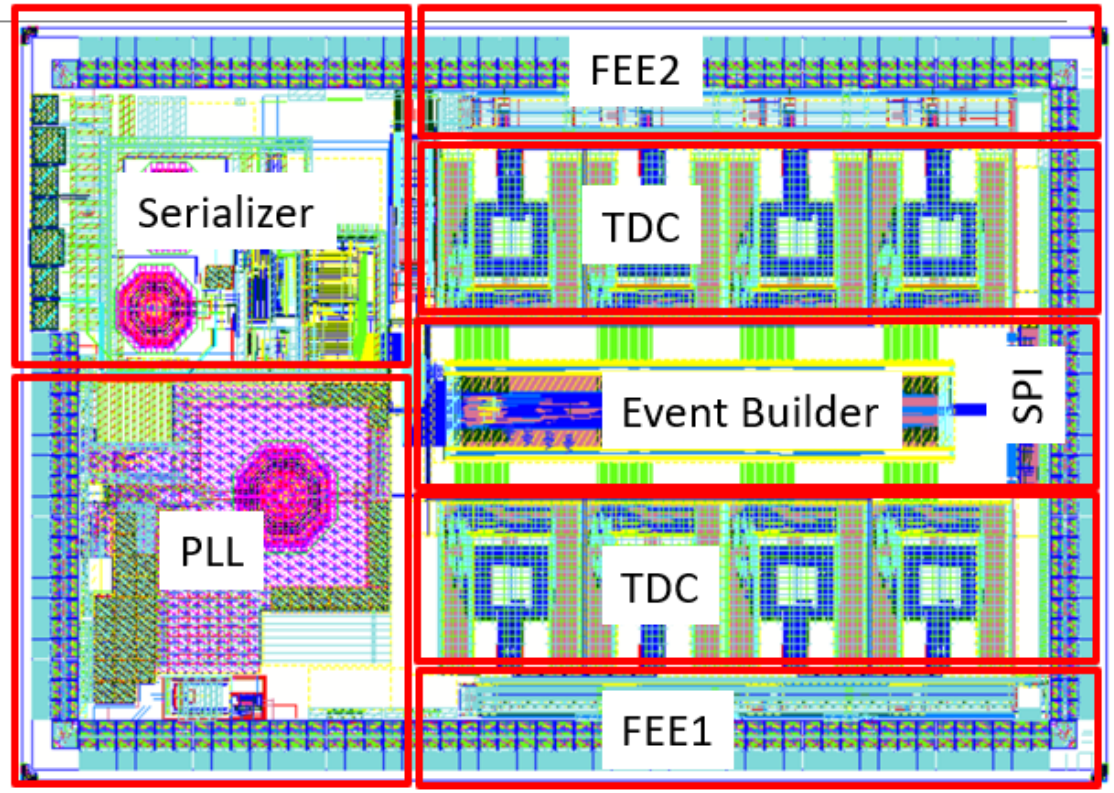



- 流片工艺: 55nm
- 输入动态范围：16-？ fC
- 通道数：64/128
- 功耗：20mW/ch
- 供电：1.2V
- TID：？
- 时间分辨（辐照后）：30ps @16fC w/ 10fF Cs
- 转换时间：23.1ns

- FEE（PA+SH+Discri）：阻抗匹配、放大+成形+甄别
- Calib：刻度电路
- DAC：提供阈值和输入电荷刻度
- TDC：TOA前沿时间测量，TOT修正time walk,电荷测量
- PLL：为TDC和serializer提供时钟
- Serializer：TDC数据串行输出
- Event Builder：TDC数据整理打包、编码
- I2C：配置寄存器

# FPMROC_V0芯片　Previous experience & ongoing R&D




- 2种前放方案
  - 方案1：带宽大，增益小
  - 方案2：带宽小，增益大

- 流片工艺：SMIC 55nm
- 2024年7月中旬提交流片，预计11月下旬回来

# 仿真结果

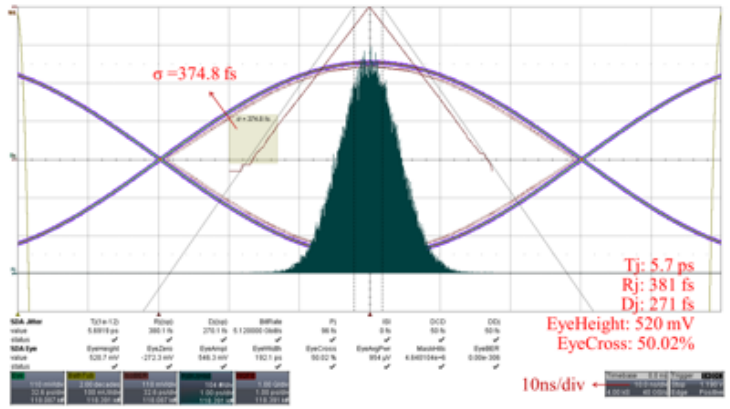
| Parameter | FPMROC Simulation |
|---|---|
| FEE | < 5 ps |
| TDC TOA resolution | 13.0 ps |
| TDC TOA range | 0.7ns-24.3ns |
| TDC TOA INL | <0.7LSB |
| TDC TOA DNL | <0.6LSB |
| TDC TOT range | 200ps~3.25ns |
| Core Power Consumption | 40mW/ch |

## PLL

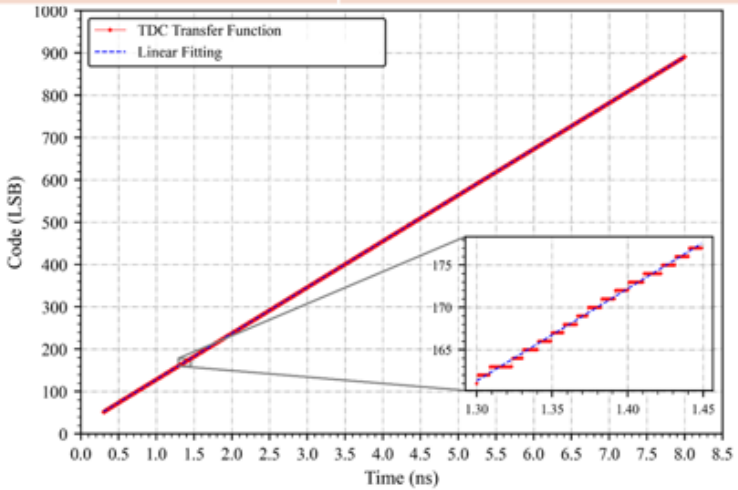
- 锁频范围：4.74~5.92GHz
- 5.12GHz二分频时钟噪声：随机晃动Rj < 460fs

## Serializer

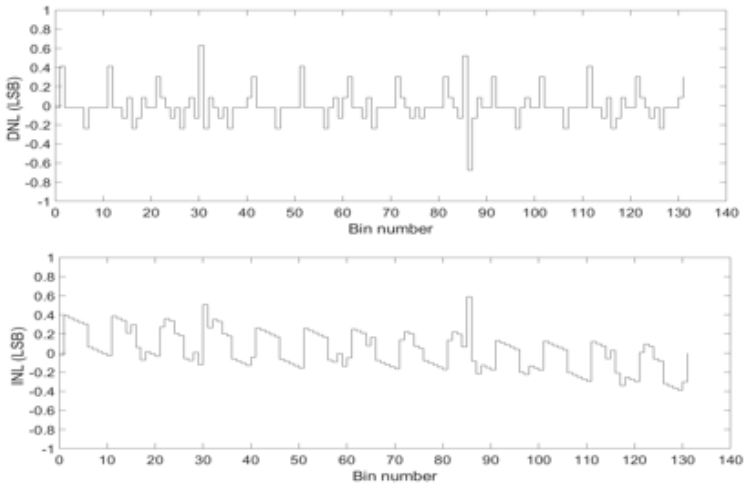
- 64:1 并串转换
- 最高串行速率10 Gbps



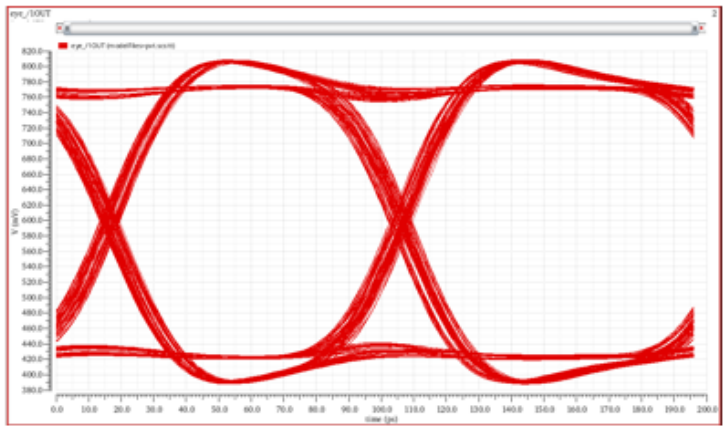

PLL jitter performance




TOA transfer function




TOA INL/DNL



Serializer eye diagram

# OTK AC-LGAD ASIC小结

- 针对高精度时间分辨为核心目标的ASIC及电子学系统研发已开展
- 当前主要问题：
  - 探测器需进一步优化，特别是电极长度 vs Cd vs 探测器排布
    - 例：电极尺寸7cm→2cm，总功耗将降低几倍，但通道数增加4倍，且排布方案需重新考虑。应探测器电子学联合优化至一个合理值，不应盲目一味降低尺寸
- 工作方案：
  - OTK ASIC研发队伍与SiPM ASIC队伍有重叠
  - 预计探测器最终优化并确定最终需求预计需要半年到一年，需结合实测
    - 与SiPM ASIC第一版研发时间错开
  - 以3年prototype为目标，不需要工程批流片
    - 基于针对FASTPMT研发的FPMROC，来实现探测器联调，可满足时间分辨性能（功耗未优化）
  - 针对最终CEPC OTK的读出芯片，待探测器最终优化后，以5年为长期目标进行研发

# Backup

# SiPM ASIC

# Timeline for all the FE ASICs – SiPM FE for CAL & Muon

- **2024：**
  - **Detector's final requirements to FE**
  - **SiPM's final selection for FE design**
- **2025：**
  - **The first version of SiPM ASIC: with main analog performance and basic digital functionality**
  - **Test & verification of the SiPM ASIC 1st with main performance**

- **If mostly verified**
  - **2026：**
    - **Chip debugging & optimization (2nd MPW)**
  - **2027：**
    - **1st Engineering**
    - **Prototype for the 7000chn HCAL**
  - **Comment:**
    - **Rough price of the existing chip is too high for a mass production prototype**
    - **Self-R&D is necessary for the final CEPC ECAL**

- **If critical issues found**
  - **2026：**
    - **Contact for existing chip (minor modification might needed); find for (international) collaboration**
  - **2027：**
    - **7000chn HCAL prototype based on xxx chip**
  - **2026~2029：**
    - **SiPM ASIC design with 2 MPW + 1~2 engineering run, aiming for real CEPC CAL**

# HGCROC2 overview

## Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

## Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

## Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

## Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

## Ancillary blocks

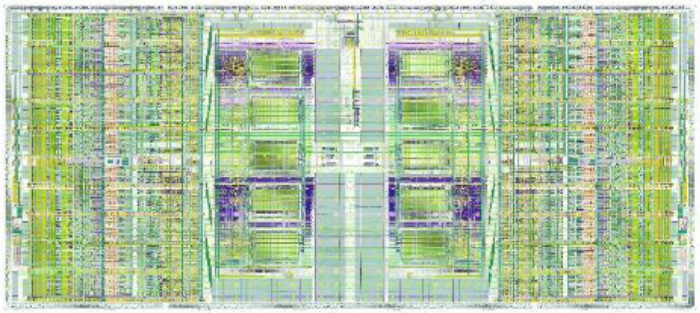
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

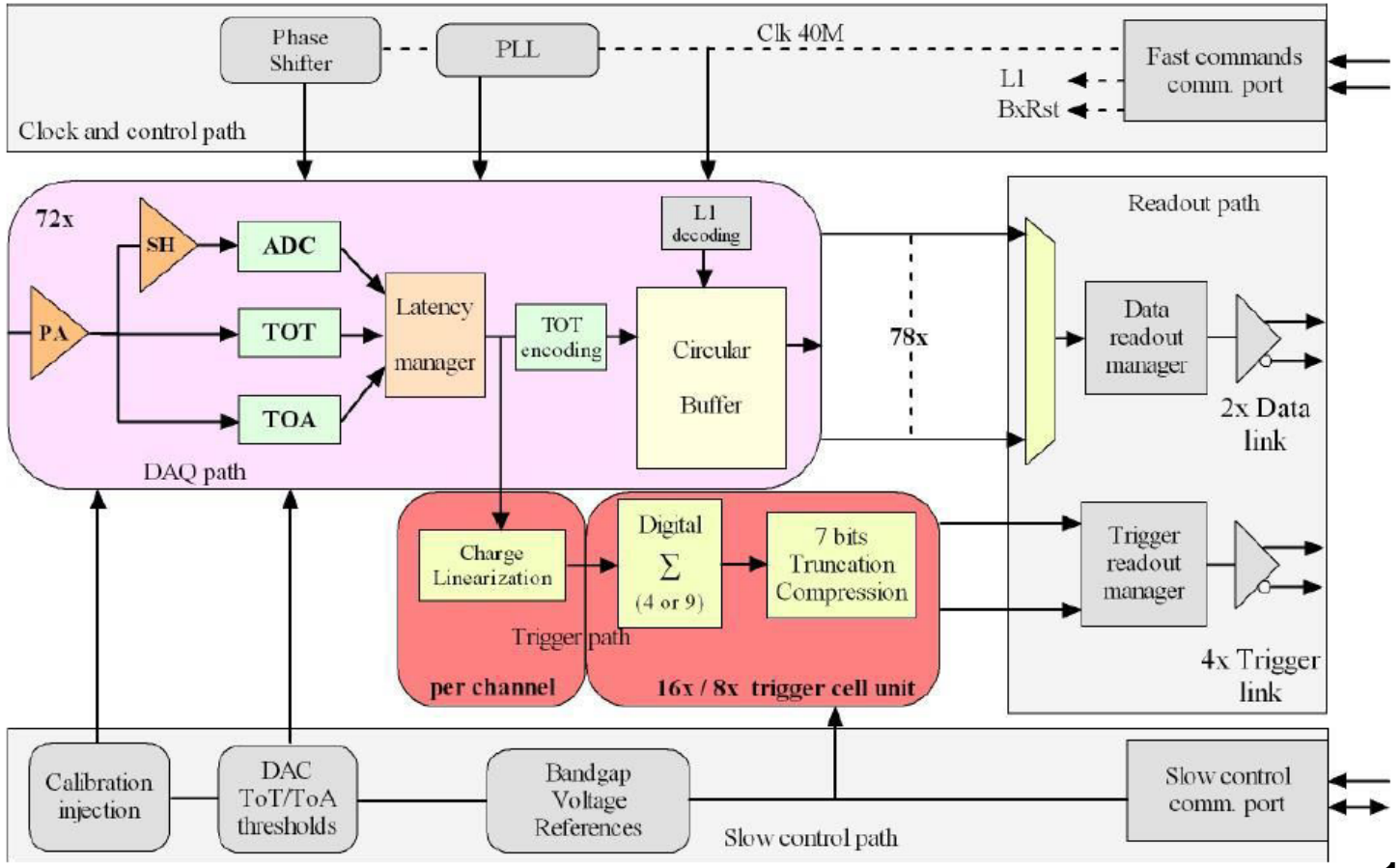
AGH

CERN

Irfu

ΩMEGA Microelectronics





# 参考芯片：DIET

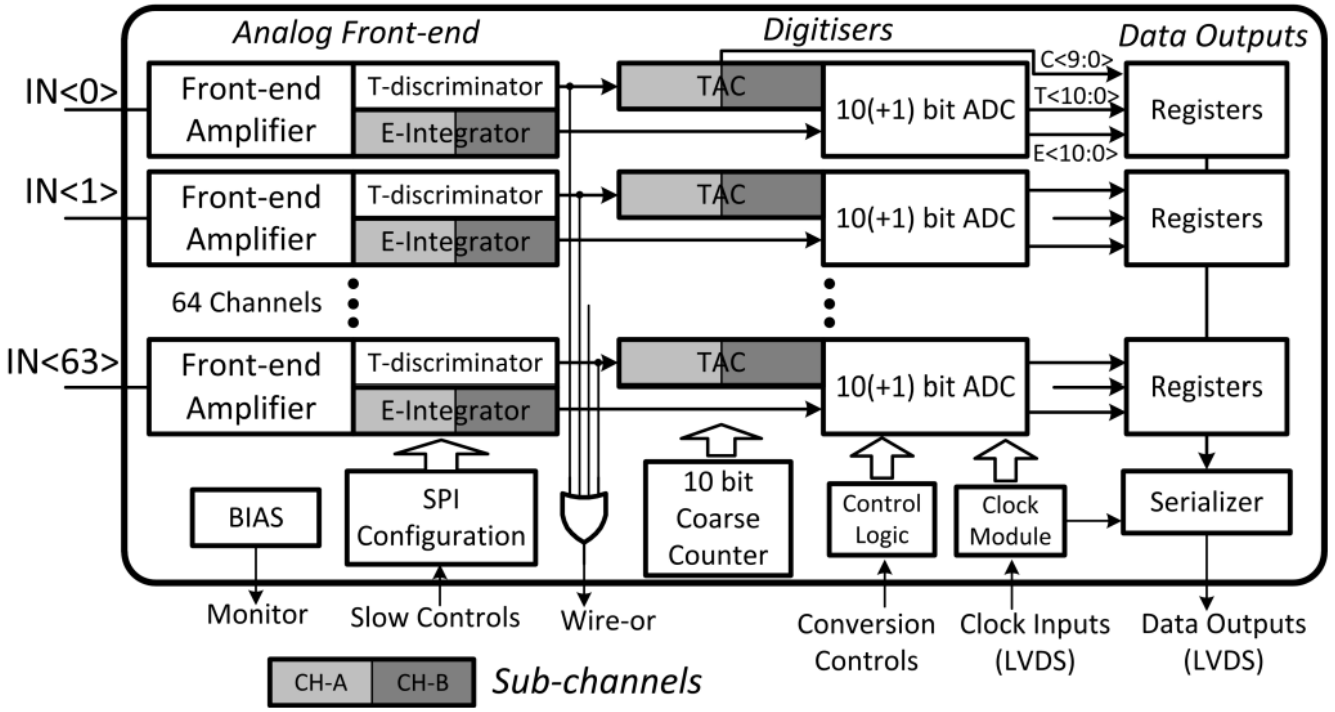



**Figure 1**. The block diagram of the DIET ASIC.

**Table 1**. The specification of the DIET ASIC.

| Parameters | Specifications |
|---|---|
| Maximum Input Current | 5 mA |
| Input Dynamic Range | 0 ~ 46 pC (Low Range)<br>0 ~ 96 pC (High Range) |
| Integral Non-Linearity for Energy | Better than 1% |
| ADC Resolution | 10 bit (1 extra bit for calibraion) |
| Timing Jitter | ~ 25 ps rms @ $C_{in}$ = 12 pF and threshold is 20 photoelectrons (80 μA) |
| (Fine) TDC Resolution | 10 bit (1 extra bit for calibration) |
| (Fine) TDC Bin Width | 25 ps |
| Power Consumption | 5 mW / channel |
| Conversion Dead Time | 12.5 μs |
| Readout Bandwidth | 200 Mbps |
| Number of Channels | 64 |

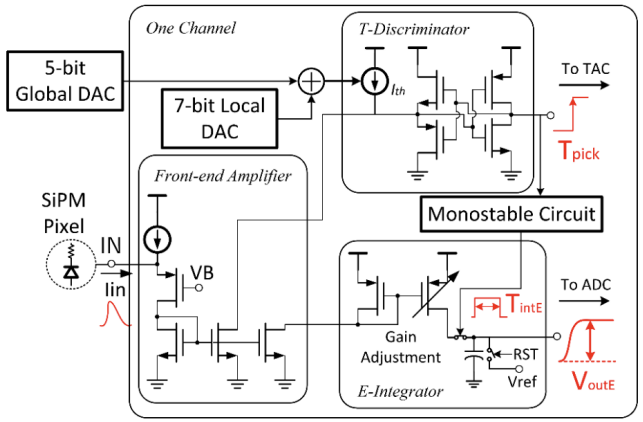



**Figure 2**. The block diagram of the analog front-end circuit.

# 参考芯片：SPIROC2C

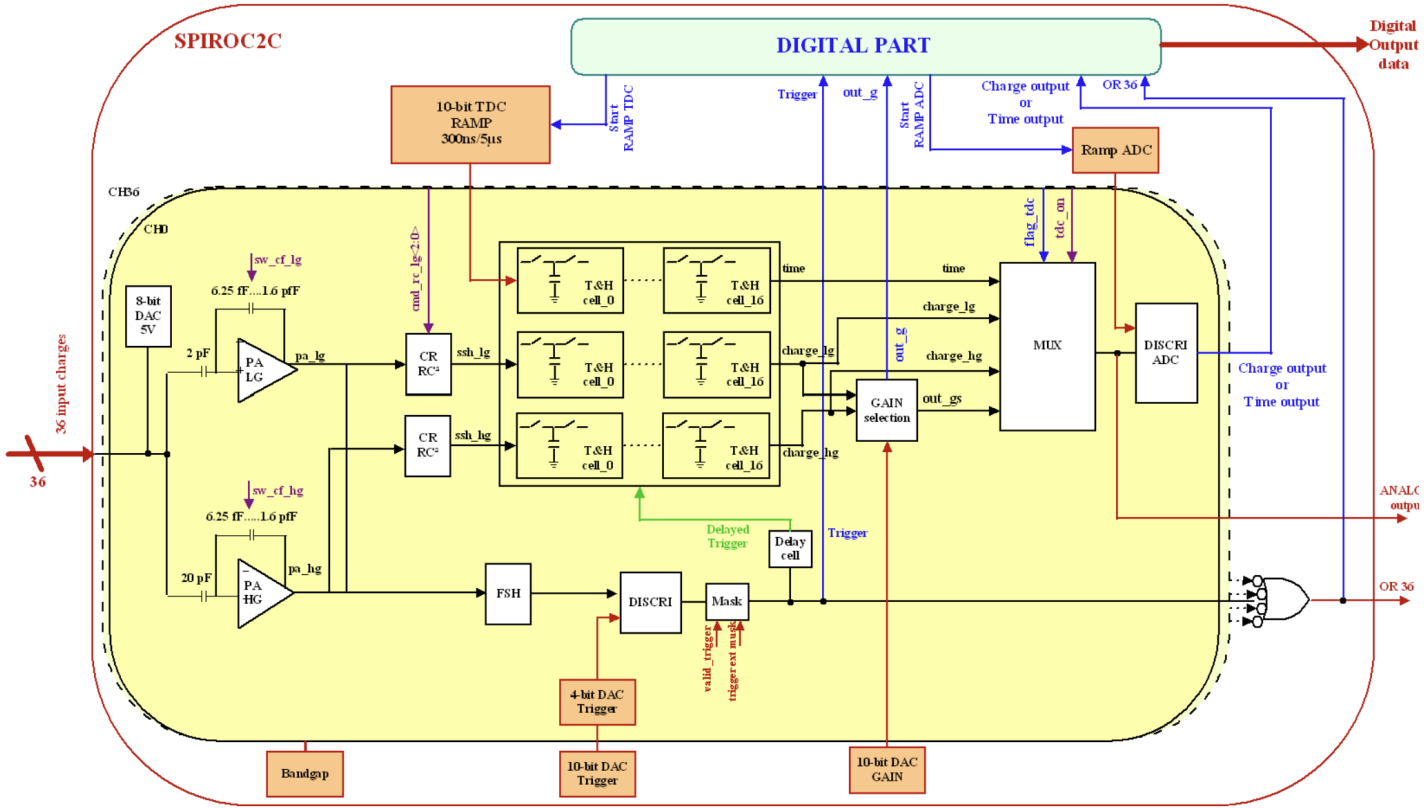



**TABLE I** SPIROC MAIN SPECIFICATIONS

| | |
|---|---|
| dynamic range | 80 fC – 200 pC |
| signal to noise ratio | ~7 (SiPM gain = $10^6$) |
| analog output INL | $< \pm 1\%$ |
| pedestal uniformity | $\sigma = 2$ mV |
| crosstalk | $< \pm 0.3\%$ |
| effective noise charge | $1.5 \times 10^5$ electrons @ 50pF (50ns shaping) |
| ADC resolution | 0.6 mV (LSB) |
| timing resolution | 100 ps |
| time walk @ 1/2 MIP | 3ns |
| time jitter @ 1/2 MIP | $< \pm 2$ ns |
| trigger efficiency | 100%@1/3 photon electron |
| trigger noise | 8 mV |
| input DAC INL | $< \pm 2\%$ |
| input DAC range | 0.5 – 4.5 V |
| threshold DAC range | 2 V |
| threshold DAC INL | $\leq \pm 1\%$ |
| power consumption | $25\mu$W per channel[1] |

# OTK ASIC

# ALTIROC （vernier ）

- 采用游标型延迟链结构
- 时间分辨：25ps @ 4fC
- 像素尺寸1.3mm*1.3mm（Cs=4pF）
- 功耗：4.4mW/ch

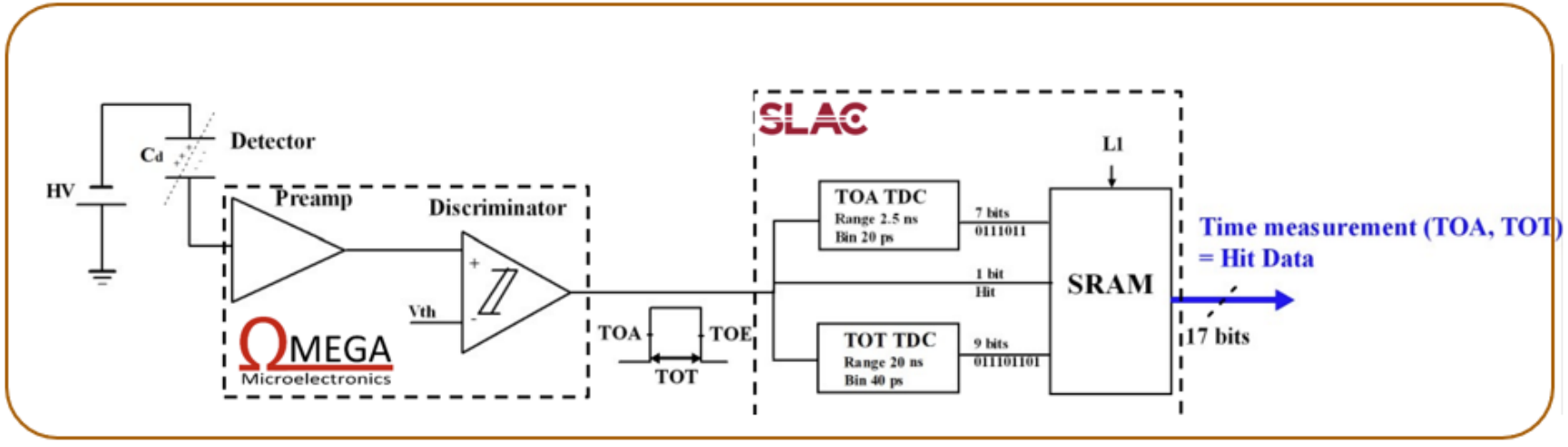
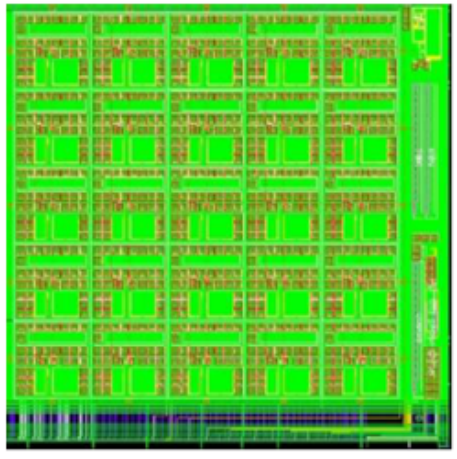
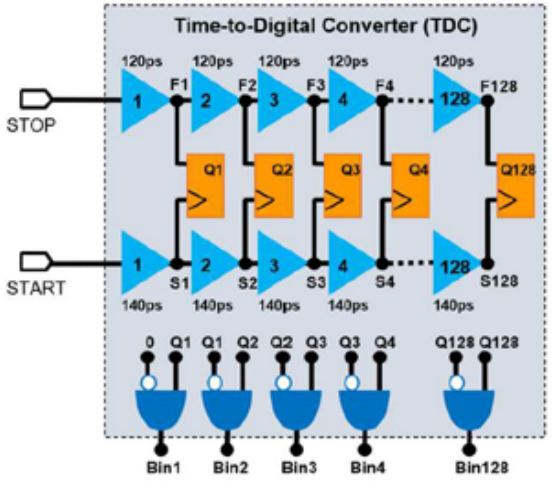
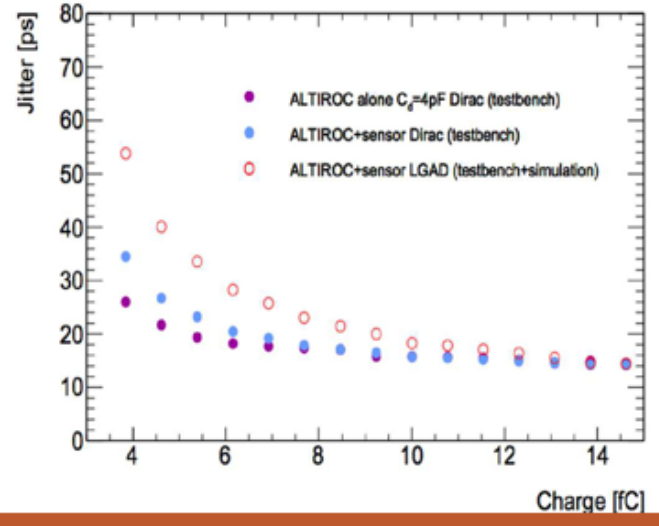



TABLE II. ASIC REQUIREMENTS

| Criteria | | Max. | Conditions |
|---|---|---|---|
| Total hit jitter | initial : | 35 ps | at 10 fC |
| | final : | 70 ps | at 4 fC |
| ↳ Landau jitter | | 25 ps | for un-irradiated LGAD |
| ↳ Clock jitter | | 15 ps | |
| ↳ Electronic jitter | | 20 ps | |
| ↳ Time walk jitter | | 10 ps | |
| ↳ Front-end jitter | | 10 ps | |
| ↳ TDC jitter | | 10 ps | |
| TDC conversion time | | 25 ns | between 2 bunch crossings |
| Single PAD noise (ENC) | | 3000e⁻ | (= 0.5 fC) |
| Minimum detectable charge | | 2 fC | |
| Dynamic Range up to | | 50 fC | |
| TID tolerance | | 2 MGy | |
| Neutron fluence | | 2.5 $10^{15}$ | $n_{eq}/cm^2$ |
| Full chip SEU probability | | 5% per h | |
| Supply voltage | | 1.2 V | |
| Power dissipation | | 1.2 W | Full targeted ASIC : 225 ch. |
| ↳ Per channel | | 4.4 mW | |
| ↳ Common part | | 200 mW | |
| Temperature | | -30 °C (± 10) and room temp. for qualif. | |

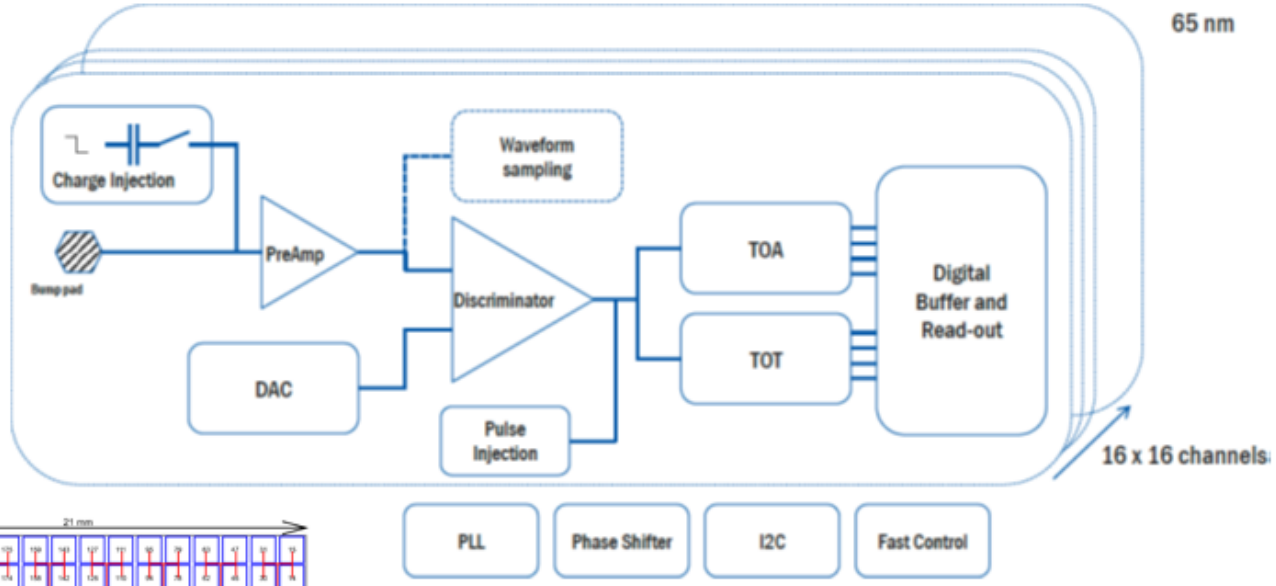


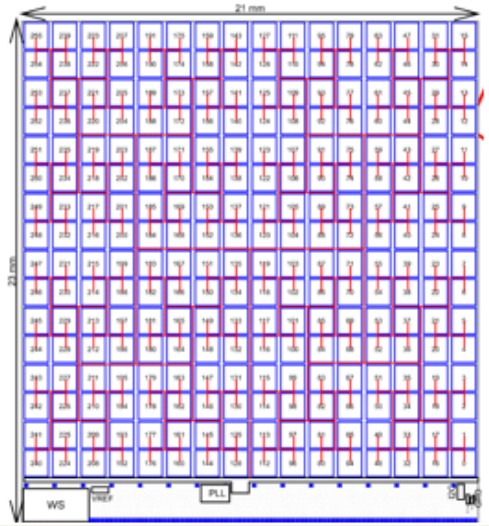


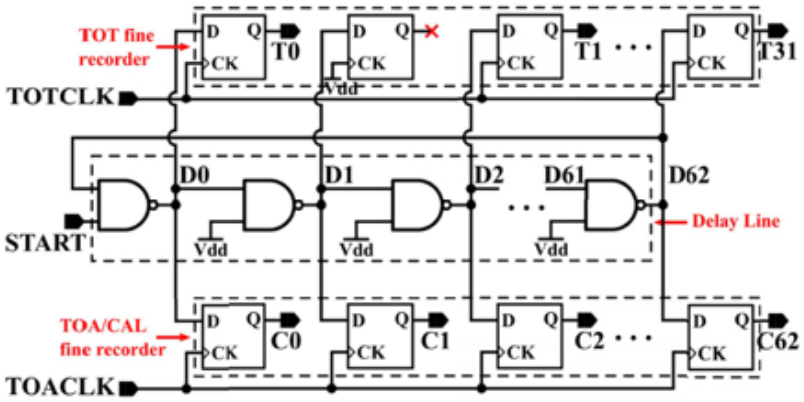



# ETROC

- 总体结构与AlTIROC类似，FEE结构类似
- TDC核心延迟链采用单链结构
- 时间分辨：20ps @16fC
- 功耗：4mW/ch（FEE 1.5mW/ch）
- 像素尺寸1.3mm*1.3mm（Cs=4pF）





# Plan

2024.11-2024.12 LGAD读出方案研究和ASIC功能模块设计 。

2025.1-2025.6 ASIC功能模块流片，ASIC测试系统设计，ASIC性能测试，抗辐照测试。

2025.7-2025.12 ASIC设计改进，多通道集成设计 ，提交流片。

2026.1-2026.6 多通道ASIC测试系统设计，ASIC性能测试，抗辐照测试，与LGAD联调测试 。

2026.7-2026.12 多通道ASIC设计改进，128通道流片。

2027.1-2027.6 128通道ASIC性能测试，LGAD读出电子学系统样机测试、联调 。

2027.7-2027.12 128通道ASIC工程批