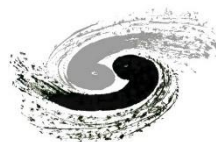




# Progress of CEPC ref-TDR TDAQ

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On behalf of CEPC TDAQ Group



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# Progress of TDAQ

## ■ TDAQ meeting

- Oct. 31<sup>th</sup> (Thu. afternoon), <https://indico.ihep.ac.cn/event/23791/>

## ■ Discussion of IDRC comments and recommendations

- Track trigger for Cal & Muon detector
- Low energy events: gamma-gamma collisions
  - Include in pair production of background simulation

## ■ Trigger simulation study

- BDT: energy + centre of gravity for Ecal&Hcal
  - Higgs: 1.34MHz->3.4kHz
  - Trigger efficiency 95%->99.9%, background 5%->0.25%
- Tracking @ Muon detector

## ■ Trigger rate discussion

## ■ Work plan for TDR

The screenshot shows the agenda for the TDAQ meeting on Thursday, Oct. 31, 2024, from 2:00 PM to 5:00 PM in Asia/Shanghai. The agenda is as follows:

Time	Topic	Speakers
2:00 PM - 2:10 PM	Introduction	Mr Fei LI (IHEP,CAS, Beijing, China), Jingzhou ZHAO (高能所), Xiaolu Ji (Institute of High Energy Physics, CAS)
2:10 PM - 2:20 PM	Simulation	Boping Chen, dong Liu (中国科学院高能物理研究所)
2:20 PM - 3:10 PM	Detector Survey	
2:20 PM	Vertex	Hongyu ZHANG (EPC, IHEP, CAS, China), 韩彦 (高能所)
2:30 PM	ITK&OTK	Sheng DONG (IHEP, CAS), Xiangyi Mu (高能物理研究所)
2:40 PM	TPC&DC	Hongyu ZHANG (EPC, IHEP, CAS, China), 韩彦 (高能所)
2:50 PM	Ecal&Hcal	Boping Chen, dong Liu (中国科学院高能物理研究所)
3:00 PM	Muon	Junhao YIN (南开大学), 刘明 季 (中科院高能物理研究所)
3:10 PM - 3:20 PM	Trigger Hardware	Jingzhou ZHAO (高能所), Sheng DONG (IHEP, CAS), dong Liu (中国科学院高能物理研究所)
3:20 PM - 3:30 PM	Readout Protocol	Hongyu ZHANG (EPC, IHEP, CAS, China), Sheng DONG (IHEP, CAS), 韩彦 (高能所)
3:30 PM - 3:40 PM	HLT	Boping Chen, Junhao YIN (南开大学), YI LIU (DESY), 启东/Qidong 周 (山东大学 Shandong University)
3:40 PM - 3:50 PM	DAQ software	Hongyu ZHANG (EPC, IHEP, CAS, China), Xiangyi Mu (高能物理研究所), Xiaolu Ji (Institute of High Energy Physics, CAS), YI LIU (DESY), 韩彦 (高能所)
3:50 PM - 4:00 PM	DCS&ECS	Sheng DONG (IHEP, CAS), 韩彦 (高能所)

# Trigger & Data Rate

## ■ Higgs 240GeV(50MW)

- Bunch cross rate: 1.34(2.9) MHz
- Physical event rate: 8 Hz (Higgs: 0.02 Hz)

## ■ Z pole 91GeV(10MW)

- Bunch cross rate: 12(14.5) MHz
- Physical event rate: 13.2 kHz
- L1 trigger rate: 120 kHz, DAQ: 240 GB/s
- HLT rate: 25 kHz (50 GB/s)

## ■ Z pole 91GeV(50MW)

- Bunch cross rate: 39.4(43.3) MHz
- Physical event rate: 66 kHz
- L1 trigger rate: 400 kHz, DAQ: 800 GB/s
- HLT rate: 100 kHz (200GB/s),

	Higgs	Z		W	$t\bar{t}$
SR power per beam (MW)	30	30	10	30	30
Bunch number	268	11934	3978	1297	35
Bunch spacing (ns)	576.9 ( $\times 25$ )	23.1 ( $\times 1$ )	69.2 ( $\times 3$ )	253.8 ( $\times 11$ )	4523.1 ( $\times 196$ )
Train gap (%)	54	17	17	1	53
Luminosity per IP ( $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ )	5.0	115	38	16	0.5

	Higgs	Z	W	$t\bar{t}$
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 ( $\times 15$ )	23.1 ( $\times 1$ )	138.5 ( $\times 6$ )	2700.0 ( $\times 117$ )
Train gap (%)	54	9	10	53
Luminosity per IP ( $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ )	8.3	192	26.7	0.8

- Compress 99% background -> 1% @ L1
- Compress 90% background -> 0.1% @ HLT
- Data size per BX @ Higgs: 300 Kbyte
  - Unknown @Z
- Event size < 2 MByte
  - Related to occupancy and read out window

# Working Plan for TDR

- 先根据河南技术方案修改一个版本，一周。后面三周扩充内容。
- 模拟：
  - 第一周：事例率 ( Cal+Muon), muon tracking
    - 双gamma光子应对策略
  - 第二周：L1算法(Cal+Muon)算法，TDR editing
  - 第三周：TPC、OTK tracking，low lum. Z background.
  - 第四周：Global trigger start，TDR draft 0.1
  - 12月，TDR draft 1.0
    - HLT algorithm 结果
    - Global trigger
    - trigger efficiency

## Chapter 12 TDAQ and online

12.1	Introduction . . . . .	
12.2	Requirements and Design Considerations . . . . .	
12.2.1	Requirements . . . . .	
12.2.2	Event rate & background rate estimation . . . . .	
12.2.3	Technology survey . . . . .	
12.2.4	TDAQ policy consideration . . . . .	
12.2.5	TDAQ Interface with electronics . . . . .	
12.3	Trigger Simulation and Algorithms . . . . .	
12.4	Hardware Trigger . . . . .	
12.4.1	Previous experience on large facilities . . . . .	
12.4.2	System architecture . . . . .	
12.4.3	Common Trigger Board . . . . .	
12.4.4	Trigger Control and Distribution . . . . .	
12.4.5	Resource cost estimation . . . . .	
12.5	Software and High Level Trigger . . . . .	
12.6	Data Acquisition System . . . . .	
12.6.1	Previous experience on large facilities . . . . .	
12.6.2	Overview of System Functionality . . . . .	
12.6.3	Detector Readout . . . . .	
12.6.4	Dataflow . . . . .	
12.6.5	Network . . . . .	
12.6.6	Online Software . . . . .	
12.7	Detector Control System . . . . .	
12.8	Experiment Control System . . . . .	
12.9	Summary . . . . .	4

# Working Plan for TDR

## ■ 硬件触发

### – 11月

- Hardware trigger structure design for TDR
- trigger board/ TTC detailing
- BEE interface
- basic trigger primitives

### – 12月 :

- trigger primitives for each L1 detectors
- common trigger board structure finalize
- L1 algorithm deployment design, boards num

# Working Plan for TDR

## ■ HLT

- 11月
  - 编辑一页的FPGA加速
  - GPU, 概念性描述
  - 离线软件状况

## ■ DAQ

- 11月
  - system architecture
  - software layer data flow
  - RDMA/GPU/FPGA/Mem buffer
- 12月
  - Network/hardware
  - Online software

## ■ DCS

- 11月
  - DCS requirement from each detectors
  - farmwrok design

## ■ ECS

- 11月
  - framework design
  - control network
- 12月
  - IT infrastructure
  - hardware
  - control/computing room
  - monitoring

# Backup

# Findings--revised

- The baseline plan is to transmit the full raw data to the **front-end** electronics and connect the trigger to the back-end electronics.
  - Transmit the full raw data from front-end electronics(on-detector) to **back-end** electronics(off-detector)
- A hierarchical trigger scheme is foreseen to bring event data rates down from **~3MHz** to **~1kHz** in ZH running and **~40MHz** to **~100kHz** at the Z pole.
  - The bunch cross rate in ZH running is about **1.34 MHz** when bunch space is 346.2 ns (2.9 MHz) and there is 54% bunch train gap.



# Comments

- The detailed (bottom-up) design of the TDAQ must await further details on the sub detector design.
  - We will closely follow the design of each sub detector. Especially background study and data rate estimation from each sub detectors.
- Work on the trigger primitives is needed to bring the rate down to an acceptable input for the second-level trigger, and to inform further planning for the processing farms in the DAQ design. Should it be needed, a track trigger could provide a powerful additional primitive.
  - More simulation works on trigger primitive and more discussion with physics and detector experts are needed. Track trigger simulation will be next main work.
- High-level triggering will also need to weigh the physics-versus-bandwidth tradeoff for lower-energy events, e.g. from gamma-gamma collisions.
  - We need more study for low-energy events of beam induced background. And few gamma-gamma collisions are included in the available background sample data. <sub>9</sub>

# Recommendations

- A simple simulation of sub detector-based trigger inputs using simple, robust algorithms should be prioritized to allow more detailed specification of the requirements for TDAQ hardware and identify areas that need further attention. This should include an appropriate safety factor for beam-related backgrounds.
  - Basic trigger simulation study for each sub detectors are in progress.
  - And the safety factor needs to be discussed carefully.
- Further work should include an evaluation of benefits of implementing a track trigger as a complement to the calorimeter and muon primitives, and to clarify the bandwidth foreseen for gamma-gamma events.
  - We will move forward this after finish simple trigger simulation.

# Event Rate

## Higgs 240GeV(30MW/50MW)

- BX rate: 0.8(1.74)/1.34(2.9) MHz
- Physical event rate: **5Hz/8Hz** (Higgs: 0.02Hz)

## Z pole 91GeV(10MW/50MW)

- BX rate: 12(14.5)/39.4(43.3) MHz
- Physical event rate: **13.2kHz/66kHz**

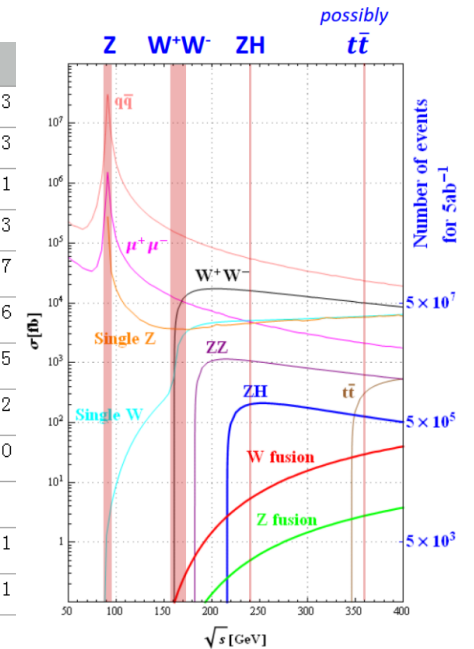
	Higgs	Z		W	$t\bar{t}$
SR power per beam (MW)	30	30	10	30	30
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	Higgs	Z	W	$t\bar{t}$
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 (×15)	23.1 (×1)	138.5 (×6)	2700.0 (×117)
Train gap (%)	54	9	10	53
Luminosity per IP ( $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ )	8.3	192	26.7	0.8

Process	Luminosity[ $ab^{-1}$ ]	Final states	X-sections(fb)	Events generate	Scale factor	Events expected
$e^+e^- \rightarrow e^+e^-$	5.6	$e^+e^-$	24770.90	4000000	346.79%	138717040
$e^+e^- \rightarrow \mu^+\mu^-$	5.6	$\mu^+\mu^-$	5332.71	4000000	746.60%	29863176
$e^+e^- \rightarrow \tau^+\tau^-$	5.6	$\tau^+\tau^-$	4752.89	4000000	665.40%	26616184
$e^+e^- \rightarrow \nu\bar{\nu}$	5.6	$\nu\bar{\nu}$	54099.51	3999999	757.39%	302957256
$e^+e^- \rightarrow q\bar{q}$	5.6	$q\bar{q}$	54106.86	9999023	303.03%	302998416

Higgs, Sample generation for CEPC, August 24, 2020

过程	xsection(nb)	百分比	事例率kHz
Bhabha	0.0586	0.001371951	0.068597543
muon	1.5361	0.035963374	1.798168703
tau	1.5249	0.035701158	1.78505791
qq	30.6522	0.717633315	35.88166573
电子中微子	2.9607	0.069316296	3.465814777
muon中微子	2.9896	0.069992906	3.499645306
tau中微子	2.9909	0.070023342	3.501167095
中微子总	8.9411	0.209330202	10.46651012
总共	42.7129	1	50
		亮度	
30MW		1.15E+36	4.91E+01
50MW		1.92E+36	8.20E+01



Z pole, ref: MC /cefs/data/stdhep/CEPC91/  
2fermions/wi\_ISR\_20220618\_50M/2fermions/

# Trigger Rate

- Compress 99% background -> 1% @ L1
- Compress 90% background -> 0.1% @ HLT
- Related to occupancy and read out window Z pole 91GeV(10MW)
  - DAQ: 240 GB/s, storage rate: 25 kHz (50 GB/s)
- Z pole 91GeV(50MW)
  - DAQ: 800 GB/s, storage rate: 100 kHz (200GB/s)

## ■ Data size per BX

- 300Kbytes @ Higgs
- Unknown @Z

## ■ Event size < 2 MByte

	Higgs	Z(10MW)	Z(50MW)	W	tt
Bunch cross rate(MHz)	1.34	12	39.4	6.5	0.18
Phy. event rate(kHz)	0.008	13.2	66		
L1 trigger rate(kHz)	1.34	120	400		
High level trigger rate(kHz)	0.14	25	100		

# Data Rate

## Data rate before trigger

- <1 TB/s @ Higgs
- Several TB/s @ Z

## L1 trigger rate

- O(1k) Hz @ Higgs
- O(100k) Hz @ Z

## Event size < 2 MB

- Related to occupancy and read out window

## Storage rate after HLT

- <100 Hz(200 MB/s) @ Higgs
- 100 kHz (200 GB/s) @ Z

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024	512*128	1024	128		128	8~16				
Data Width /hit	32bit	42bit	32bit	48bit		48bit	48bit				
Avg. data rate / chip	0.18Gbps/chip, 1Gbps/chip inner	3.53Mbps/chip	21.5Mbps/chip	2.9Mbps/chip	38.8Mbps/chip	~70Mbps/module Inmost	10kHz/ch	10kHz/ch	5kHz/channel	5kHz/channel	10kHz/channel
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.39 M chn	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43,176 chn, 288 modules
Avg Data Vol before trigger	474.2 Gbps	101.7 Gbps	298.8 Gbps	249.1 Gbps	27.9 Gbps	34.4 Gbps	460.8 Gbps	187 Gbps	811.2 Gbps	537.6 Gbps	24 Gbps
Occupancy(%)	0.022	0.025(Strip)		0.35(Strip)		0.0028	0.58		0.002		0.038
Sum	3.2 Tbps = 400GB/s										

Collected from each detectors @Higgs