Preliminary consideration of the electronics room requirement with current detector design

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IHEP, CAS

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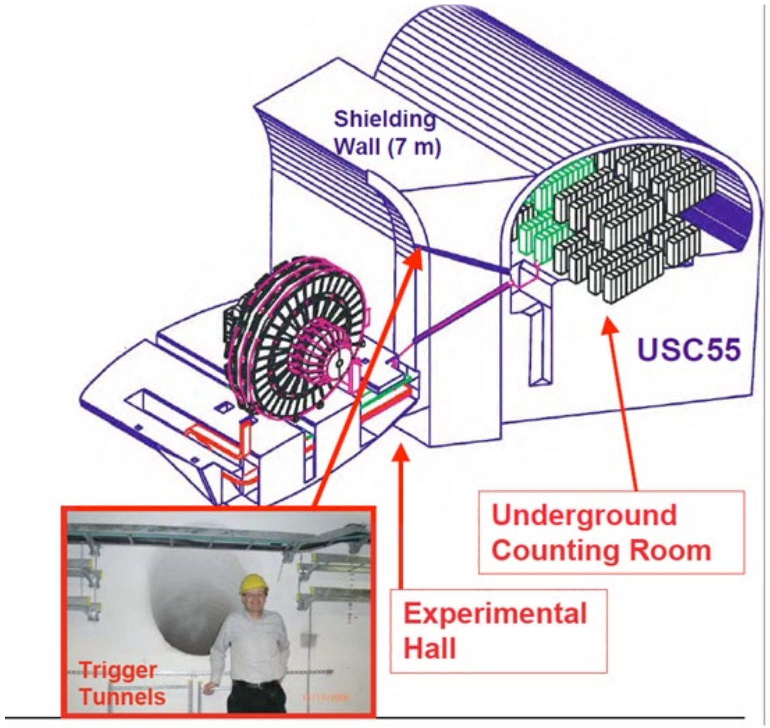
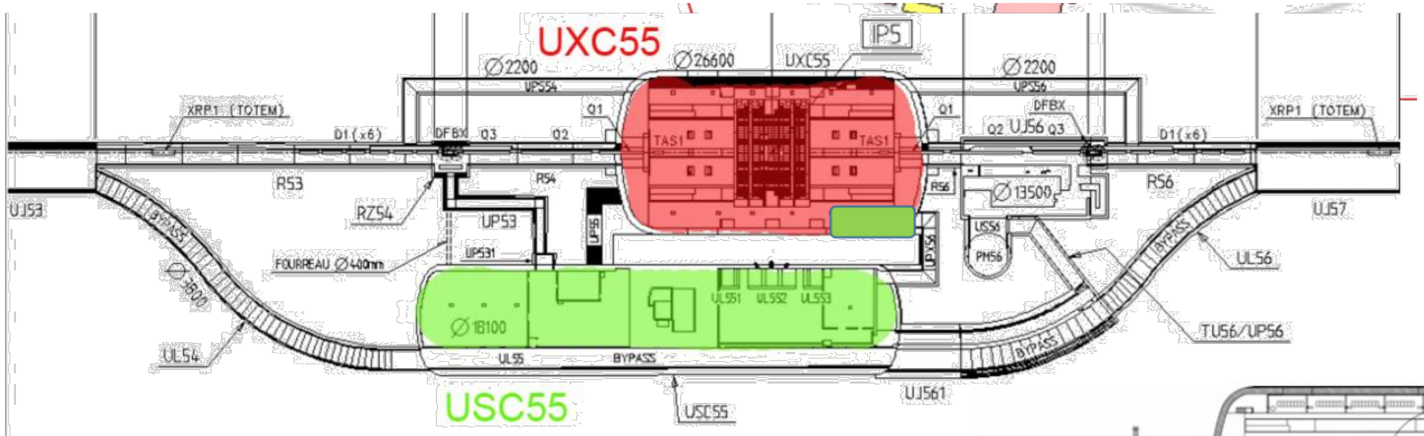
CEPC Day

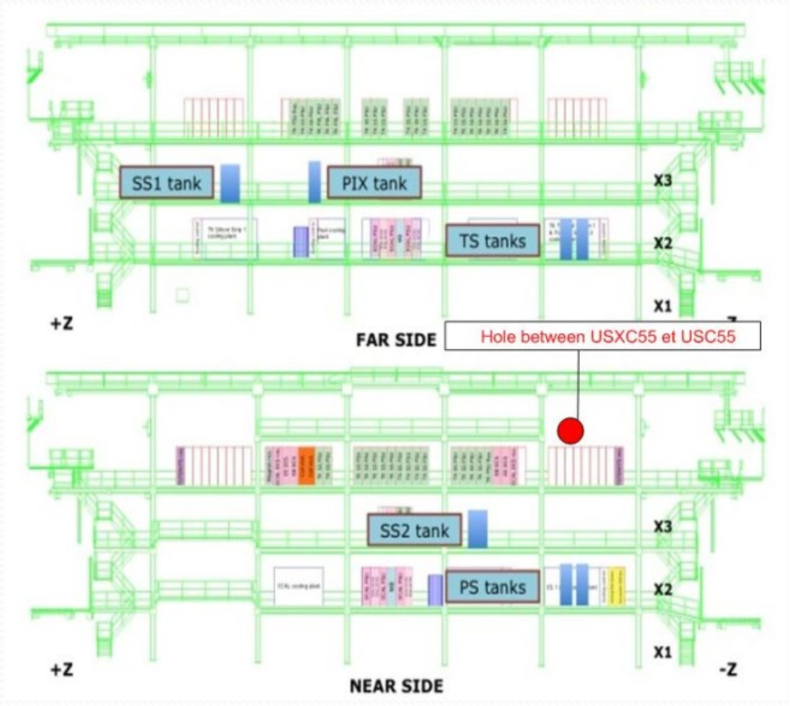
Outline

- Motivation
- Considerations on data link / power / HV according to the current
- Key parameters to calculate the cabling and crates
- Detailed calculation for each sub-detector
- Summary of the cabling and crates
- Comparison with the CMS counting room
- Rough estimation of the electronics-TDAQ room

Motivation – an example from CMS







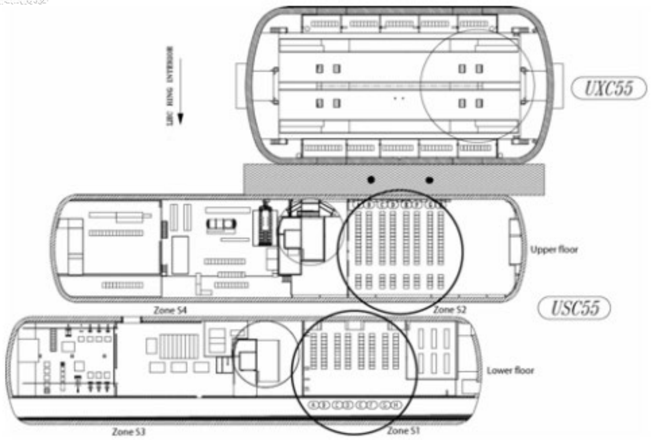
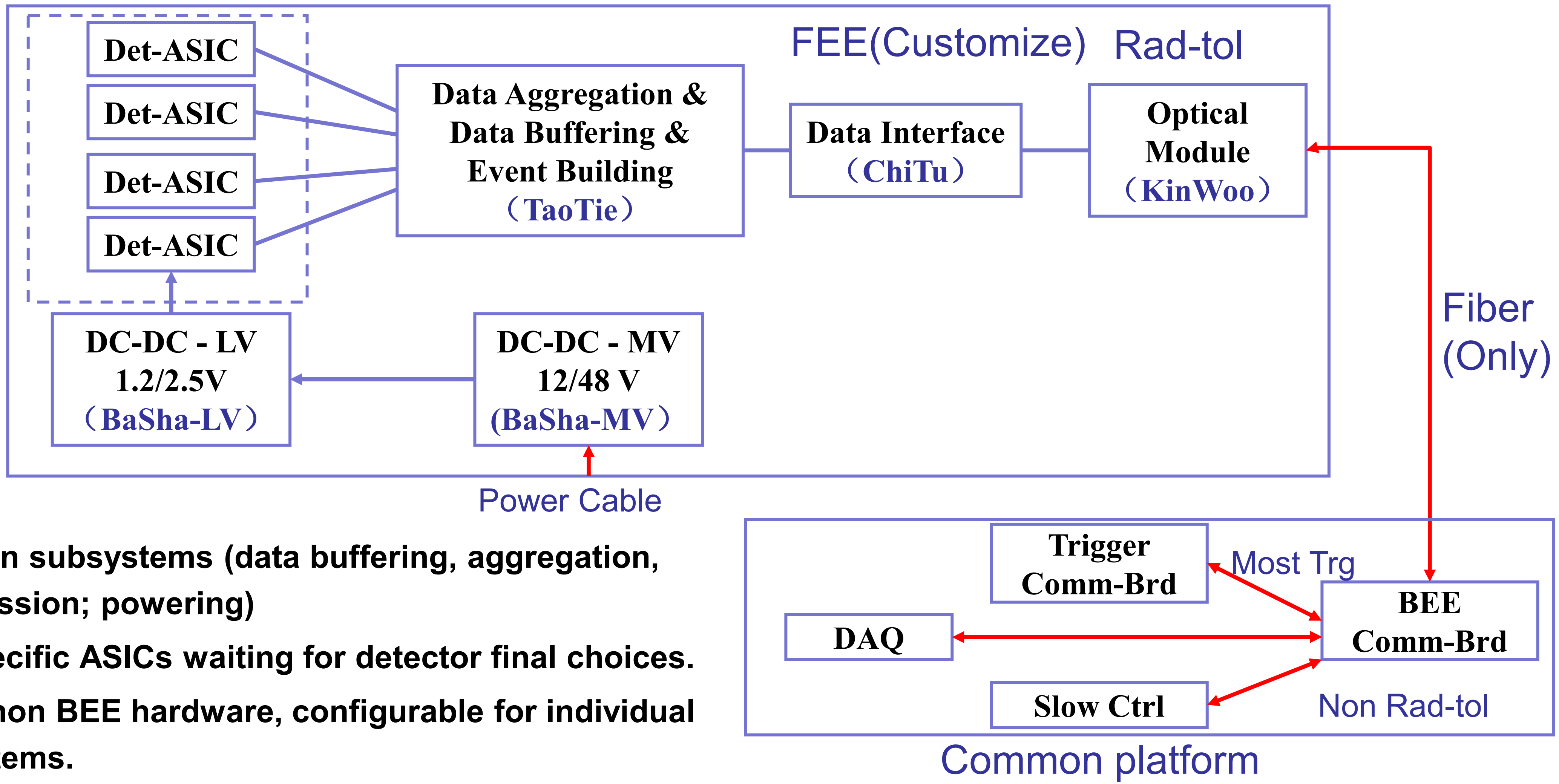


Figure 4: Point 5 Underground Area; The experimental cavern UXC55 with the adjacent, albeit a 7 meter thick concrete wall, underground counting room USC55, consisting of two floors.

https://cds.cern.ch/record/1027431/files/p165.pdf
https://doi.org/10.1007/978-3-031-12851-6_49
http://hep.wisc.edu/wsmith/cms/doc07/smith_trig_MEG_feb07.pdf

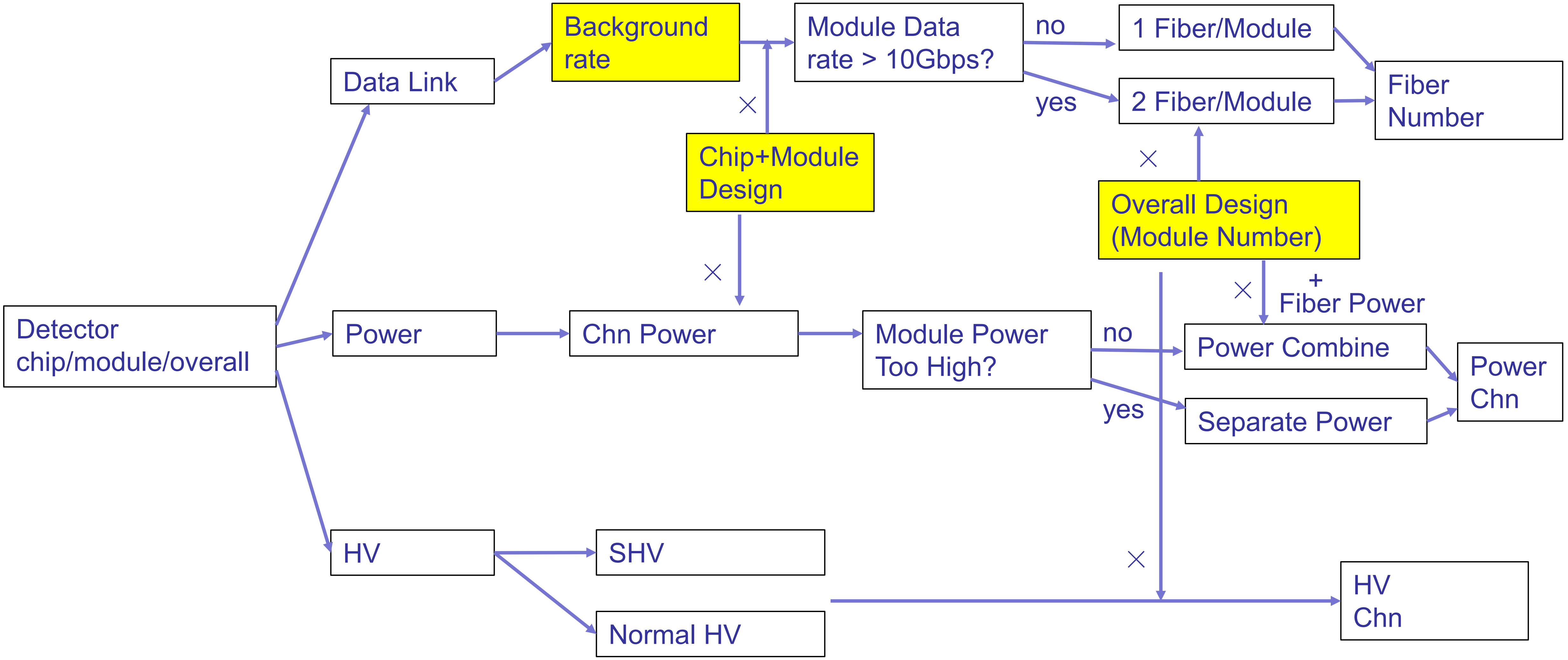
- **For the floorplan of the detector hall, to estimate the space requirement, and location preference**
- **Also connected to the installation strategy**

Global framework of the Elec-TDAQ system



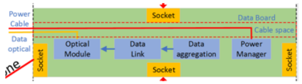
- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choices.
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

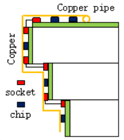
Consideration according to the detector design

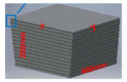


An example of sub-detector consideration (ECAL)

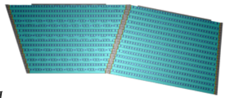
ECAL电缆估算

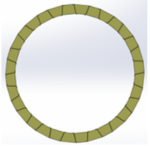


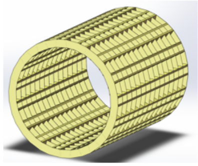




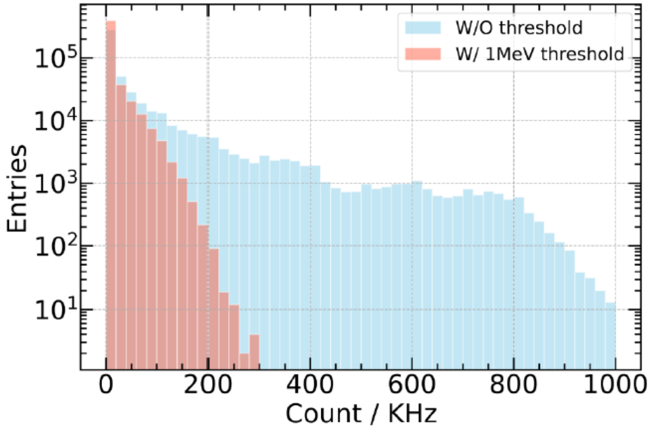
- ECAL桶部，正反梯形排布
  - 模块数量：Phi：32，Z：15，共480个模块
- 每个模块：
  - 1层到28层，奇数层每层36根，偶数层晶体数目不一致
  - 正梯形晶体数量1000，反梯形晶体数量992
- 电缆估算：1根/模块
  - AWG15（线径1.45mm，电流：6.5A/7.4A）
  - AWG18（线径1.08mm，电流：3.2A/3.7A）
  - 模块功耗估计：1000*2*20mW = 40W
- 光纤估算：1根/模块
  - 模块数据量估算：待定
- 桶部电缆总计
  - 类型：高压，低压（正负？），光纤
  - 电缆双向走向，每端240根（平均方案）
  - 电缆双向走向，一端224根，一端256根
- 未确定电缆：刻度方案







层数	反梯形	正梯形
2	27	39
4	29	37
6	29	37
8	31	37
10	31	37
12	33	37
14	35	35
16	35	35
18	37	35
20	37	35
22	39	33
24	41	33
26	41	33
28	43	33



- **The overall detector design: ~480 Module (Dual-trapezium scheme), ~1000 bar/module**
- **Current bkgrd estimation: avg. event rate 100kHz / crystal bar w/ threshold; Data width 48bit/event (current ASIC scheme)**
- **@Dual readout each crystal bar, total data rate: 1000*100kHz*48bit*2ends=9.6Gbps, not possible for 1 fiber for each module, at least 2 fibers for each module**
  - **For max. bkgrd rate@300kHz@Higgs, also needs enough room**
  - **For Z pole, bkgrd will be much higher, also needs extra room**

An example of sub-detector consideration (ECAL)

- **Data Link:**
  - Fibers: 480*2=960, -> 60 BEE Brds, 6 crates
- **Power:**
  - ASIC: 15mW/ch, each module 1000*2*15mW=30W
    - Within the capability of DC-DC power module
  - Data Link + Optical Power: 1W each
  - Total Power: 31W/0.85*480=17.5kW
    - Efficiency of the DC-DC: 85%
  - Power chn 100W/chn, each module per power cable: 480 power chn -> power crates 10
- **HV:**
  - Sch 1: one HV chn for each module, (limitedly) compensated for each SiPM in ASICs
  - HV channels = module number = 480， -> 2 HV crates

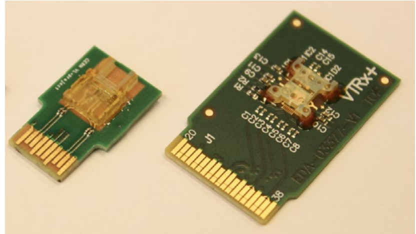
  - Alt sch2：HV chn for each SiPM? Too many channels & too large control data volume (×)
  - Alt sch3：HV chn for sub-region of a module, to compensate the temperature gradient
    - Maybe much optimized than sch1，but rely on the detector simulation

Note for the calculation

- Avg. & Max background rate both are important
  - Max bkgrd rate to calculate the room for the data rate
  - Avg bkgrd rate to calculate the total data rate for the electronics –TDAQ interface
- Detailed detector design, including the module vs. chip, is necessary for the electronics cabling, powering and HV scheme
  - Chip on module to evaluate electronics readout scheme (data link, power, aggregation)
  - Overall detector design to evaluate the cabling, HV and crate channels
- According to the current electronics design, most detector module following the "1 fiber + 1 Power" manner
  - Most module data rate at the level of Gbps, a fiber channels @10Gbps level is proper
  - Although the room for a power channel at the module level is large, current scheme not consider power channel merge
    - ➢ Otherwise needs extra power aggregation board on detector, means extra room and increasing difficulty for Mechanics
    - ➢ Several detector with enough space (esp. endcaps) with very low power, power channel merge can still be considered

Main parameters for the room calculation – Data Crates

- Optical Link
  - By using MTX interface for fibers, multiple fiber channels can be integrated in small unit
    - ➢ Can be 1Rx + 4Tx as a normal design
  - Each Tx channel at 10Gbps rate, with 8b10b protocol, and the max valid data rate to be 8Gbps
    - ➢ Major constraint for the detector module
    - ➢ If module data rate too high (>8Gbps valid data), multiple Tx fiber channels should be used, while the size of the optical module unchanged
- Crates for data
  - The common BEE Board considered with 16 optical channels, each @10Gbps/Link
  - BEE Board to be designed following the µTCA standard
    - ➢ µTCA crate height 9U, total room for 14 cards
    - ➢ 2 Ctrl cards for each crate, 1 TTC card (clocking), 1 reserved card
    - ➢ 10 valid slots for BEE boards in each data crate
- Racks for data
  - Height of a rack 42U
  - Height for the heat dissipation 2U each
  - Reserve some room for the possible Switch to DAQ
  - Max 3 crates in each Data Rack (= 30 BEE Boards = 480 optical channel)



VTRx+
4Tx + 1Rx
Array Optical
Module

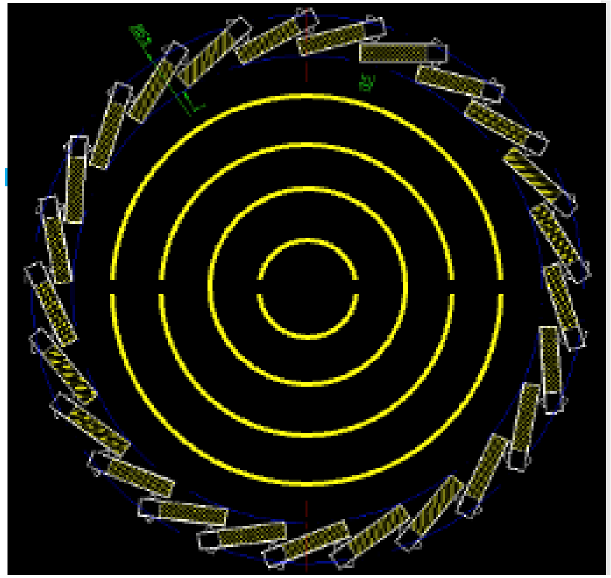
Main parameters for the room calculation – Power Crates

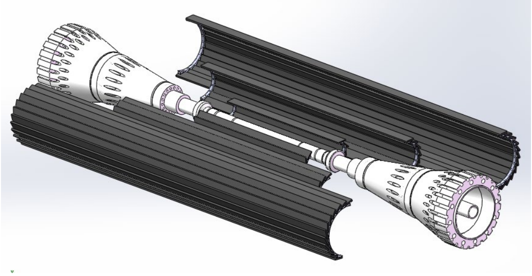
- **MV(110V DC to 48V DC) Power Crate & Racks:**
  - In the electronics room, near the Data Racks
  - A crate with a height 3U
    - Type1： 48 channels, with the capability of 100W output for each channel
    - Type2: 96 channels, with the capability of 40W output for each channel
  - Concerning the room for heat dissipation, a 42U Power Rack for 10 Power Crates is proper
- **Pwr-HV (380V AC to 110 DC) Power Crate & Racks:**
  - Power for the MV Power Racks, may be on the ground or far from radiation
  - A crate with a height 6U & total power of 60kW~70kW for a total 10 channels
  - A rack for 5 power crates (6U + 2U cooling)

Main parameters for the room calculation – Det-HV Crates

- **Detector HV crates & racks**
  - Usually the power of the detector HV source is low, channel density is the major constraint
  - (Ref. from the Det-HV crates provided for ATLAS-HGTD) a crate with a height 8U with 14×16=224 channels, independent tuning for each channel
  - 2U height for heat dissipation for each crate
  - A 42U Det-HV Rack can hold 4 Det-HV Crates
    - If SHV is needed (as for TPC), SHV-connector is larger, height of the crate -> 10~12U, and a Det-SHV Rack will be for 3 Det-SHV crates

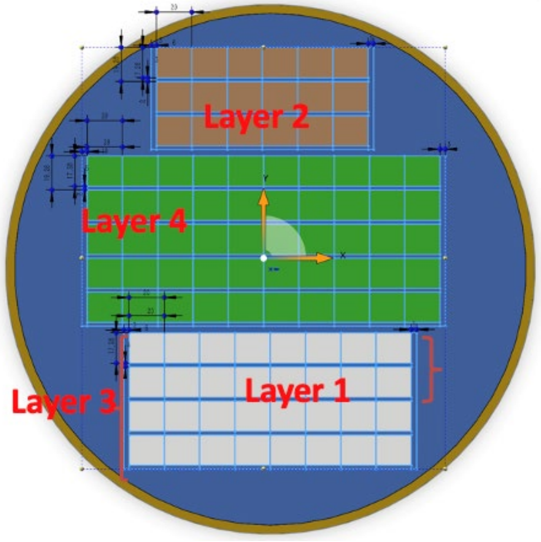
VTX-Data Link





	A	B	C	D	E	F
1	Layer	Hit density (Hits/cm2/BX)	BXRate (Hz)	Hit density (kHits/cm2/s)	Safe factor	Cluster size
2	VTX-1 (Higgs)	0.65	1.34E+06	870	1.5	3
3	VTX-2 (Higgs)	0.43		580	1.5	
4	VTX-3 (Higgs)	0.09		116	1.5	
5	VTX-4 (Higgs)	0.08		110	1.5	
6	VTX-5 (Higgs)	0.05		70	1.5	
7	VTX-6(Higgs)	0.05		68	1.5	

- **VTX scheme: Inner 4 layers stitching, with 1 typical double-sided ladder (layer 5&6)**
- **Bkgrd rate @50MW @Higgs with safety factor 1.5**
- **Assume RSU@stitching = ladder chip = 1024*512 matrix, then data rate for the innermost layer for a "chip" is 2Gbps, other layers according the bkgrd ratio**
- **Inner 2 layers needs 2 fiber chns for each row, due to the high data rate**
  - **possible to merge into less optical MTX interfaces**
- **In total 88 fibers = 6 BEE Brd = 1 Data Crate**



From Zhijun

Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8（2 fiber chns）
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12（2 fiber chns）
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25

VTX-Power

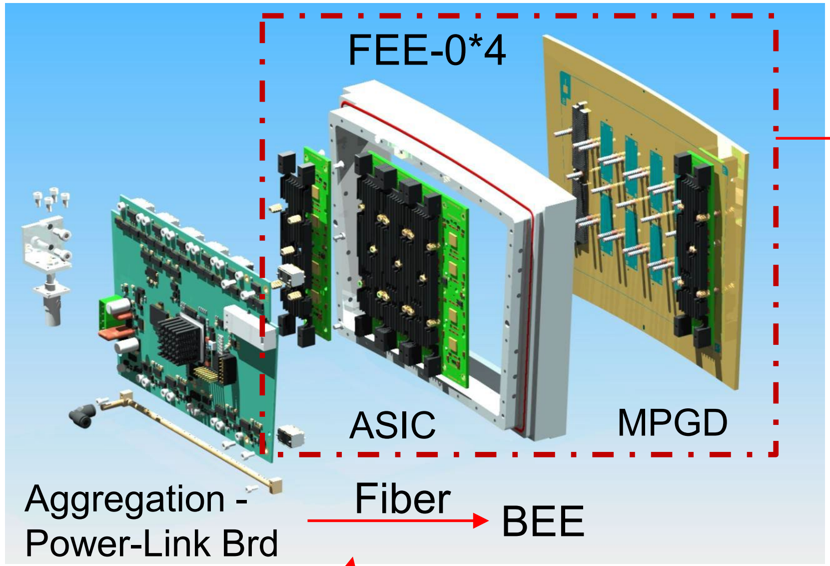
Layer	Comment	Power/chip	Chips/Row	Power /row	Rows	Chip Power of Layers	Total Power/Layer (Chip+Link) *1.18
1	Stitching	200mW	8	1.6W	2*2=4	6.4W	(6.4+4) *1.18=12.2
2	Stitching	200mW	12	2.4W	3*2=6	14.4W	(14.4+6) *1.18=24
3	Stitching	200mW	16	3.2W	4*2=8	25.6W	(25.6+8) *1.18=39.5
4	Stitching	200mW	20	4W	5*2=10	40W	(40+10) *1.18=58.8
5	Ladder-side0	200mW	29	5.8W	25	145W	(145+25) *1.18=200
6	Ladder-side1	200mW	29	5.8W	25	145W	(145+25) *1.18=200

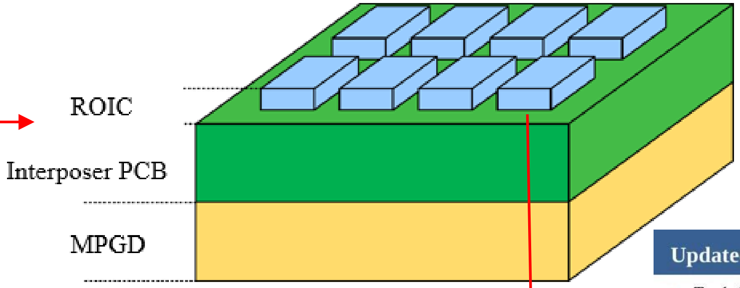
- **For simplicity, assume the power of Unit(RSU/Chip) is the same 200mW(40mW/cm2 * 2.6cm*1.6cm)**
  - **Main contribution of power: analog static power + data link, not varying with bkgrd rate**
- **Extra cost by using optical: fixed 1W each set**
  - **0.75W for Data Interface & 0.25W for 1 Rx+4Tx VTRx**
- **Efficiency of BaSha DC-DC is 85% = extra efficiency cost of DC-DC 18% (1÷85%=118%)**
- **Total power: 449.8W**
  - **16 power channels each layer for 1~4, each chn for a semi-; 2 chn for each ladder in 5/6 layer, 50 chn in all**
  - **Power will be provided from both ends for long barrel**
  - **66 power channels = 2 power crate**
    - **Very likely to be merged due to the limited room for VTX**

VTX-Det-HV

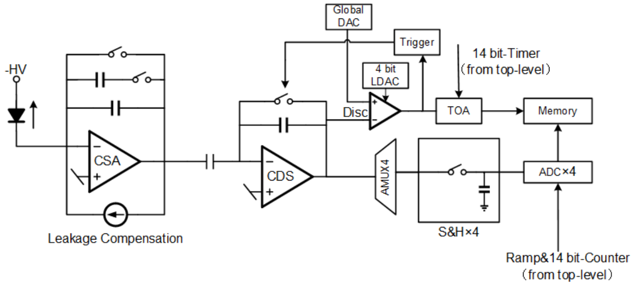
- There is no actual need for "High Voltage"
- However, may be the only detector to use negative voltage for sensors
  - Depend on R&D, ranges < -10V
- Not cost-effective to developed a dedicated power module for VTX
  - Can be treat as a "Det-HV"
- Det-HV Crates (similar to VTX Power Crates):
  - 16 HV channels each layer for 1~4, each chn for a semi-; 2 chn for each ladder in 5/6 layer, 50 chn in all
  - HV will be provided from both ends for long barrel
  - 66 HV channels = 1 Det-HV crate

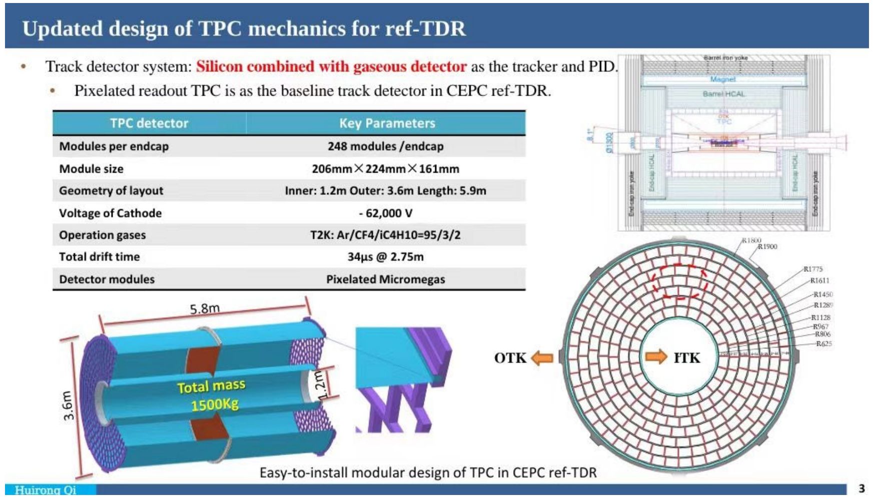
Preliminary readout scheme of Pixel TPC





An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





Updated design of TPC mechanics for ref-TDR

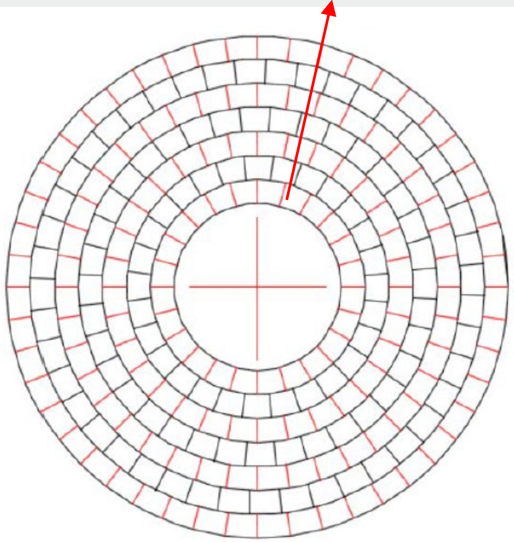
- Track detector system: **Silicon combined with gaseous detector** as the tracker and PID.
  - Pixelated readout TPC is as the baseline track detector in CEPC ref-TDR.

TPC detector	Key Parameters
Modules per endcap	248 modules /endcap
Module size	206mm×224mm×161mm
Geometry of layout	Inner: 1.2m Outer: 3.6m Length: 5.9m
Voltage of Cathode	- 62,000 V
Operation gases	T2K: Ar/CF4/iC4H10=95/3/2
Total drift time	34μs @ 2.75m
Detector modules	Pixelated Micromegas

Easy-to-install modular design of TPC in CEPC ref-TDR

Huirong Qi 3

From Huirong



~248 Module/Endplate

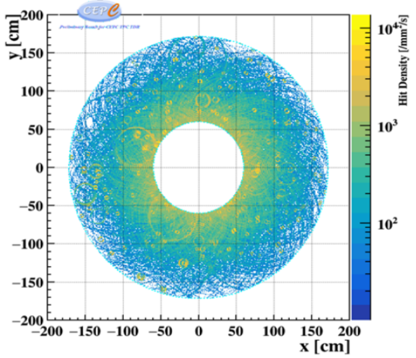
128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

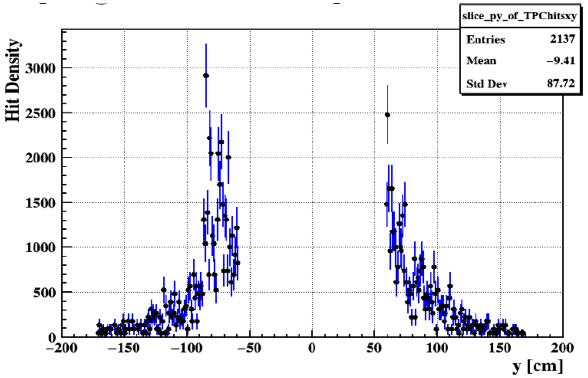
Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn
Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

TPC——Data Link

- Module number: 248 * 2 endcap=496 modules
- Data rate concerning bkgrd rate:
  - 30Mbps~100Mbps per module, avg. @ 70Mbps, much less than the max capability of optical
- Data Link:
  - Each module per fiber link, w/o inter-module data aggregation, to maximize the reliability
  - Not too much cost variation for the BEE
  - The alternative scheme by data aggregation is also listed below

Sch.	Module	Data Rate/module	Module/Fiber	Total Fiber	Total BEE	Total crate
1	248*2=496	100Mbps	1	496	248/16*2=32	4
2	248*2=496	100Mbps	16	246/16*2=32	3	1



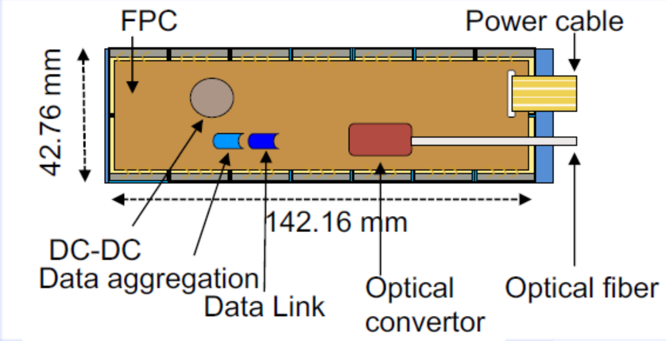


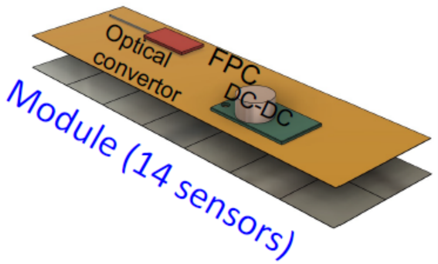
Background rate analysis
https://cds.cern.ch/record/1543486/files/LCD-Note-2013-005.pdf
https://doi.org/10.1088/1748-0221/12/07/P07005
https://www.sciencedirect.com/science/article/pii/S0168900216305381

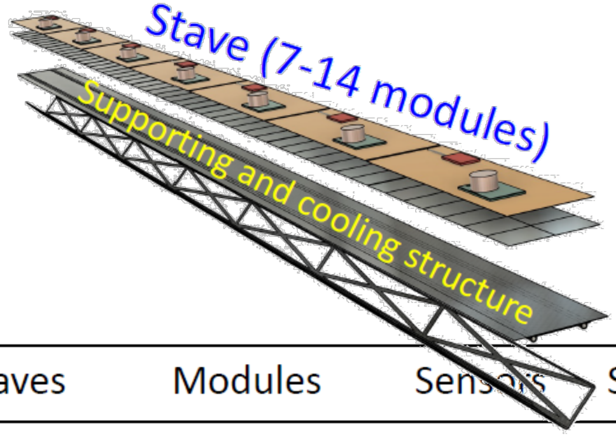
TPC——Power & HV

- **The power spec for each endcap of TPC is 10kW**
  - **Avg. power for each module is 40.3W**
  - **Concerning the cost of data link 1W, total power per module ~42W**
  - **Suitable to provide power for each module with an independent power channel**
    - ➢ **Max. the flexibility for installation and reliability; min. the complexity in case that the power has to be distributed between modules**
- **Power crates**
  - **In total 496 module = 496 channels = Power Crates 6**
    - ➢ **Assuming independent distribution for the two endcaps**
- **Det-HV crates**
  - **Requirement for independent tuning for each module, has to be 1 chn for each module**
  - **In total 496 module = 496 channels = Power Crates 4**
    - ➢ **Assuming independent distribution for the two endcaps**

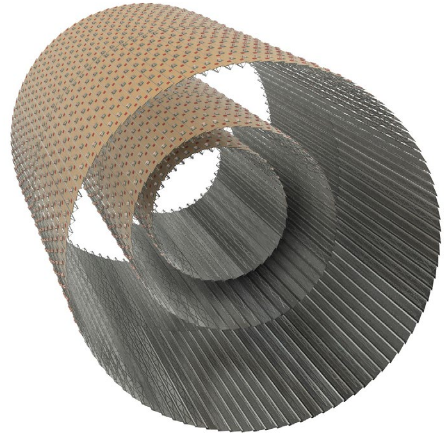
ITK——Detector, stave & module



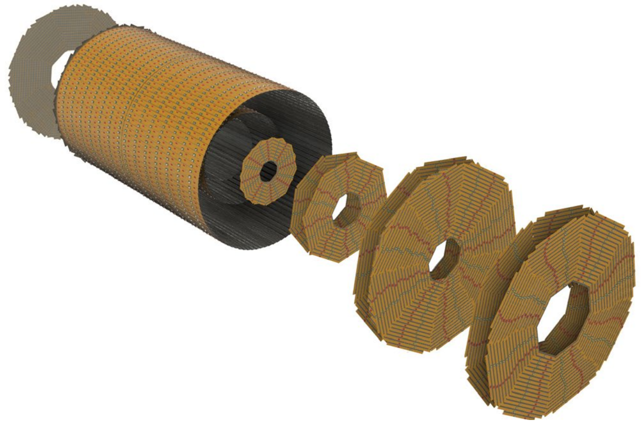




- **Each module with a Data Link & Power Module assembled**



Barrels	Modules/Stave	Staves	Modules	Sensors	Sensor area
ITKB1	7	40	280	3920	1.6 m^2
ITKB2	10	58	580	8120	3.2 m^2
ITKB3	14	96	1344	18816	7.5 m^2
Total		194	2204	30856	12.3 m^2



Endcap	1 (per Sector)	2	3	4	Total
Ladder Type	6	8	15	12	18
Ladder Number	7	10	18	15	1600
Chip Number	48	98	260	236	20544
Active Area (mm^2)	20181.03	42796.32	116080.28	106081.77	9.12e6
Module Area (mm^2)	23184	47334	125580	113988	9.92e6
Power Consumption (W)	46.368	94.668	251.16	227.98	1.98e4
Avg. Hit Rate (Hz/mm^2)	3.9e2	1.6e3	8.9e2	2.4e2	-
Data Rate (Hz)	2.89e8	2.42e9	3.58e9	8.75e8	2.29e11

ITK——Data Link (Barrel)

	HVCMOS Pixels (Barrel)	CMOS Strips (Endcap)
Pixel Size (Strip Pitch Size)	$34 \times 150\ \mu m^2$	20 μm
Chip size	$2 \times 2\ cm^2$ (active area: $1.92x1.74\ cm^2$)	$2.1 \times 2.3\ cm^2$ (active area: $2.05x2.05\ cm^2$)
Array size (Strip number)	512 rows × 128 columns	1,024
Spatial resolution	σ_φ ~8 μm (bending), σ_z~40 μm	σ_φ~4.2 μm (bending), σ_r~21 μm
Timing resolution	~3-5 ns	~3-5 ns
Data size per hit (1 readout)	42 bit (14b BXID, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)
Data rate per chip	Maximum ~0.1 Gbps* (pair production)	Maximum ~0.2 Gbps* (pair production)
LV / HV	1.2 V / 150 V	1.8 V / 150 V

* Maximum hit rate: barrel~4.1×10^5, endcap~7.5×10^5

Hit Rate Conclusion

	Z [mm]	R_in [mm]	R_out [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKE1	500.5	75	240	3.9	23
ITKE2	715	101.9	350	16	38
ITKE3	1001	142.6	600	8.9	75
ITKE4	1500	213.7	600	2.4	6.3
OTKE	2903	406	1810	0.3	3.5

tel:2903%20406%201810%200.3%203.5

	R [mm]	Half_Z [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKB1	240	500.5	1	4.6
ITKB2	350	715	2.1	41
ITKB3	600	1001	2.1	27
OTKB	1800	2000	0.7	0.9

ITKB	Modules/layer	Avg bkgrd rate (Hz/cm^2)	Avg Chip Data rate (Mbps) (42bit & $4cm^2$)	Avg Module Data rate (Mbps) (14 chips)	Max bkgrd rate (Hz/cm^2)	Max Module Data rate (Mbps) (14 chips)
1	280	10k	1.68	23.5	46k	108.2
2	580	21k	3.53	49.4	410k	**964.3**
3	1344	21k	3.53	49.4	270k	635.0

- **Data width~42bit/event**
- **Barrel Module: 2*7=14 chips**
- **Max Data rate per module ~1Gbps**
- **Enough room left for a fiber channel, 1 fiber for 1 module**

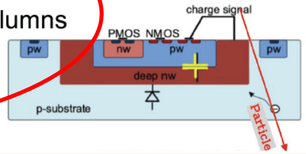
In total 2204 Modules = 2204 fibers, each layer is independent with other layers on BEE

BEE Boards: 18+37+84=139, -> 14 Data Crates

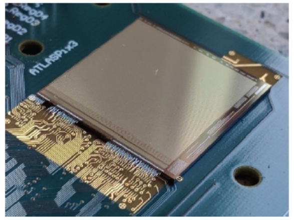
ITK——Power (Barrel)

Technology Survey and our Choice for ITK: Option 1

- CMOS sensor technology:
  - Cost-effective due to widespread use in the semiconductor industry
  - Combine the active detection layer and the readout electronics into a single device
- HVCMOS pixels:
  - Large depletion depth (full depletion), large signal
  - Radiation hard
  - Relatively large capacitance, leading to increased noise and power consumption
- New HVMOS (COFFEE) pixels R&D for CEPC:
  - Utilizes 55 nm process instead of the 180 nm used in ATLASPix3
    - More functionality and less power consumption
  - Wafer resistivity: 1k-2k Ω·cm
  - Pixel size: 34 × 150 μm^2
  - Array size: 512 rows × 128 columns
  - Power consumption: ~200 mW/cm^2



- ATLASPix3
  - TSI 180nm HVCMOS on 200 Ωcm substrate
  - Pixel size 50 × 150 μm²
  - 372 rows × 132 columns
  - 20.2 × 21 mm² reticle size
  - Each pixel has 7-bit TOT + 10-bit timestamp
  - Continuous / triggered readout with 8b10b / 64b66b coding
  - Power consumption ~160 mW/cm².

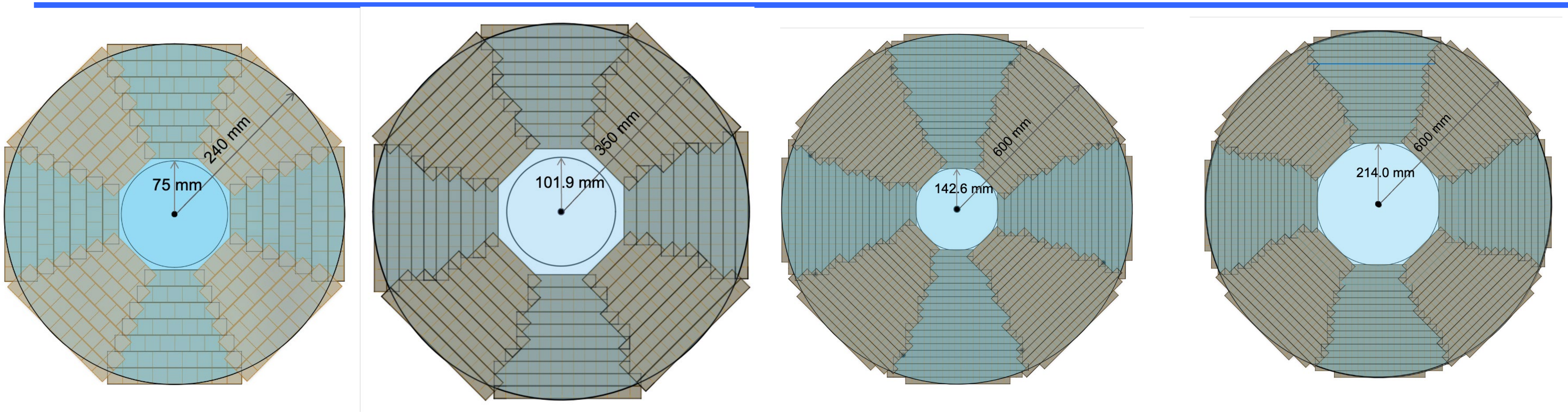


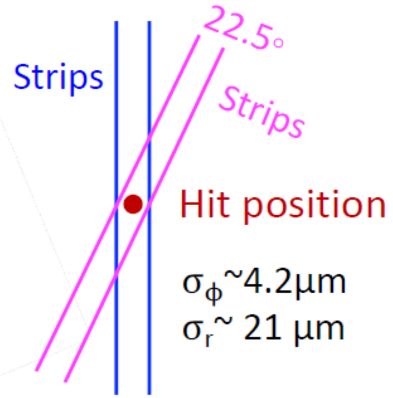
4

ITKB	Modules/layer	Layer power (W)	Data Link Power (W)	Total Power(chip+data)/85%
1	280	3.14k	280	4.02kW
2	580	6.50k	580	8.32kW
3	1344	15.1k	1344	19.29kW

- Estimated chip power 200mW/cm^2， 14 chips per module， Module power 11.2W
- Extra power: Data Link 1W per module
- 1 Power channel for each module for reliability & installation simplicity
- Power channels: 280 + 580 +1344=2204, -> Power Crates 3+12+14=29, each layer independent
- HV range 50~200V (normal HV), independent tuning for each module
  - Det-HV channels also 2204, -> Det-HV Crates 10

ITK——Detector Design Endcap





- **8 sectors for each endcap layer; each endcap by two layers overlapped @22.5°**
- **Different size of module at different radius & different layers**
- **Assume 1 fiber + 1 power for each module, chip number matters for data rate & power**
- **1st Endcap：9+9+8+7+6+5+4=48 chips，7 ladders**
- **2nd Endcap：13+13+12+11+10+10+9+7+7+6=98 chips，10 ladders**
- **3rd Endcap：17+22+22+21+20+19+19+18+17+16+16+15+14+13+12+12+10+8+8=299 chips，19 ladders**
- **4th Endcap：15+21+22+21+21+19+19+18+17+16+15+14+13+12+11+11+9=274 chips，17 ladders**

ITK——Data Link (Endcap)

Hit Rate Conclusion

	Z [mm]	R_in [mm]	R_out [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKE1	500.5	75	240	3.9	23
ITKE2	715	101.9	350	16	38
ITKE3	1001	142.6	600	8.9	75
ITKE4	1500	213.7	600	2.4	6.3
OTKE	2903	406	1810	0.3	3.5

tel:2903%20406%201810%200.3%203.5

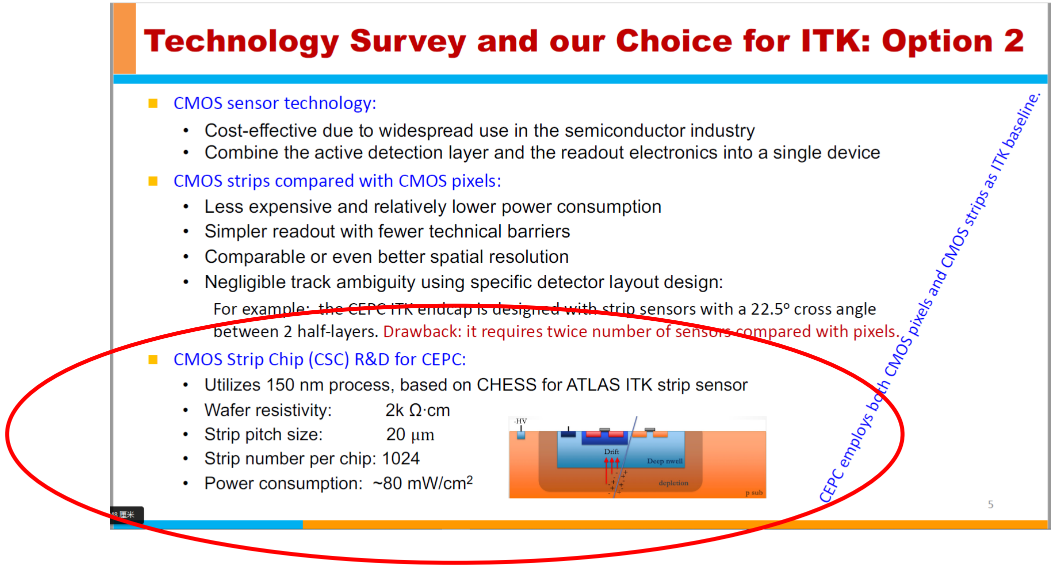
	R [mm]	Half_Z [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKB1	240	500.5	1	4.6
ITKB2	350	715	2.1	41
ITKB3	600	1001	2.1	27
OTKB	1800	2000	0.7	0.9

Endcap	1 (per Sector)	2	3	4	Total
Ladder Type	6	8	15	12	18
Ladder Number	7	10	18	15	1600
Chip Number	48	98	260	236	20544
Active Area (mm^2)	20181.03	42796.32	116080.28	106081.77	9.12e6
Module Area (mm^2)	23184	47334	125580	113988	9.92e6
Power Consumption (W)	46.368	94.668	251.16	227.98	1.98e4
Avg. Hit Rate (Hz/mm^2)	3.9e2	1.6e3	8.9e2	2.4e2	-
Data Rate (Hz)	2.89e8	2.42e9	3.58e9	8.75e8	2.29e11

ITKE	Ladder Max chips	Avg bkgrd rate (Hz/cm^2)	Max bkgrd rate (Hz/cm^2)	Avg Module Data rate (Mbps)	Max Module Data rate (Mbps)	Modules/Ladders(Fibers)
1	9	39k	230k	47.2	278.4	7*8*2layer*2Endcap =224
2	13	160k	380k	279.7	664.3	10*32=320
3	22	89k	750k	263.3	**2218.9**	19*32=608
4	22	24k	63k	71.0	186.4	17*32=544

- **Max module data rate 2.2Gbps, enough room left by using 1 fiber for each ladder**
- **Ladders in total：224+320+608+544=1696，=106 BEE，=12 Data Crates (symmetry from two side)**

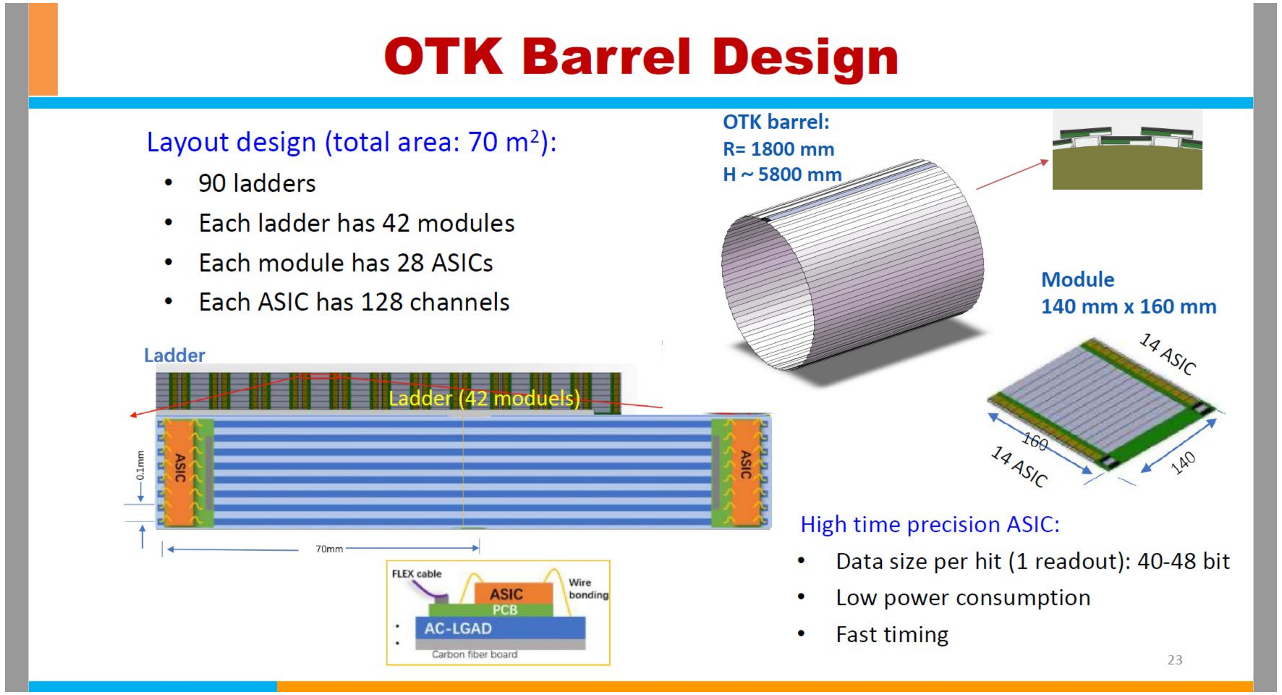
ITK——Power (Endcap)

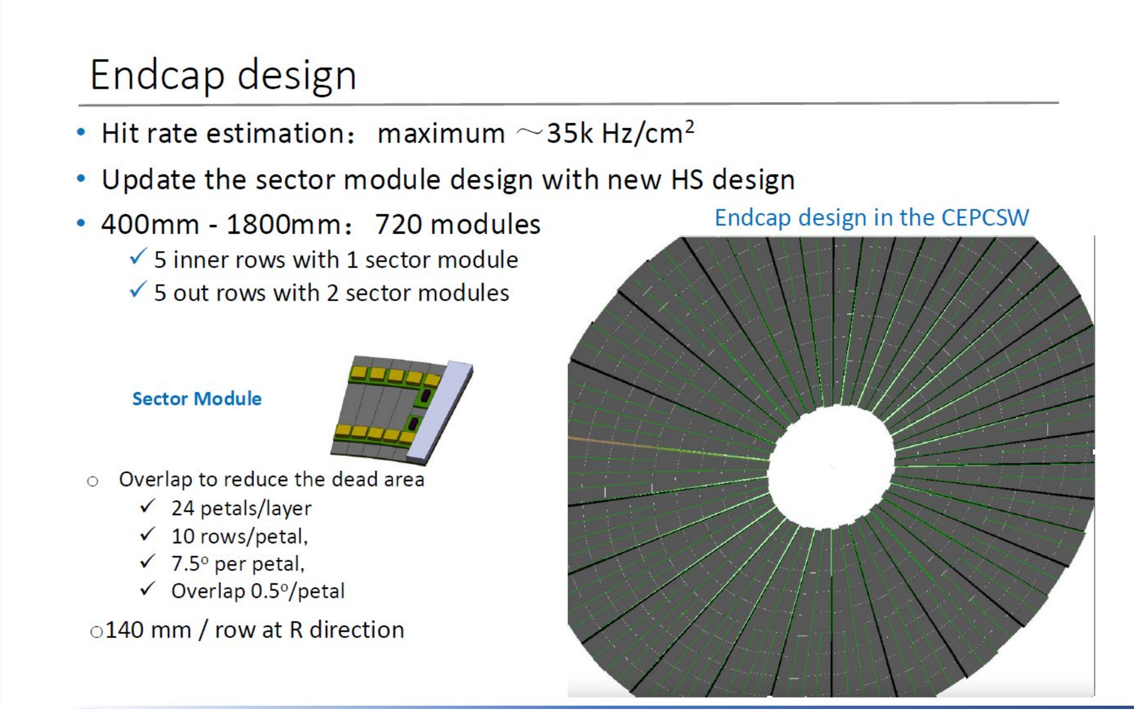


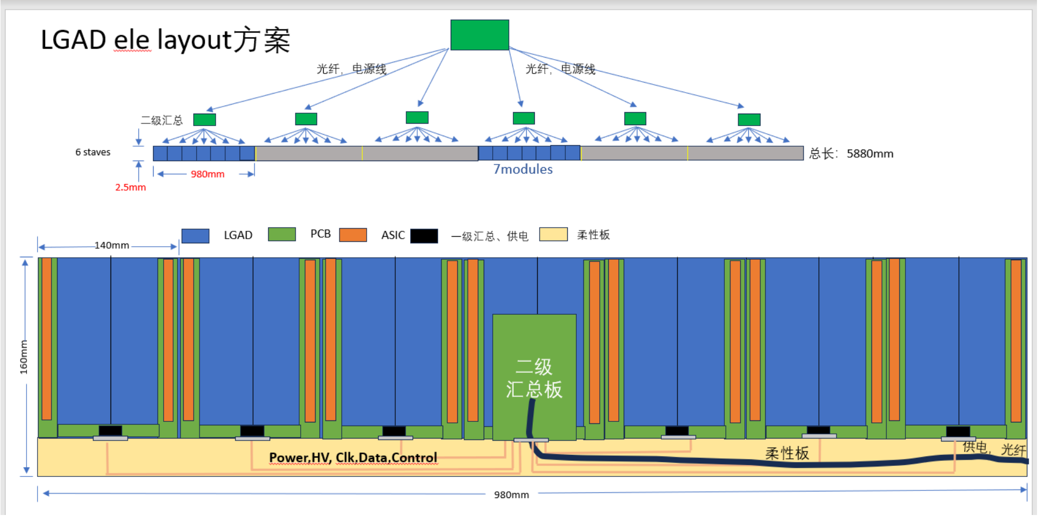
- **Power density 80mW/cm^2， Chip Power 336mW**
- **Max Ladder Power 7.39W for DC-DC consideration**
- **Total Power 11.1kW,**
- **Ladder power is relatively low, consideration to merge for the power channel at the sector level**
  - **In total 192 power channels, 2 power crates**
  - **Inner 2 endcaps, 1 power chn for each sector**
  - **Outer 2 endcaps, 2 power chns for each sector**
- **Det-HV ind. tuning for 50~200V, 1 chn for each ladder, in total 1696 Det-HV channels, = 8 Det-HV crates**

ITKE	Ladder Max chips	Ladder Max Power(W)	Chip per sector	Sector Chip Power(W)	Sector Data Link Power (W)	Sector Power(Chip+Link) ÷85% (W)	Layer Power (×8×2layer×2 endcap) (W)	Power Chn (1 Chn per sector)
1	9	3.02	48	16.1	7	27.2	870.6	1 × 32
2	13	4.36	98	32.9	10	50.5	1616.0	1× 32
3	22	7.39	299	100.5	18	139.4	4497.4	2× 32
4	22	7.39	274	92.1	15	126	4105.9	2× 32

OTK - detector design







- **Propose to use a unique ASIC for both barrel and endcaps**
- **Data width 48bit/event**

OTK-Data Link

Hit Rate Conclusion

	Z [mm]	R_in [mm]	R_out [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKE1	500.5	75	240	3.9	23
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	R [mm]	Half_Z [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
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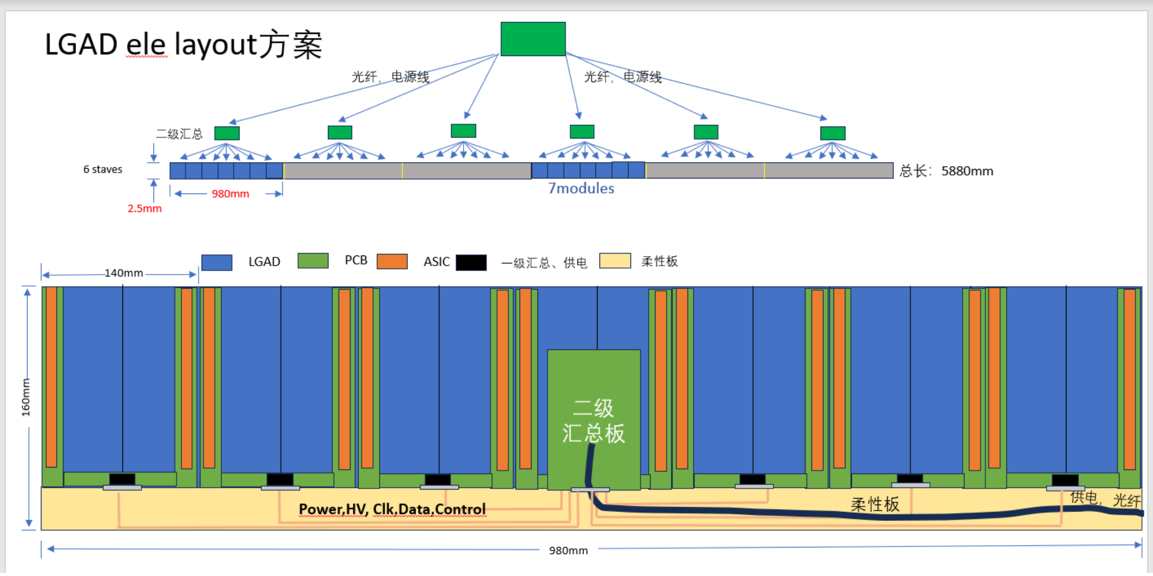


- **Barrel:**
  - Data link proposed to locate at the 2^{nd} level aggregation board, for 7 modules (1 ladder), each module 22 ASICs
  - Avg module rate 7kHz*14cm*14cm*48bit=65.9Mbps, Max 9kHz→84.7Mbps
  - For the optical data rate of 7 modules (1 ladder), avg/max to be 461.3Mbps/1355.2Mbps, with large room for the data link
  - A full 6m Stave with 6 Ladders (6 fibers), barrel in total 90 ladders, =540 fibers = 34 BEE = 4 Data Crates
- **Endcap:**
  - 48 Pedals for 2 endcaps, 10 rings each Pedal with 15 sectors (Inner 5 rings 1 sector, Outer 5 rings 2 sectors)
  - Total area 19.4m^2, =4041.7cm^2 for each Pedal, avg. Pedal data rate= 3kHz*4041.7*48bit=582Mbps, Max 35kHz→6.79Gbps
    - ➢ Consideration 1 fiber for each sector, even concerning the higher data rate for inner sectors, enough room left for the fiber
  - 48 Pedals with 720 sectors in total, =720 fibers = 45 BEE = 6 Data Crates (each endcap independent)

OTK-Power

- Chip power 20mW/ch @ 7pF Cd for 30ps
- 128 channels for each ASIC, 2.56W/chip
- Barrel:
  - 90 staves, 6 ladders per stave, 7 modules per ladder, 22 ASIC per module
  - Module power 56.32W (should be noticed for DC-DC design)
  - In total 90×6×7×22=83,160 ASICs， chip power 212.9kW
  - Data Link power 1W for each ladder， 540 fibers in total， 0.54kW
  - For DC-DC efficiency 85%, total power 251.1kW
  - To provide 1 chn for each module (not enough for 1 chn per ladder)
    - ➢ = 3780 power channel = 79 Power Crates
- Endcap:
  - According to the detail detector design, 240 ASICs for each Pedal
  - Max 23 chips for a sector, sector power 58.9W, needs a independent power channel
  - 48 Pedals for 2 endcaps = 11520 ASICs, with chip power 29.5kW
  - Data Link power 1W for each sector, 0.72kW in total
  - For DC-DC efficiency 85%, total power 35.6kW
  - 1 power chn for each sector: 720 power chns = 16 power crates (independent endcaps)

Data rate / petal

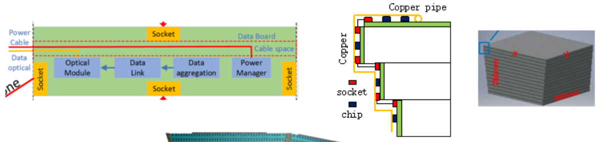
Row （140 mm/rwo）	Chip per row	Date rate （HZ）
R0（400-540）	11	1533882.59
R1：540-680	14	335365.01
R2：680-820	17	412334.029
R3:	19	489303.047
R4	23	566272.066
R5	25	643241.085
R6	29	720210.104
R7	31	797179.122
R8	34	874148.141
R9：1660-1800	37	951117.16

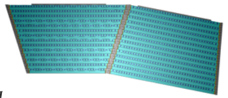
OTK- Det-HV

- **Det-HV independently tuning for 150~200V**
- **1 chn for each module/sector**
- **Barrel:**
  - **90×6×7=3780 module，=3780 Det-HV chns =17 Det-HV crates**
- **Endcap:**
  - **720 sectors, 360 Det-HV chns for each endcap by 2 Det-HV crates, in total 4 Det-HV crates**

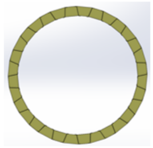
ECAL – Data Link(skip)

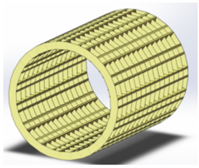
ECAL电缆估算



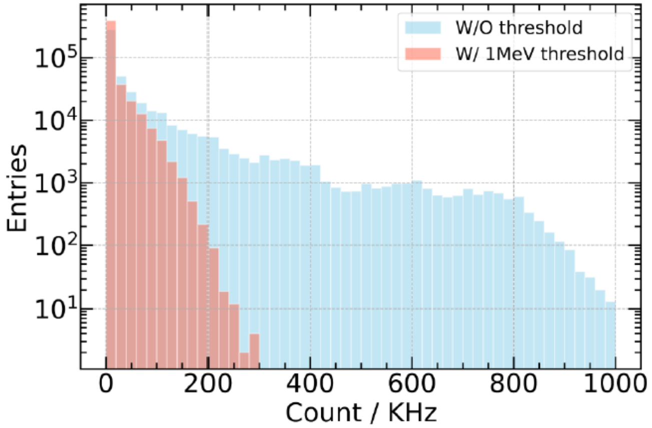


- ECAL桶部，正反梯形排布
  - 模块数量：Phi：32，Z：15，共480个模块
- 每个模块：
  - 1层到28层，奇数层每层36根，偶数层晶体数目不一致
  - 正梯形晶体数量1000，反梯形晶体数量992
- 电缆估算：1根/模块
  - AWG15（线径1.45mm，电流：6.5A/7.4A）
  - AWG18（线径1.08mm，电流：3.2A/3.7A）
  - 模块功耗估计：1000*2*20mW = 40W
- 光纤估算：1根/模块
  - 模块数据量估算：待定
- 桶部电缆总计
  - 类型：高压，低压（正负？），光纤
  - 电缆双向走向，每端240根（平均方案）
  - 电缆双向走向，一端224根，一端256根
- 未确定电缆：刻度方案





层数	反梯形	正梯形
2	27	39
4	29	37
6	29	37
8	31	37
10	31	37
12	33	37
14	35	35
16	35	35
18	37	35
20	37	35
22	39	33
24	41	33
26	41	33
28	43	33



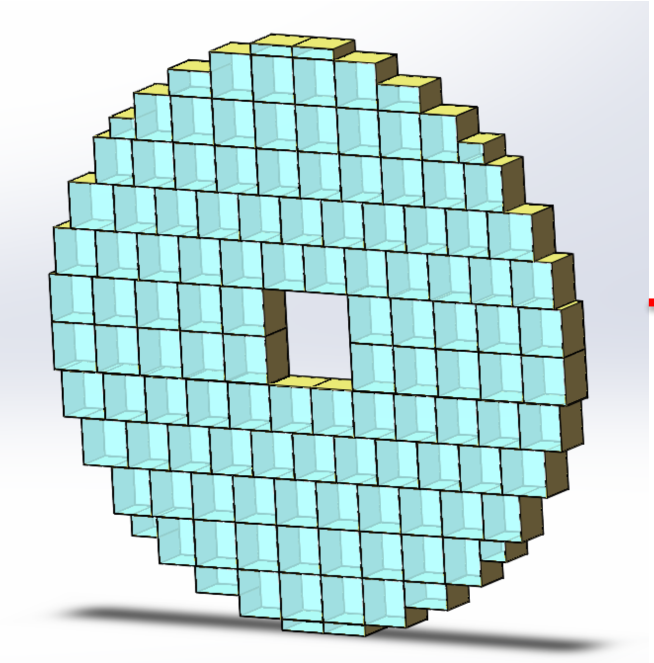
- **The overall detector design: ~480 Module (Dual-trapezium scheme), ~1000 bar/module**
- **Current bkgrd estimation: avg. event rate 100kHz / crystal bar w/ threshold; Data width 48bit/event (current ASIC scheme)**
- **@Dual readout each crystal bar, total data rate: 1000*100kHz*48bit*2ends=9.6Gbps, not possible for 1 fiber for each module, at least 2 fibers for each module**
  - **For max. bkgrd rate@300kHz@Higgs, also needs enough room**
  - **For Z pole, bkgrd will be much higher, also needs extra room**

ECAL – crates (skip)

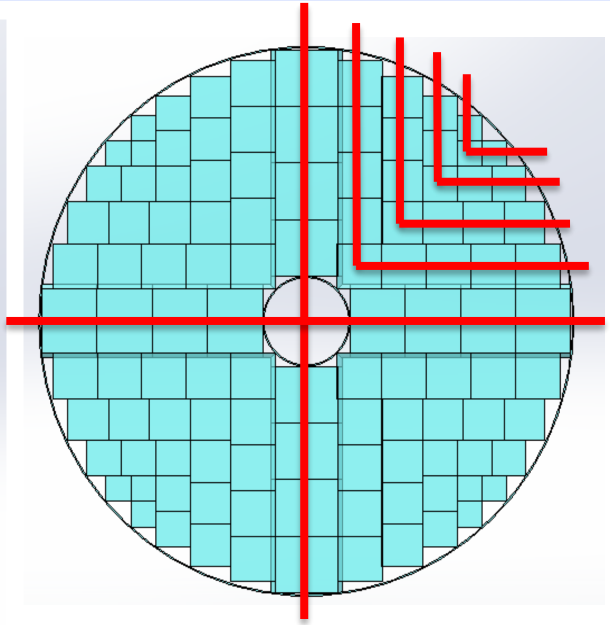
- **Data Link:**
  - Fibers: 480*2=960, -> 60 BEE Brds, 6 crates
- **Power:**
  - ASIC: 15mW/ch, each module 1000*2*15mW=30W
    - Within the capability of DC-DC power module
  - Data Link + Optical Power: 1W each
  - Total Power: 31W/0.85*480=17.5kW
    - Efficiency of the DC-DC: 85%
  - Power chn 40W/chn, each module per power cable: 480 power chn -> power crates 5
- **Det-HV:**
  - Sch 1: one HV chn for each module, (limitedly) compensated for each SiPM in ASICs
  - HV channels = module number = 480， -> 2 HV crates

  - Alt sch2： HV chn for each SiPM? Too many channels & too large control data volume (✕)
  - Alt sch3： HV chn for sub-region of a module, to compensate the temperature gradient
    - Maybe much optimized than sch1， but rely on the detector simulation

ECAL – endcap



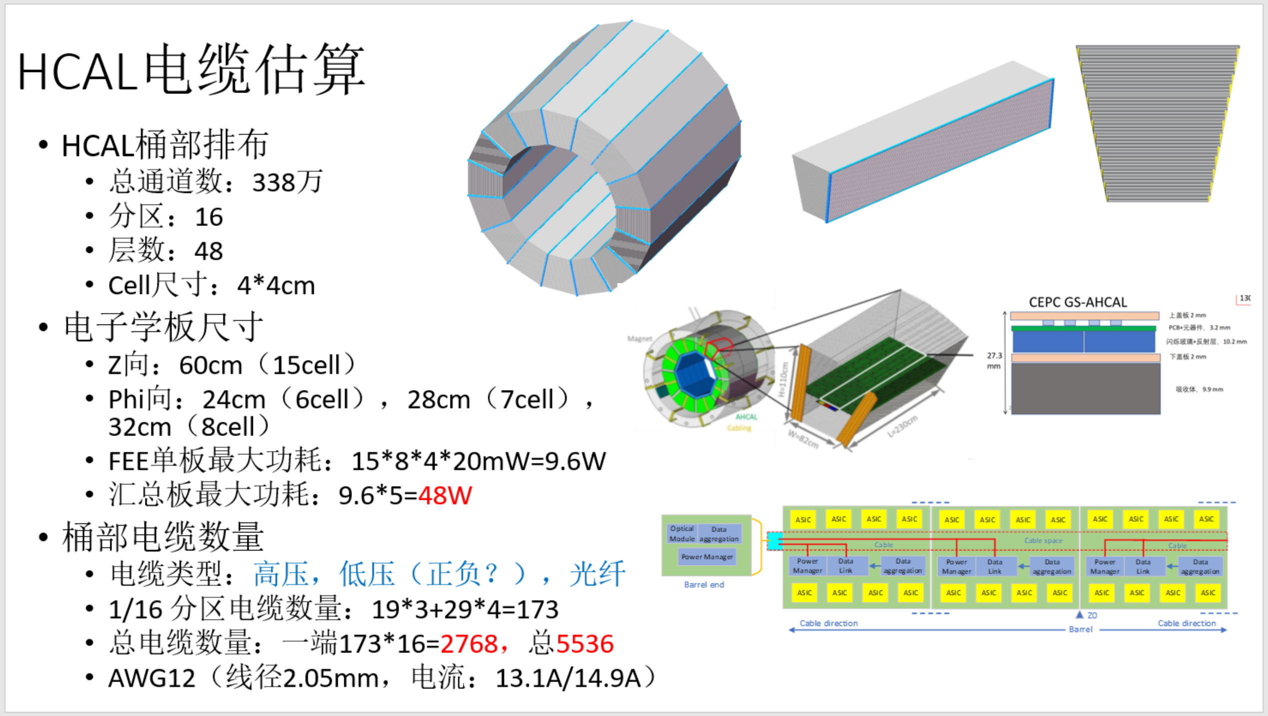
Original design



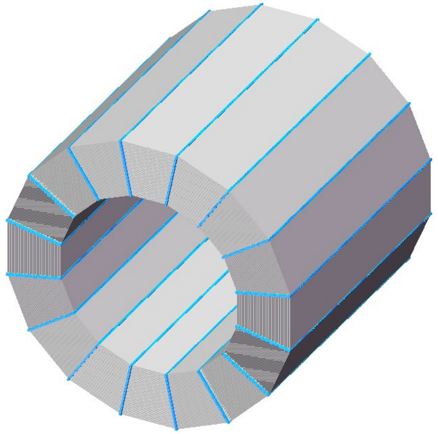
In optimization

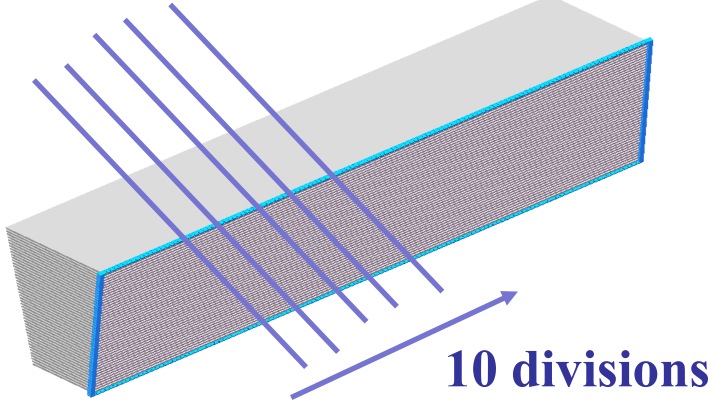
- Waiting for the final design of ECAL endcap
- According to the current design, module number 122~96, calculated by 130 modules
- Expect higher bkgrd rate than barrel, keep the scheme of 2 fibers per module
- Fibers:
  - 130module*2endcap*2 fiber=520
  - 34 BEE = 4 Data Crates (from 2 sides)
- Power：
  - Total power: 31W/0.85*260=9.48kW
  - 260 Power channels = 4 power crates

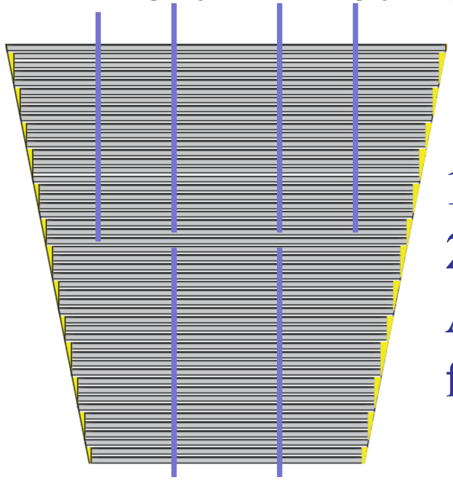
HCAL-Data Link(barrel)



- Currently, HCAL is not finalized, especially for the module design, e.g. cell size and channel number
- Data have to be aggregated at the end of barrel for each layer, also the DC-DC
- By rough estimation, the bkgrd will be low, the aggregated data rate for each layer board should not exceed 8Gbps (10Gbps for the fiber)
  - Then 1 fiber for each aggregation board is reasonable
- Fibers：
  - Aggr. board number every 1/16 sector：19*3+29*4=173
  - 1 fiber per aggregation board: 173*16*2=5536 fibers
  - =346 BEE = 36 Data Crates







1~19layer 3PCBs width
20~48layer 4PCBs width
Aggr Brd for 5 PCBs along z from both ends, with 1 fiber

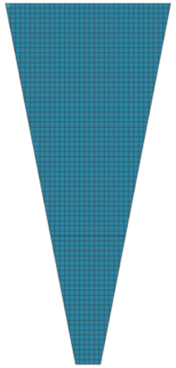
HCAL-Power (barrel)

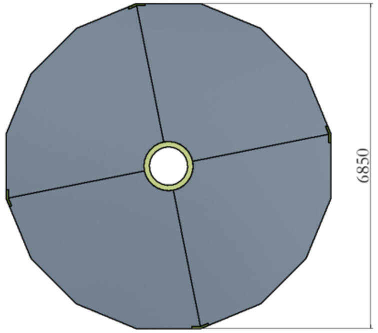
- **Max PCB size – corresponding to GS cells：**
  - Z direction：60cm（15cell）
  - Phi direction：24cm（6cell），28cm（7cell），32cm（8cell）
- **Concerning the light collection, every 4cm*4cm GS cell may use 1~4 SiPMs**
- **Max SiPM channels for the largest PCB: 15*8*(1~4)=120~480**
- **ASIC Power 15mW/ch，Power for the max PCB: (120~480)*15mW=1.8W~7.2W**
- **Every Aggregation board provides power for 5 PCBs: (1.8~7.2)*5=9~36W**
- **Power for Barrel:**
  - ASIC power: total channel 3.38M * 15mW/chn*(1~4)=50.7kW~202kW
    - Match with the calculation: 15*8 (PCB cells) *173 Brds * 10 div *16 sections = 3.32M cells
  - Data Link power 1W for 5536 fibers = 5536W
  - For DC-DC efficiency 85%, total power [(50.7~202)+5.5]/0.85=66.1~244.2kW
  - 1 power channel for each aggregation board for installation simplicity:
    - 5536 power channels = 116 power crates

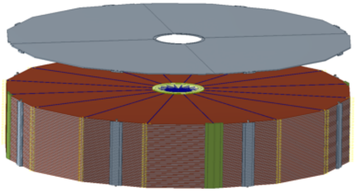
HCAL-Data Link (Endcap)

HCAL电缆估算

- HCAL端盖部排布
  - 总通道数：单端112万，总共224万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 端盖电缆数量
  - 电缆类型：高压，低压（正负？），光纤
  - 每区功耗：1459*20mW=30W
  - 1/16 分区电缆数量：48
  - 总电缆数量：一端48*16=768，总1536
  - AWG12（线径2.05mm，电流：13.1A/14.9A）
- 未确定电缆：刻度方案







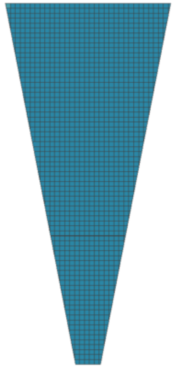
- **Fibers**
  - 1 fiber for each sector at each layer
  - 48layer*16sector*2endcap=1536
  - =96BEE = 10 Data Crates

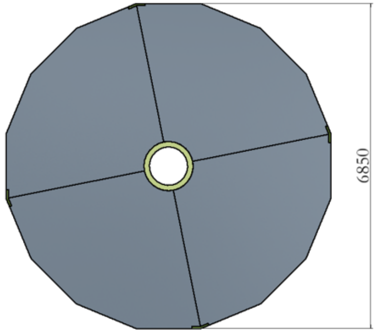
- **Current design for HCAL:**
  - 48 layers with 16 sectors
- **Needs input of the bkgrd rate, assuming 1 fiber is enough (data rate < 8Gbps) for each sector at each layer**
- **Rough calculation:**
  - each endcap 1.12M channels -> 1458 GS cells for each sector
  - Even if the bkgrd is at the level of ECAL of 100kHz avg., total data rate of each sector per layer is 7.0Gbps, within the safety region for using 1 fiber

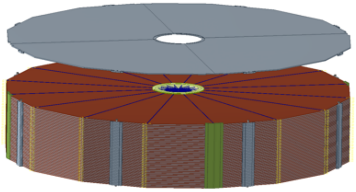
HCAL-Power (Endcap)

HCAL电缆估算

- HCAL端盖部排布
  - 总通道数：单端112万，总共224万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 端盖电缆数量
  - 电缆类型：高压，低压（正负？），光纤
  - 每区功耗：1459*20mW=30W
  - 1/16 分区电缆数量：48
  - 总电缆数量：一端48*16=768，总1536
  - AWG12（线径2.05mm，电流：13.1A/14.9A）
- 未确定电缆：刻度方案







- **each endcap 1.12M channels -> 1458 GS cells for each sector**
- **If each GS cell with 1~4 SiPM channels, each sector 1458~5832 ASIC channels**
  - **Common SiPM ASIC as ECAL, 15mW/chn max**
- **Each sector 21.9~87.5W (<u>should be noticed for DC-DC design)</u>**
- **Chip power 2.24M*15mW/ch * (1~4) = 33.6~134.4kW**
- **Data link power : 1536W for 1536 fibers**
- **Total power: (33.6~134.4k+1536)/0.85=41.3~159.9kW**
- **1 power chn for each sector at each layer: 1536 power chns = 16 power crates**

CAL——Det-HV

- **SiPM HV 40~60V depends on device type**
- **Currently not clear for ECAL & HCAL detector HV scheme**
  - Scheme 1：HV for each module, compensate SiPM in ASIC
    - ➢ Limited compensation range by ASIC, may see large gradient by temperature
  - Alt sch2：HV chn for each SiPM? Too many channels & too large control data volume (✕)
  - Alt sch3：HV chn for sub-region of a module, to compensate the temperature gradient
    - ➢ Maybe much optimized than sch1，but strongly rely on the detector simulation and careful design – future work
- **Currently only simply considering Det-HV for each module**
  - ECAL barrel：480 modules，480 Det-HV chns，2 Det-HV crates
  - ECAL endcap：260 modules，260 Det-HV chns，2 Det-HV crates
  - HCAL barrel：5536 aggregation boards，5536 Det-HV chns，26 Det-HV crates
  - HCAL endcap：1536 sector layer，1536 Det-HV chns，32 Det-HV crates

Muon

Muon	Module	Channel/Module	Readout Channel	Hit rate/Hz (worst case)	Data format	Raw data rate / Gbps
Barrel	192	169.5	32544	10 k	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	15.63
Inner endcaps	64	144	9216	10k~100 k, Average 20 k		8.85
Outer endcaps	64	256	16384	10 k		7.87
Total			~58.2 k			~32.4

- **Needs detailed design of the overall detector, only provides a estimation from BELLE2**
- **Assuming bkgrd not high, 1 fiber for each module:**
  - **Barrel 192 fibers = 12 Data crates； Endcap 128 fibers， 8 Data crates**
- **Power： Assuming common ASIC for SiPM as CAL with a 15mW/chn, the max module power is 3.84W, a low power crate is enough with 96chn/crate**
  - **Barrel 2， inner endcap 2， outer endcap 2 power crates**

Summary table

Detector	Max data rate per fiber (Gbps)	Fibers per module	Fiber sum	BEE sum	Data crate sum	Module Max Power (W)	Total Power (kW)	Power channels	Power crate sum	HV requirements	HV channels sum	HV crates sum	Trg boards sum	Trg crates sum	Comment
VTX	8	1~2	88	6	1	25	0.45	66	2	~-10V	66	1			
TPC	0.1	1	496	32	4	42	20	496	6	SHV	496	4			
ITK-Barrel	0.96	1	2204	139	14	11.2	31.59	2204	29	50~200 V	2204	10			
ITK-EndCap	2.2	1	1696	106	12	7.4	11.1	192	2	50~200 V	1696	8			
OTK-Barrel	1.4	1	540	34	4	56.3	251.1	3780	79	150~200 V	3780	17			
OTK-EndCap	0.7	1	720	45	6	58.9	35.6	720	16	150~200 V	720	4			Not finalized
ECAL-Barrel	4.8	2	960	60	6	30	17.5	480	5	40~60V	480	2			
ECAL-EndCap	?	2	520	34	4	30	9.5	260	4	40~60V	260	2			Not finalized
HCAL-Barrel	?	1	5536	346	36	9	66.1	5536	58	40~60V	5536	26			Not finalized
HCAL-EndCap	?	1	1536	96	10	21.9	41.3	1536	16	40~60V	1536	32			Not finalized
Muon-Barrel	?	1	192	12	2	2.54	0.49	192	2	40~60V	192	1			No Det scheme
Muon-EndCap	?	1	128	8	2	3.84	0.38	128	4	40~60V	128	2			No Det scheme
Sum			14616	918	101		485.11	15590	223		17094	109			

Requirement from Sub-Detector for FEE Data – updated

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	42bit （9b X+7b Y +14b BX + 6b TOT + 5TDC + 1b polarity）	32bit (10b chn ID + 10b BX + 6b TOT + 5b chip ID)	40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID)		48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/ chip	Avg：2.9Mbps/chip Max：3.85Mbps/chip	Avg：38.8Mbps/chip Max：452.7Mbps/chip	~70Mbps/ module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)	Needs detector finalization	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	Needs detector finalization	Needs detector finalization
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	Needs detector finalization
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization

A summary of FEE power – updated

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 336mW/chip	20mW/chn 2.56W/chip		280μW/chn 35mW/chip	15mW/chn 240mW/chip				
Max chips@module	29	14	22	22	3	1115	64	Needs detector finalization	8	92	Needs detector finalization
Power@module (W)	5.8	11.2	7.39	56.3	58.9	39.7	30	Needs detector finalization	9	21.9	Needs detector finalization

Preliminary consideration for the TDAQ

- Very early stage for the trigger scheme, many aspects not clear
  - Physics goal for the trigger scheme
  - Needs further discussion on sub detectors that participate in the trigger decision, and information that can be attracted from detectors
  - Trigger algorithm vs related resources depend on complexity
- Needs to define the requirement for the trigger latency
  - From electronics: can rely on big RAM, then the restore capability can be enough
    - ➢ Ref parameters: 8GB ram on BEE, a 16-chn BEE with max data rate of 160Gbps, can hold a buffer length to be 8G×8/160=0.4s
  - From detector: response speed of many detectors not finalized, some slow detectors will affect the trigger latency
- Current rough estimation: Trigger system needs 160 Trg boards = 20 ATCA crates = 10 Racks
- Note:
  - Z pole bkgrd is too high at current stage (esp. ECAL), not clear for the future optimization.
  - However future upgrade is necessary, and reserved room should be pre-allocated.

CMS board type & number

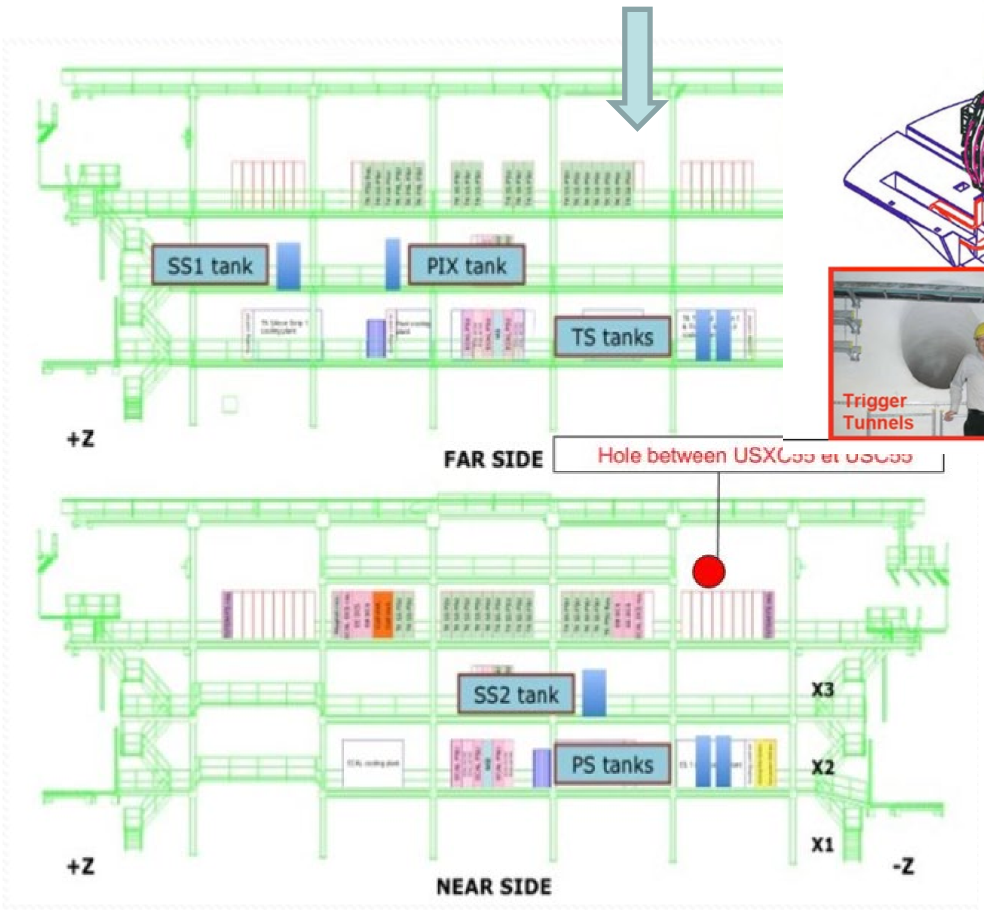
Table 1.2: CMS Phase-2 detector projected data links, ATCA back-end configuration and event size summary. Data are obtained from the technical design reports wherever possible. Average throughput estimated from event size assuming 750 kHz Level-1-accept rate.

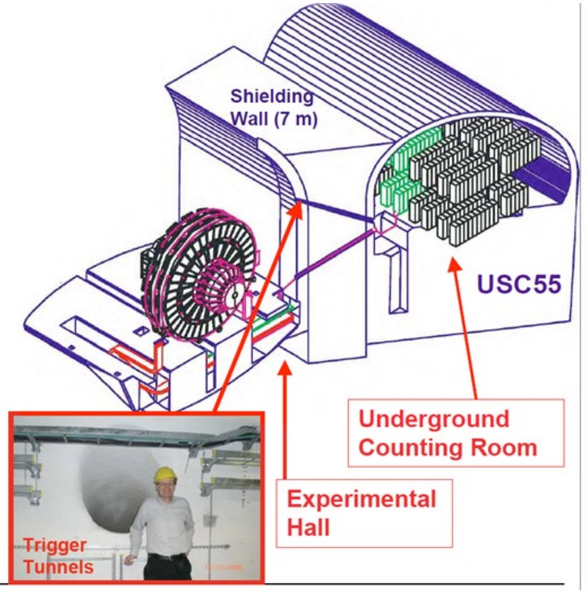
Subdetector	Front-end lpGBT links[a]	Sub-event size (MB)	Back-end boards	Back-end crates	Average throughput (Tb/s)	Notes
Outer Tracker	13 000	1.15	216	18	6.90	([b])
Track Trigger		0.01		18	0.06	
Inner Tracker	1 260	1.44	24	4	8.64	([c])
MIP Timing Det. - BTL	1 000	0.02	11	1	0.14	
MIP Timing Det. - ETL	438	0.04	5	1	0.22	
ECAL Barrel	10 000	1.58	108	12	9.49	
HCAL Barrel	other	0.24	18	2	1.45	
HCAL - HO	legacy	0.03	-	1	0.18	([d])
HCAL - HF	other	0.06	-	1	0.36	([d])
Endcap CALO	8 000	2.00	108	9	12.00	
Endcap CALO TPG	9 000	0.20	144	12	1.50	
muon DT	3 840	0.13	84	8	0.78	
muon CSC	other	0.20	-	2	1.20	([d])
muon GEM - GE1/1	other	0.002	-	1	0.01	([d])
muon GEM - GE2/1	144	0.001	8	1	0.01	
muon GEM - ME0	216	0.12	12	1	0.71	
muon RPC	other	-	-	-	-	([e])
Level1		0.15	120	14	0.90	([f])
Total		7.4	>858	>106	44	

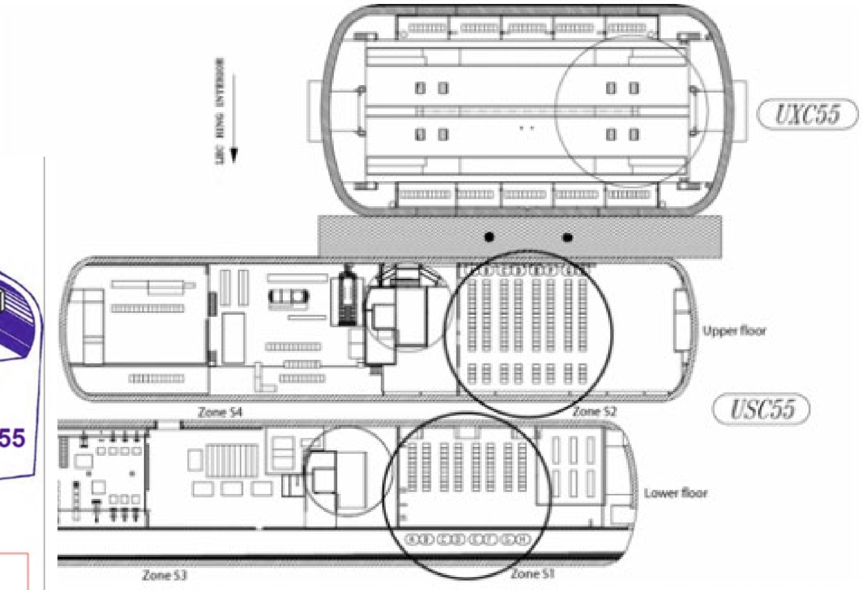
- **The total number of data crates of CMS matches with our calculation for CEPC**
- **Why choose CMS for a comparison? Similar detector scale, similar trigger framework (both are backend trigger)**

CMS counting room

https://cds.cern.ch/record/1027431/files/p165.pdf







ure 4: Point 5 Underground Area; The experimental cavern
C55 with the adjacent, albeit a 7 meter thick concrete wall,
derground counting room USC55, consisting of two floors.

- **USC55 size： 19m×17m × 85m***
- **Racks located centralizedly (see table below)**

CMS USC55 counting room

*: https://doi.org/10.1007/978-3-031-12851-6_49

CMS racks organization

Upper Floor (Zone S2)

+Z	A	B	C	D	E	F	G	H -Z
01	--	--	--	ECAL spare	Cal Reg Trig	HCAL HTR	--	--
02	TOTEM	TOTEM	DAQ	ECAL ULR	Cal Reg Trig	HCAL HTR	DAQ	x
03	TOTEM	TOTEM	CASTOR HV	ECAL ULR	%Cal Reg Trig	HCAL HTR	EBE DCS	x
04	TOTEM	TOTEM	CASTOR HV	ECAL ULR	Cal Reg Trig	HCAL HTR	EBE DCS	x
05	TOTEM	DAQ	UX DCS	ECAL SRP/TST	%Cal Reg Trig	%HCAL HTR	Presh. HV	x
06	RAMSES	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
07	Access	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*08	ASSM	EB HV	HCAL SrcDrv	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*09	ASSM	EE HV	HPD HV	DAQ	Cal Reg Trig	HCAL HTR	EE HV	x
10	ASSM	Presh. DCS	HPD HV	FRL PC	Cal Reg Trig	DAQ	Presh. DCS	x
11	ASSM	ECAL LV	HPD HV	x	TOTEM Trig	EBE Lt Mn	ECAL Cool	DSS
12	ASSM	ECAL LV	HPD HV	x	CASTOR Trig	EBE Lt Mn	ECAL Cool	DSS
13	ASSM	Presh. LV	HPD HV	Presh. Misc	ZDC	EBE Lt Mn	ECAL Cool	DSS
14	ASSM	Rack Pwr	PMT HV	Presh. Misc	DAQ PP	EB Misc	EE Misc	DSS
15	ASSM	Rack Pwr	DSS	DSS	DSS	DSS	DSS	DSS
				<-- Passageway -->				
16	Fire Det.	TTC PCs	DAQ PC	DAQ Switch	Netwk	DCS PCs	Spare PCs	UPS PCs
*17	Fire Det.	TK PCs	DAQ PC	DAQ Switch	Netwk	HCAL PCs	Trig PCs	UPS PCs
*18	Fire Det.	TK/Pixel PCs	DAQ PC	DAQ Switch	Netwk	ECAL DCS/ES PCs	Muon PCs	UPS PCs
19	Fire Det.	TOTEM PCs	DAQ PC	DAQ Switch	Netwk	ECAL FED PCs	Align PCs	UPS PCs

Lower Floor (Zone S1)

+Z	A	B	C	D	E	F	G	H -Z
00	--	--	Presh. ULR	Presh. ULR	TK. FEC	TK. FEC	DT/RO/SC	--
01	--	--	DAQ	DT TrkFnd	Opt.Cpl.	RPC Trig	Pixel FEC	--
02	TK. Ctrl	DAQ	DAQ	DT TrkFnd	TTC	RPC Trig	Pixel Ctrl	RPC B HV
03	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	DT TrkFnd	%TTC	RPC Trig	Pixel FED	RPC B HV
04	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	Global	RPC Trig	Pixel FED	RPC B HV
05	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	%Cal Global	%RPC Trig	DAQ	RPC B HV
06	TK. Ctrl	DAQ	DAQ	FRL PC	TTS	DAQ	CSC FED	RPC B HV
07	TK. Ctrl	DAQ	DAQ	DT HV	TTS	x	CSC FED	RPC B HV
*08	TK. Ctrl	TK. FED TEC-	TK. FED TEC+#	DT HV	BPTX	BRM#	CSC FED	RPC E+ HV
*09	TK. Ctrl	TK. FED TEC-	TK. FED TEC+#	DT HV	LHC	DAQ#	DAQ PP	RPC E+ HV
10	TK LV Mon	TK. FED TEC-	TK. FED TEC+	DT HV	BPM	DSS	ME1/1 HV	RPC E- HV
11	CSC HV	DAQ	DAQ	DT HV	DSS	DSS	DSS	RPC E- HV
12	CSC HV	TK. Ctrl	Work Area	DAQ PC	Work Area	Work Area	Work Area	Work Area
13	CSC HV	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area
14	BCAM	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area
15	Rack Pwr	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area
				<-- Passageway -->				

- **Counts for electronics, trigger, HV racks, about 30 row*7 col=210 racks**
- **DAQ & slow control racks in 4 row*7 col=28 racks**

CMS racks organization

Floorplan of the racks should consider the detector arrangement

Sensitive racks related to trigger & timing needs careful arrangement

Rack Layout in USC55 (version 5.6)

Both floors are shown. Racks are installed out to #11, 15 on S1,2. Row A is closest to the shaft. Racks 0 (S1) and 1 (S2) are closest to the interaction hall (UXC55).
* Rack rows are spaced 1.5 m front face to front face (B-C,D-E,F-G,H-J)) and 1.0 m rear face to rear face (A-B,C-D,E-F,G-H,J-K). *There is a 30 cm optional gap between racks 8 & 9 (and 17 & 18 on S1) to improve access over an underfloor structural beam. #There is a 30 cm gap between racks S1C08 and S1C09 and also between S1F08 and S1F09 for a vertical structural column. %There are holes between the floors located at E05 and F05. RED RACKS HAVE CRITICAL LENGTH FIBERS TO THE DETECTOR. GREEN RACKS HAVE NON-CRITICAL PATH FIBERS TO THE DETECTOR. DAQ RACKS ARE BLUE. GREY RACKS ARE RESERVATIONS.
Definition of abbreviations. Information about racks. Rack Wizard (rack entry tool).

+Z			Lower	Floor	(Zone S1)			-Z
	A	B	C	D	E	F	G	H
00	--	--	Presh. ULR	Presh. ULR	TK. FEC	TK. FEC	DT/RO/SC	--
01	--	--	DAQ	DT TrkFnd	Opt.Cpl.	RPC Trig	Pixel FEC	--
02	TK. Ctrl	DAQ	DAQ	DT TrkFnd	TTC	RPC Trig	Pixel Ctrl	RPC B HV
03	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	DT TrkFnd	%TTC	RPC Trig	Pixel FED	RPC B HV
04	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	Global	RPC Trig	Pixel FED	RPC B HV
05	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	%Cal Global	%RPC Trig	DAQ	RPC B HV
06	TK. Ctrl	DAQ	DAQ	FRL PC	TTS	DAQ	CSC FED	RPC B HV
07	TK. Ctrl	DAQ	DAQ	DT HV	TTS	x	CSC FED	RPC B HV
*08	TK. Ctrl	TK. FED TEC-	TK. FED TEC+#	DT HV	BPTX	BRM#	CSC FED	RPC E+ HV
*09	TK. Ctrl	TK. FED TEC-	TK. FED TEC+#	DT HV	LHC	DAQ#	DAQ PP	RPC E+ HV
10	TK LV Mon	TK. FED TEC-	TK. FED TEC+	DT HV	BPM	DSS	ME1/1 HV	RPC E- HV
11	CSC HV	DAQ	DAQ	DT HV	DSS	DSS	DSS	RPC E- HV
12	CSC HV	TK. Ctrl	Work Area	DAQ PC	Work Area	Work Area	Work Area	Work Area
13	CSC HV	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area
14	BCAM	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area
15	Rack Pwr	TK. Ctrl	Work Area	Work Area	Work Area	Work Area	Work Area	Work Area

<-- Passageway -->

https://cmsdoc.cern.ch/~wsmith/USC55_racks_v56.html

Summary for the Racks

- No safety factor for all the former calculation
- In total
  - 101 Data Crates, 3 crates per rack, = 34 Data Racks
  - 472 (LV) Power Crates, 10 crates per rack, = 48 Power Racks
  - 164 Det-HV Crates, 3/4 crates per rack, = 42 Det-HV Racks
  - 20 Trigger crates = 10 Trigger Racks
- Every LV rack needs an AC-DC power-HV crate, about 134 power-HV crates
  - 5 crates per rack, = 27 Power-HV Racks

- In general, rack backup, room for future upgrade, uncertainty due to the un-finalized detector scheme, esp. the extra space requirements that the trigger algorithm usually asks the rack layout to be corresponded to the detector arrangement, will decrease the density of the rack and crate usage.

Requirement of the Elec-TDAQ room

- Considered a safety factor of ×1.5 according to the minimum number of racks, racks of:
  - 34 × 1.5=51 data racks, 48 ×1.5= 72 power racks
  - 42 ×1.5=63 Det-HV racks, 10 ×1.5=15 trigger racks, & 27 ×1.5= 41 Power-HV racks
  - In total of 242 racks are needed
  - At the similar level as the CMS total racks of about 210 racks
- Considering the racks heat dissipation
  - spacing 1.5m, plus rack thickness of 0.5m, -> rack pitch to be 2m
- The total requirement for the electronics room can be 10 rows * 16 columns * 2 floors = 320 rack capacity, equals to 20m×32m×2floors
  - Also similar to the space as CMS
- However, the height of each electronics room can not be decided yet, needs global design from the mechanical point of view

- **backup**