COFFEE IVCV test

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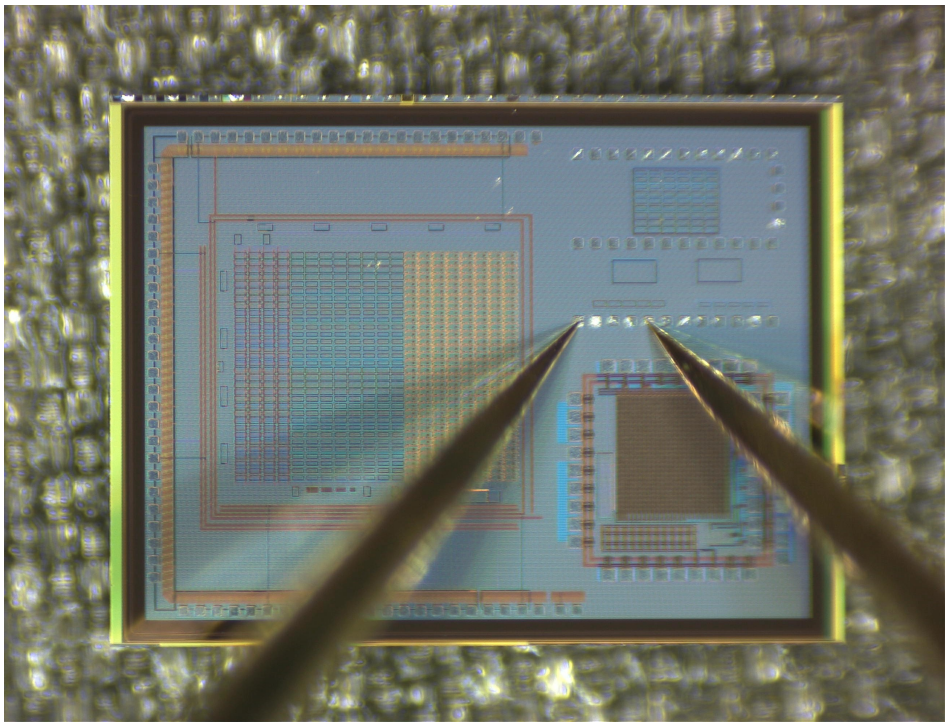
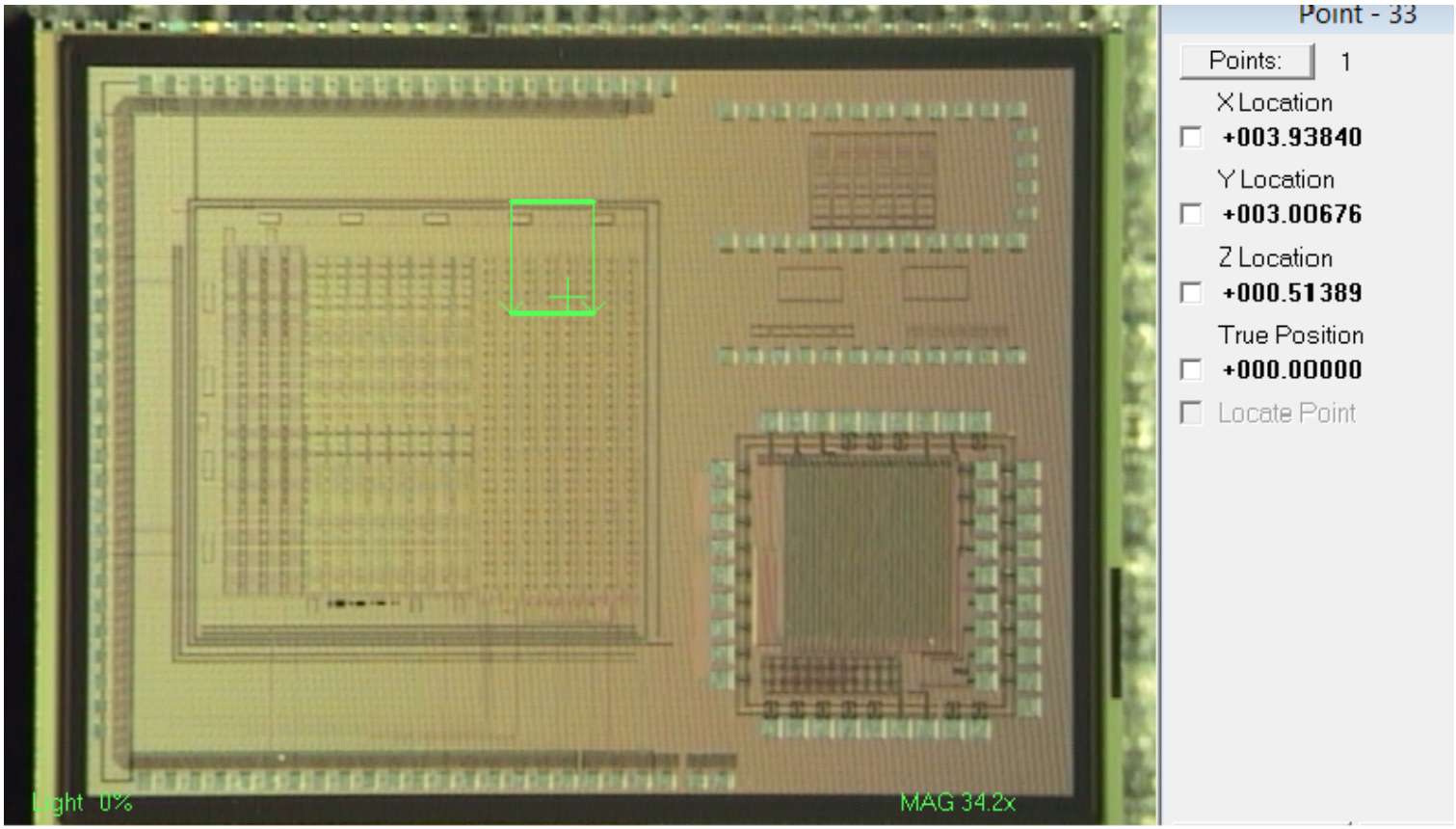
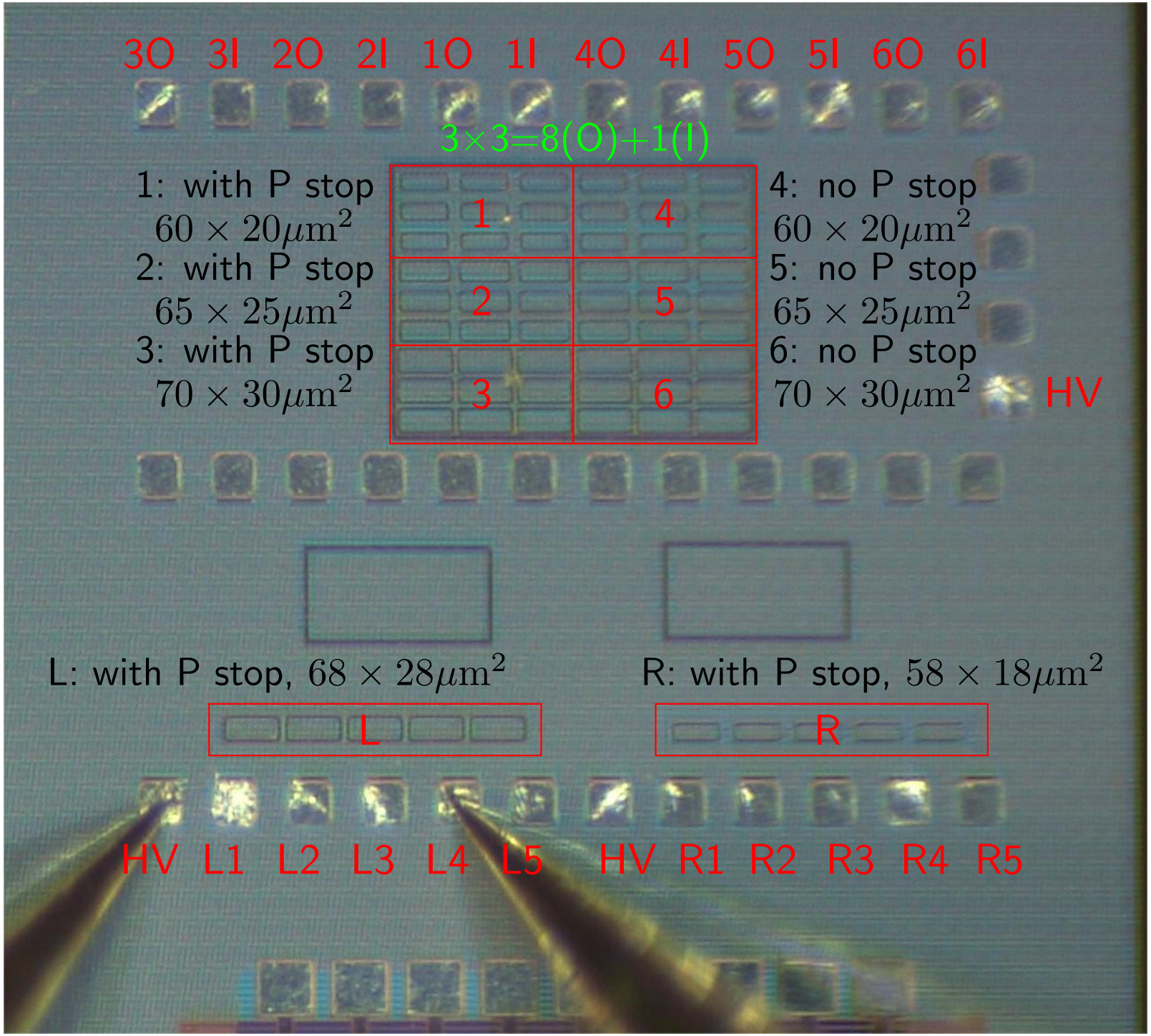
January 11, 2024



Chip size

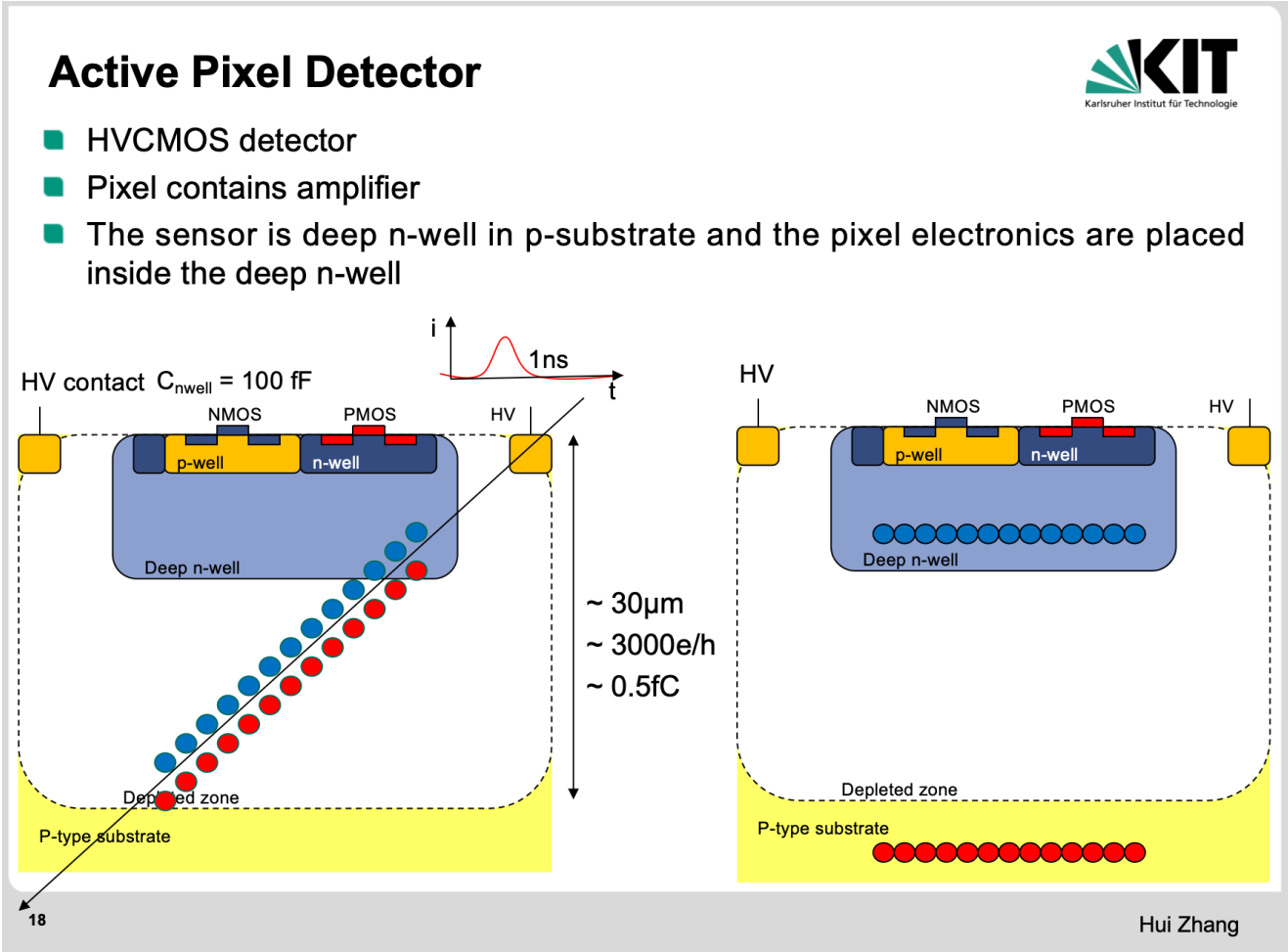
- Area $\sim 4 \times 3\mathrm{mm}^2$, thickness $\sim 500\mu\mathrm{m}$




3O 3I 2O 2I 1O 1I 4O 4I 5O 5I 6O 6I
3×3=8(O)+1(I)
1: with P stop
$60 \times 20\mu m^2$
2: with P stop
$65 \times 25\mu m^2$
3: with P stop
$70 \times 30\mu m^2$
1
2
3
4
5
6
4: no P stop
$60 \times 20\mu m^2$
5: no P stop
$65 \times 25\mu m^2$
6: no P stop
$70 \times 30\mu m^2$
HV
L: with P stop, $68 \times 28\mu m^2$
R: with P stop, $58 \times 18\mu m^2$
L
R
HV L1 L2 L3 L4 L5 HV R1 R2 R3 R4 R5

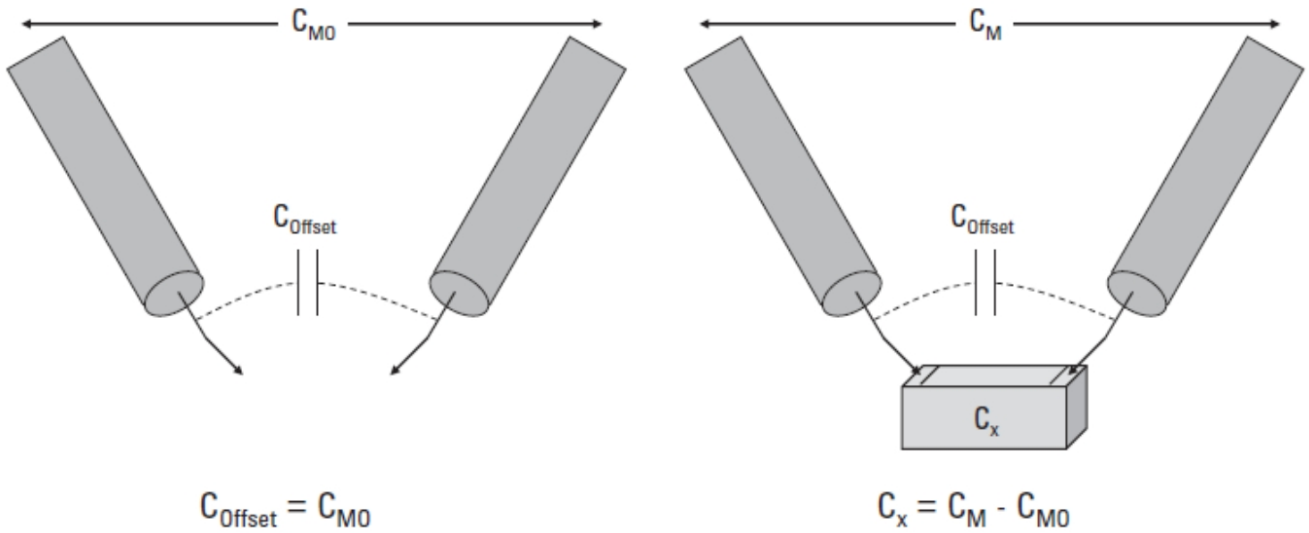
HVCMOS depletion, i.e. TSI 180nm process

- 160V gives $\sim 55\mu\mathrm{m}$ depletion depth.
- Would not expect fully depleted for COFFEE2.



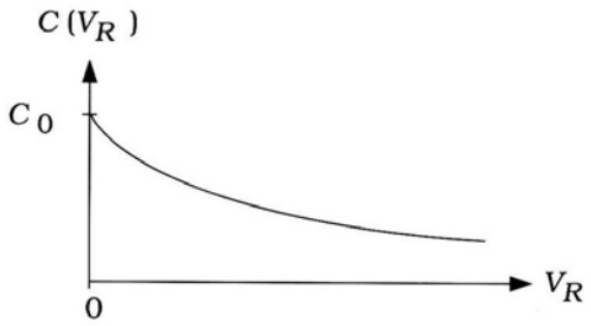
What changed

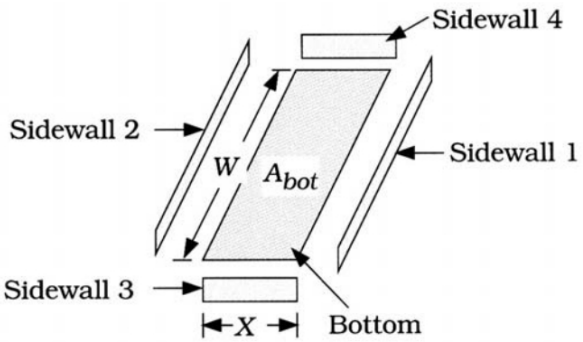
- Improved COFFEE2 test procedure than COFFEE1.
- SourceMeter(2470) is programmed to scan automatically, making test faster, more stable and more reliable.
- LCR meter open corrected in the right way. After correction, offset for 10kHz/100kHz (1MHz) $\sim$ 1fF (-50fF, acceptable).
- Consider offset, results are consistent for 10kHz $\sim$ 1MHz.



Capacitance: sidewall & bottom?

- Ideal PN junction has $\frac{1}{C^2} \propto V_R$, $C = C_0/\sqrt{1+\frac{V_R}{\phi_0}}$





- **Q:** do we have sizeable sidewall effect?

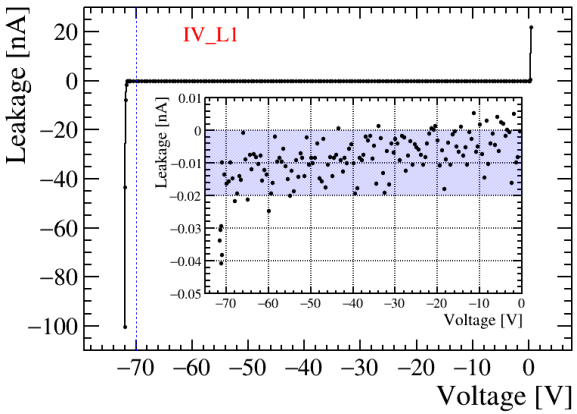
$$\mathrm{C} = \mathrm{C}^{\mathrm{bot}} + \mathrm{C}^{\mathrm{sw}} \propto \frac{\mathrm{C}_0^{\mathrm{bot}}}{\sqrt{\phi_0^{\mathrm{bot}} + \mathrm{V_R}}} + \frac{\mathrm{C}_0^{\mathrm{sw}}}{\sqrt{\phi_0^{\mathrm{sw}} + \mathrm{V_R}}}$$

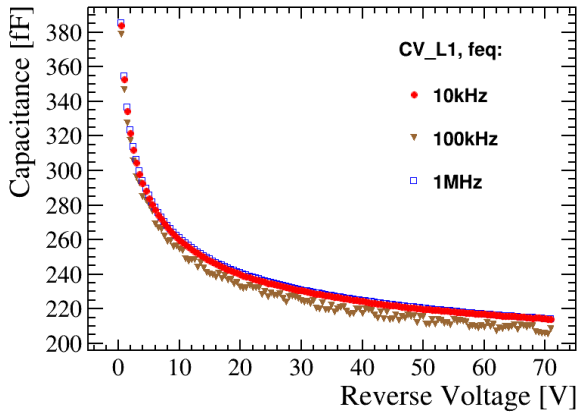
Roughly, $\quad \frac{1}{\mathrm{C}^2} \propto \mathrm{p_0} + \mathrm{p_1} \cdot \frac{1}{\mathrm{V_R}} + \mathrm{p_2} \cdot \mathrm{V_R} \not\propto \mathrm{V_R}$

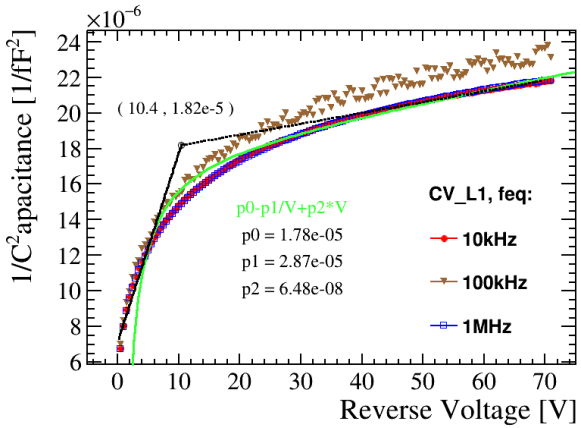
- If correctly, the function obtained by taking any 3 points (i.e 5V, 30V, 60V) should be able to roughly describe the distribution.

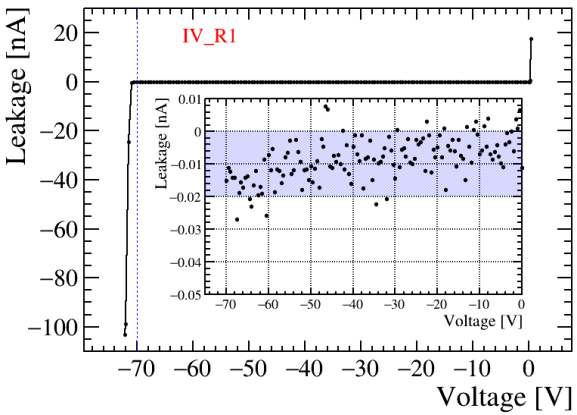
Single pixel: L1 & R1 (DNW: $\mathrm{L} \sim 12\mu\mathrm{m}, \mathrm{R} \sim 22\mu\mathrm{m}$)

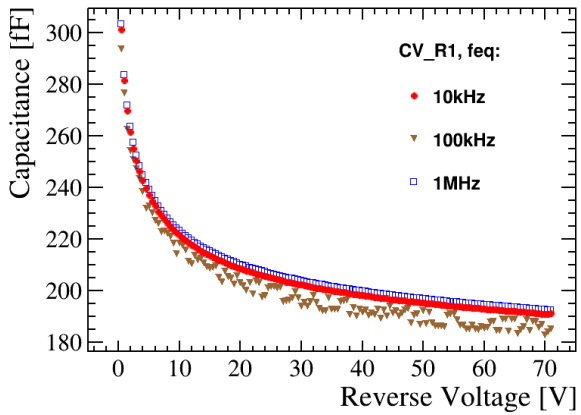
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(L1)} \sim 210\mathrm{fF}$, $\mathrm{C_{max}(R1)} \sim 190\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

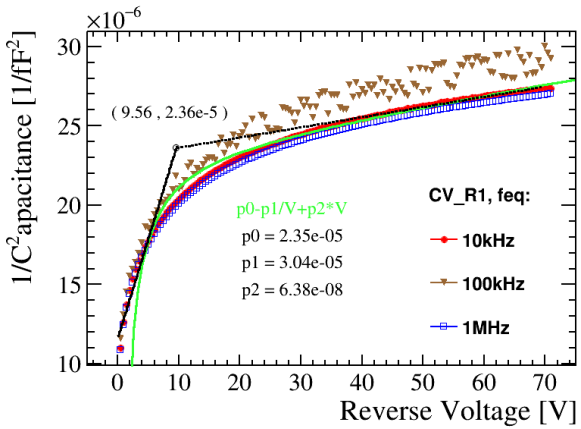






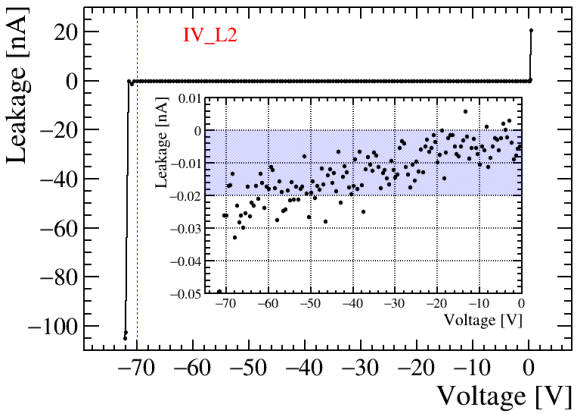


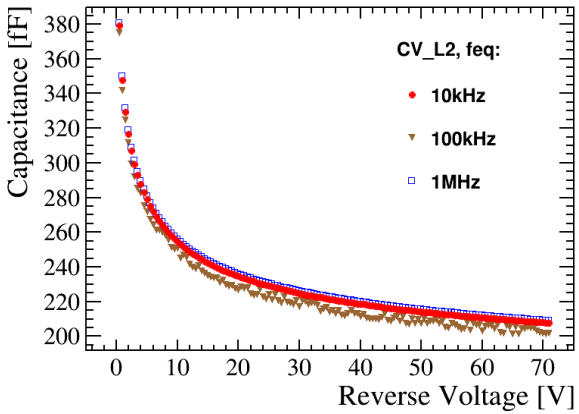


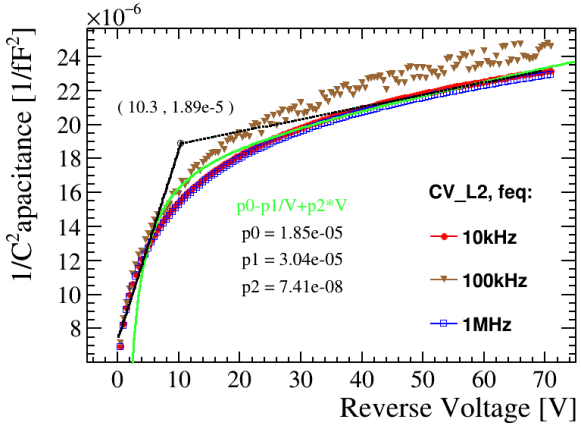


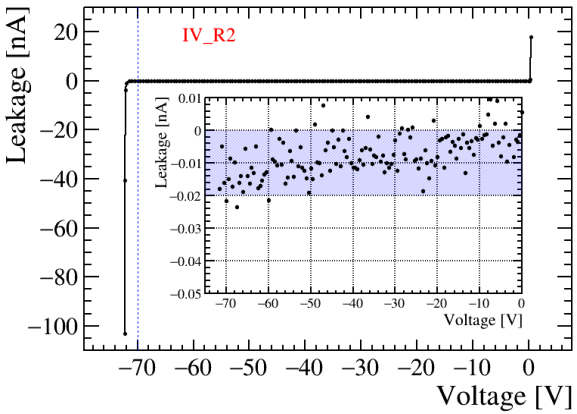
Single pixel: L2 & R2

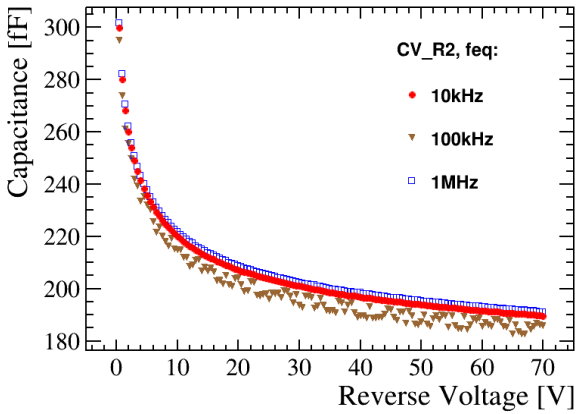
- Breakdown voltage > 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(L2)} \sim 210\mathrm{fF}$, $\mathrm{C_{max}(R2)} \sim 190\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

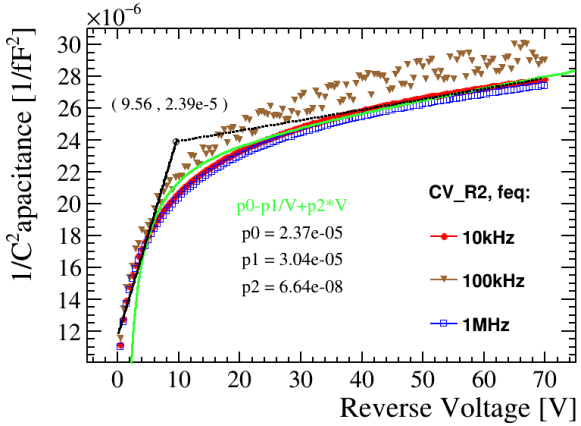






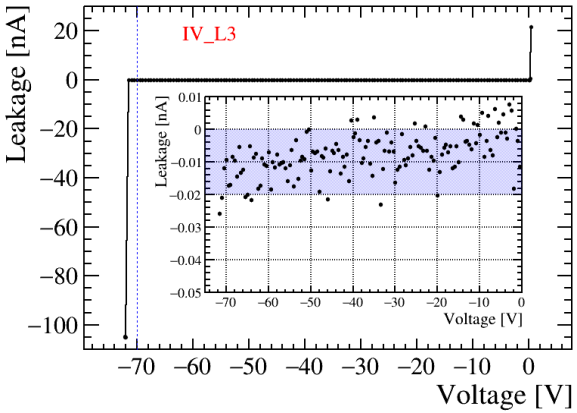


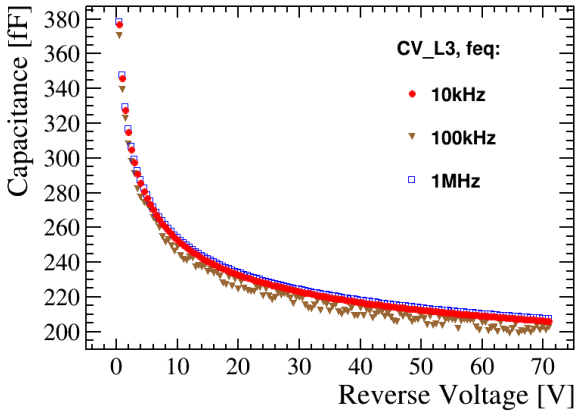


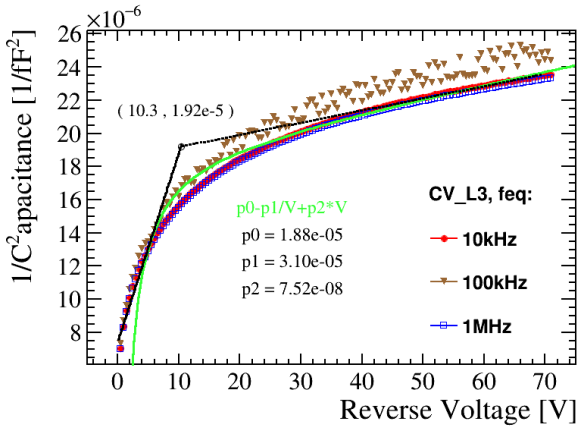


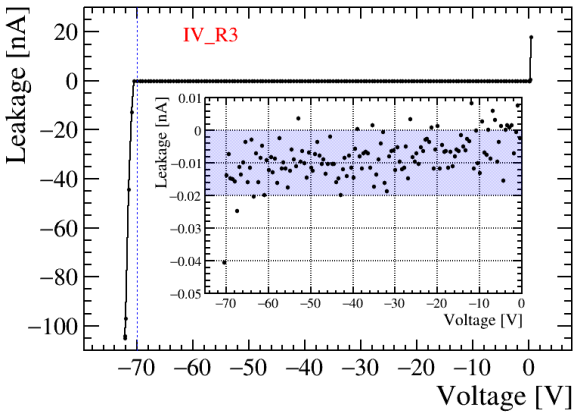
Single pixel: L3 & R3

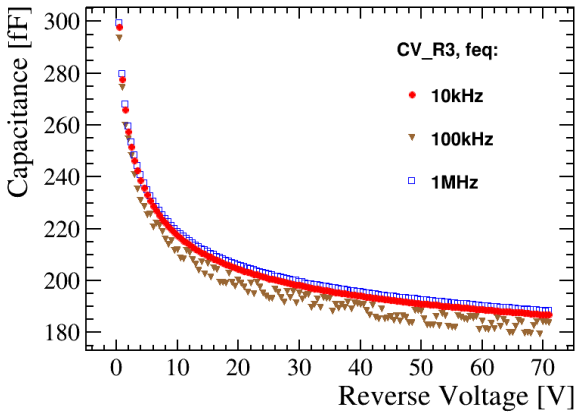
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(L3)} \sim 210\mathrm{fF}$, $\mathrm{C_{max}(R3)} \sim 190\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

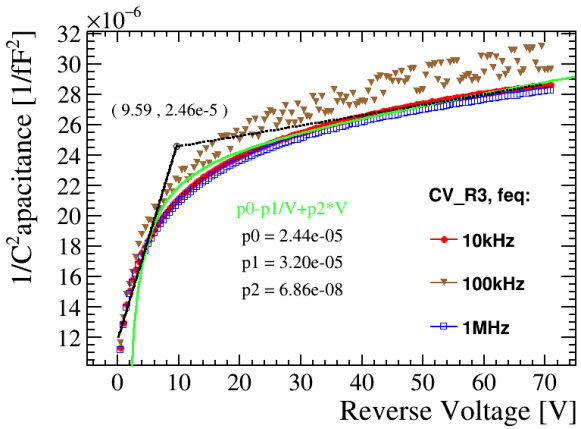






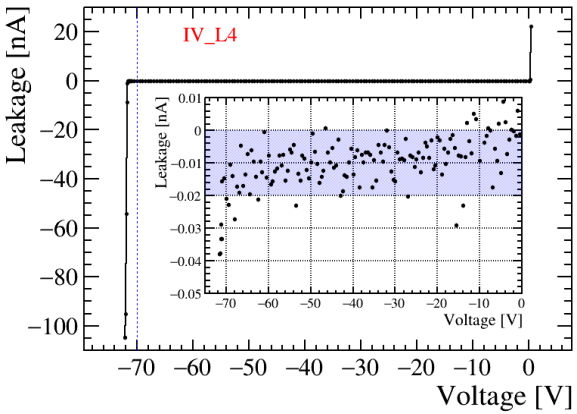


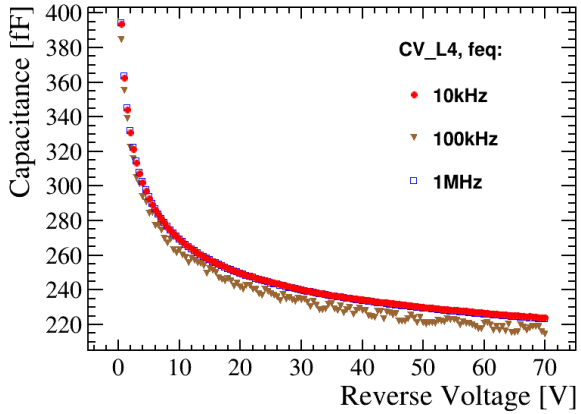


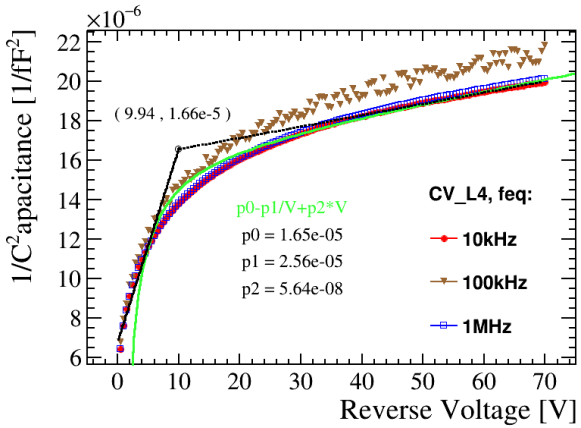


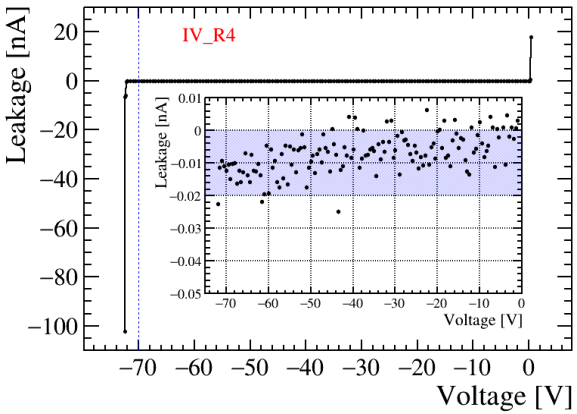
Single pixel: L4 & R4

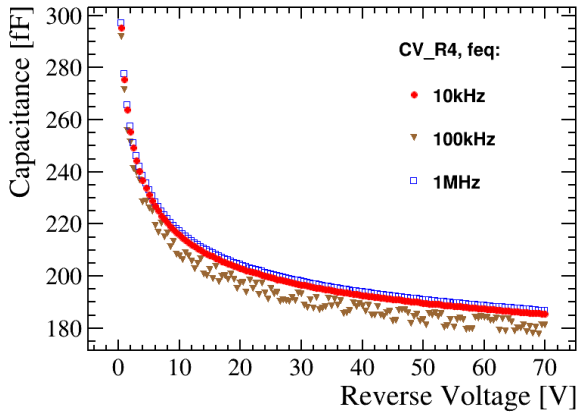
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(L4)} \sim 220\mathrm{fF}$, $\mathrm{C_{max}(R4)} \sim 180\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

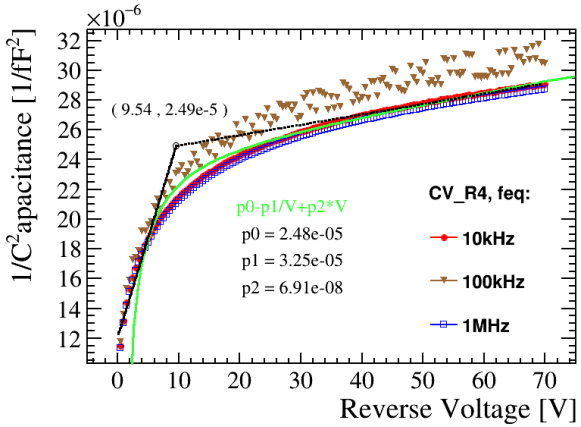






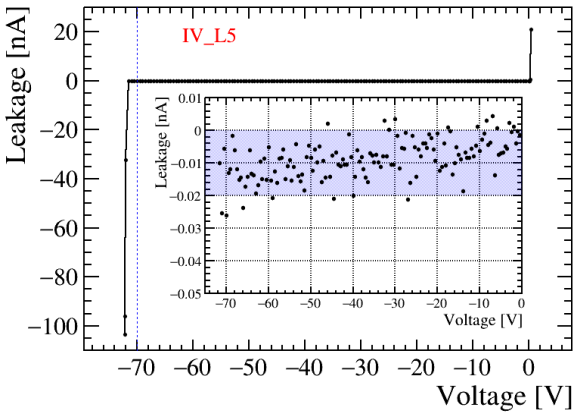


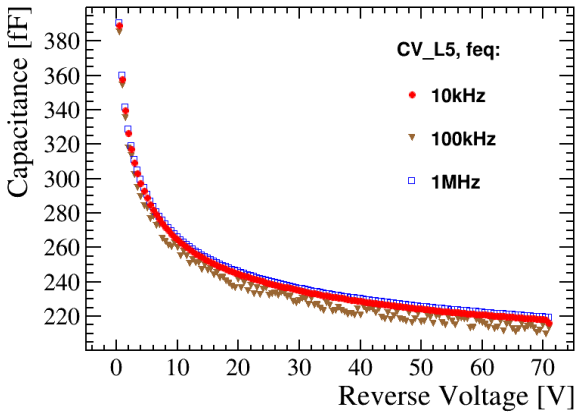


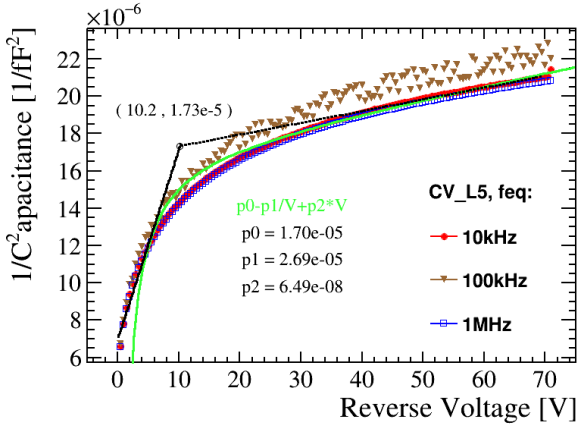


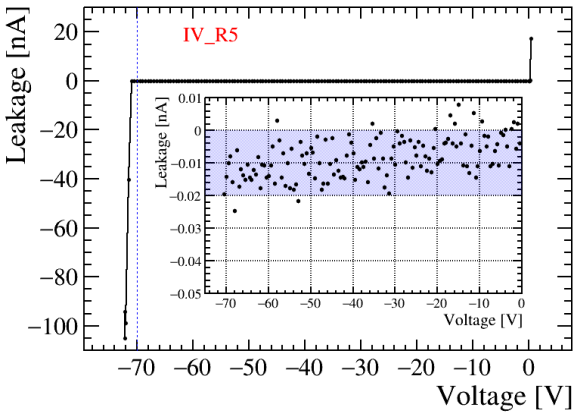
Single pixel: L5 & R5

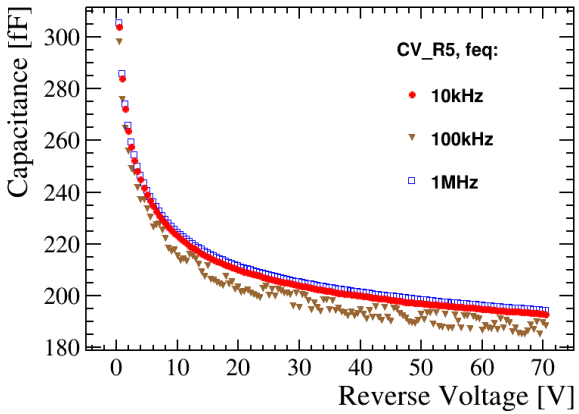
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(L5)} \sim 220\mathrm{fF}$, $\mathrm{C_{max}(R5)} \sim 190\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

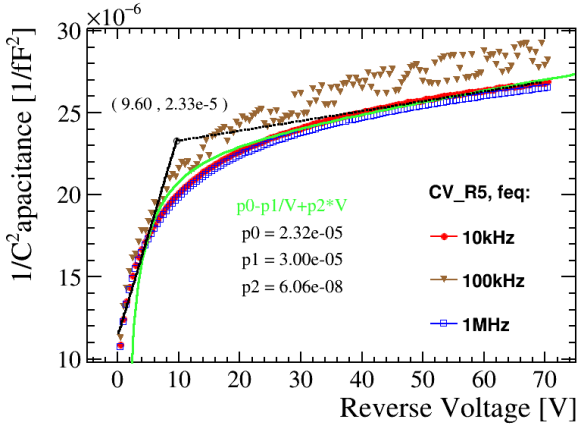






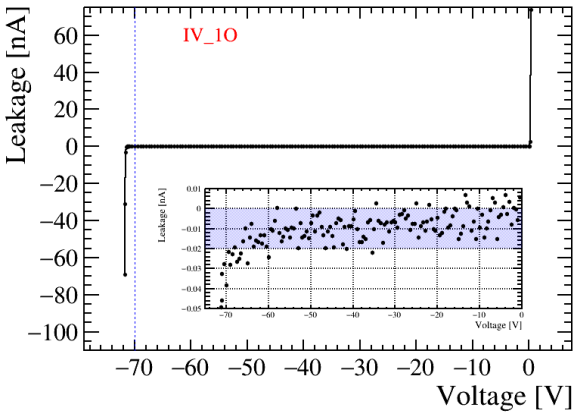


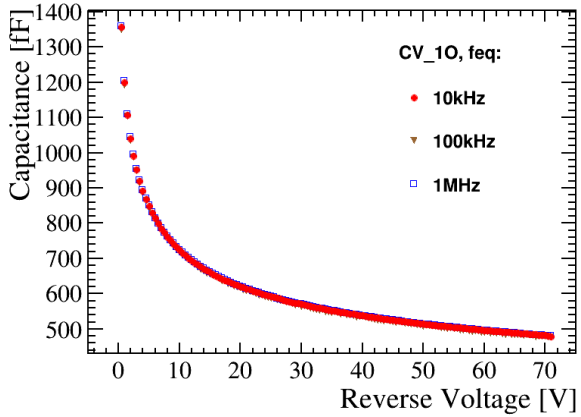


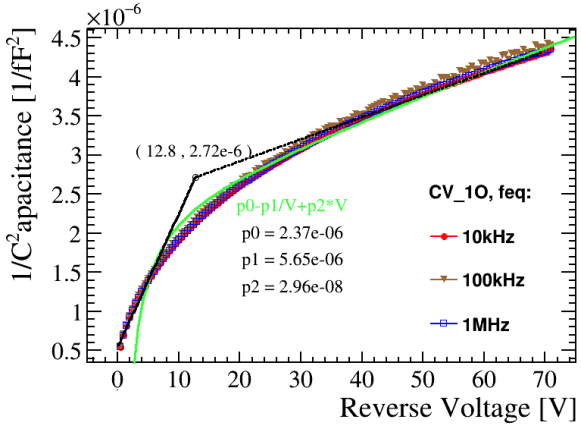


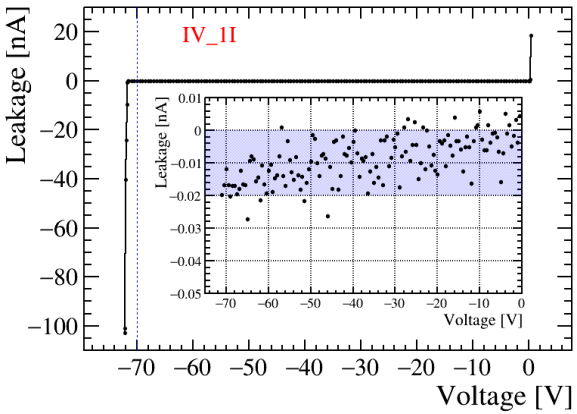
Multi pixel: Sector1

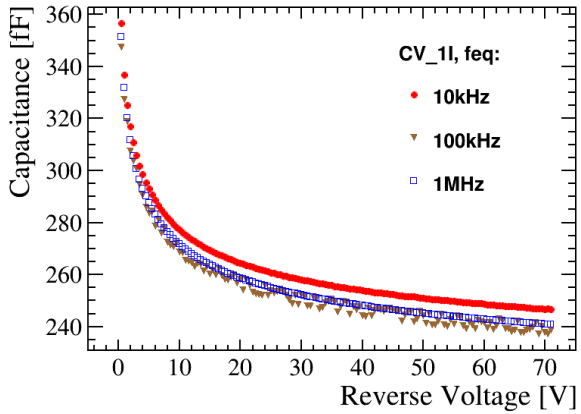
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(1O)} \sim 480\mathrm{fF}$, $\mathrm{C_{max}(1I)} \sim 240\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

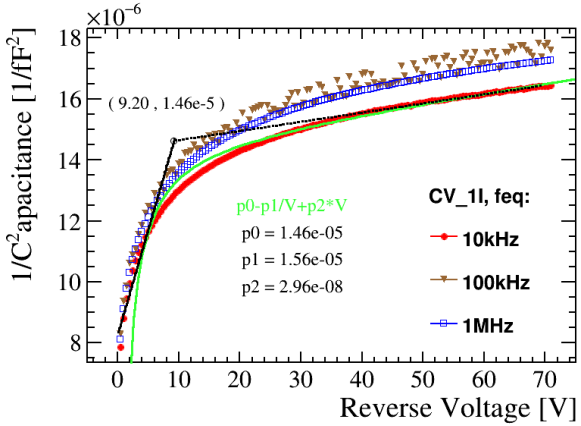






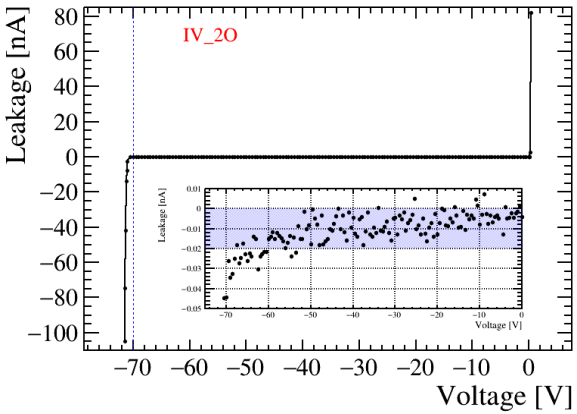


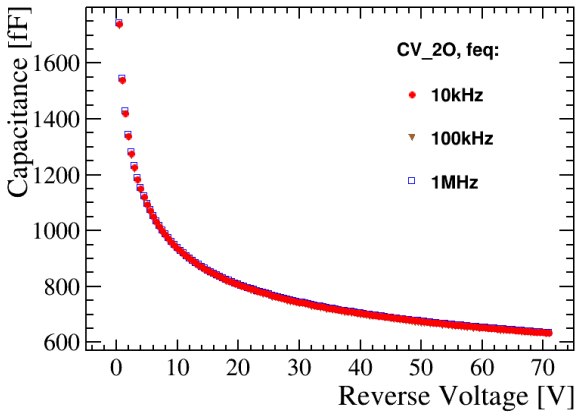


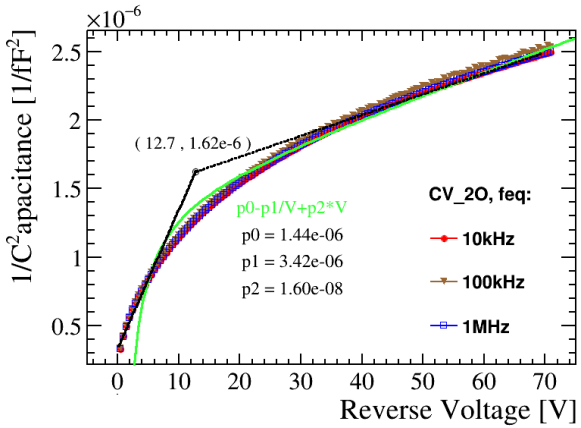


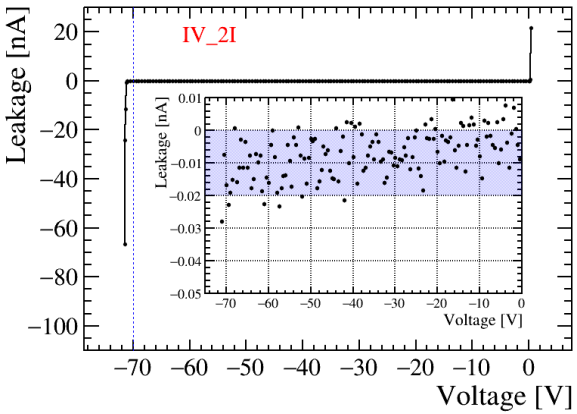
Multi pixel: Sector2

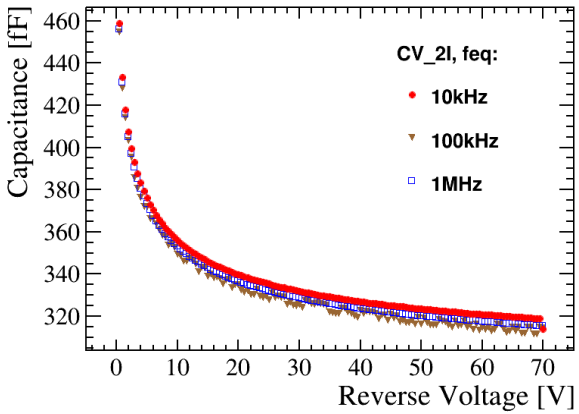
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(2O)} \sim 630\mathrm{fF}$, $\mathrm{C_{max}(2I)} \sim 310\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

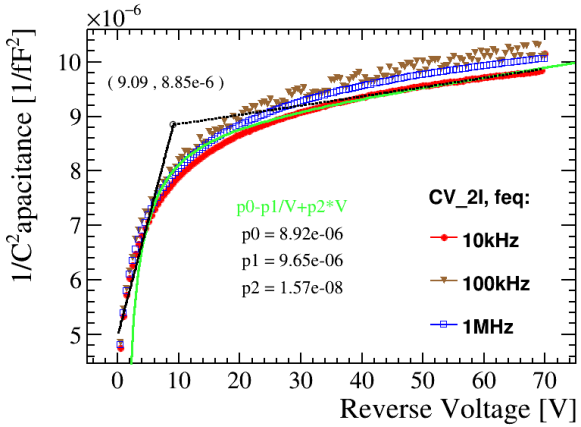






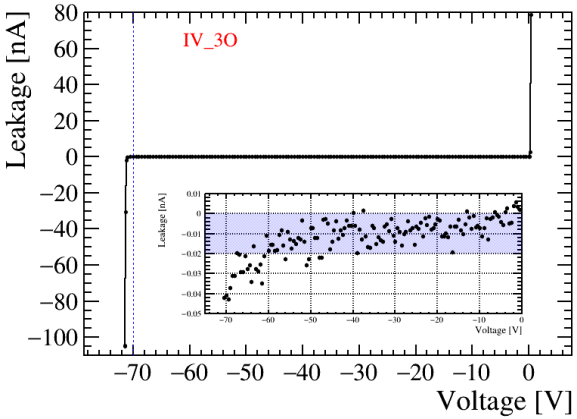


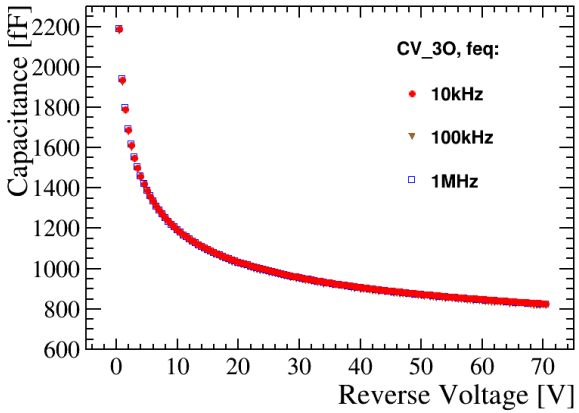


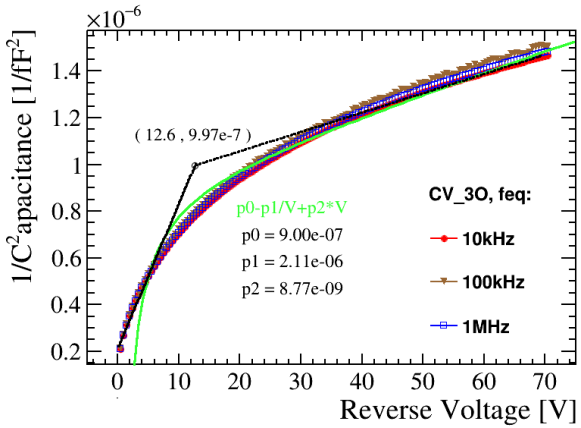


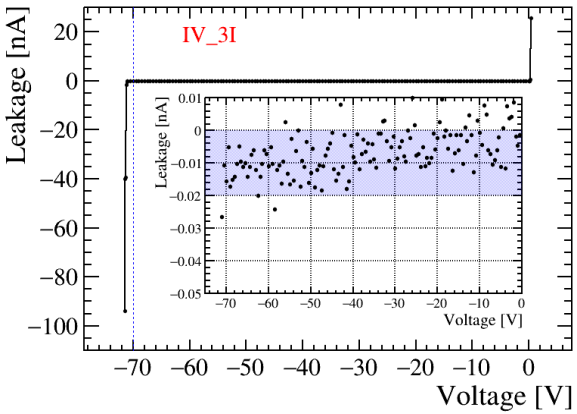
Multi pixel: Sector3

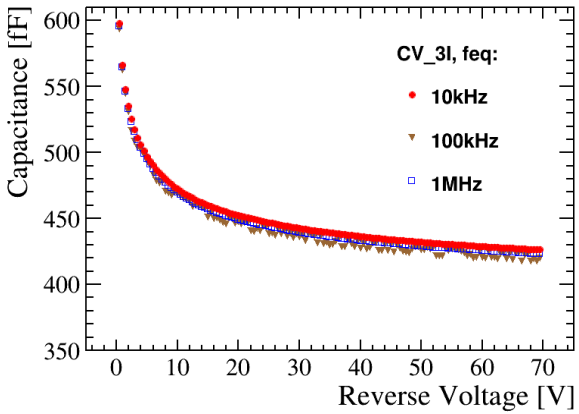
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(3O)} \sim 830\mathrm{fF}$, $\mathrm{C_{max}(3I)} \sim 420\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

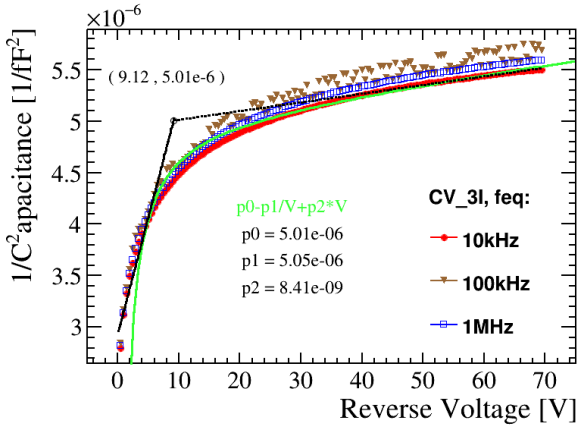






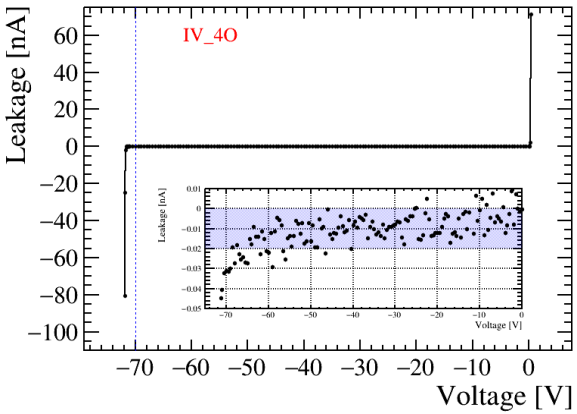


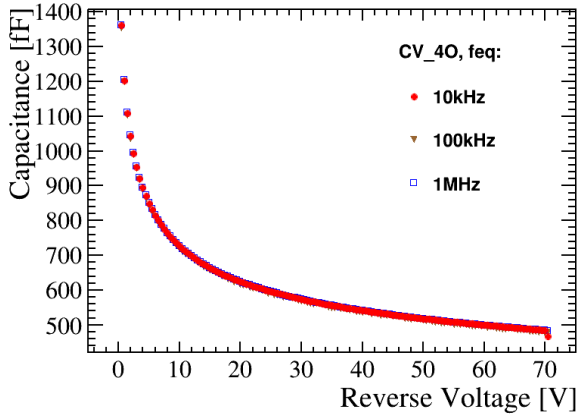


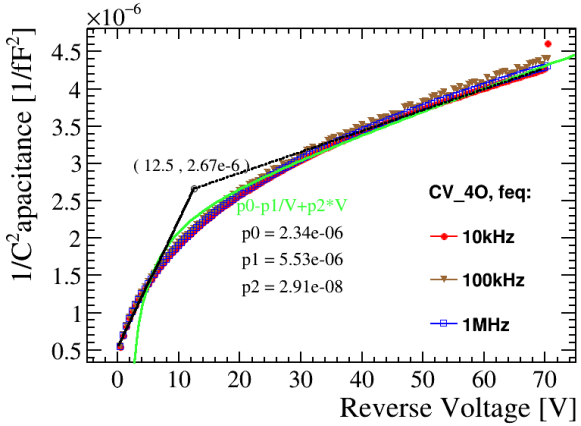


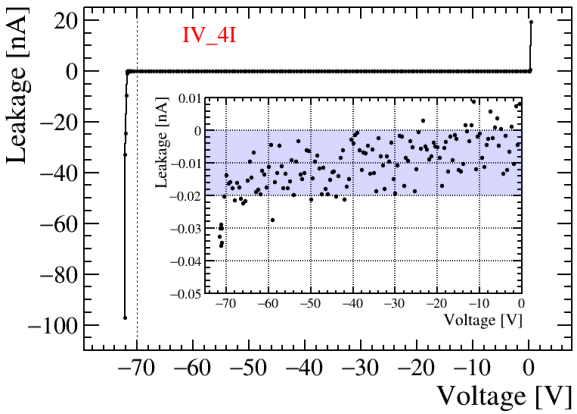
Multi pixel: Sector4

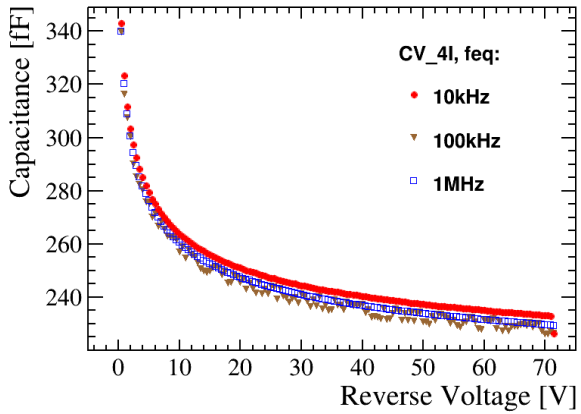
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(4O)} \sim 480\mathrm{fF}$, $\mathrm{C_{max}(4I)} \sim 230\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

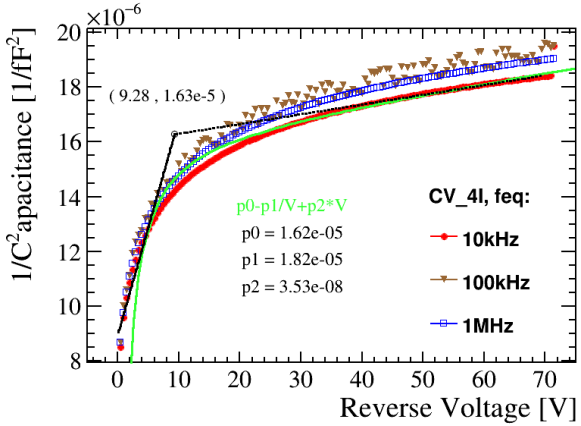






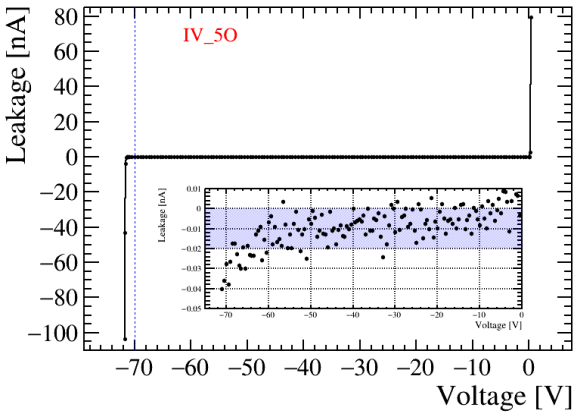


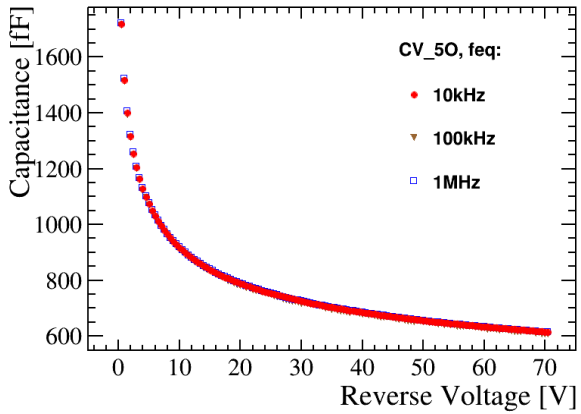


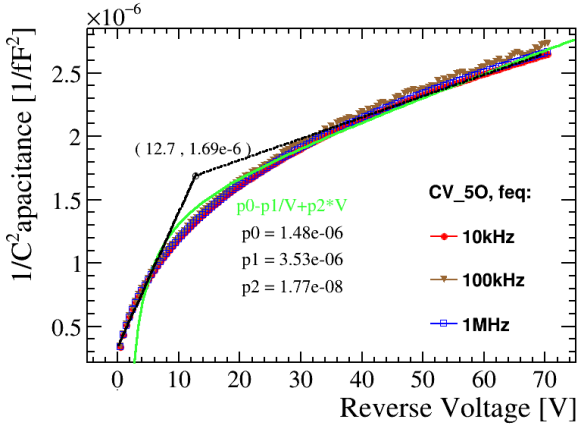


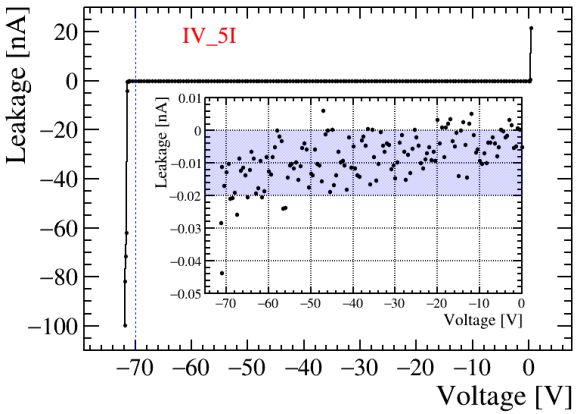
Multi pixel: Sector5

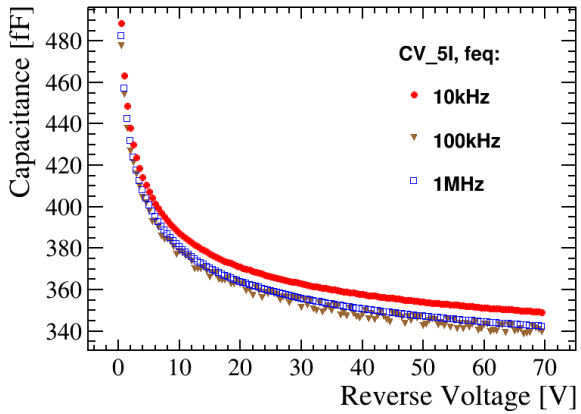
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(5O)} \sim 620\mathrm{fF}$, $\mathrm{C_{max}(5I)} \sim 350\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

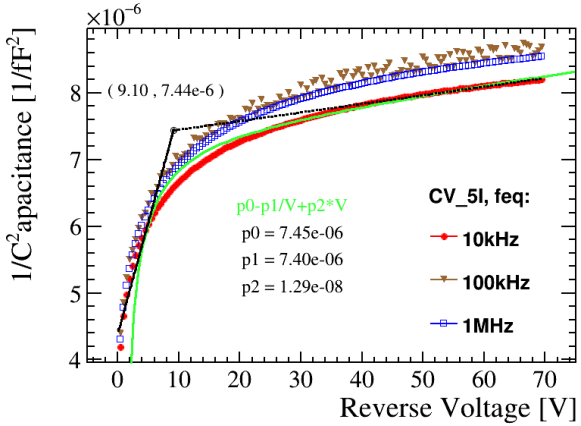






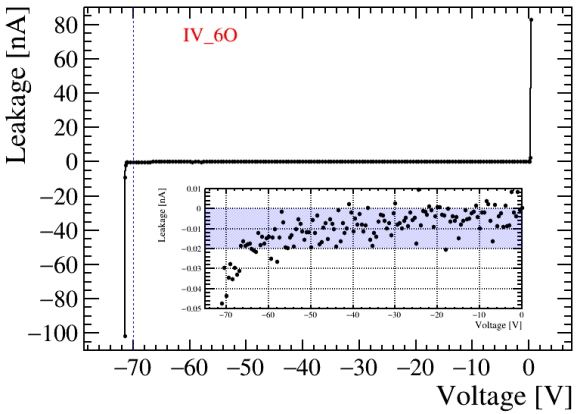


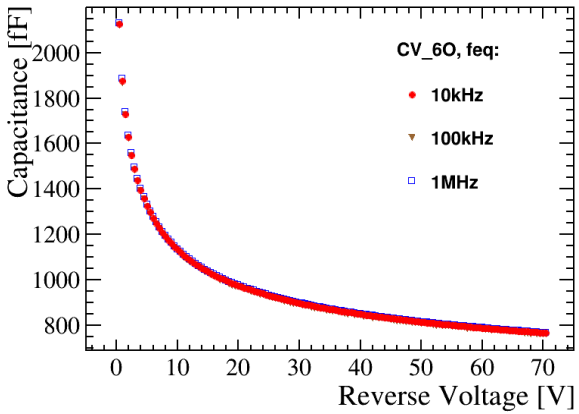


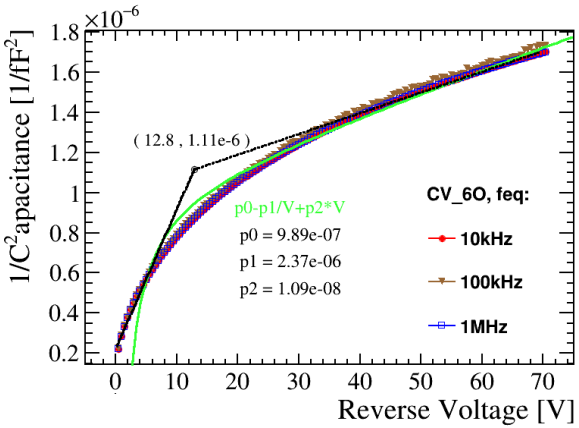


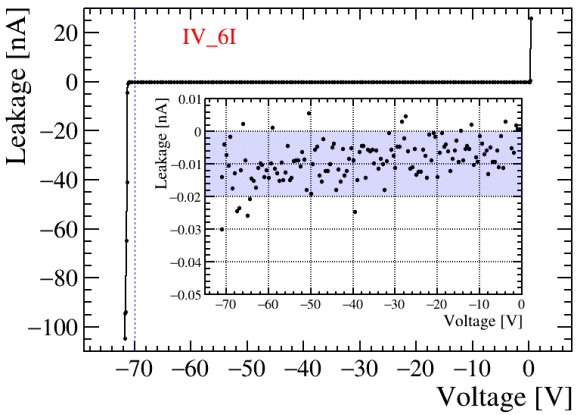
Multi pixel: Sector6

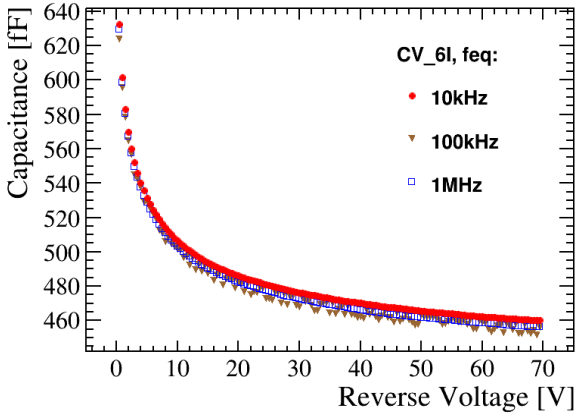
- Breakdown voltage $>$ 70V, leakage$\sim$ 10pA
- Before breakdown, $\mathrm{C_{max}(6O)} \sim 770\mathrm{fF}$, $\mathrm{C_{max}(6I)} \sim 460\mathrm{fF}$
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{V}$ for $\mathrm{V} \in (30, 70)\mathrm{V}$

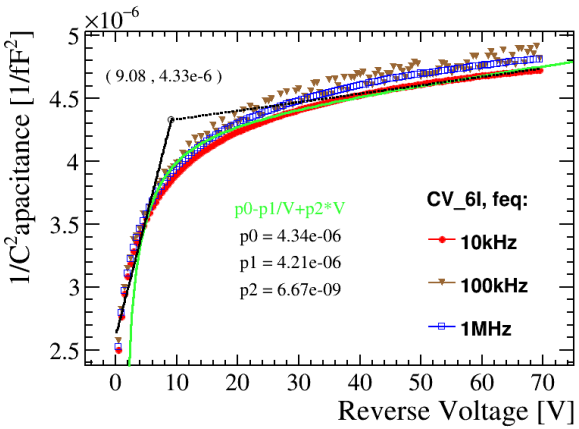






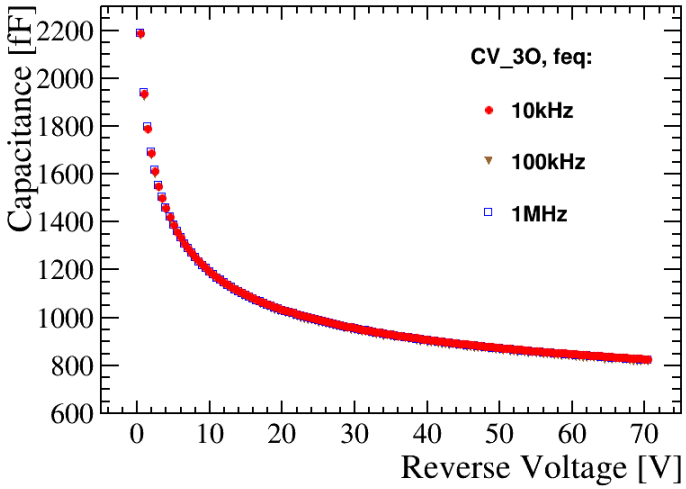


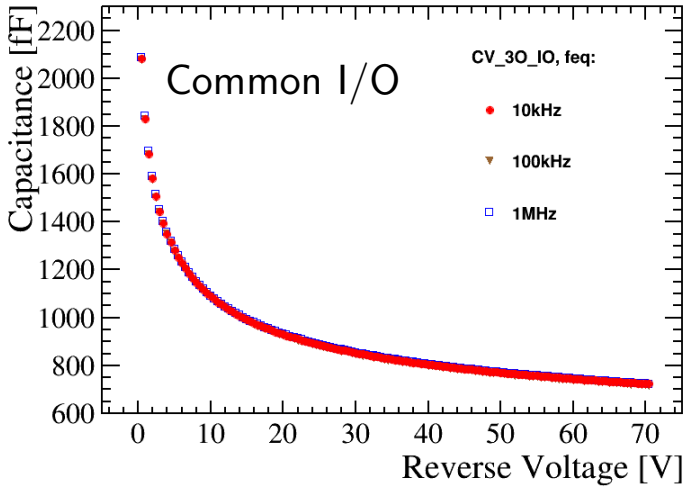


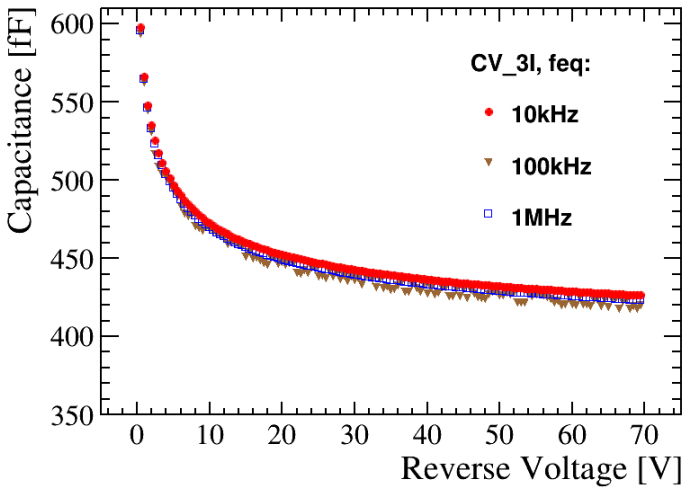


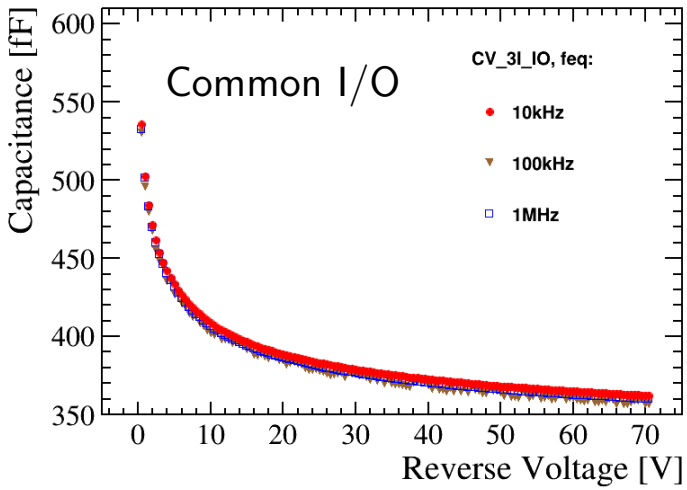
O/I: Sharing effect

- To avoid adjacent bias, retest C(O)&C(I) under I&O common 0V.
- C(O)/C(I) decreased $\sim 100/60$fF (no matter with V_R) after common 0V. Limited sharing effect, up to 15%.



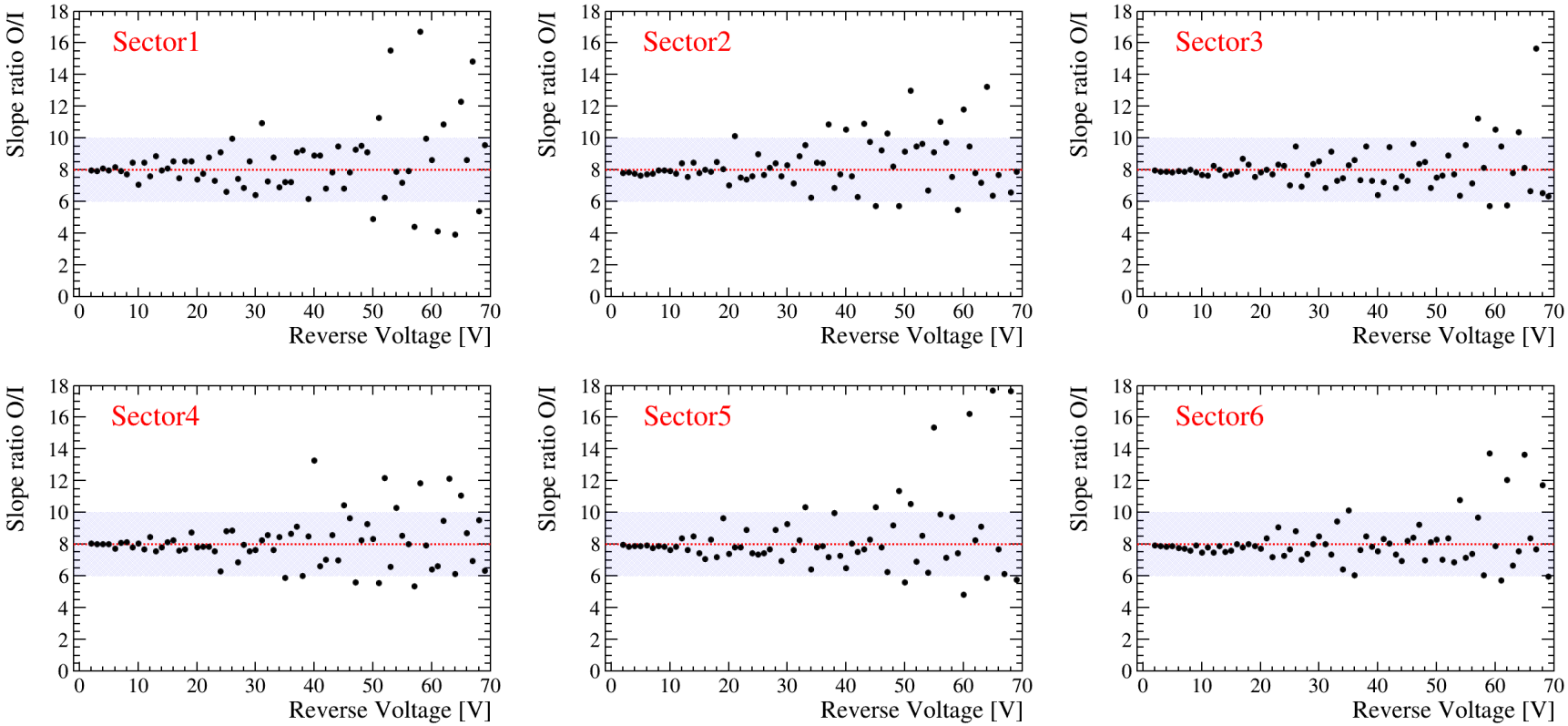






O/I: Slope

- If offset 0, ideal diode in N parallel, for any reverse voltage, $\mathrm{C(N)} = \mathrm{N} \times \mathrm{C(1)}$
- For offset non-0, proportional relationship would be broken for C but still keep true for CV curve slope. Slope doesn't lie :)
  - Comes from pixel gap, DNW or circuit line length?

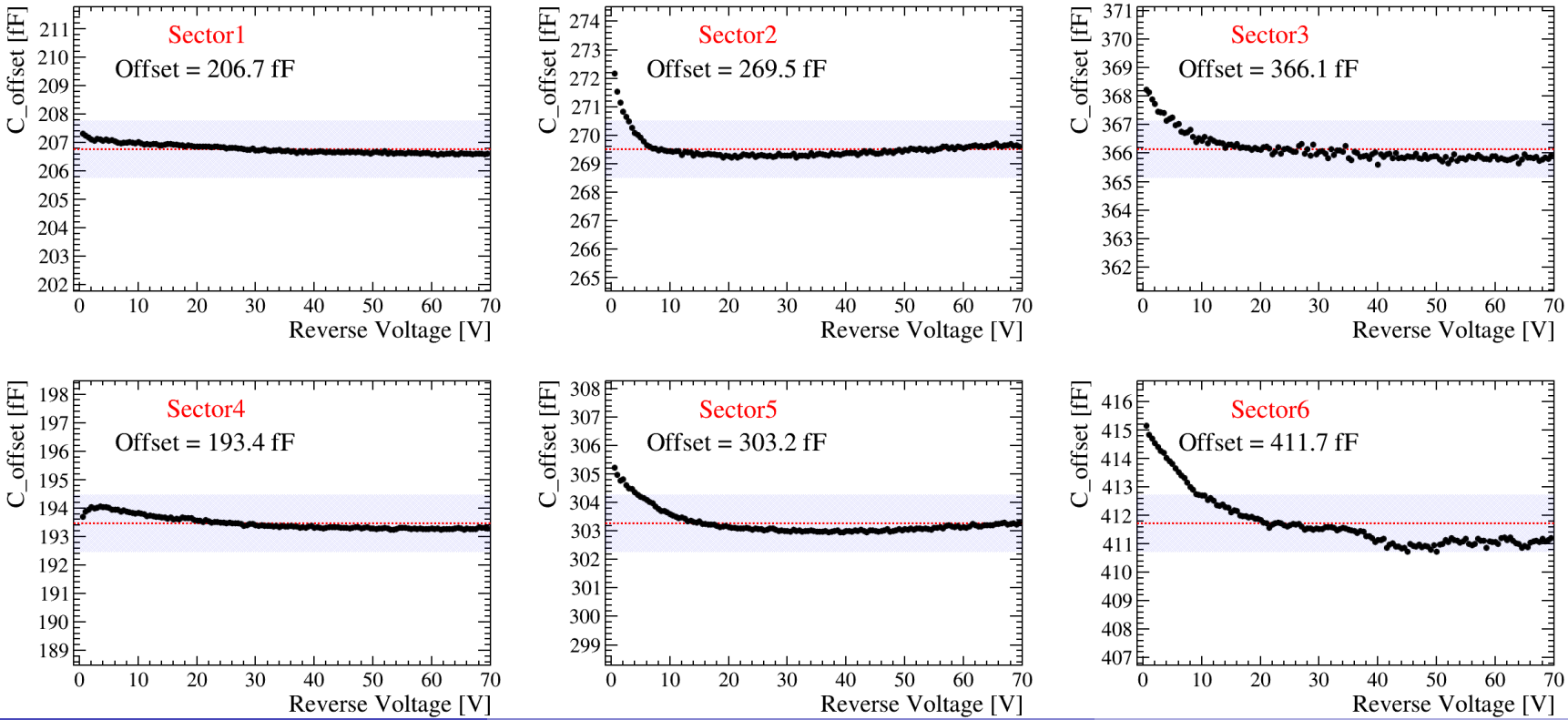


O/I: Offset

- Slope implies offset non-0. Assuming offset universally for O&I at any V_R, we should have:

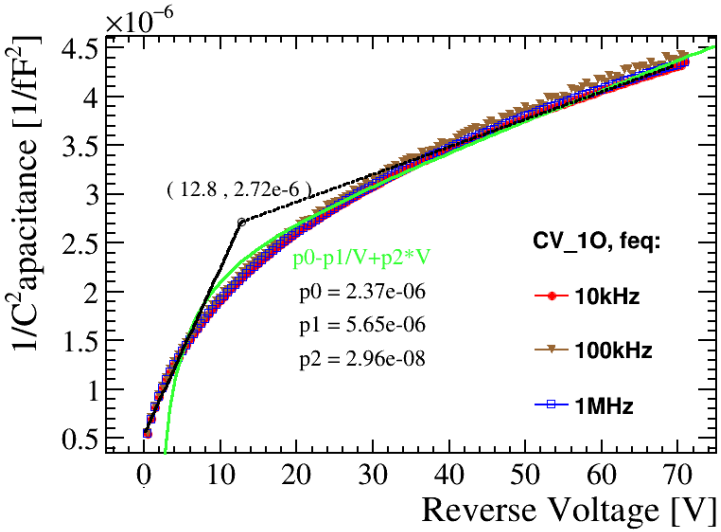
$$\frac{C(O) - \text{Offset}}{C(I) - \text{Offset}} = 8 \Longrightarrow \text{Offset} = \frac{8 \cdot C(I) - C(O)}{7}$$

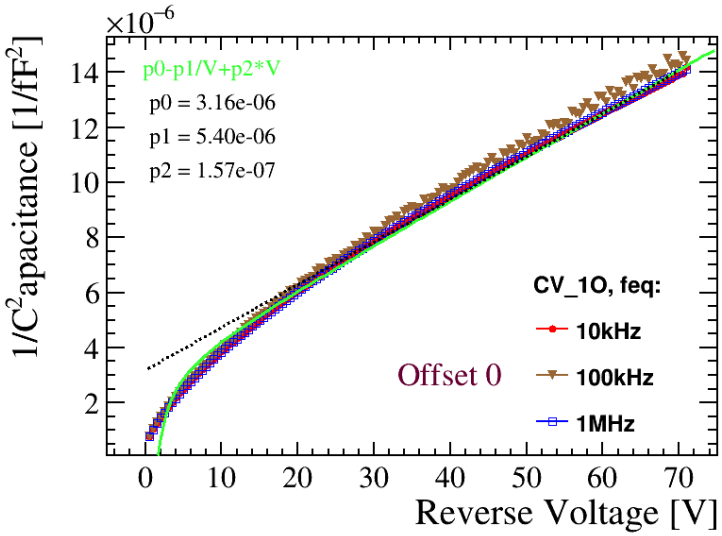
- Same level in row ($1 \leftrightarrow 4, 2 \leftrightarrow 5, 3 \leftrightarrow 6$), increasing in colum (pixel gap $20/15/10\mu m$, correlated to the offset value!).

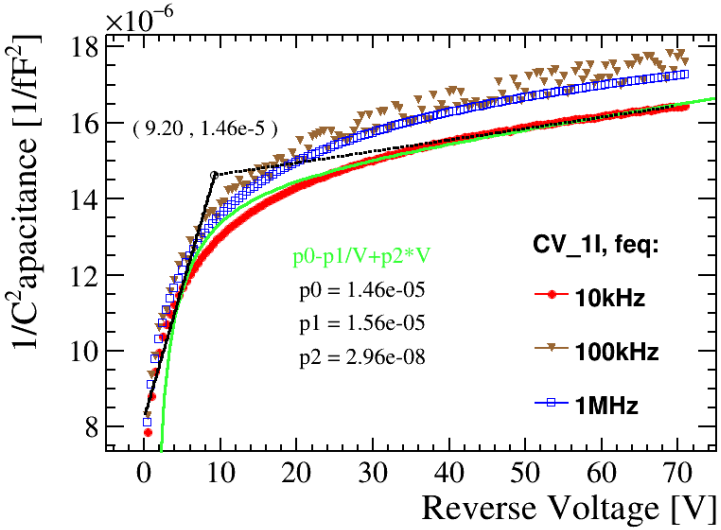


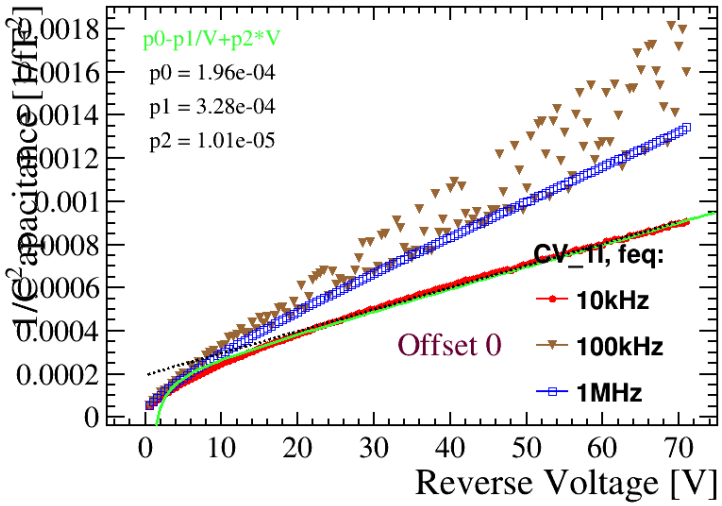
Offset 0: Sector1

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



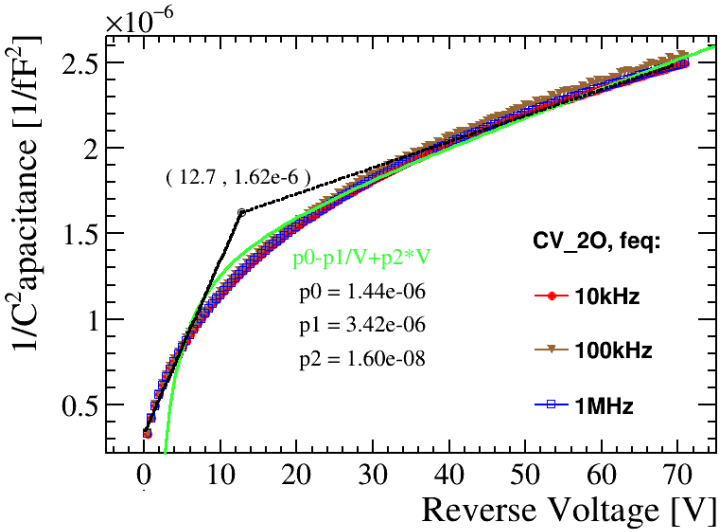


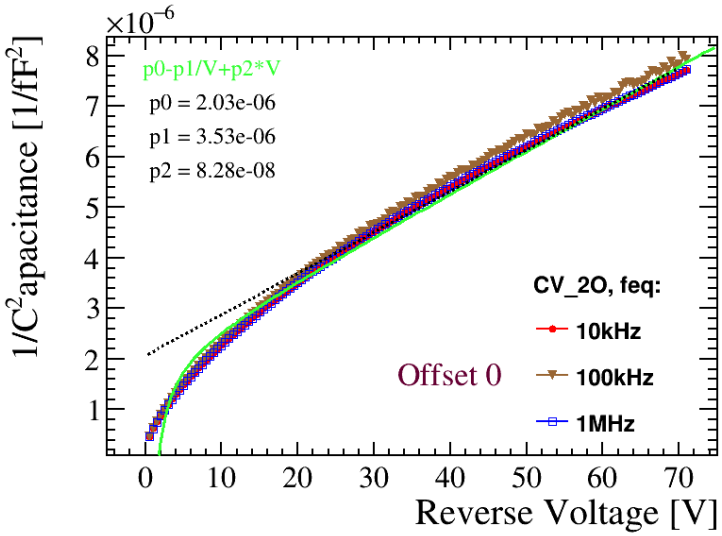


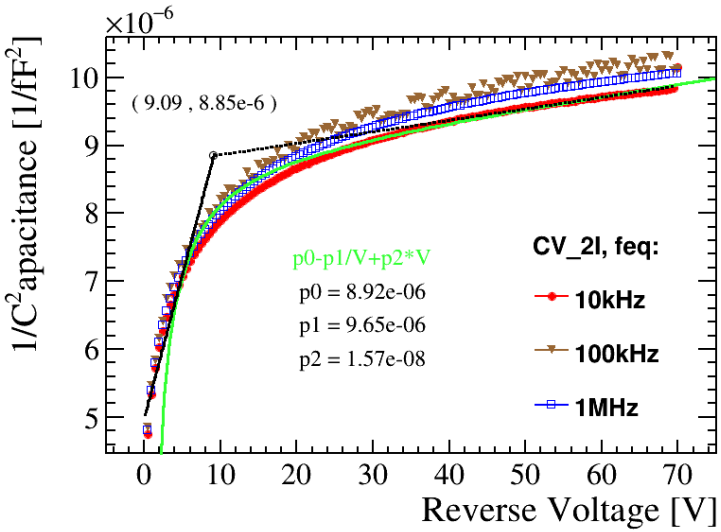


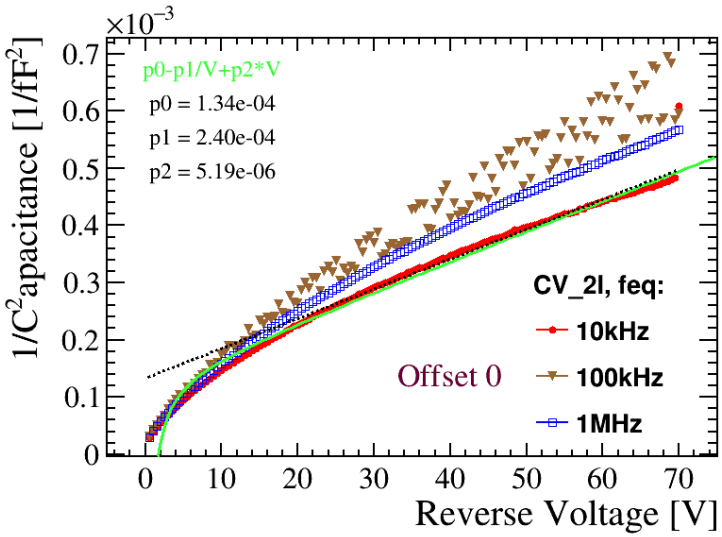
Offset 0: Sector2

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



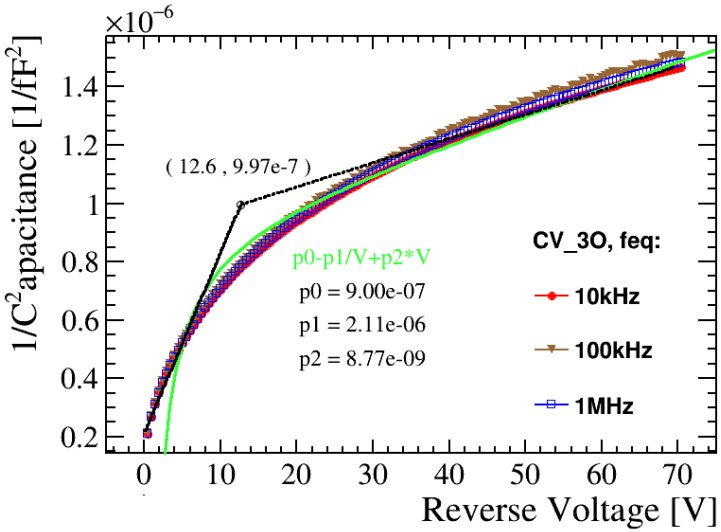


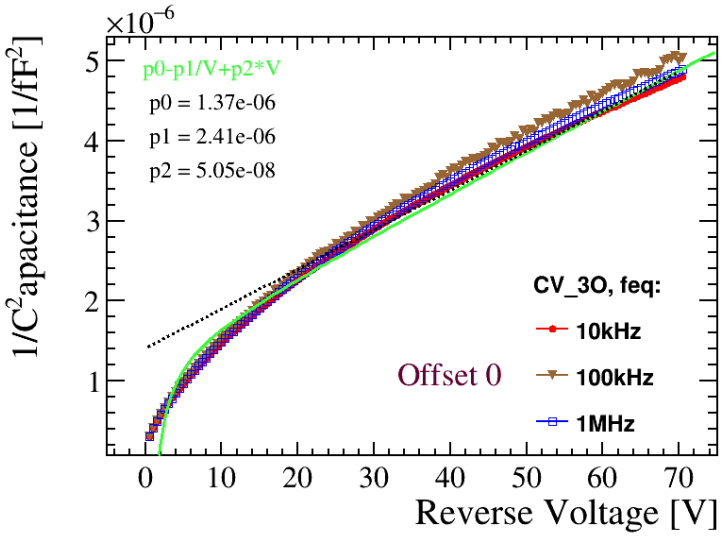


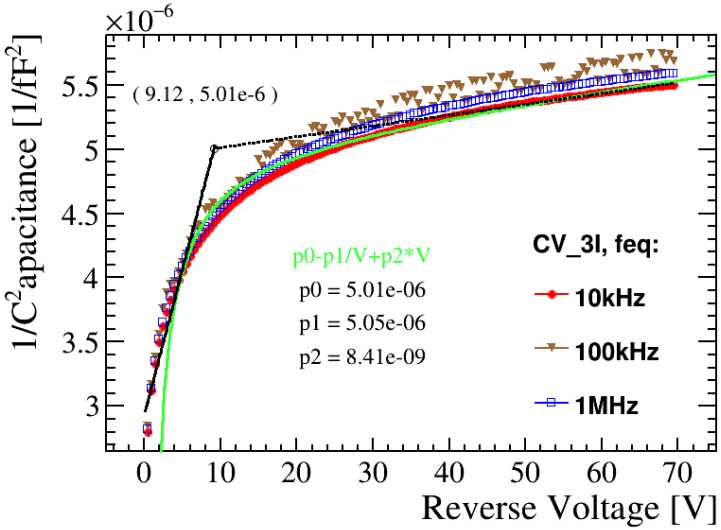


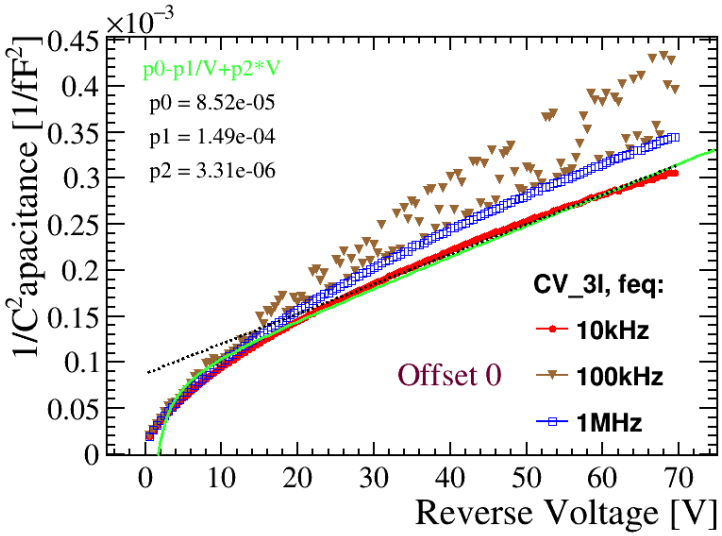
Offset 0: Sector3

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



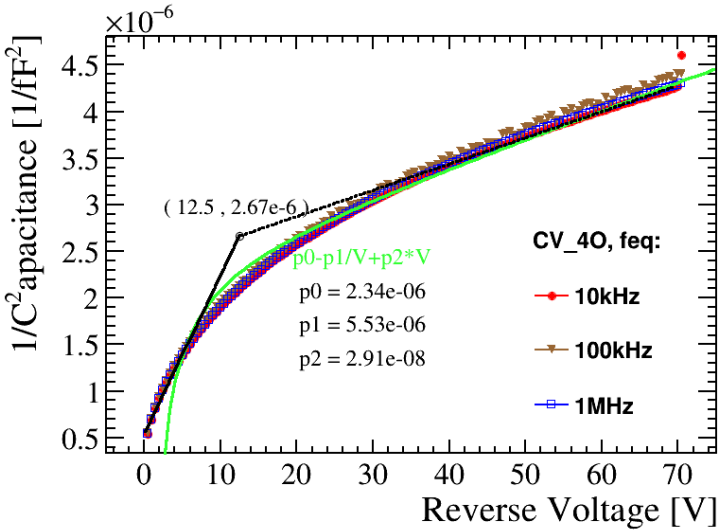


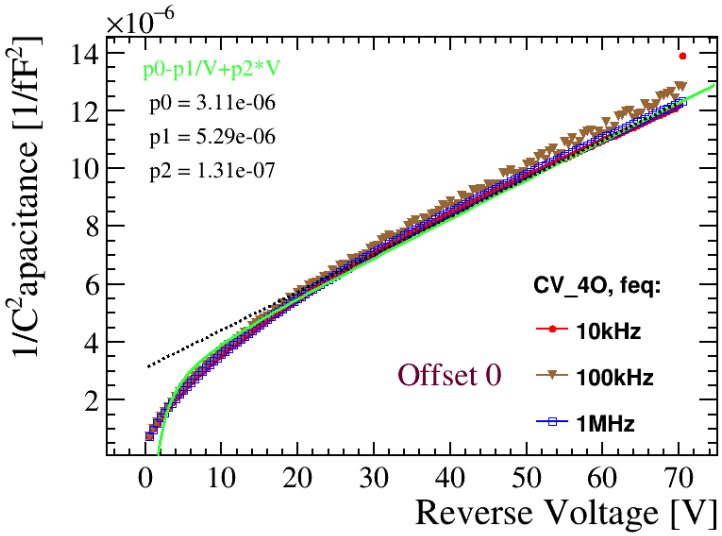


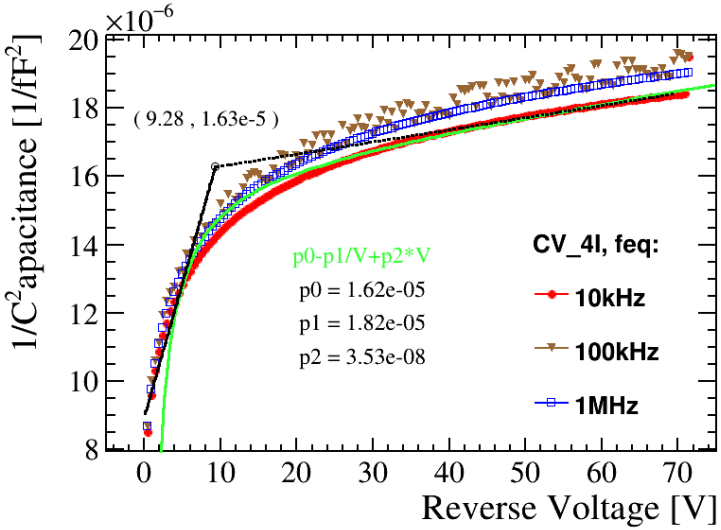


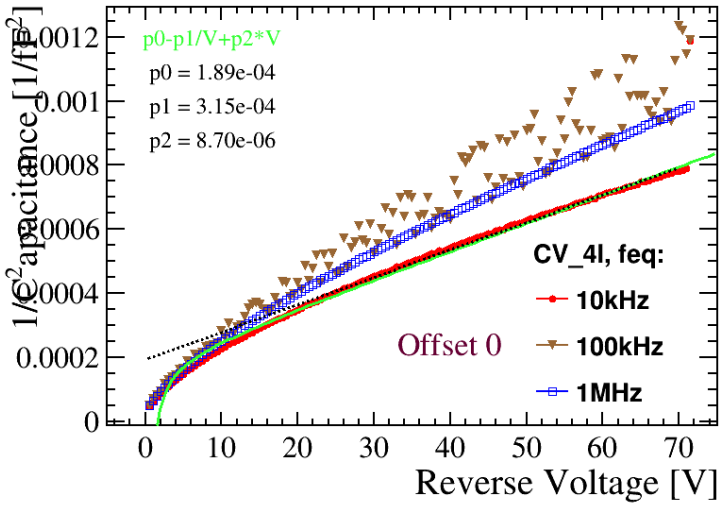
Offset 0: Sector4

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



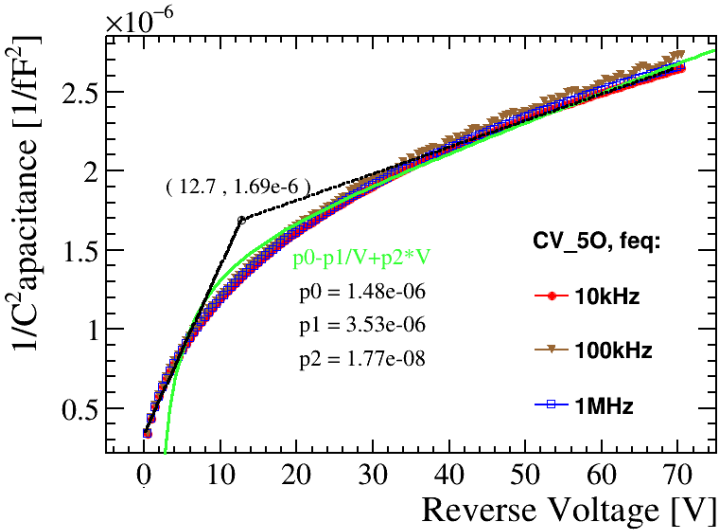


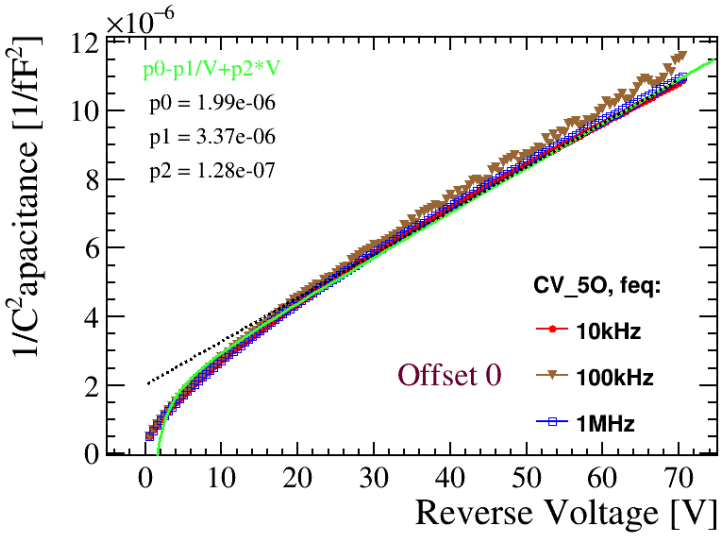


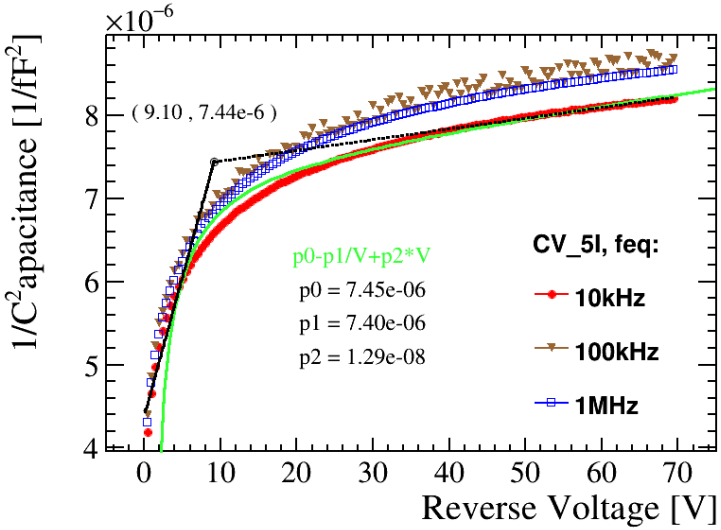


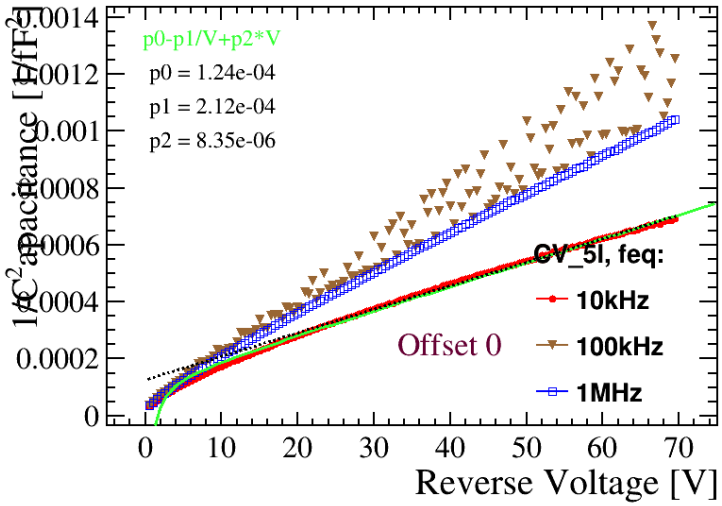
Offset 0: Sector5

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



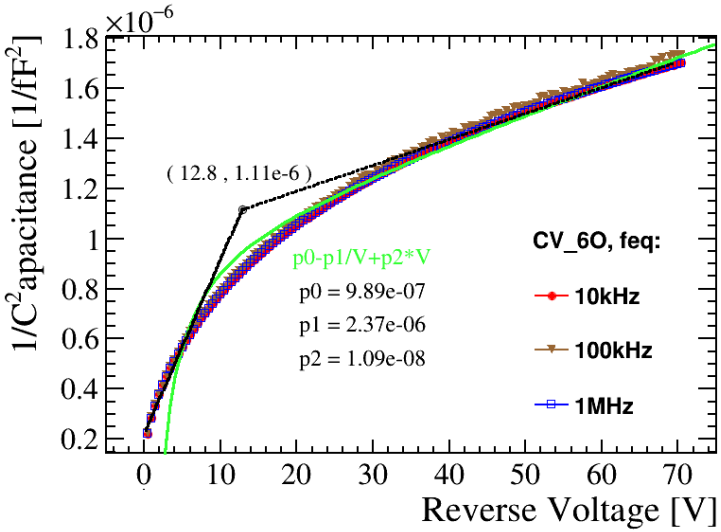


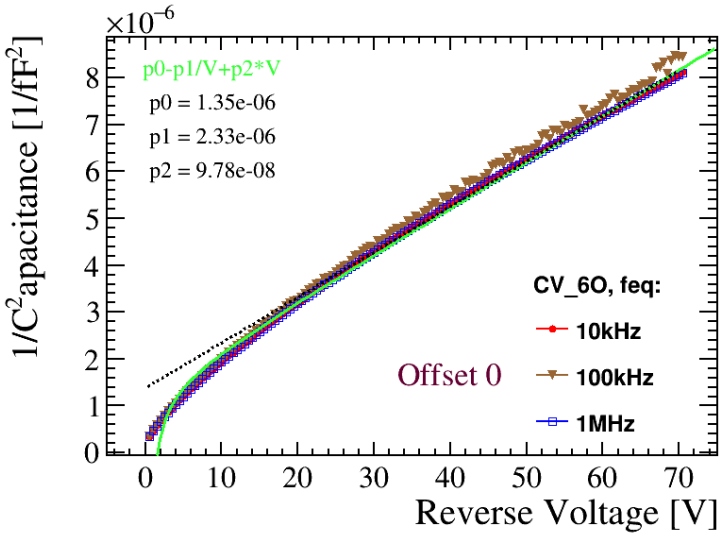


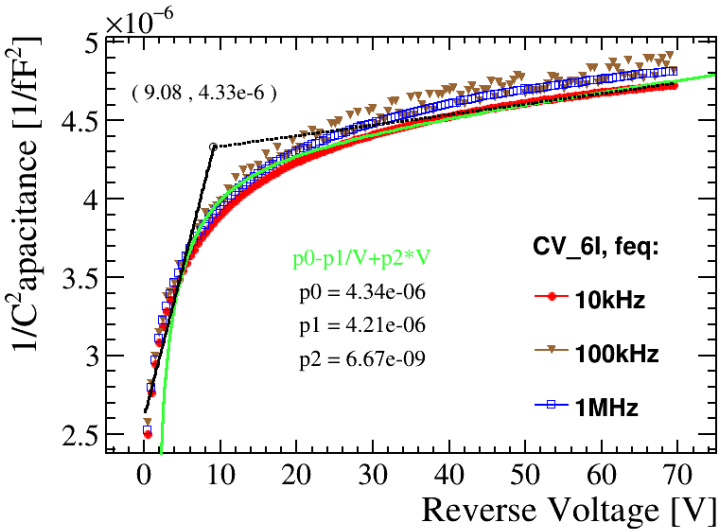


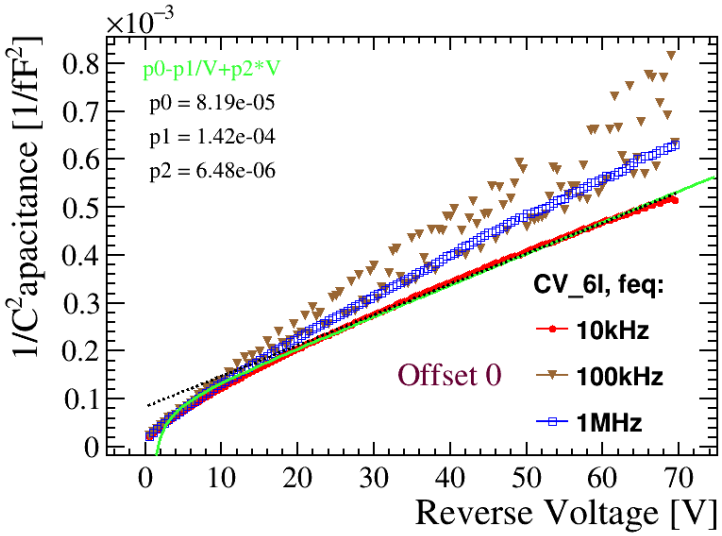
Offset 0: Sector6

- Improved but lower band ($1 \sim 15\mathrm{V}$) still nonlinear.



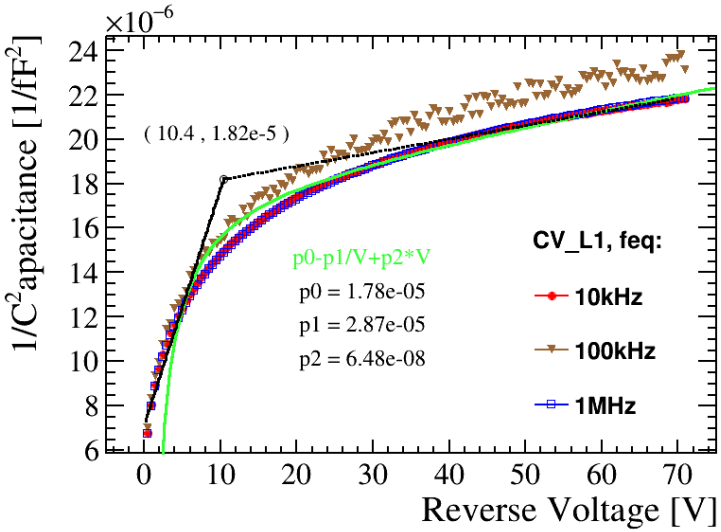


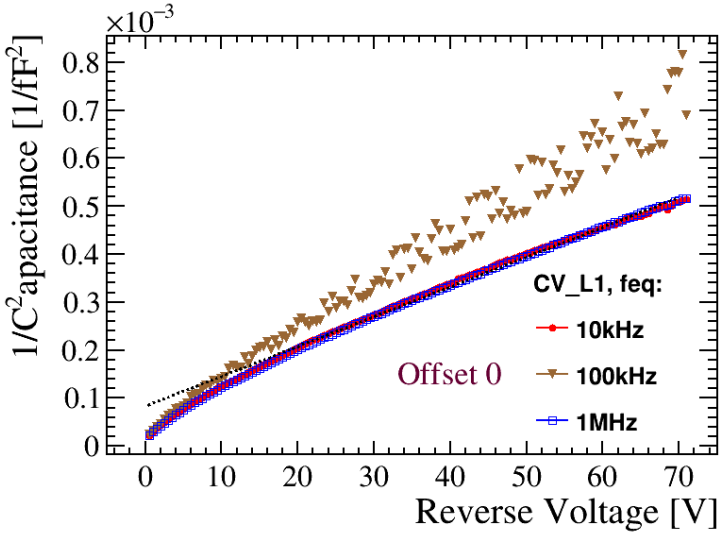


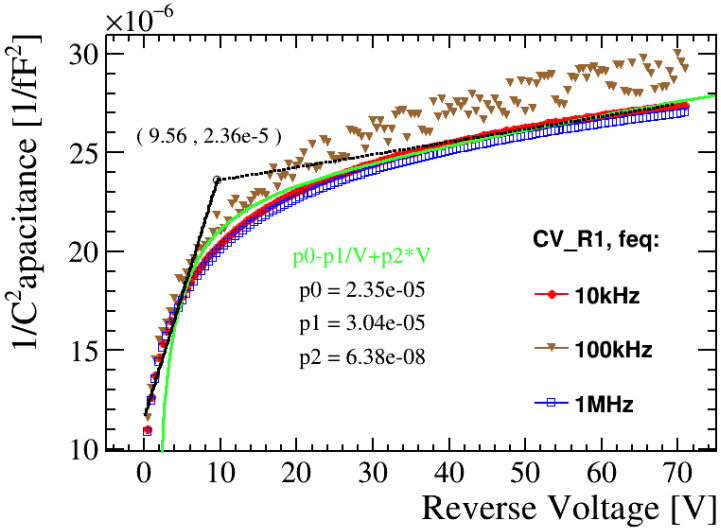


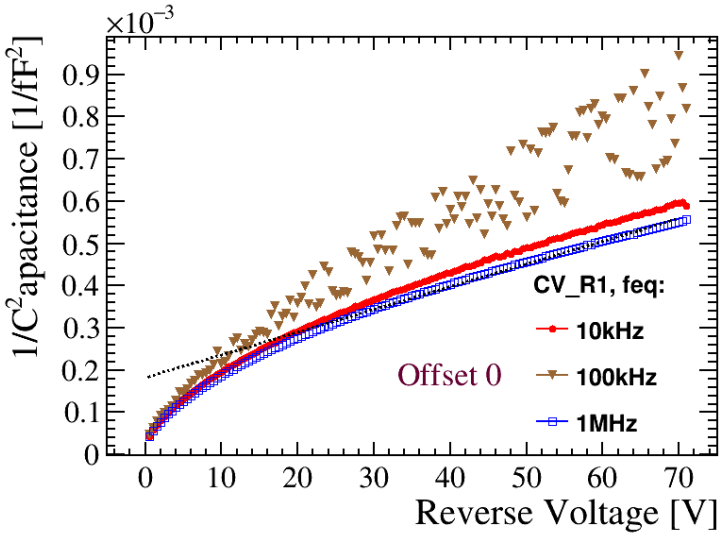
Offset 0: L1&R1

- Artificial offset 170fF(150fF) for L(R) .



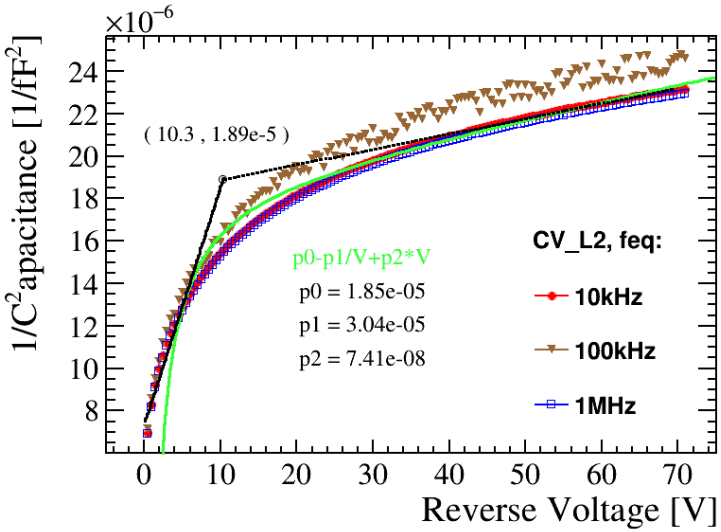


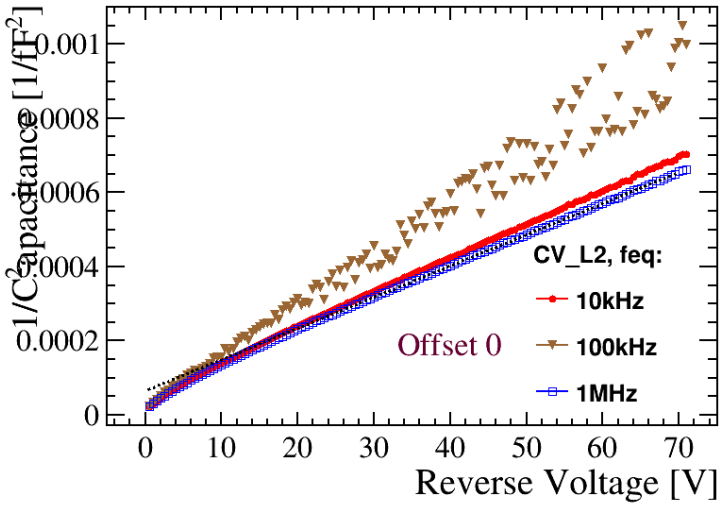


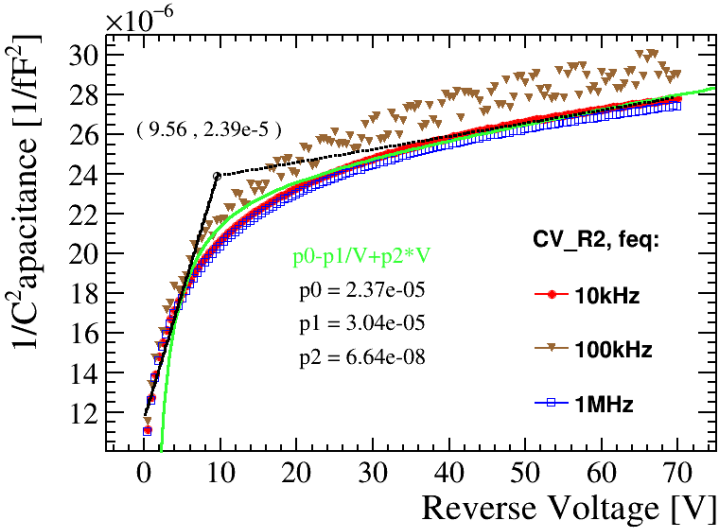


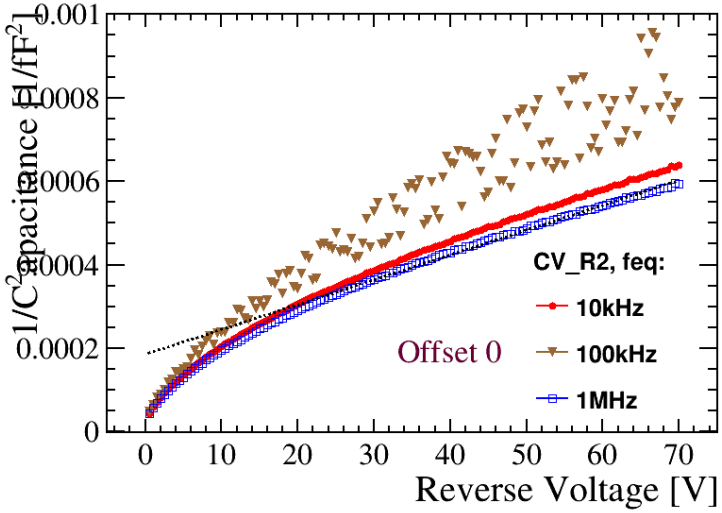
Offset 0: L2&R2

- Artificial offset 170fF(150fF) for L(R) .



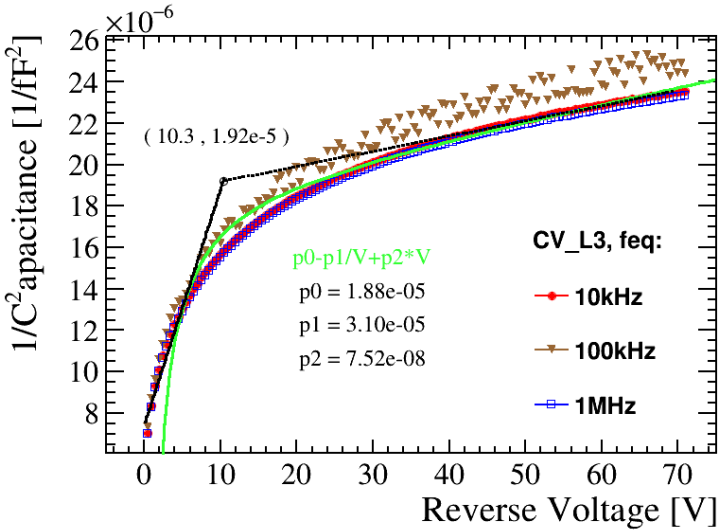


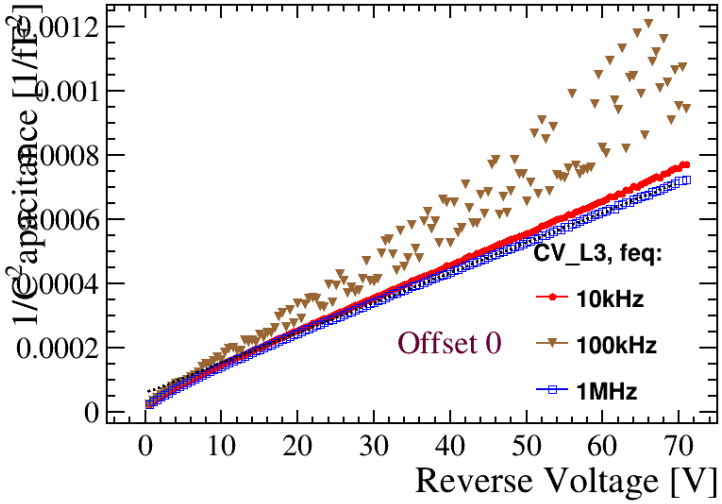


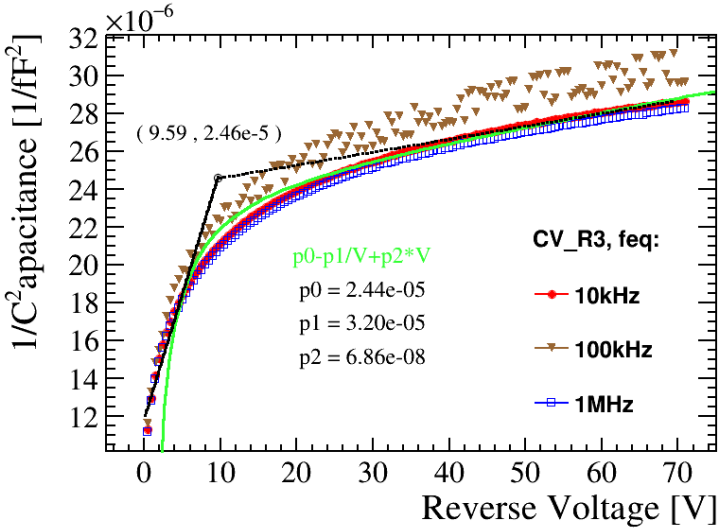


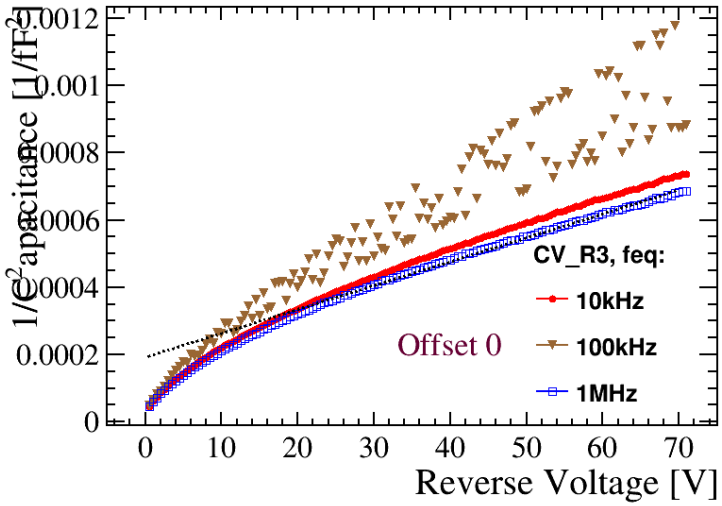
Offset 0: L3&R3

- Artificial offset $170\mathrm{fF}(150\mathrm{fF})$ for L(R) .



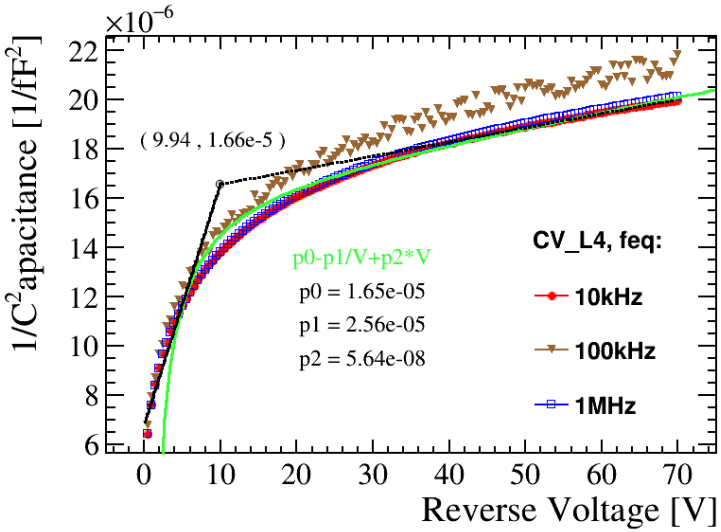


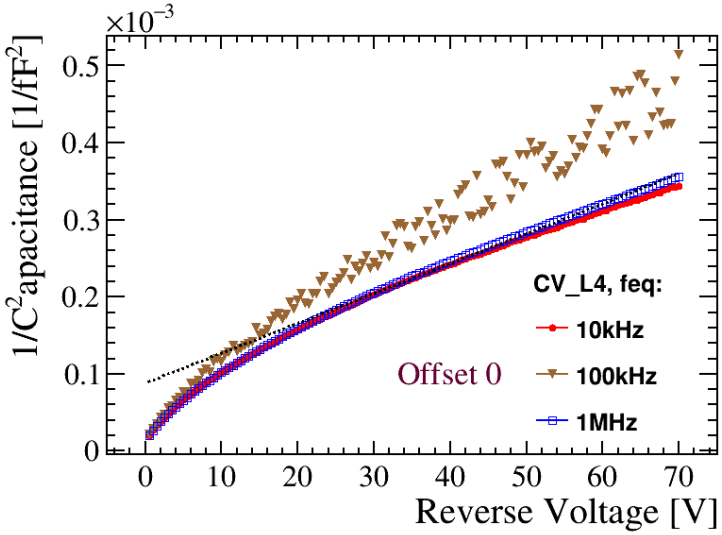


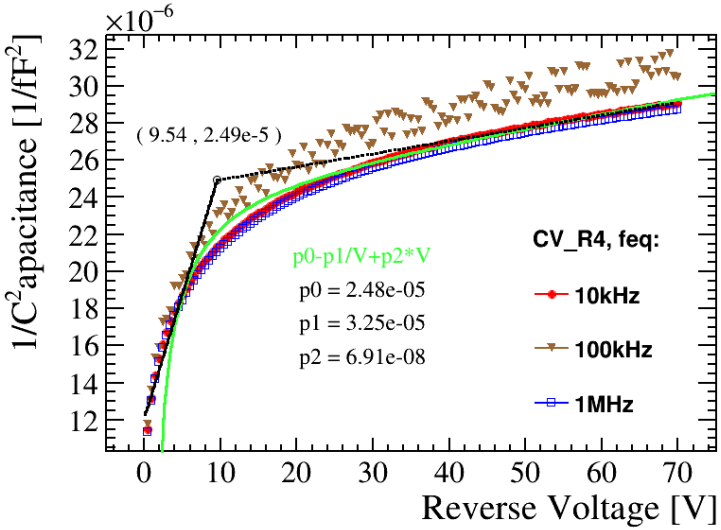


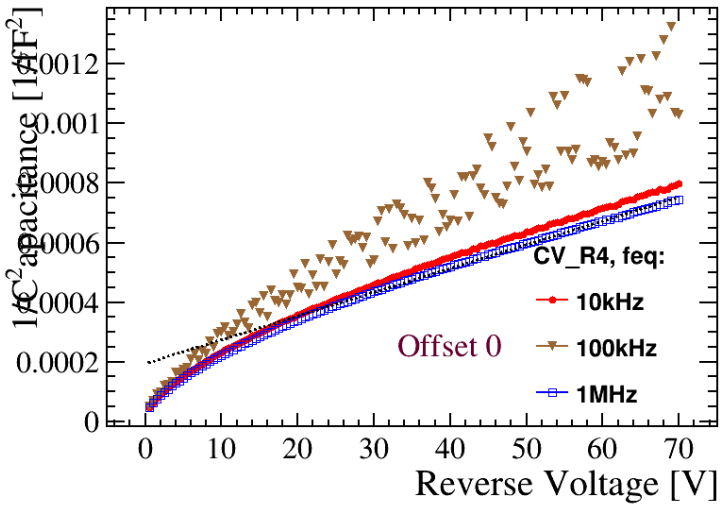
Offset 0: L4&R4

- Artificial offset 170fF(150fF) for L(R) .



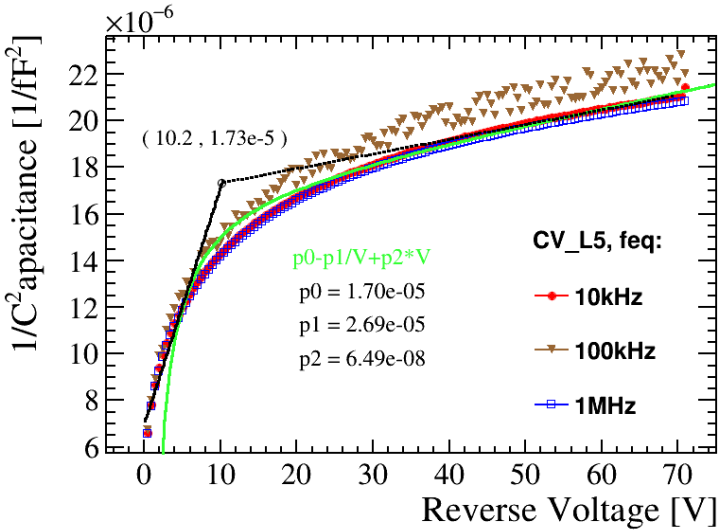


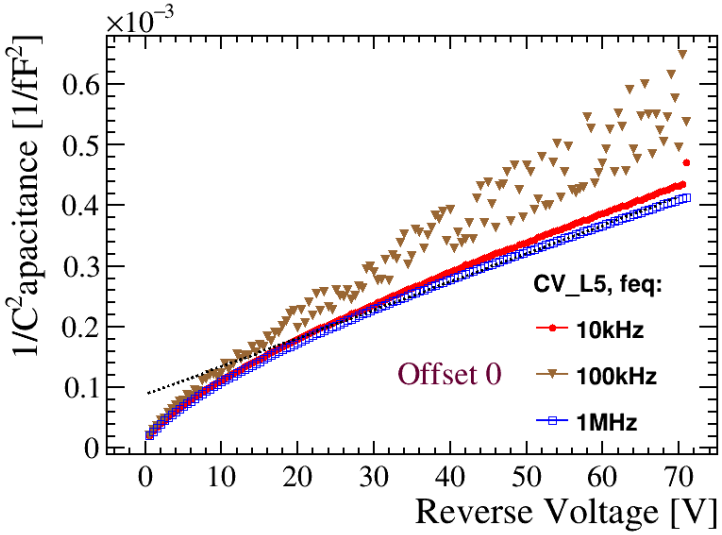


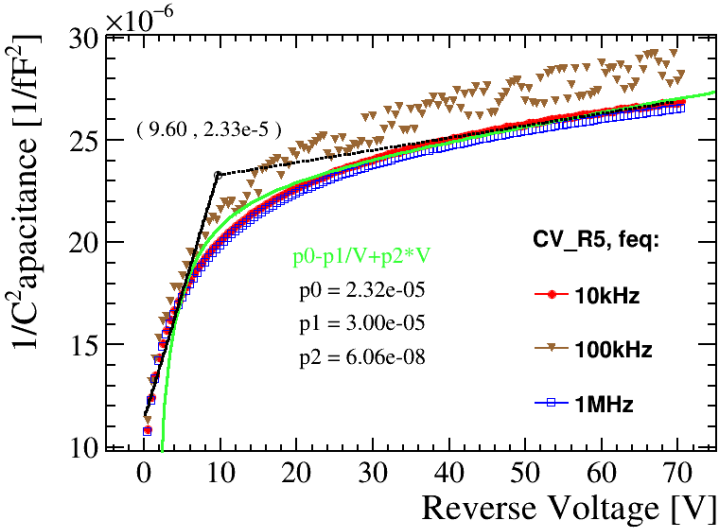


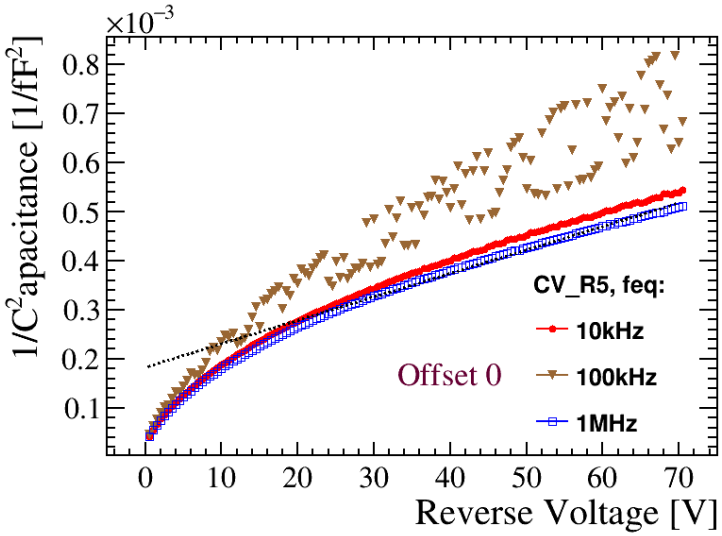
Offset 0: L5&R5

- Artificial offset 170fF(150fF) for L(R) .



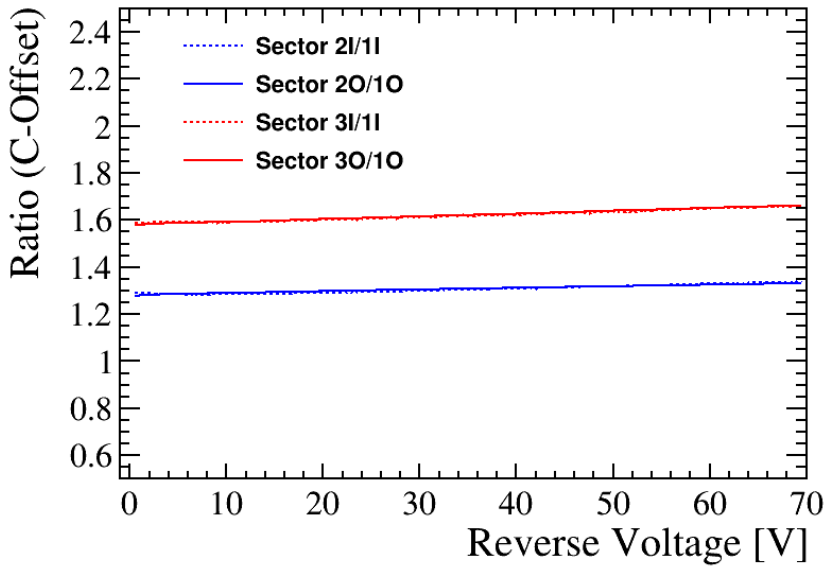


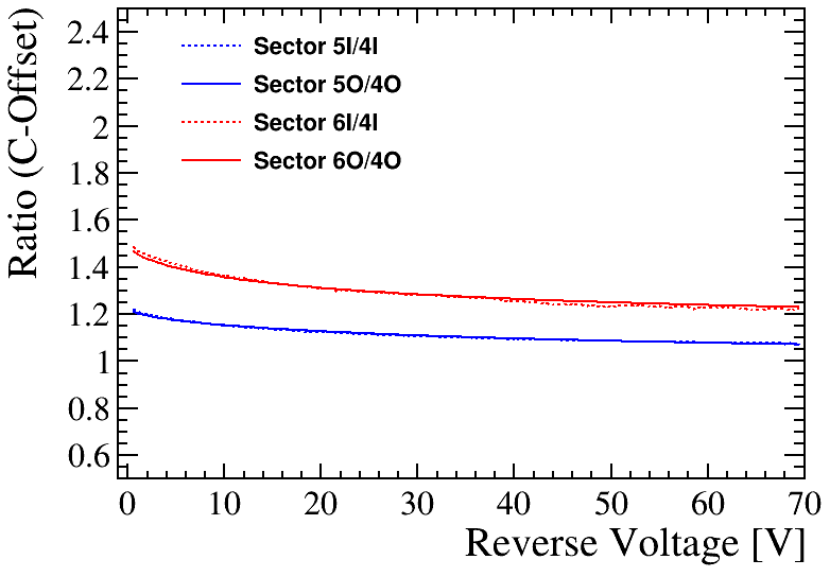




After offset 0, C vs.s Area

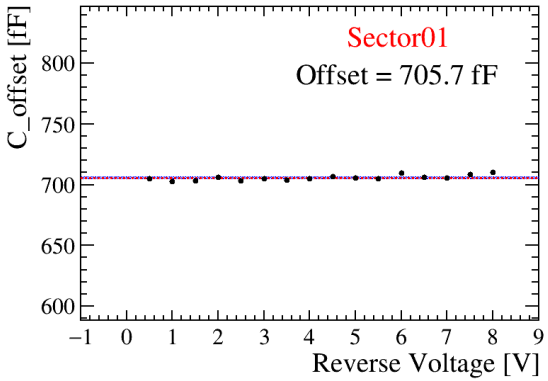
- Pixel size ratio for S2(5)/S1(4)=1.35, S3(6)/S1(4)=1.75.
- Ideally, after offset 0, $\mathrm{C} \propto \mathrm{Area}$. Roughly OK for Sector 1/2/3.
- Seems P stop works.

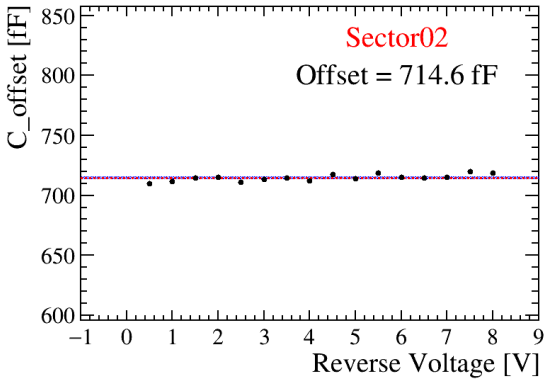


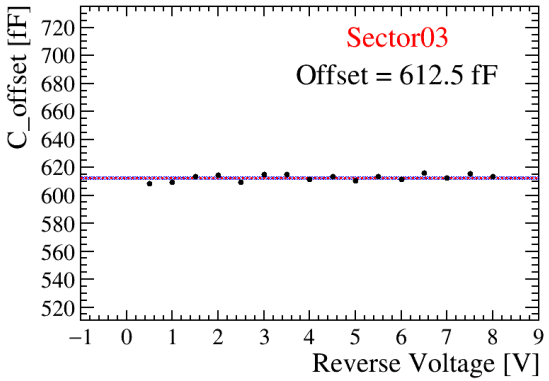


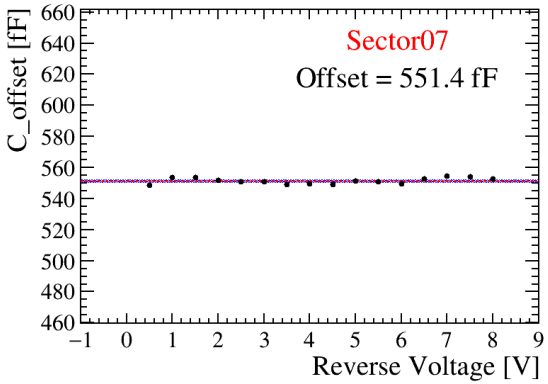
Offset not correlated with route wire

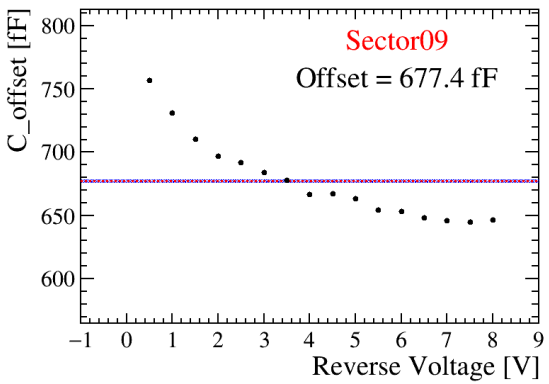
- For COFFEE1, same route wires for Sector 01/02/03/07/09.
- Offset values should not only comes from route wire.

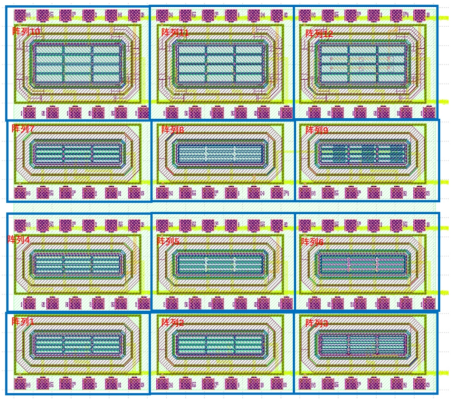












Conclusion

General:

- Promising COFFEE2: Breakdown voltage $>$ 70V, leakage$\sim$ 10pA, and seems all pixels not fully depleted.
- For single pixel in L&R, $\mathrm{C} \sim 200\mathrm{fF}$, and $\mathrm{C(L)} \sim \mathrm{C(R)} \times 110\%$.
- For multi-pixels, $\mathrm{C(O)} \sim \mathrm{C(I)} \times 200\%$, except for Sector5&6.

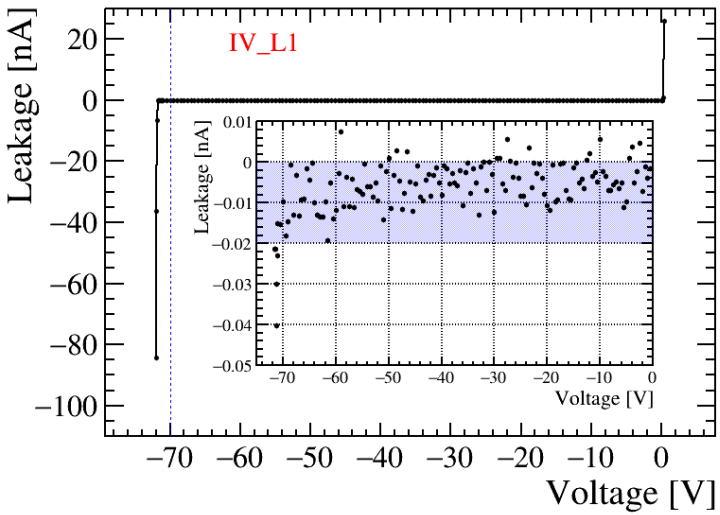
Additional:

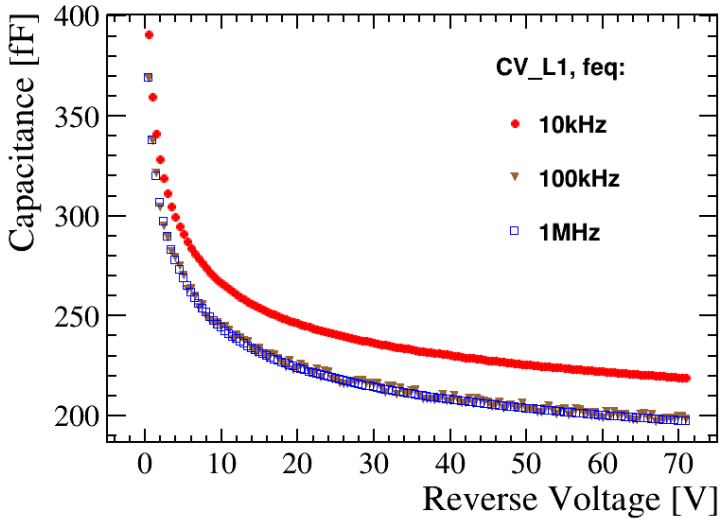
- Roughly, $\frac{1}{\mathrm{C}^2} \propto \mathrm{p_0} - \mathrm{p_1}/\mathrm{V_R} + \mathrm{p_2} \cdot \mathrm{V_R}$, probably sizeable sidewall effect.
- C positively correlated with area. Sharing effect is limited.
- The slope of the CV curve imply parallel's proportional relationship.

Next:

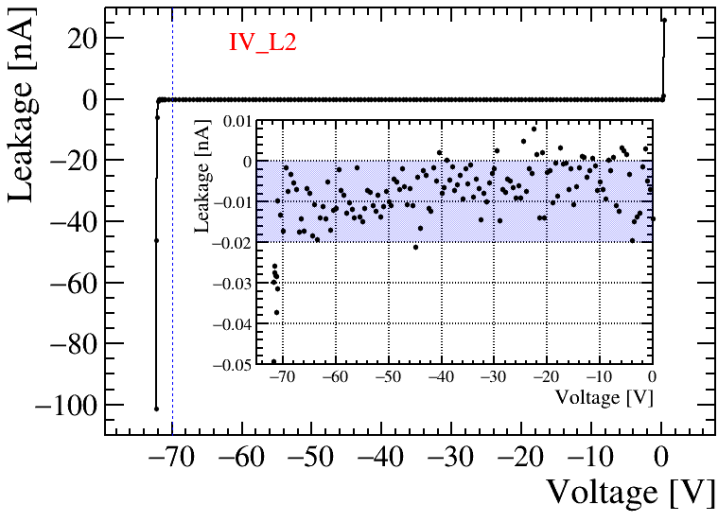
- Test more chips, also would retest COFFEE1 in case of previous open correction may wrong.
- Try test COFFEE2 with laser since obvious light current seen.
  - Special test board design ongoing.

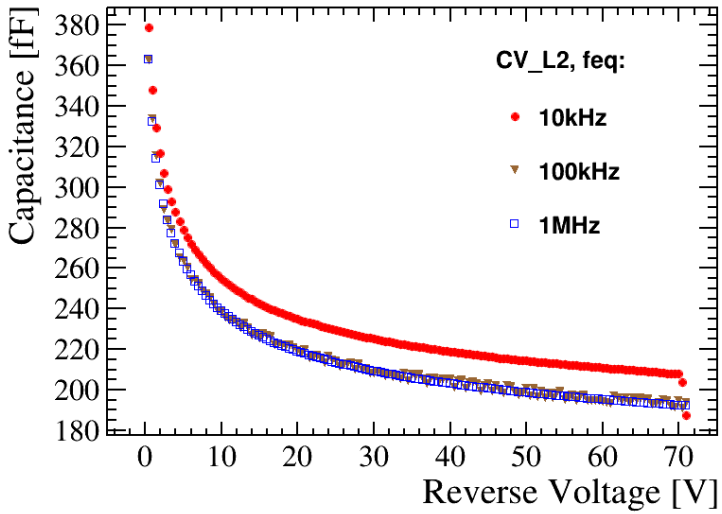
Backup: IVCV - COFFEE2 chip 2, L1



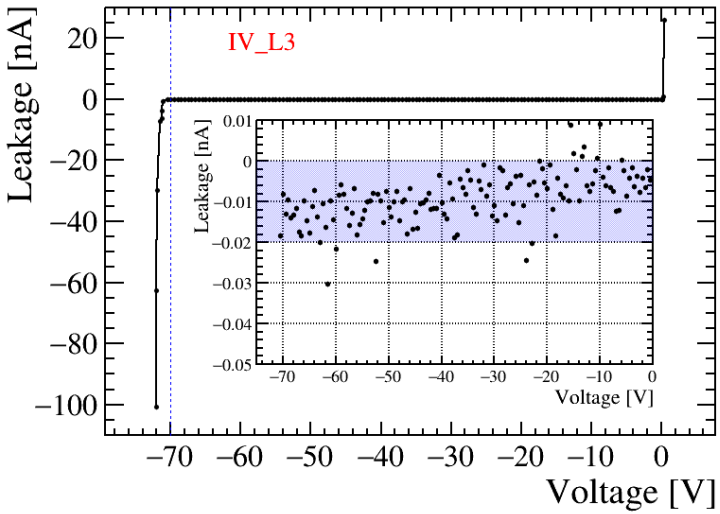


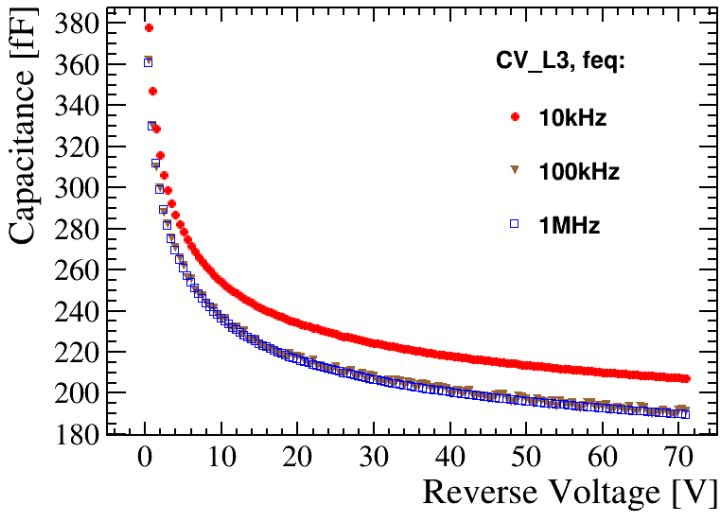
Backup: IVCV - COFFEE2 chip 2, L2



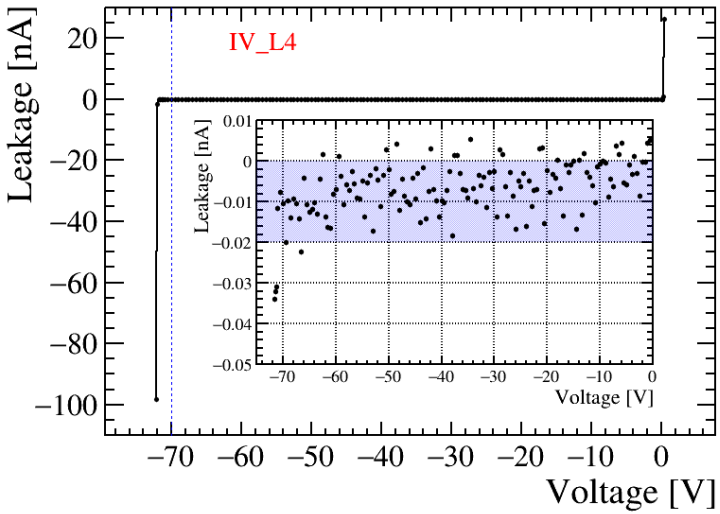


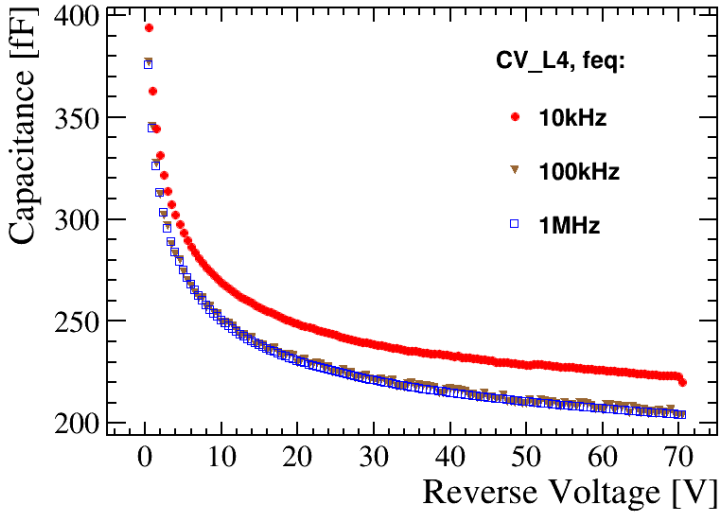
Backup: IVCV - COFFEE2 chip 2, L3



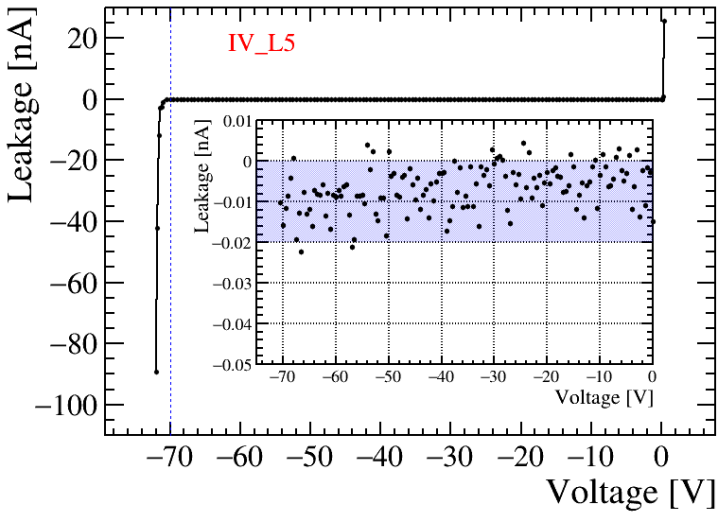


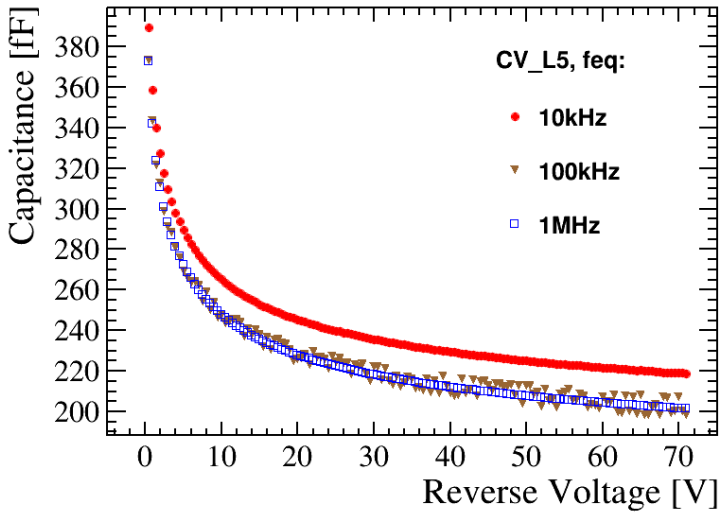
Backup: IVCV - COFFEE2 chip 2, L4



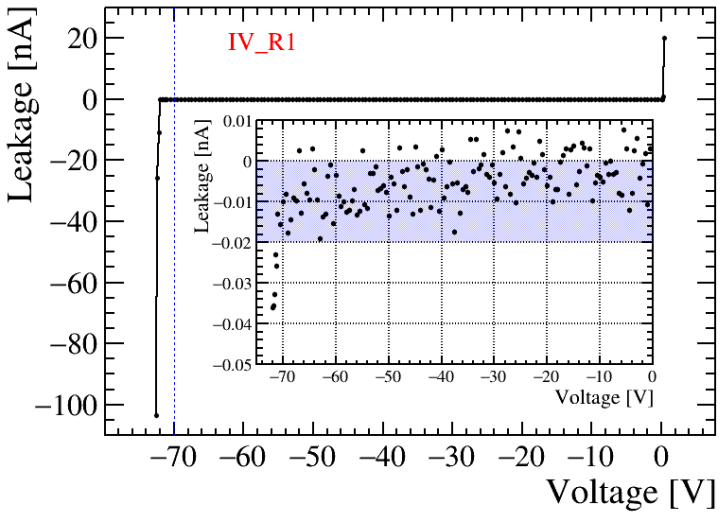


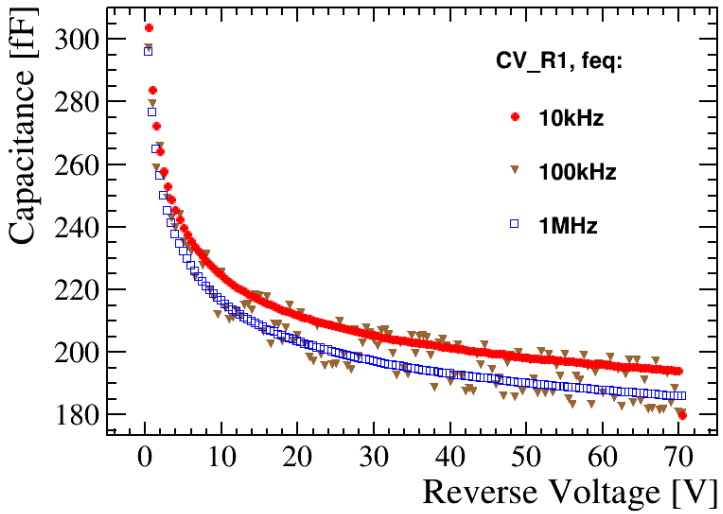
Backup: IVCV - COFFEE2 chip 2, L5



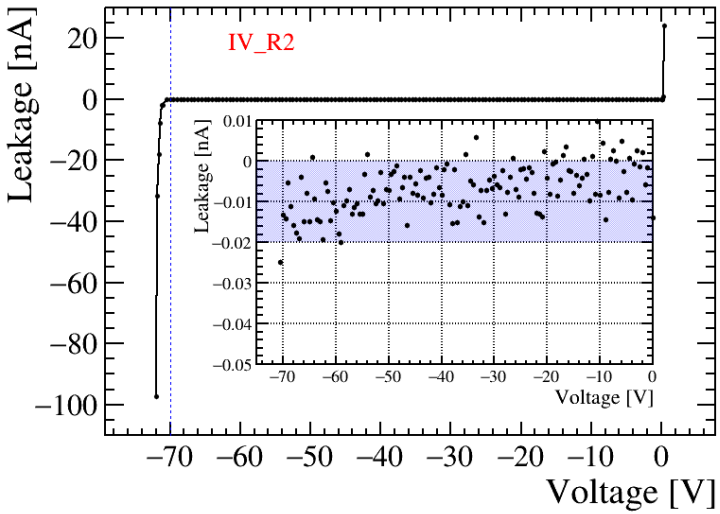


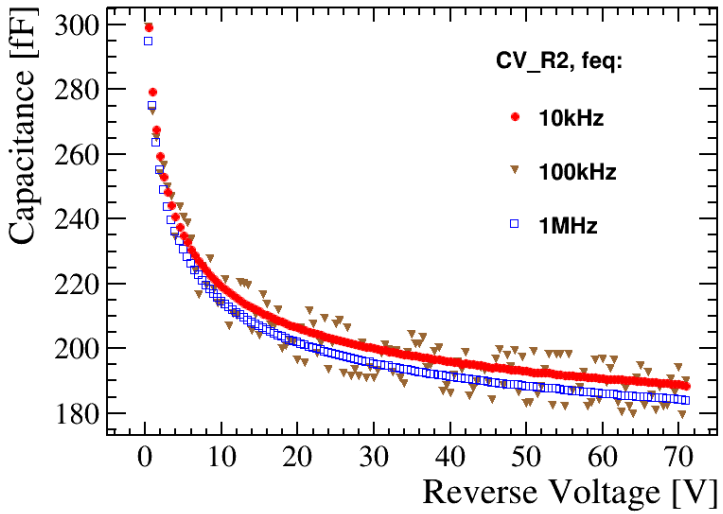
Backup: IVCV - COFFEE2 chip 2, R1



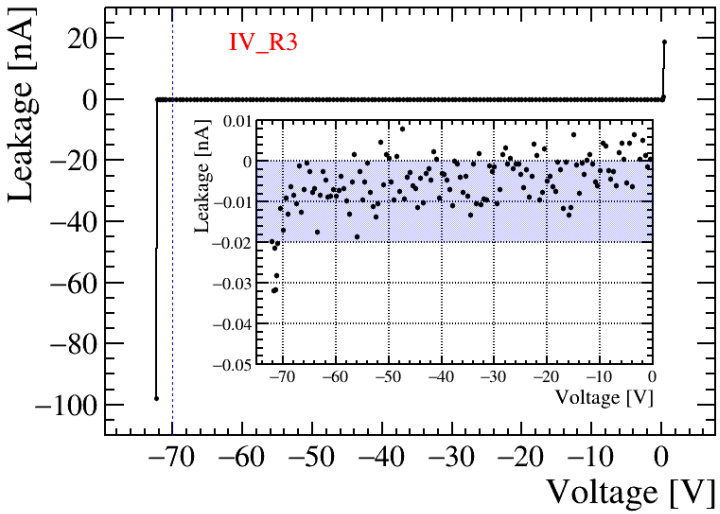


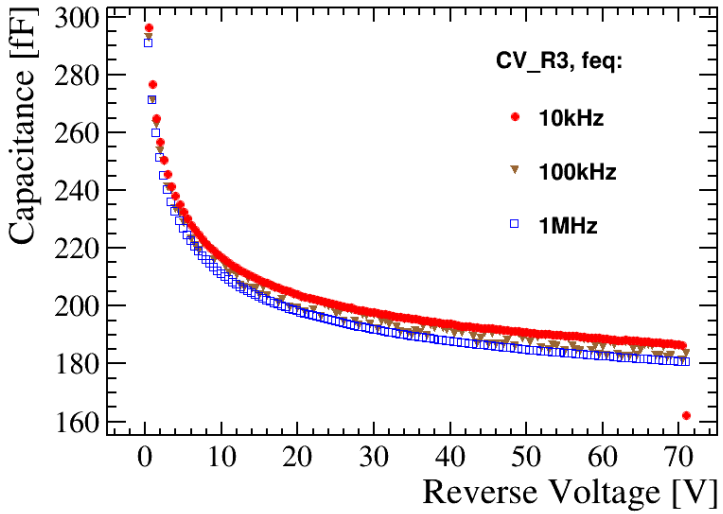
Backup: IVCV - COFFEE2 chip 2, R2



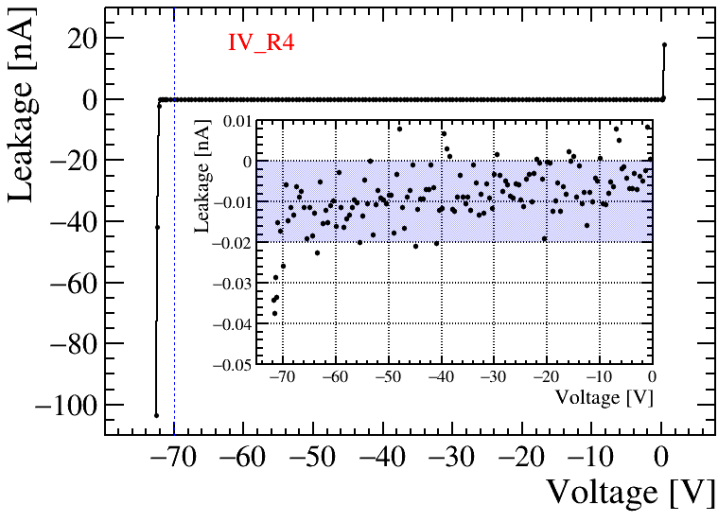


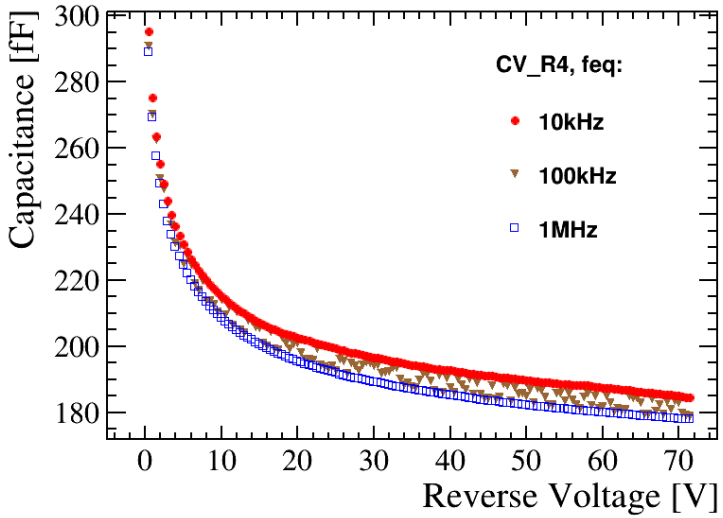
Backup: IVCV - COFFEE2 chip 2, R3



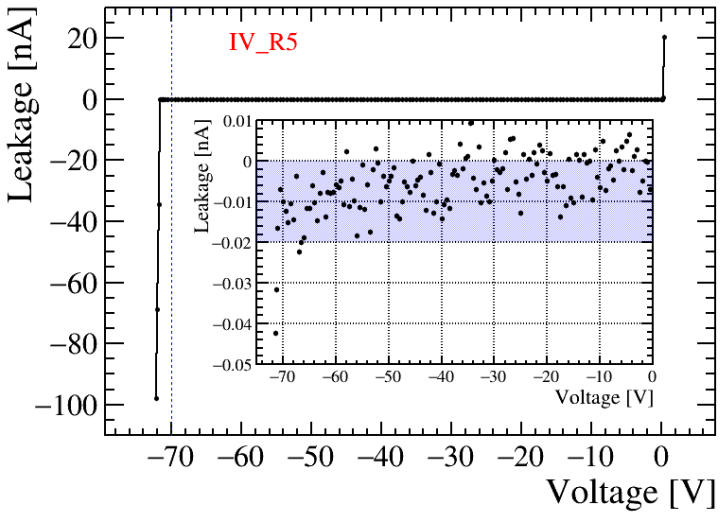


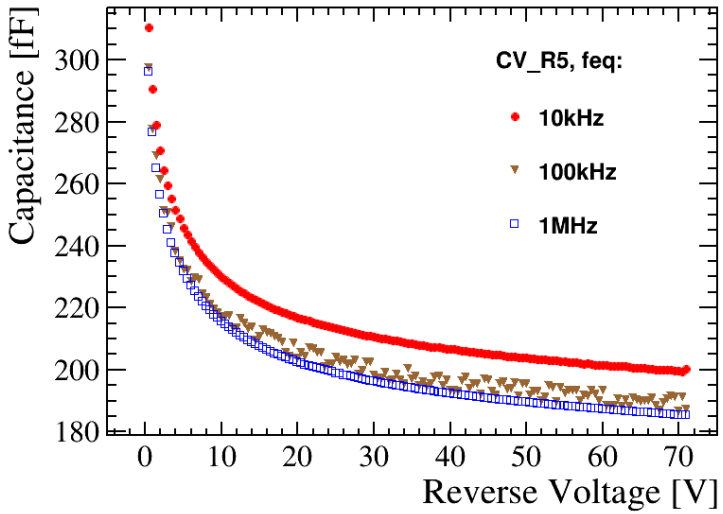
Backup: IVCV - COFFEE2 chip 2, R4



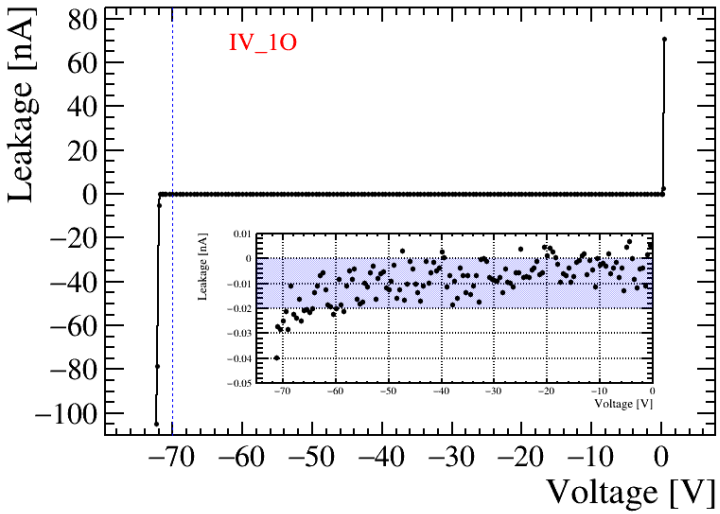


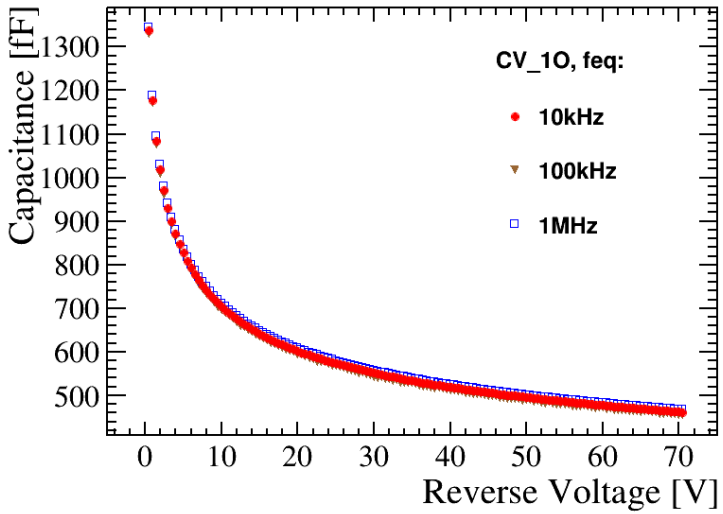
Backup: IVCV - COFFEE2 chip 2, R5



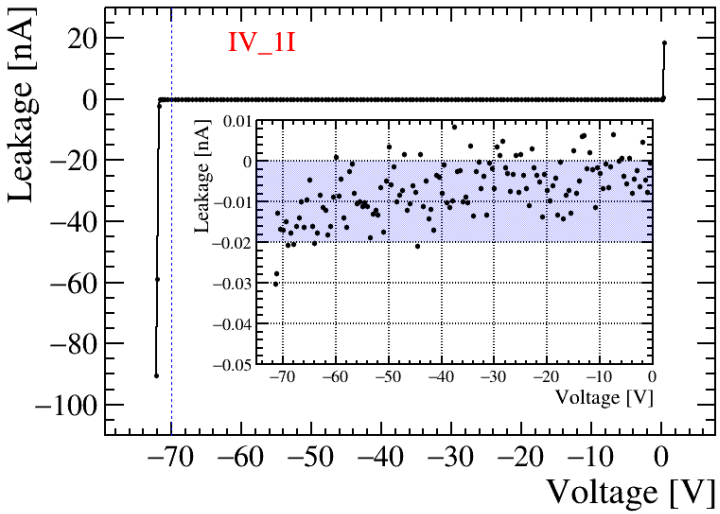


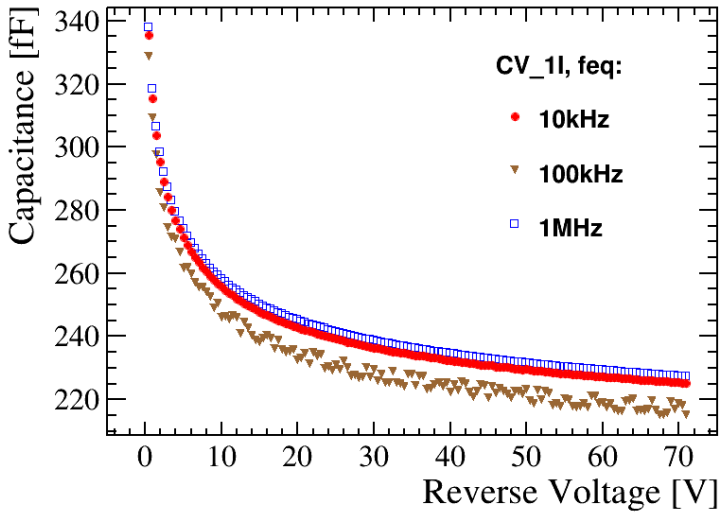
Backup: IVCV - COFFEE2 chip 2, 1O



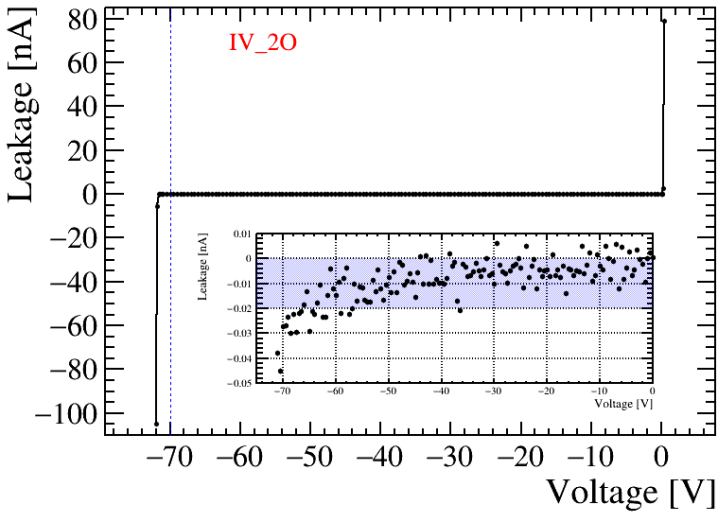


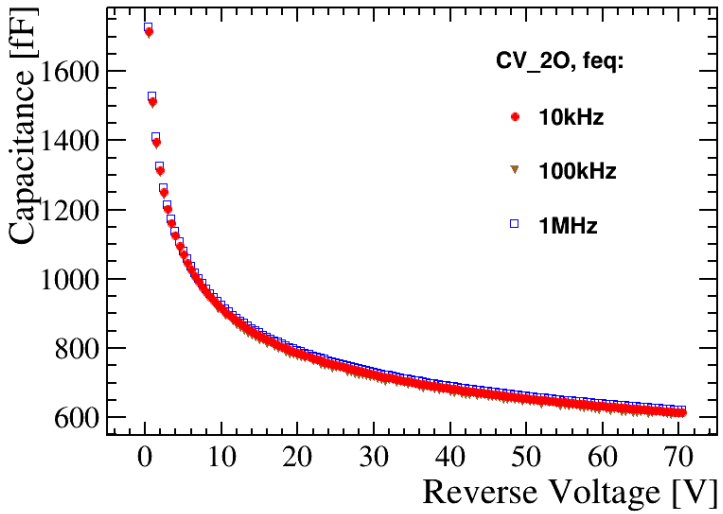
Backup: IVCV - COFFEE2 chip 2, 1I



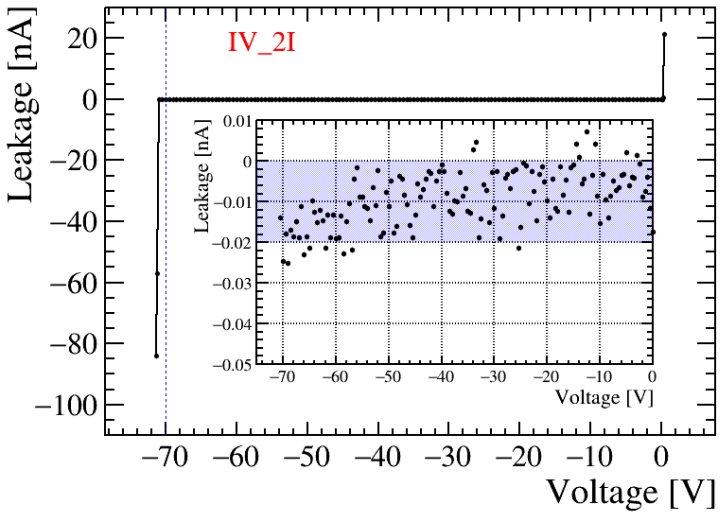


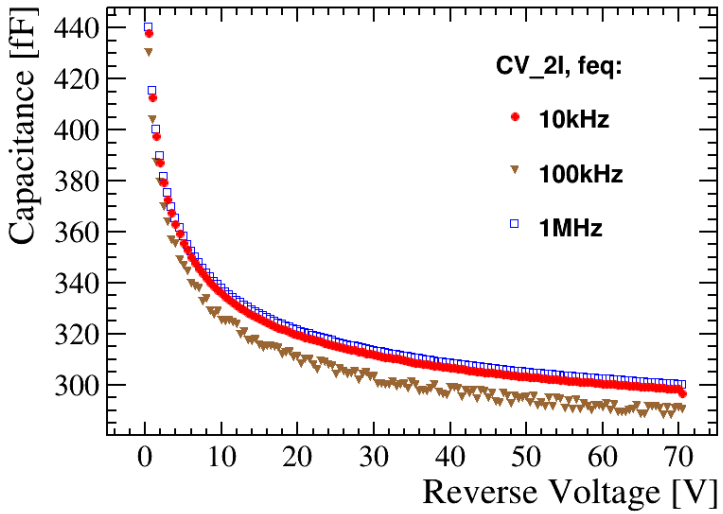
Backup: IVCV - COFFEE2 chip 2, 2O



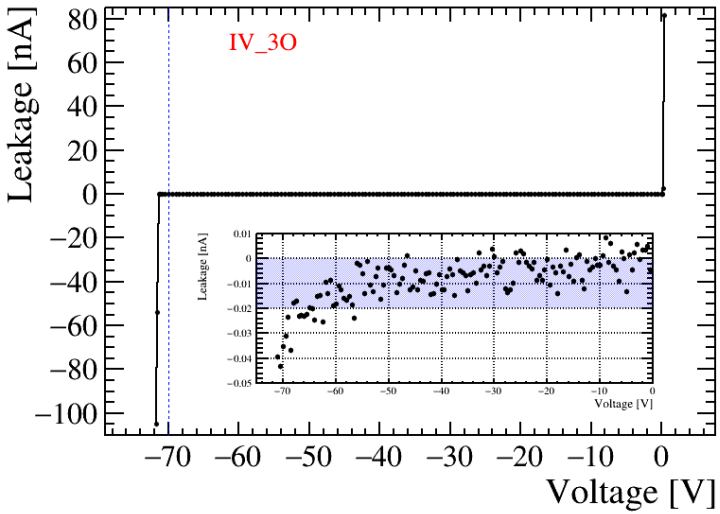


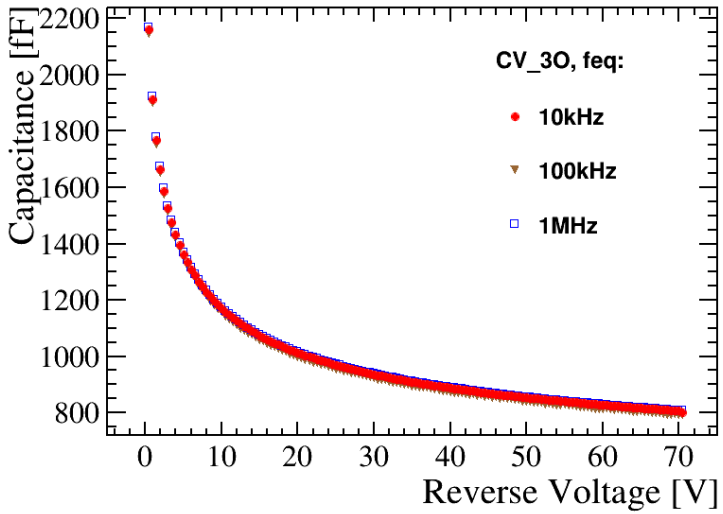
Backup: IVCV - COFFEE2 chip 2, 2I



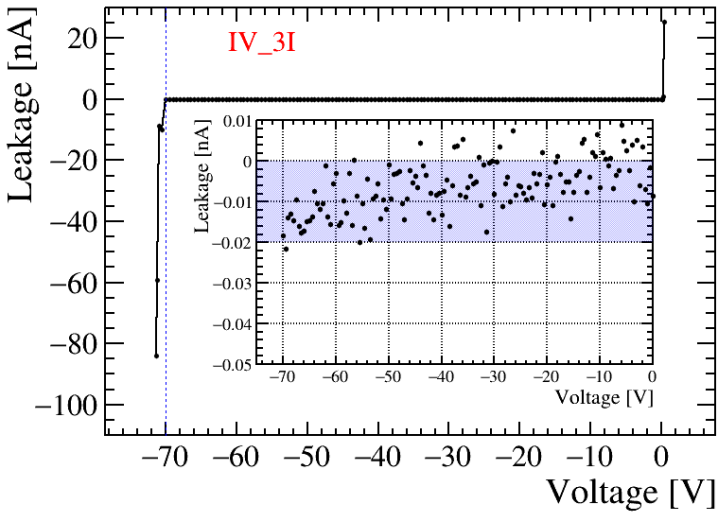


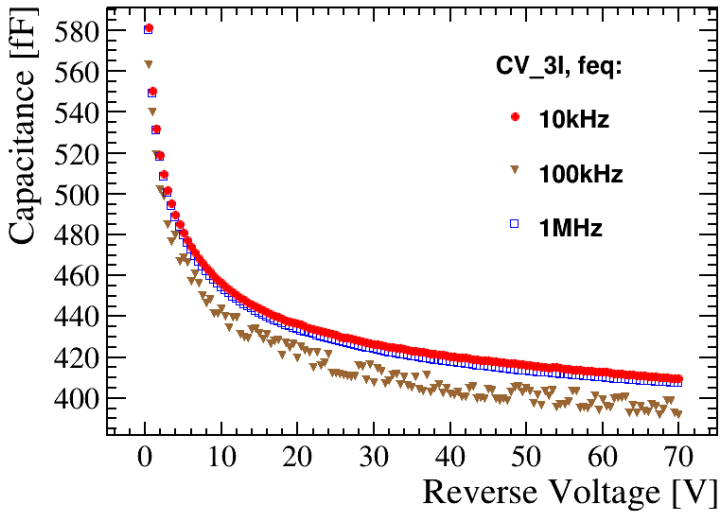
Backup: IVCV - COFFEE2 chip 2, 3O



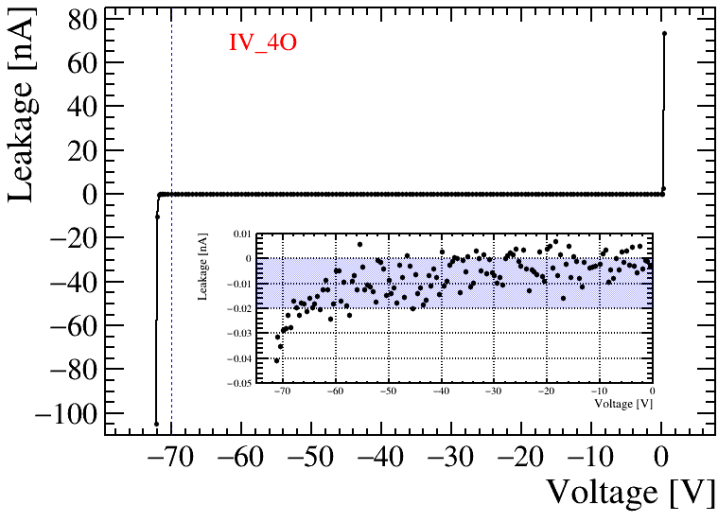


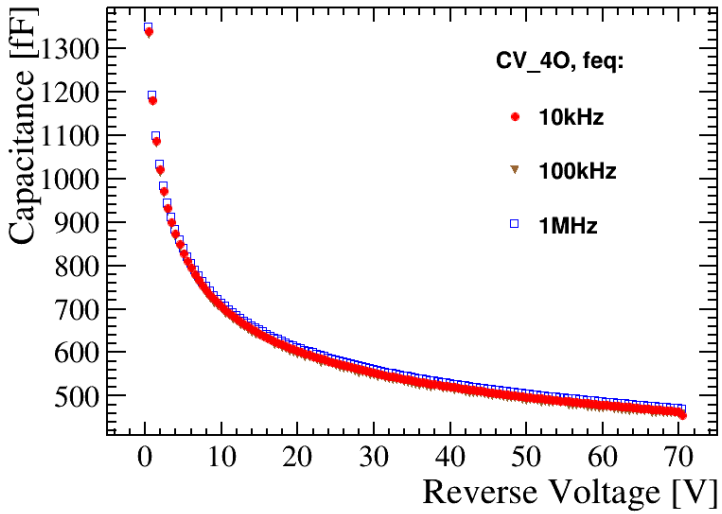
Backup: IVCV - COFFEE2 chip 2, 3I



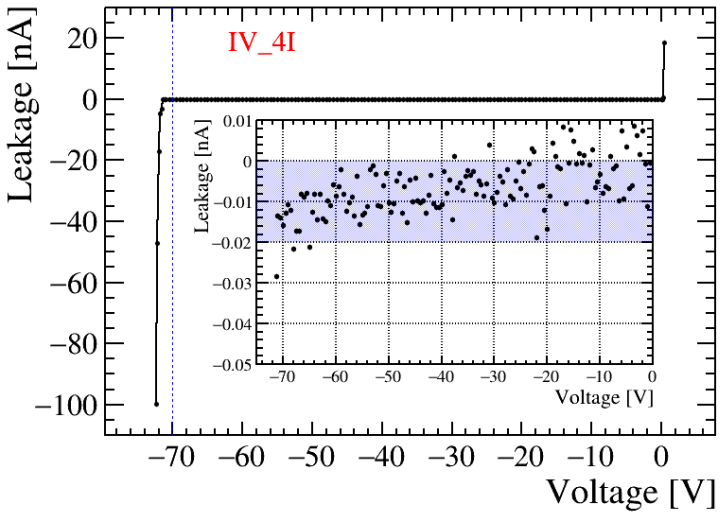


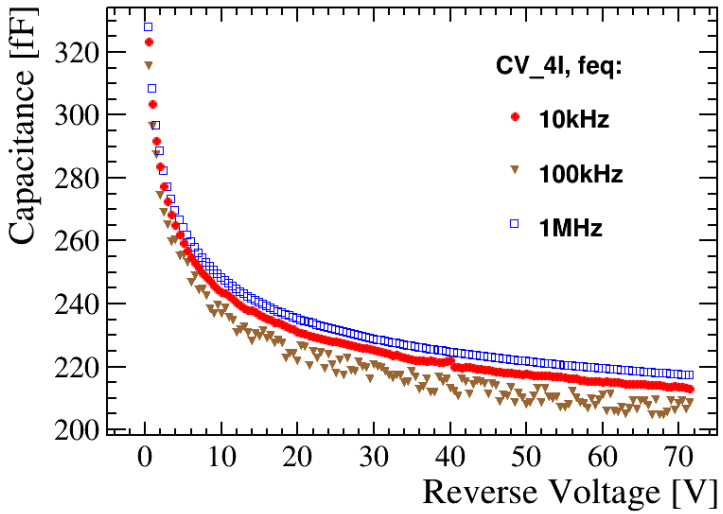
Backup: IVCV - COFFEE2 chip 2, 4O



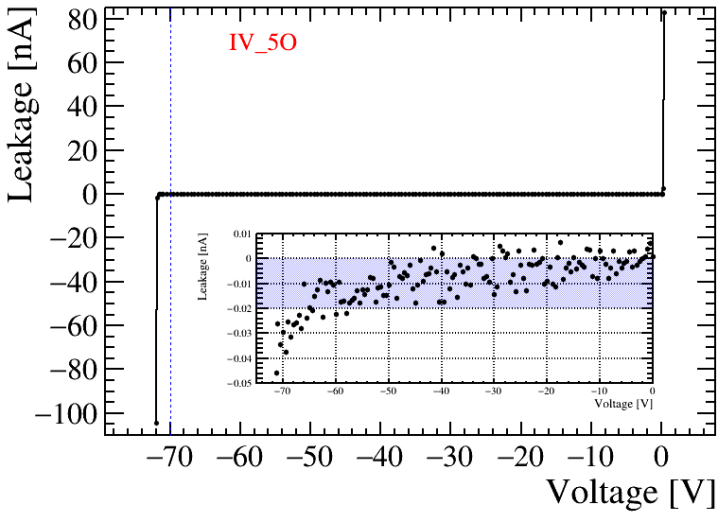


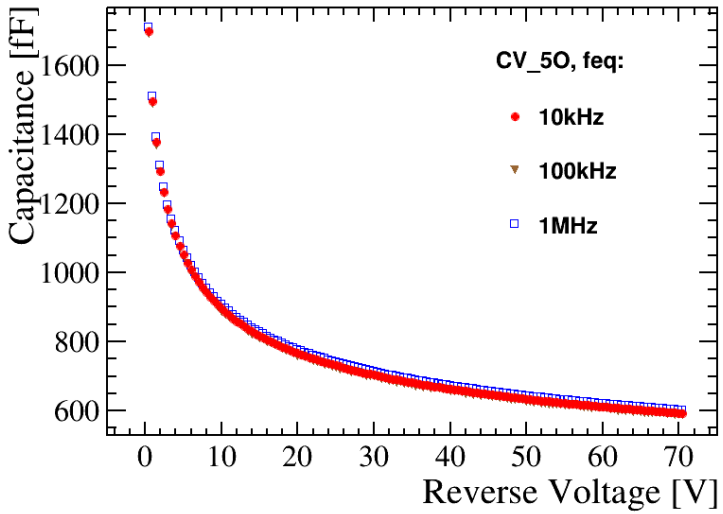
Backup: IVCV - COFFEE2 chip 2, 4I



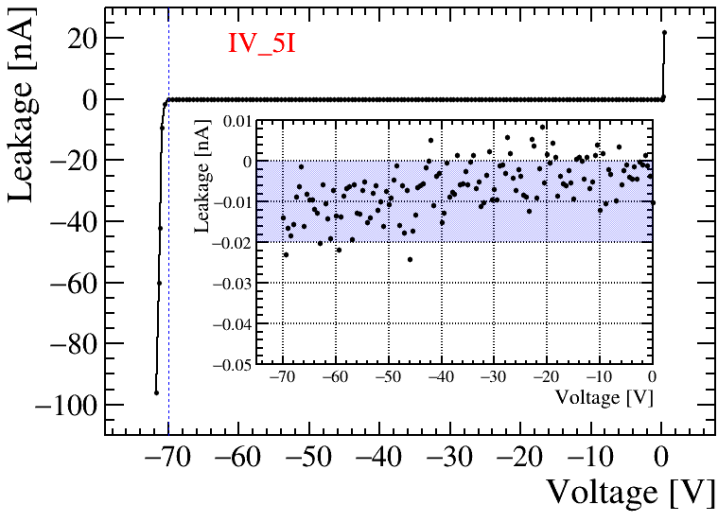


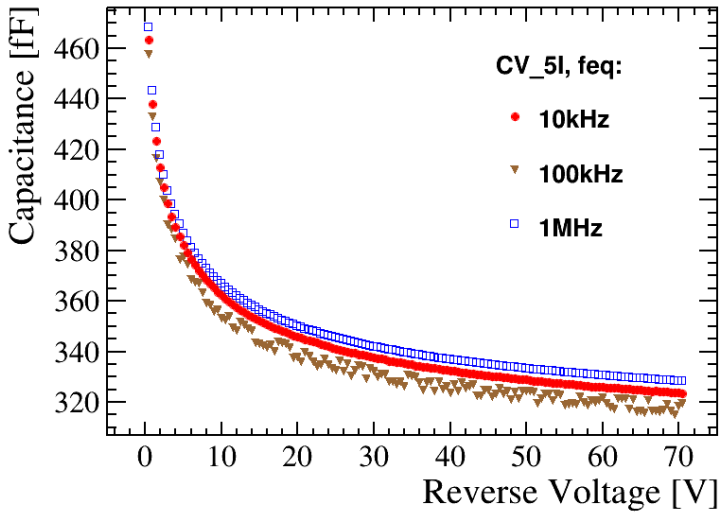
Backup: IVCV - COFFEE2 chip 2, 5O



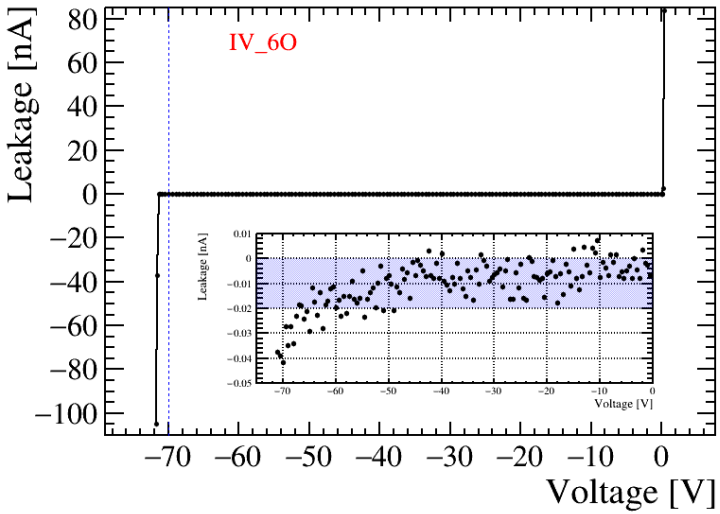


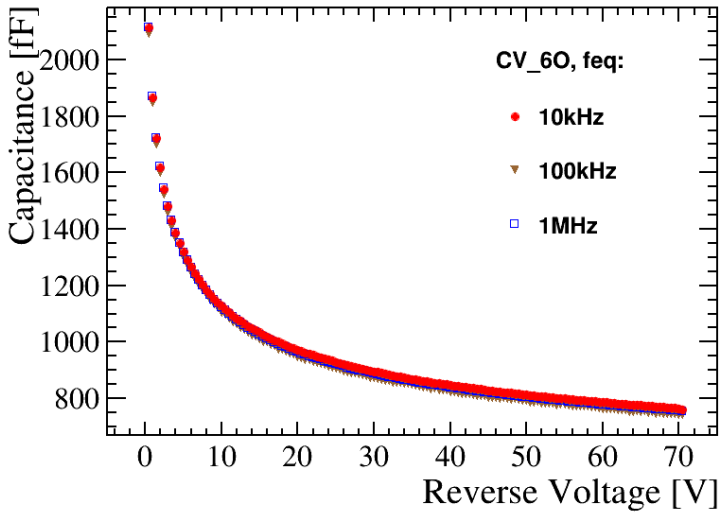
Backup: IVCV - COFFEE2 chip 2, 5I



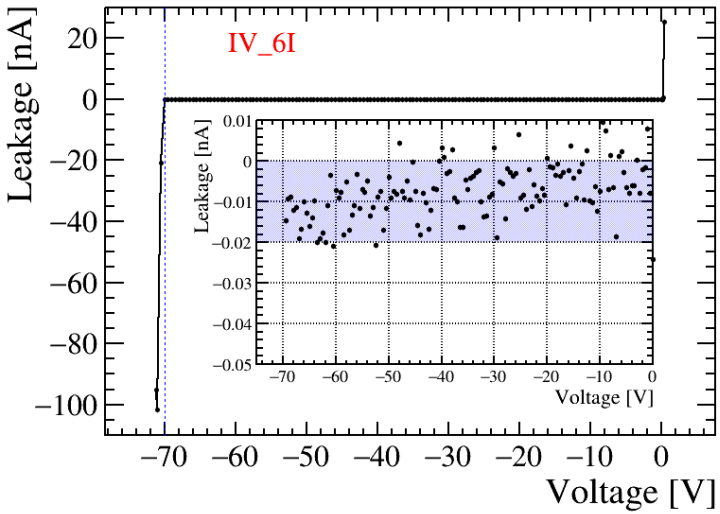


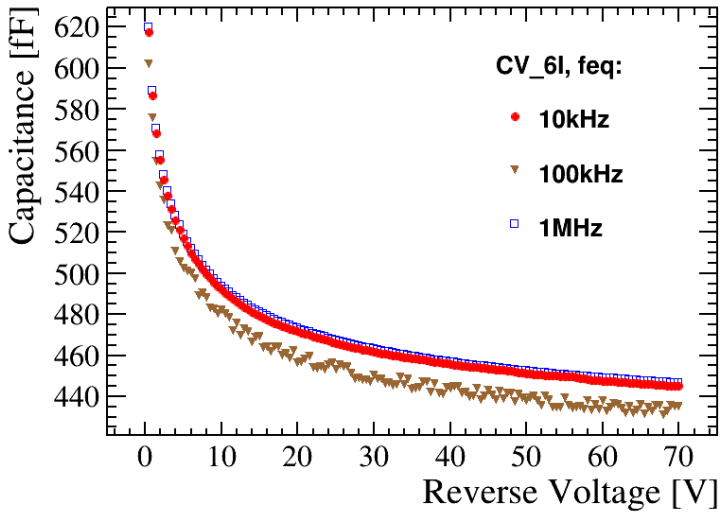
Backup: IVCV - COFFEE2 chip 2, 6O





Backup: IVCV - COFFEE2 chip 2, 6I





Backup: test Feq.

100kHz fluctuates more, need redo open correction. Before & After: