COFFEE2 Circuit Test with Caribou Board

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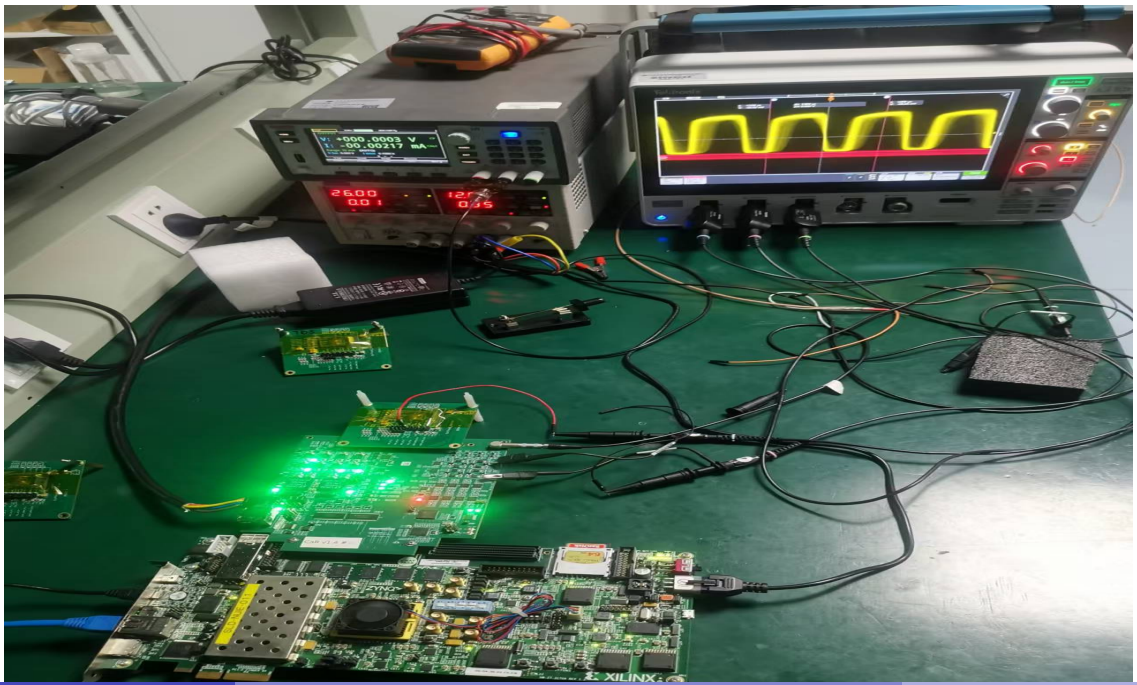


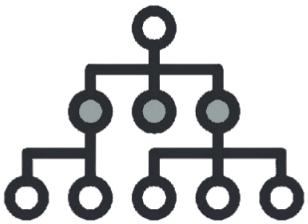
ZC706 evaluation board

Xilinx ZC706 evaluation board

Zynq-7000 XC7Z045-2FFG900C SoC

Processing System (PS)

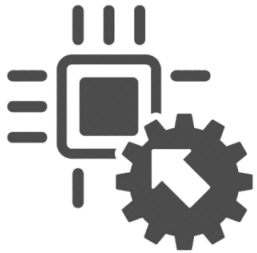
2 x ARM Cortex-A9 MPCore CPUs
Yocto-based Linux
Network/ssh control interface
Caribou DAQ software (Peary)



https://www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html

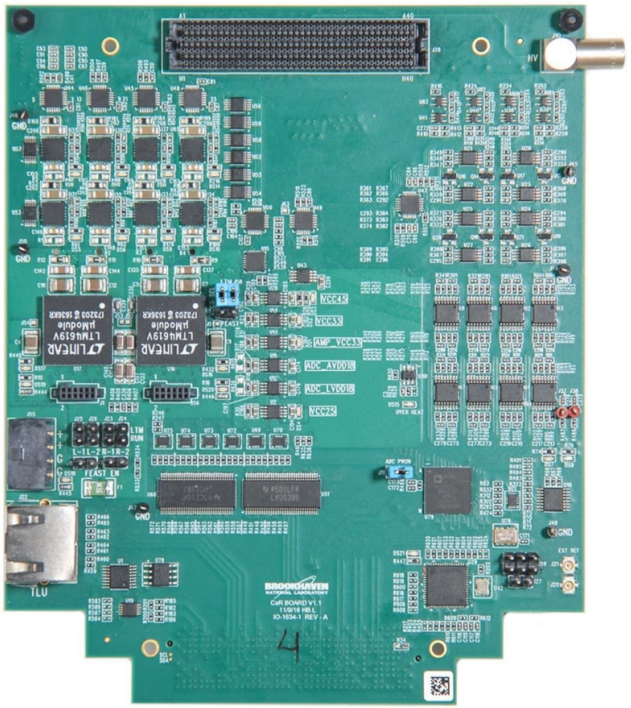
Programmable Logic (PL)

Kintex-7 FPGA
AXI control interface
Caribou firmware



Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



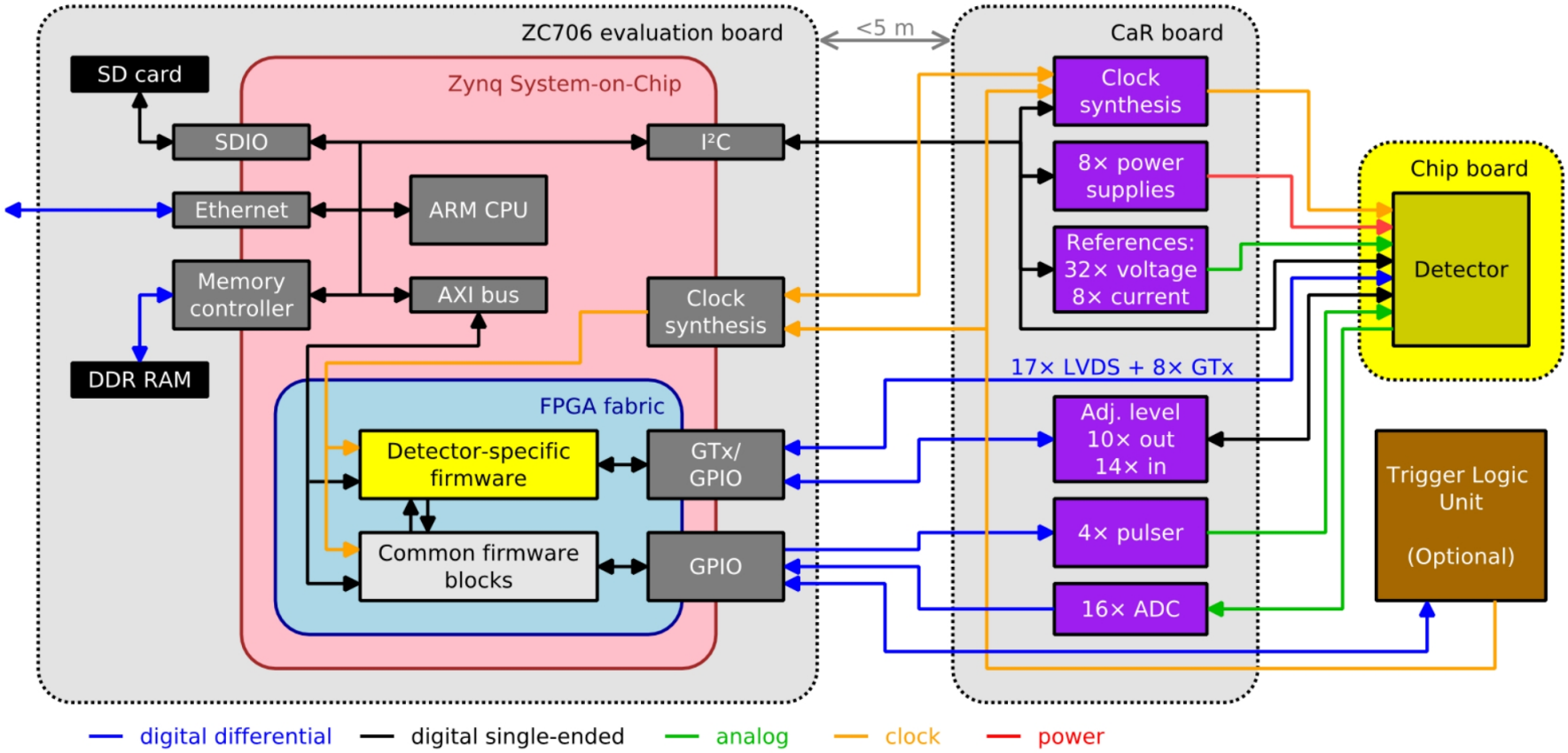
https://gitlab.cern.ch/Caribou/hardware/carboard

Resources for various target applications

20 CaR boards v1.4 produced and distributed within RD50 common project

DAQ System

Caribou system architecture



Setup: Tested Bias PIN

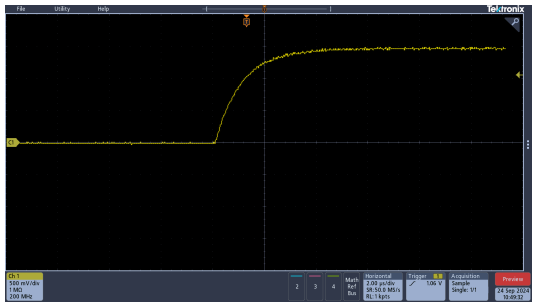
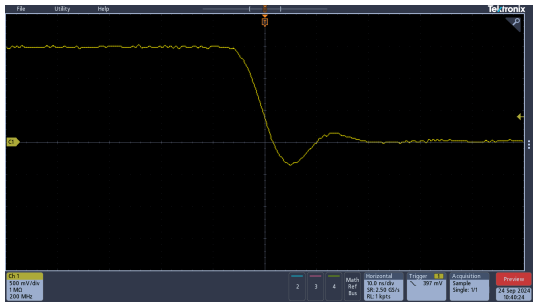
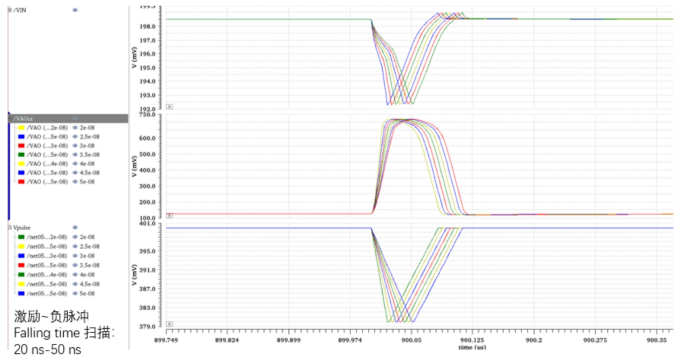
PIN	VDDD	BL	TH_left	COM_BIAS	CLAMP	VDDA
V_{set}[V]	1.2	0.55	0.8	0.8	1.2	1.2
V_{out}[V]	1.23	0.55	0.8	0.8	1.2	1.2
PIN	VB2_FB	VB1_FB	IBN	IBFOLL	VCAS_rt	IBP
V_{set}[V]	0	0.475	0.6	0.5	1.5	0.76
V_{out}[V]	0	0.474	0.6	0.5	1.5	0.76
PIN	VDD_grd	IOUT	VDDA_rt	VB1	TH_rt	VBO
V_{set}[V]	1.2	1.2	0.65	0.7	0.6	1.5
V_{out}[V]	1.23	1.2	0.68	0.7	0.6	1.5
PIN	BL	VNFOLL	VCAS_lt	VN	VP	VB2_SB
V_{set}[V]	0.55	0.4	0.72	0.535	0.73	0
V_{out}[V]	0.55	0.4	0.72	0.536	0.73	0
PIN	P_WELL	VB1_SB	VDDA_left			
V_{set}[V]	0	0.29	0.8			
V_{out}[V]	0	0.29	0.844			

Other bias pins default connect to HV, PWR_OUT or GND

Setup: Tested pulse configuration

Pulse rise/fall time about $4\mu s/20\text{ns}$. Q: require $\sim$ ns? - 20ns fall time works in simulation.

- INJ_BIAS (voltage) + INJ_CTRL (analog switch) = pulse
- INJ_BIAS: I2C protocol among SoC and CaR, DAQ system integrated, easy to control
- INJ_CTRL: Hardware manager or AXI protocol among FPGA and CaR. Need build firmware, configured by Zijun with former method

Setup: Configurable PIN

BIAS: current source, i/o $5\mu A$ configured

VBG/VDAC: BG output/DAC output. getADC $\longrightarrow$ 0.6V

VOUT_1COL: Analog output $\overset{FMC}{\longrightarrow}$ CaR pin(ADC_IN_G2)$\overset{ADC\ block}{\longrightarrow}$Diff. digital signal $\overset{FMC}{\longrightarrow}$ ZC706 FPGA pin: [T24 T25]

Sel_row$<0...4>$: row selector. Digital input, FPGA pin: [W25 W26], [V28 V29], [R28 T28], [T30 U30], [R25 R26]

Row_sel$<0>$: Digital output for validate Sel_$<0>$, FPGA pin [N26 N27]

VCAL: external pulse injection. CaR(INJ_CTRL_1), FPGA pin:[T24 T25]

D_out_1stcol, D_out_234cols: Digital output. H-level if pixel triggered in 1 or 234 (in total) colum. FPGA pin: [P23 P24], [P21 R21]

Setup: Problem PIN - FPGA pin NOT connected to FMC

Few pins of FPGA could not connected for ZC706 due to factory design

Col_sel< 19 >: Digital output. H-level if colum 19 selected

A_out_1stcol, A_out_234cols: Analog output for colum0 or colum 123 (in total)

Sel_col< 0...4 >: colum selector. Digital input, FPGA pin: [P30 R30], [1 break], [T29 U29], [3 break], [P25 P26]

COM_ROW: Digital pulse output after buffer for row 32

COM_PIXEL: 1 pixel comparator output after buffer

CSA_OUT_COL: CSA output after buffer for colum 1

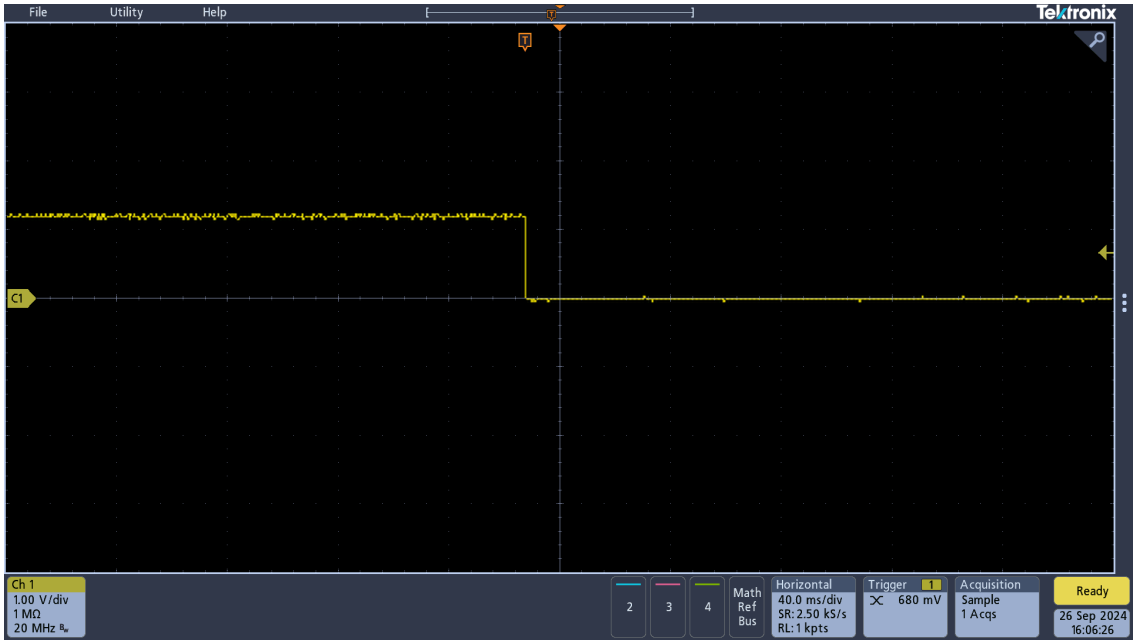
CSA_OUT_PIXEL: CSA output after buffer for 1 pixel

VOUT_1COL,VOUT_7COL, VOUT_SP: Analog output for colum 4, 5-11 or outside 4 signal pixels

COL_CON: Test input from external signal

Digital switch test

Switch Sel_row[4,0] to 0 or !0, Row_sel[0] gives 1 or 0, En_row also works



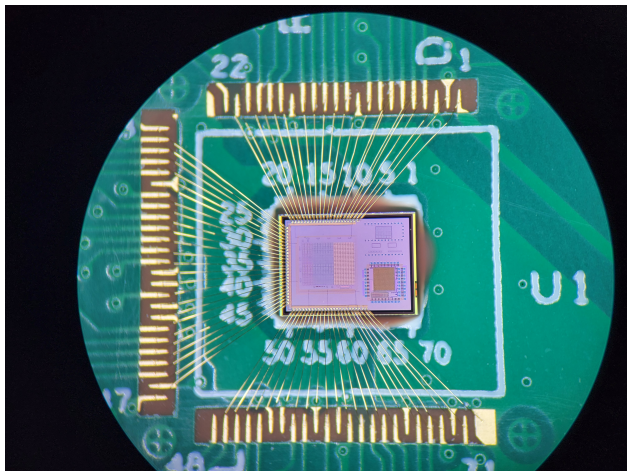
Modifying wire-bonding for colum selector

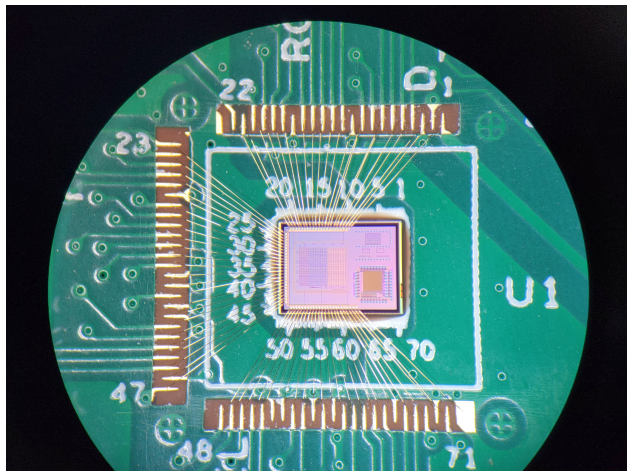
Row-Colum mask: ~~foalting~~ pin convert to 0/1 or random code?

row bit index	4	3	2	1	0	col bit index	4	3	2	1	0
CaR pin index	1	2	4	5	7	CaR pin index	6	~~9~~	3	~~8~~	0

Modifying the wire-bonding for ~~foalting~~ pin (connect bit 3/1 to neighbor) to ensure the certain 0 or 1 level

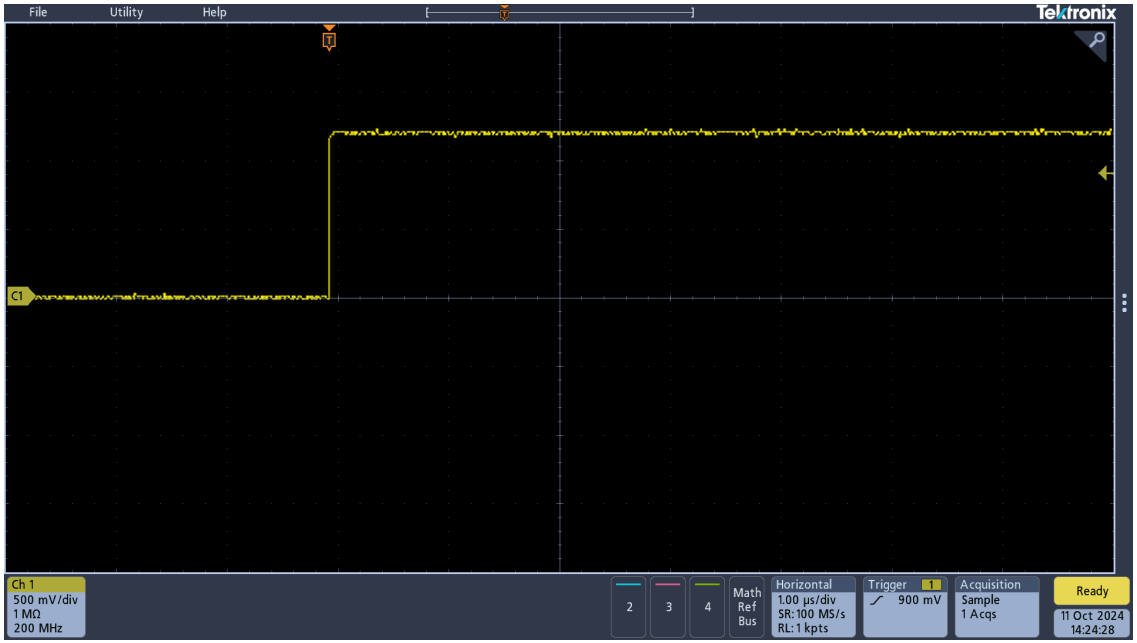
- case1: 1⇔0, 3⇔2, enable colum 0,3,12,15,16,19
- case2: 1⇔2, 3⇔4, enable colum 0,1,6,7





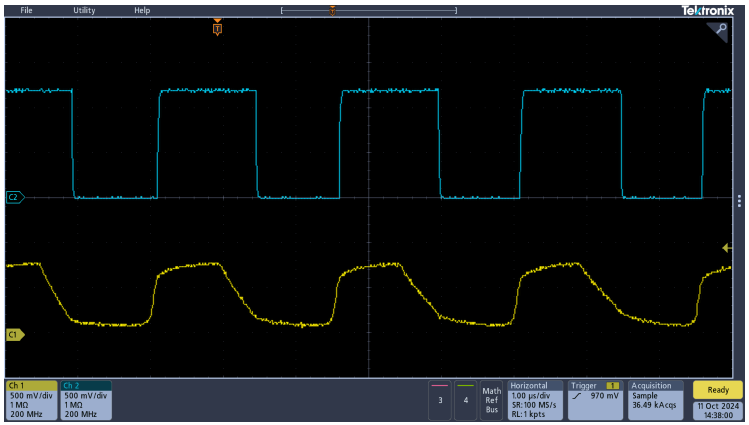
Colum selector validation

Switch Sel_col[4,0] to 10011, Col_sel[19] gives 1

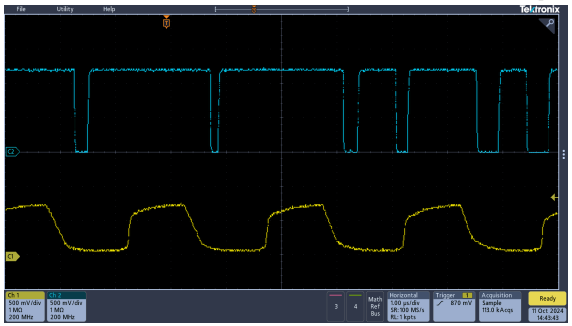


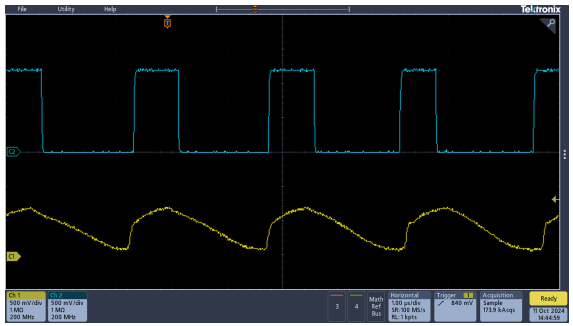
CSA analog out test

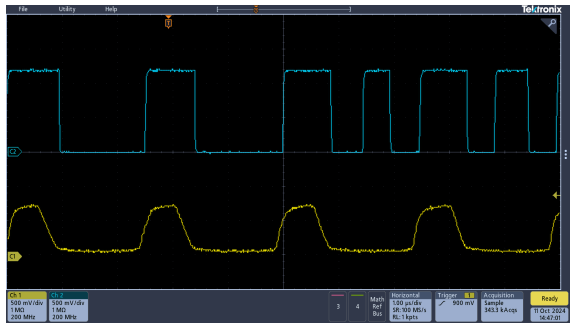
- i.e. Switch Sel_row[4,0] and Sel_col[4,0] to ALL 0 (pixel 0, other rows also tried)
- The abnormal CSA baseline analog output after buffer (A_out_1st_col) and digital output after discriminator (D_out_1stcol). Pulse injection doesn't affect the output
- Similar for other colums (tried 3,6,7 and last 8 colums)



- The discriminator output also not stable

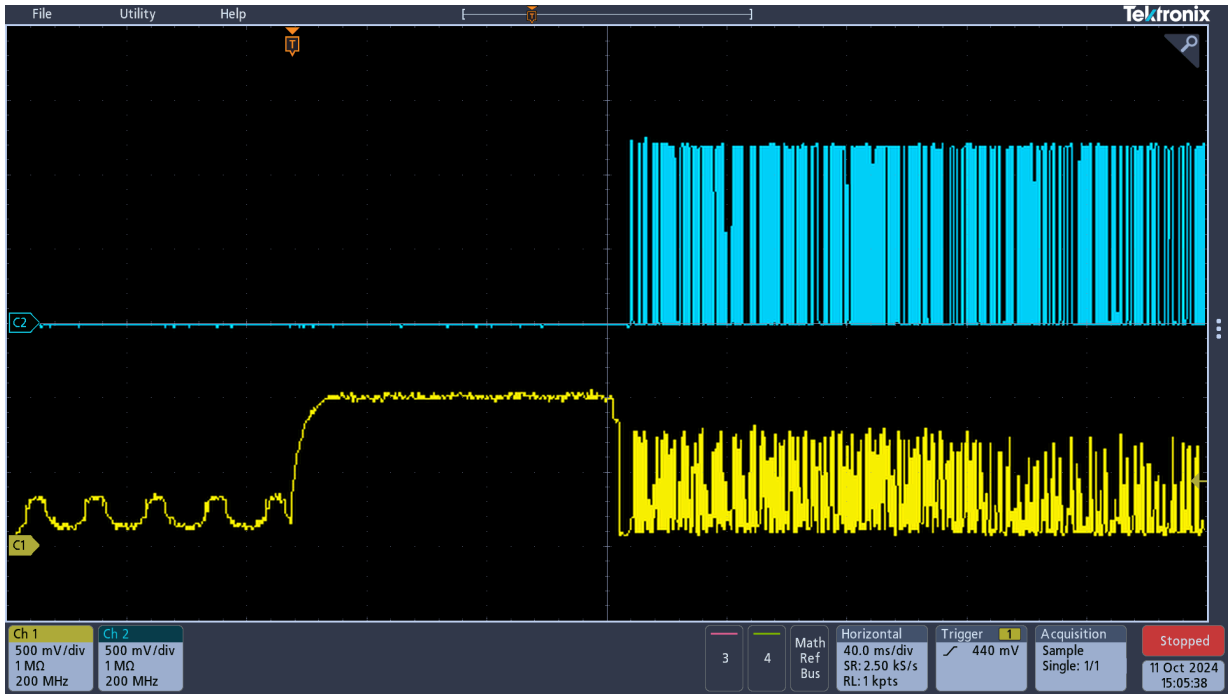






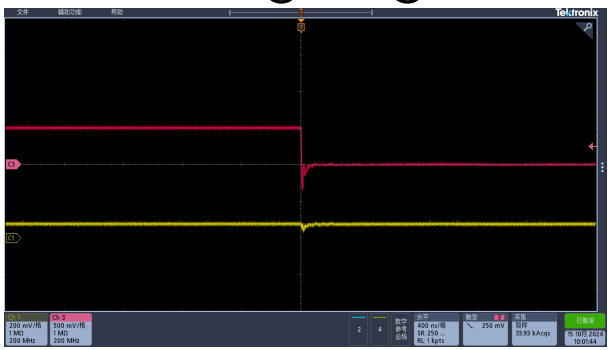
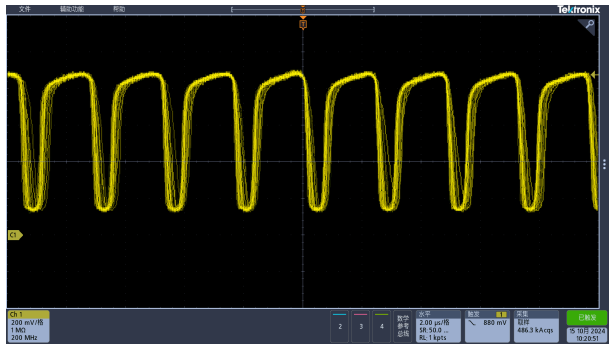
What happen at the very beginning?

- At the time scale of power on. Not sure if there is self-oscillation

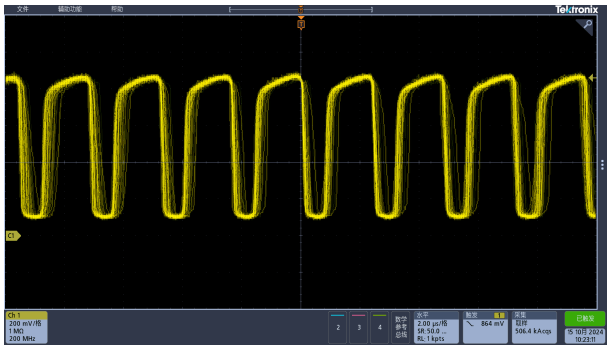
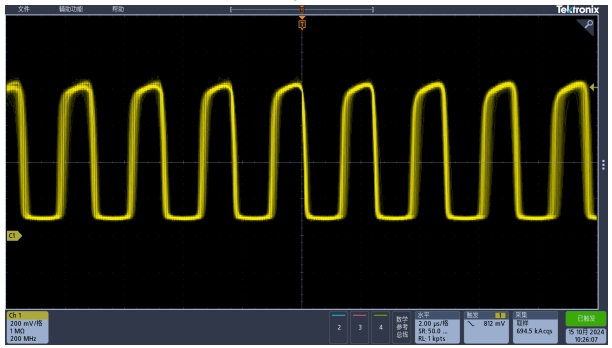
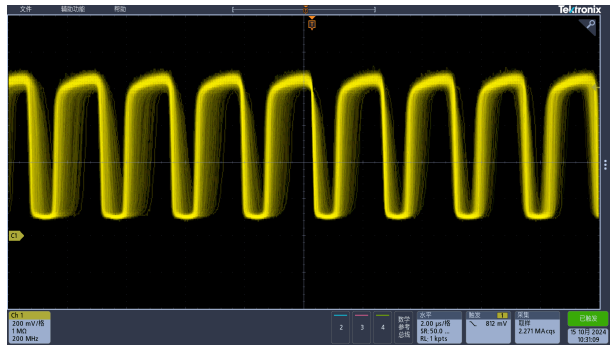


Check a CSA baseline for all TBs

2 (modifying wire-bonding) + 3 (from Weiguo) = 5 TBs in total.
CSA_OUT_PIXEL, analog output of a single pixel after buffer, independent of the row and column gating.

TB1, TB3

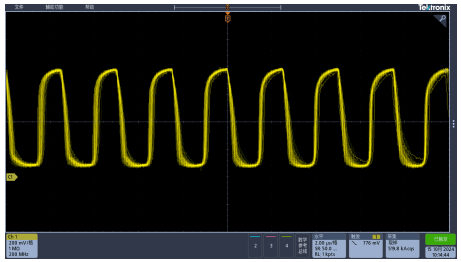
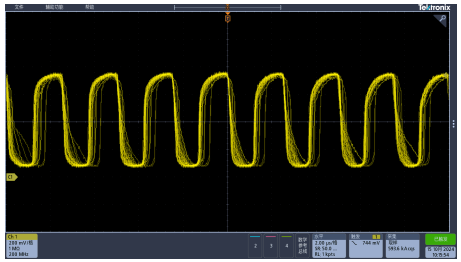
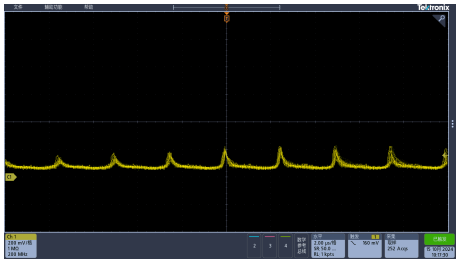
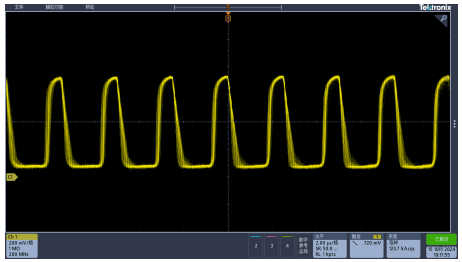




TB4, TB5, TB6

Adjust reference voltage did not affect to much.

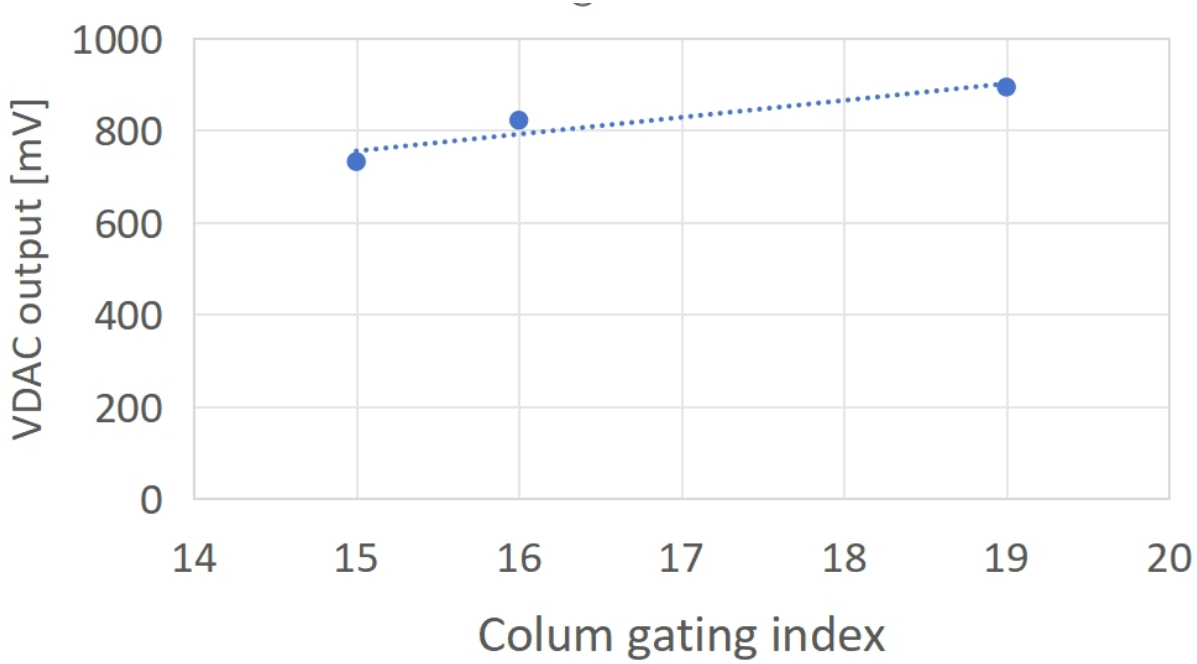
Check CSA in same colum, i.e. TB1

TB1 colum0, change row0, row4, row8, roe16

VDAC test

- VDAC controlled by 6 bit input from colum$<19-14>$, should proportion to colum gating. i.e. TB1 allows colum 15,16,19
- Not a perfect linear dependency



Conclusion

- Caribou system prepared, bias voltage and pulse function verified
- 5 chips tested with (modified) designed board
- Not seen expected CSA analog output
- Row-Colum digital gating works well
- Discriminator seems work
- VDAC changed with colum selection
- What can we try:
  - 1. Try FIB to modify the connection among diode and CSA to avoid the X-talk
  - 2. Investigate the CSA analog output with the simulation
  - 3. Re-do the test with the new externally adjustable board to avoid any potential X-talk from CaR system