

CEPC Silicon Tracker Progress Report (12)

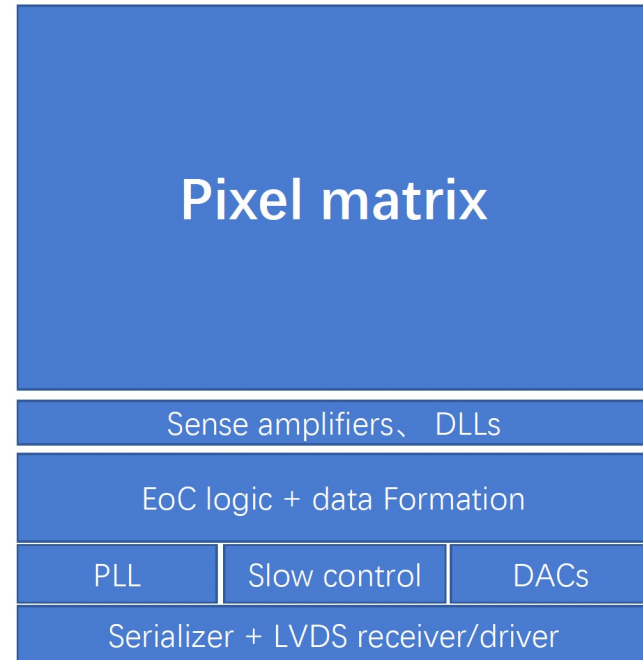
Qi Yan on behalf of the Silicon Tracker Group

Nov 19, 2024, IHEP

Upcoming MPW Submission Plan for HVCMOS Pixels

- Submission plan update for 2025:
 - Two MPW windows in the first half of 2025: January and April
 - Initial plan: 1 MPW to implement all periphery functions

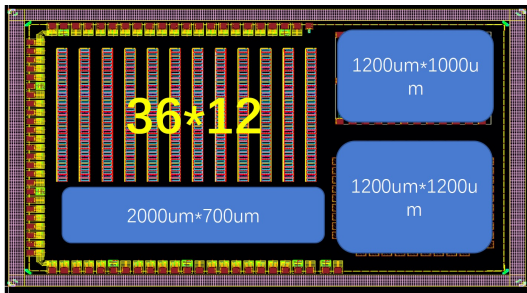
1. Sensors & Guard ring;
2. In-Pixel
 1. Amps;
 2. Discriminators;
 3. Threshold tuning;
 4. Test/mask structure
 5. Memories;
 6. VCDL;
 7. Fine-time stamp control unit;
3. Pixel matrix:
 1. Column-rain, Token-ring & fast or
 2. ...addr. / TS bits / readout method for minimize cross-talk
4. SenseAmp;
5. DLL;
6. Biasing: Bandgap, Current/Voltage DAC;
7. Slow control interface:
8. PLL;
9. EoC logic: interaction with matrix
10. Data Formation: data package, scrambler
11. Fast readout: LVDS Driver & receiver



- To demonstrate part of key performance by ref-TDR release (June 2025?):
 - 1st submission in January: all basic functions except DAC
 - 2nd submission in April or later 2025: DAC included, all other modules optimized

Preparation Towards Next Submission (COFFEE3 ...)

- 15 active designers:
 - preparation for some modules started right after COFFEE2
 - A few modules already in the layout phase
 - However, it remains an extremely challenging task



General layout planning

Pixel size: $34\ \mu\text{m} \times 144\ \mu\text{m}$
 MPW size: $3\ \text{mm} \times 4\ \text{mm}$

- | | |
|---|----------------|
| 1. Top integration、DFT、verification | 周扬、+ 多方合作 |
| 2. Sensors & Guard ring | 邓建鹏、赵梅 |
| 3. In-Pixel | |
| 1. Amps; | 李乐怡、李鹏戎、陆卫国 |
| 2. Discriminators; | |
| 3. Threshold tuning, in-pxel DAC; | |
| 4. Test/mask structure | 李乐怡、周扬 |
| 5. Memories; | |
| 6. VCDL; | |
| 7. Fine-time stamp control unit; | 赵泽轩、魏晓敏 |
| 4. Pixel matrix: | |
| 1. Column-rain, Token-ring, fast or ...addr. readout method for minimize X-talk | 李乐怡、周扬 |
| 2. TS bits、clock gating、readout method for minimize power | 赵泽焯、魏晓敏 |
| 5. SenseAmp; | 李乐怡、周扬 |
| 6. DLL; | 赵泽轩、王雨颀、施展、魏晓敏 |
| 7. EoC logic + Data Formation: 64b/66b, serializer | 张晓旭、陈洋、魏晓敏 |
| 8. Biasing: Bandgap, Current/Voltage DAC; | |
| 9. Slow control interface: | 张晓旭、魏晓敏 |
| 10. PLL: | 王雨颀、施展 |
| 11. Fast readout: driver & receiver | 陈洋、施展 |

新加入:
 吴慧敏
 谢鑫豪
 王小龙

Staff and students from IHEP, NWPU, DMU, SDU, NJU, ...