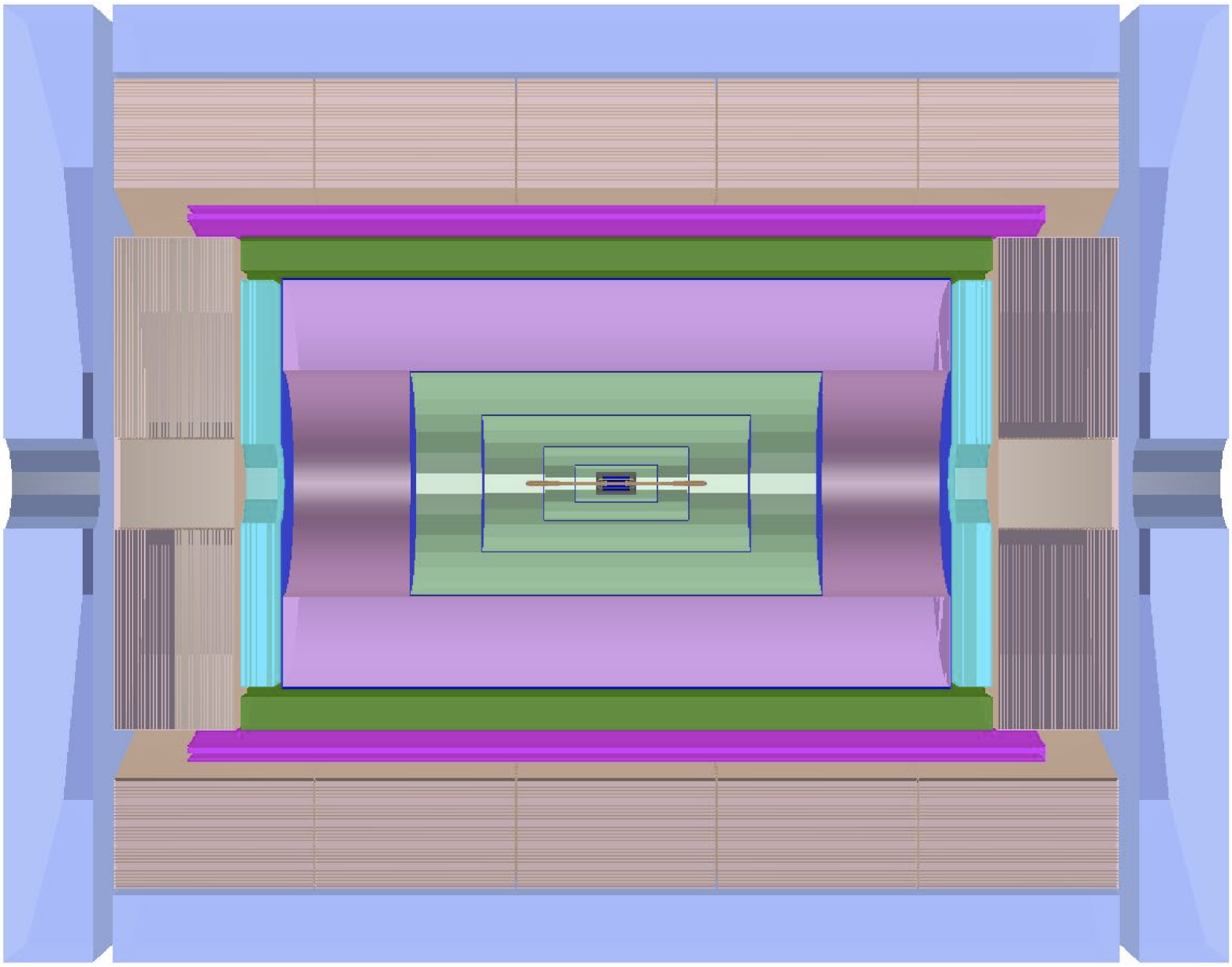

TDR: electronics

Technical Design Report of the CEPC Reference Detector

Author: the CEPC study group

Institute:

Date: June 9, 2025

Version: 0.1

Bio: Information

Contents

Chapter 0 Example chapter

[1]

- Every people please keep their chapter self-consistent.
- Please keep the style same with examples, such as figure, table, citations, and so on
- Please use bibtex for reference: add entries to the reference.bib file and cite them in your chapter

0.1 Main text

For portable version, simply download lastest ElegantBook-master from GitHub or CTAN (to be more accurate, download) [2]

0.2 Figures

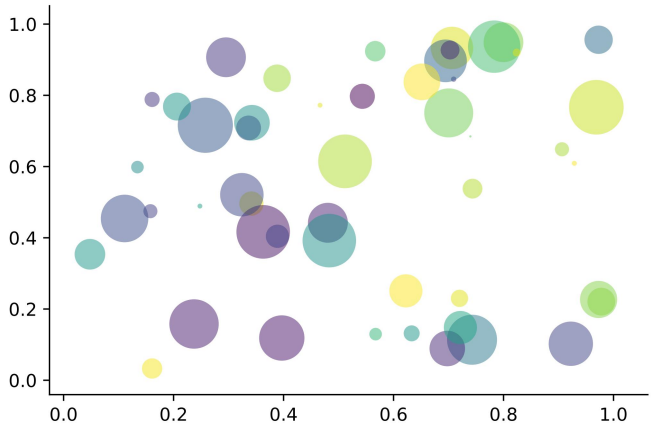

Figure 1: Matplotlib: Scatter Plot Example

0.3 Tables

[1]

Table 1: Caption is above the table, no vertical line, limited number of horizontal lines

Characteristics	**Value1**	**Value2**
Chip width	5 cm	4 cm
Chip thickness	100 μm	
Position resolution	$5-10$ μm	15, 40 μm

References

[1] Frank Mittelbach et al. *The LaTeX Companion*. 2nd. Addison-Wesley Series on Tools and Techniques for Computer Typesetting. Boston, MA, USA: Addison-Wesley, 2004.

[2] Tobias Oetiker et al. *The Not So Short Introduction to LaTeX 2ε*. 4.2. 2006.

Chapter 1 Electronics System (Wei Wei, Jingbo Ye)

1.1 Introduction (Wei Wei)

The main task of the CEPC electronic system is to design the front-end electronics for each sub-detector. This involves amplifying, converting to digital, and processing the detector signals, as well as reading and storing the signals and interfacing with the trigger system. The system also handles key signals like clocks, collision points, and controls to synchronize and control all sub-detectors.

In this chapter, the readout requirements of each sub-detector's electronic system will be introduced in Section 1.2. Key requirements such as background noise, data rates, and power consumption will be summarized based on the front-end electronic readout schemes provided in the sub-detector chapters. The detailed designs of the Front-end ASIC of each sub-detector will also be described in Section 1.3. In Section 1.4, the overall requirements of the CEPC electronic system will be analyzed, clarifying the design ideas and technical choices, defining the readout strategy for the electronic and trigger systems, and providing a unified baseline solution and framework structure for the CEPC electronic system. Section 1.3 will detail the specific design of front-end electronic readout chips for each sub-detector and more general front-end readout chip designs. Additionally, Section 1.5 will introduce the design of key components in the universal platform, including data interfaces, front-end power modules, and back-end electronic boards. Section 1.6 will discuss detector readout schemes based on wireless transmission as an upgrade scheme. Sections 1.7 , 1.8, and 1.9 will cover detector clock synchronization, front-end power distribution, and back-end electronic algorithms and interface designs with the trigger system. Finally, as part of the overall team introduction, the composition of team members and collaboration partners, as well as the previous RD on electronics systems for large particle physics experiments, will be presented in Section 1.11, along with an overview of the team's overall research foundation. In Section 1.12, the electronic system design will be summarized and research plans outlined.

1.2 Detector requirements (Wei Wei)

For the CEPC electronics system, in addition to meeting the front-end electronics readout requirements of each sub-detector, a complete universal electronics framework needs to be designed for the overall spectrometer design. This allows the electronics systems of each sub-detector to be designed with universal interfaces and standards, further modularizing the design of sub-detector electronics and enhancing design independence, plug-and-play capability, and upgradeability. At the system level, this approach also enables more efficient scheduling and communication among various systems. In the previous chapters on each sub-detector, based on the preliminary universality framework provided by the electronics system, corresponding preliminary readout schemes for detectors have been proposed. These schemes include specific organization of front-end electronic chips in modules, taking into account the different operational modes of the CEPC accelerator (such as Higgs, Low LumiZ, etc.), as well as considering the front-end electronic schemes based on background estimates provided by the MDI system. These parameters, as inputs for the design of the universal electronics framework, are summarized in Table 1.1.

From Table 1.1, it can be seen that for different sub-detector systems, targeted research and development of 5 6 front-end ASIC chips will be conducted to detect the physical signals of the detectors. In these ASICs, considerations have been made to merge similar requirements to reduce the variety of ASICs developed in parallel. For example, for the ECAL, HCAL, and Muon detectors, as they will all use SiPM devices in the detectors, a plan is in place to combine the common requirements of the three detectors to design a SiPM readout ASIC with a certain level of universality to simultaneously meet the needs of the three detectors. Additionally, in the design process of front-end chips, apart from detector systems such as Vertex and Inner Tracker that require the use of MAPS technology, for other front-end ASIC designs, it is considered to adopt a unified CMOS 55nm/65nm process from the same foundry, which will allow for the sharing of circuit modules used in chip design as much as possible, thereby accelerating the chip design process and improving the reliability of chip design. This approach embodies the idea of a universal electronics framework in the

Table 1.1: Requirement from Sub Detectors @ Higgs

Specs	Vertex	ITK	TPC	OTK	ECAL	HCAL	Muon
Channels per chip	1024 × 512	512 × 128	128	128	8 16		
Signal processing	XY addr. + BX ID	XY addr. + timing	ADC + TOT + BX ID	TOT + TOA	ADC + TDC / TOT + TOA		
Data Width / hit	32 bit	42 bit	48 bit	40 48 bit	48 bit		
Max Data rate	2Gbps/chip @Triggerless @Low LumiZ Innermost	Avg. 3.53Mbps/chip; Max. 68.9Mbps/chip	70 Mbps / module innermost	Avg. 38.8Mbps/chip; Max. 452.7Mbps/chip	Avg. 0.96Gbps/module; Max. 9.6Gbps/module	Max. 350Mbps/module-layer	Avg. 15.4Mbps/chip; Max. 153.6Mbps/chip
Data aggregation	10 20:1@2Gbps	14:1@O(100Mbps)	i. 279:1 FEE-0; ii. 4:1 Module	i. 22:1@O(50Mbps); ii. 10:1@O(500Mbps)	i. 4:1 side ii. 7*4/14*4 back board@O(100Mbps)	10:1 (40cm*40cm PCB - 4cm*4cm tile)	24:1 @O(400Mbps)
Detector Channel/module	1,882 chips/RSU @Stiching/Ladder	30,856 chips for 2204 modules	492 modules	1.48M channels in 94680 chips for 4500 modules	92500 chips for 740 modules	5.62M channels with 7072 aggregation boards	43.2k channels with 72 aggregation boards
Avg. Data Volume before trigger	474.2Gbps	400.5Gbps	34.4Gbps	277Gbps	710Gbps	1348.8Gbps	24.1Gbps

design of front-end ASICs. Specific ASIC schemes will be detailed in Section 1.3.

The third and fourth rows of the table also summarize the data width of the front-end chip outputs for each subdetector, as well as the average data rate and maximum data rate per chip. This takes into account the detector background provided by the MDI system through overall simulation, and considers the arrangement of modules in each subdetector. Based on the detector module size, detector operating mode, and key information to be detected, combined with the preliminary design of the front-end chip, the data width is determined. Furthermore, based on the detector size corresponding to each channel of the front-end chip, combined with the background counting rate, an estimate of the data rate per chip or module is provided. This will also serve as one of the key input parameters for the overall electronics system interface.

In the fifth row of the table, the situation between the front-end chips and the data interface on different detectors is summarized based on the chip arrangement on the modules of each subdetector, module layout, and the way the front-end of the detector is led out. For cases where there are a large number of chips on the detector, but the average data rate per chip is not high, especially for systems such as OTK and calorimeters, an effective approach is to aggregate the data from multiple chips before readout in order to save data interfaces and cable quantity. This preliminary approach has been considered in the subdetector readout scheme. In the relevant sections of the data interface, the design of data aggregation chips will be based on this, and the organization of front-end chips summarized in this table will be a key input parameter for this design.

Finally, the sixth row of the table summarizes the preliminary number of electronics channels provided by each subdetector, which already takes into account the considerations after the detector has been optimized in size. The seventh row summarizes the total data rate of each subdetector after considering the detector background data rate. These two rows will serve as key design parameters for the TDAQ and electronics interface, and will be discussed in detail in the backend electronics and trigger system sections.

1.3 Sub-detector Front-end Electronics Design (Yan Xiongbo, Chang Jinfan, Li Huaishen, etc)

1.4 Global architecture (Wei Wei)

1.4.1 Consideration on readout strategy (Wei Wei)

As a next-generation large collider experiment electronics system, to design all front-end electronics subsystems according to a unified system specification, to ensure that their data interfaces, power interfaces, etc., are supplied in a uniform manner, and furthermore, to make the backend electronics able to receive data, perform slow control, and configure the front-end electronics of each subdetector in a unified interface, and further communicate with the TDAQ system, will significantly enhancing the unity of the electronics system. This will not only facilitate the unified design and management of different subdetector systems but also enable the entire electronics system to be designed with a certain degree of maximized commonality. That is, based on the different scales of subdetectors, achieving modular design of subdetector electronics can be relatively easy by simply increasing the number of common generic modules accordingly.

To achieve this design style, it is necessary to first determine the overall strategy of the electronics and TDAQ systems. In other words, it is essential to clarify whether the electronics and TDAQ systems adopt a front-end trigger scheme or are based on a front-end triggerless readout scheme.

Table 1.2 provides a general comparison of the two typical trigger readout schemes. It can be seen that the front-end trigger-based approach is relatively traditional. In this method, while the front-end electronics of the detector process the detector signals, they also need to extract key information usable for triggering from the detector signals and send it to the trigger system. At the same time, detector data needs to be cached in the front-end electronics. Once the trigger system receives the key information, it generates trigger decision information based on the physics model and corresponding trigger algorithms, which is then sent back to the front-end electronics. The front-end electronics compare the cached data with trigger decision information to extract valid physical events and send them to the backend electronics, which further routes them to the data acquisition system.

Table 1.2: Comparison of the FEE-Triggerless readout and Trigger readout strategy

Characteristics	**FEE-Triggerless**	**FEE-Trigger**	**Superiority**
Where to acquire trigger info	On BEE	On FEE	
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	FEE-Triggerless
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	
Maturity	Mature but relatively new	Very mature	FEE-Trigger
Resources needed for algorithm	High	Low	
Representative experiments	CMS, LHCb, . . .	ATLAS, BELLE2, BESIII, . . .	

On the other hand, the backend trigger-based approach involves digitizing the detector signals in the front-end electronics and directly transferring them to the backend electronics for caching. The trigger system only communicates with the backend electronics, and the extraction of detector valid events is done solely in the backend electronics and trigger system. The comparison in Table 1.2 shows that these two main electronics frameworks have their own advantages and disadvantages without a clear superiority. In typical applications, they are supported by various large particle physics experiments such as CMS, LHCb, as well as ATLAS, BELLE2, BESIII, respectively.

The traditional front-end trigger scheme effectively eliminates detector background, reduces pressure from data transmission bandwidth, but also increases the demand for front-end electronics data caching capacity. It usually allows only short trigger delays, requires faster trigger decision speeds, and simpler trigger algorithms. On the other hand, the front-end triggerless readout method reduces the design complexity of front-end electronics by eliminating trigger-related logic. However, since detector background and valid events are both read out together, it increases the pressure on front-end data transmission. Nevertheless, with improved processing capabilities and cache space in the backend electronics compared to the front-end electronics, the front-end triggerless readout scheme can also implement relatively complex trigger algorithms. This reduces the requirements for trigger delay and trigger system design, making pure software triggering possible. In China's collider spectrometer experiments represented by BESIII, the front-end trigger-based approach is commonly adopted. Non-collider experiments represented by JUNO and LHAASO generally explore front-end waveform sampling schemes, but overall, the implementation of trigger algorithms still follows relatively traditional approaches such as data compression and detector information extraction.

[1]

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[1] Frank Mittelbach et al. *The LaTeX Companion*. 2nd. Addison-Wesley Series on Tools and Techniques for Computer Typesetting. Boston, MA, USA: Addison-Wesley, 2004.

[2] Tobias Oetiker et al. *The Not So Short Introduction to LaTeX 2$_\varepsilon$*. 4.2. 2006.