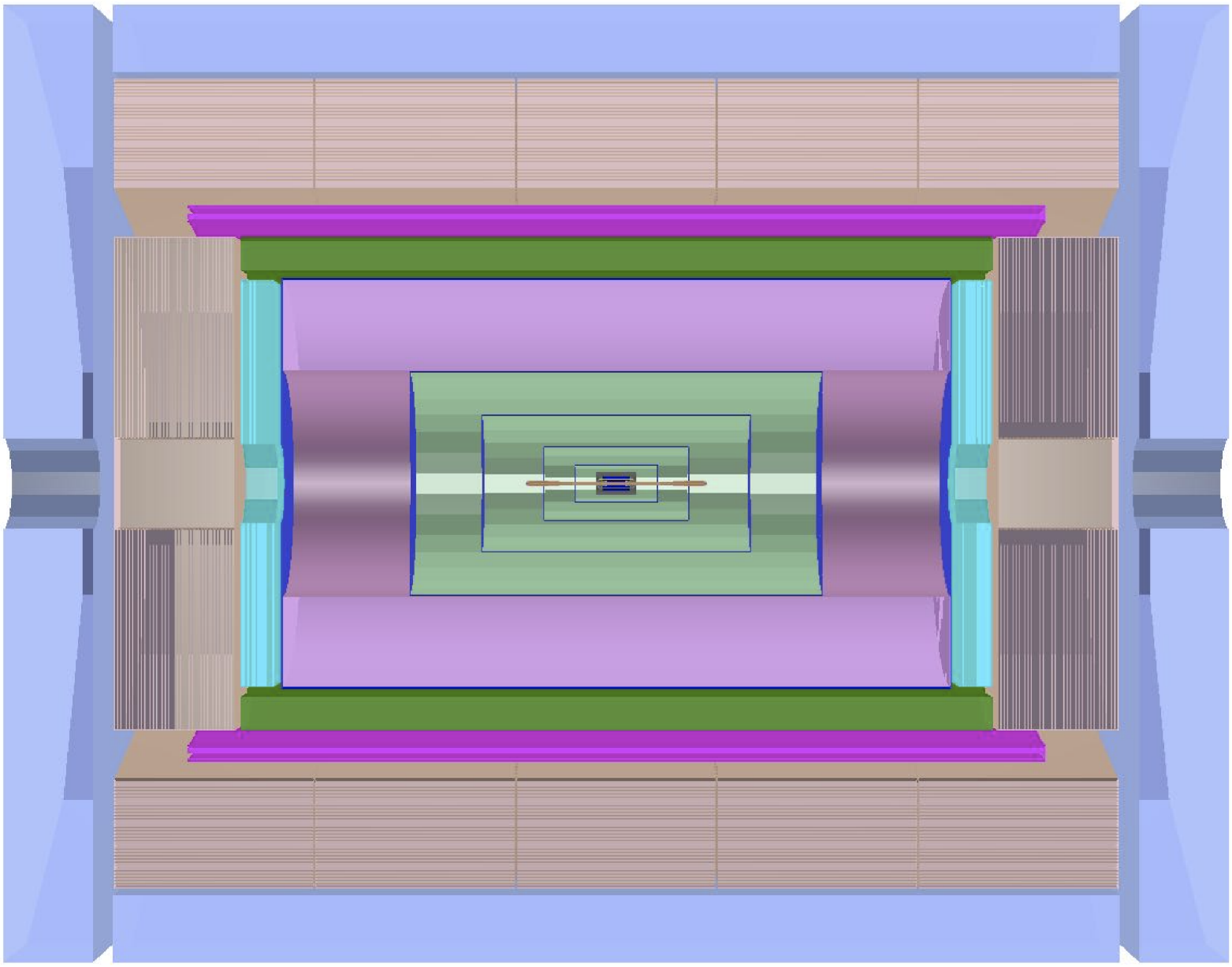


TDR: electronics

Technical Design Report of the CEPC Reference Detector

Author: the CEPC study group

Institute:

Date: June 9, 2025

Version: 0.1

Bio: Information

Contents

Chapter 0 Example chapter

[1]

- Every people please keep their chapter self-consistent.
- Please keep the style same with examples, such as figure, table, citations, and so on
- Please use bibtex for reference: add entries to the reference.bib file and cite them in your chapter

0.1 Main text

For portable version, simply download lastest ElegantBook-master from GitHub or CTAN (to be more accurate, download) [2]

0.2 Figures

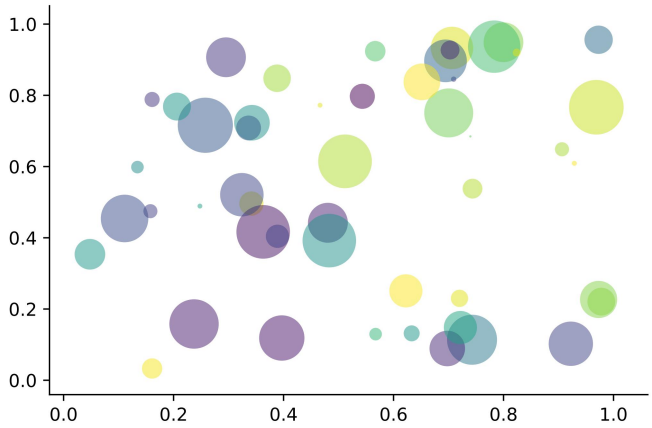


Figure 1: Matplotlib: Scatter Plot Example

0.3 Tables

[1]

Table 1: Caption is above the table, no vertical line, limited number of horizontal lines

Characteristics	**Value1**	**Value2**
Chip width	5 cm	4 cm
Chip thickness	100 μm	
Position resolution	$5-10$ μm	15, 40 μm

References

[1] Frank Mittelbach et al. *The LaTeX Companion*. 2nd. Addison-Wesley Series on Tools and Techniques for Computer Typesetting. Boston, MA, USA: Addison-Wesley, 2004.

[2] Tobias Oetiker et al. *The Not So Short Introduction to LaTeX 2ε*. 4.2. 2006.

Chapter 1 Electronics System (Wei Wei, Jingbo Ye)

1.1 Introduction (Wei Wei)

The main task of the CEPC electronic system is to design the front-end electronics for each sub-detector. This involves amplifying, converting to digital, and processing the detector signals, as well as reading and storing the signals and interfacing with the trigger system. The system also handles key signals like clocks, collision points, and controls to synchronize and control all sub-detectors.

In this chapter, the readout requirements of each sub-detector's electronic system will be introduced in Section 1.2. Key requirements such as background noise, data rates, and power consumption will be summarized based on the front-end electronic readout schemes provided in the sub-detector chapters. The detailed designs of the Front-end ASIC of each sub-detector will also be described in Section 1.3. In Section 1.4, the overall requirements of the CEPC electronic system will be analyzed, clarifying the design ideas and technical choices, defining the readout strategy for the electronic and trigger systems, and providing a unified baseline solution and framework structure for the CEPC electronic system. Section 1.3 will detail the specific design of front-end electronic readout chips for each sub-detector and more general front-end readout chip designs. Additionally, Section 1.5 will introduce the design of key components in the universal platform, including data interfaces, front-end power modules, and back-end electronic boards. Section 1.6 will discuss detector readout schemes based on wireless transmission as an upgrade scheme. Sections 1.7 , 1.8, and 1.9 will cover detector clock synchronization, front-end power distribution, and back-end electronic algorithms and interface designs with the trigger system. Finally, as part of the overall team introduction, the composition of team members and collaboration partners, as well as the previous R&D on electronics systems for large particle physics experiments, will be presented in Section 1.11, along with an overview of the team's overall research foundation. In Section 1.12, the electronic system design will be summarized and research plans outlined.

1.2 Detector requirements (Wei Wei)

For the CEPC electronics system, in addition to meeting the front-end electronics readout requirements of each sub-detector, a complete universal electronics framework needs to be designed for the overall spectrometer design. This allows the electronics systems of each sub-detector to be designed with universal interfaces and standards, further modularizing the design of sub-detector electronics and enhancing design independence, plug-and-play capability, and upgradeability. At the system level, this approach also enables more efficient scheduling and communication among various systems. In the previous chapters on each sub-detector, based on the preliminary universality framework provided by the electronics system, corresponding preliminary readout schemes for detectors have been proposed. These schemes include specific organization of front-end electronic chips in modules, taking into account the different operational modes of the CEPC accelerator (such as Higgs, Low LumiZ, etc.), as well as considering the front-end electronic schemes based on background estimates provided by the MDI system. These parameters, as inputs for the design of the universal electronics framework, are summarized in Table 1.1.

From Table 1.1, it can be seen that for different sub-detector systems, targeted research and development of 5 6 front-end ASIC chips will be conducted to detect the physical signals of the detectors. In these ASICs, considerations have been made to merge similar requirements to reduce the variety of ASICs developed in parallel. For example, for the ECAL, HCAL, and Muon detectors, as they will all use SiPM devices in the detectors, a plan is in place to combine the common requirements of the three detectors to design a SiPM readout ASIC with a certain level of universality to simultaneously meet the needs of the three detectors. Additionally, in the design process of front-end chips, apart from detector systems such as Vertex and Inner Tracker that require the use of MAPS technology, for other front-end ASIC designs, it is considered to adopt a unified CMOS 55nm/65nm process from the same foundry, which will allow for the sharing of circuit modules used in chip design as much as possible, thereby accelerating the chip design process and improving the reliability of chip design. This approach embodies the idea of a universal electronics framework in the

Table 1.1: Requirement from Sub Detectors @ Higgs

Specs	Vertex	ITK	TPC	OTK	ECAL	HCAL	Muon
Channels per chip	1024 × 512	512 × 128	128	128	8 16		
Signal processing	XY addr. + BX ID	XY addr. + timing	ADC + TOT + BX ID	TOT + TOA	ADC + TDC / TOT + TOA		
Data Width / hit	32 bit	42 bit	48 bit	40 48 bit	48 bit		
Max Data rate	2Gbps/chip @Triggerless @Low LumiZ Innermost	Avg. 3.53Mbps/chip; Max. 68.9Mbps/chip	70 Mbps / module innermost	Avg. 38.8Mbps/chip; Max. 452.7Mbps/chip	Avg. 0.96Gbps/module; Max. 9.6Gbps/module	Max. 350Mbps/module-layer	Avg. 15.4Mbps/chip; Max. 153.6Mbps/chip
Data aggregation	10 20:1@2Gbps	14:1@O(100Mbps)	i. 279:1 FEE-0; ii. 4:1 Module	i. 22:1@O(50Mbps); ii. 10:1@O(500Mbps)	i. 4:1 side ii. 7*4/14*4 back board@O(100Mbps)	10:1 (40cm*40cm PCB - 4cm*4cm tile)	24:1 @O(400Mbps)
Detector Channel/module	1,882 chips/RSU @Stiching/Ladder	30,856 chips for 2204 modules	492 modules	1.48M channels in 94680 chips for 4500 modules	92500 chips for 740 modules	5.62M channels with 7072 aggregation boards	43.2k channels with 72 aggregation boards
Avg. Data Volume before trigger	474.2Gbps	400.5Gbps	34.4Gbps	277Gbps	710Gbps	1348.8Gbps	24.1Gbps

design of front-end ASICs. Specific ASIC schemes will be detailed in Section 1.3.

The third and fourth rows of the table also summarize the data width of the front-end chip outputs for each subdetector, as well as the average data rate and maximum data rate per chip. This takes into account the detector background provided by the MDI system through overall simulation, and considers the arrangement of modules in each subdetector. Based on the detector module size, detector operating mode, and key information to be detected, combined with the preliminary design of the front-end chip, the data width is determined. Furthermore, based on the detector size corresponding to each channel of the front-end chip, combined with the background counting rate, an estimate of the data rate per chip or module is provided. This will also serve as one of the key input parameters for the overall electronics system interface.

In the fifth row of the table, the situation between the front-end chips and the data interface on different detectors is summarized based on the chip arrangement on the modules of each subdetector, module layout, and the way the front-end of the detector is led out. For cases where there are a large number of chips on the detector, but the average data rate per chip is not high, especially for systems such as OTK and calorimeters, an effective approach is to aggregate the data from multiple chips before readout in order to save data interfaces and cable quantity. This preliminary approach has been considered in the subdetector readout scheme. In the relevant sections of the data interface, the design of data aggregation chips will be based on this, and the organization of front-end chips summarized in this table will be a key input parameter for this design.

Finally, the sixth row of the table summarizes the preliminary number of electronics channels provided by each subdetector, which already takes into account the considerations after the detector has been optimized in size. The seventh row summarizes the total data rate of each subdetector after considering the detector background data rate. These two rows will serve as key design parameters for the TDAQ and electronics interface, and will be discussed in detail in the backend electronics and trigger system sections.

1.3 Sub-detector Front-end Electronics Design (Yan Xiongbo, Chang Jinfan, Li Huaishen, etc)

1.3.1 ITK readout electronics

1.3.1.1 FE board

The required bandwidth of the readout e-link of each sensor strongly depends on the radial region it covers. For monolithic HVCMOS Pixel, the number of bit per hit is 48. Considering an area of 2cm*2cm, the distribution of the average number of bit per sensor is 4 Mbps and the maximum number of bit per sensor is 70 Mbps.

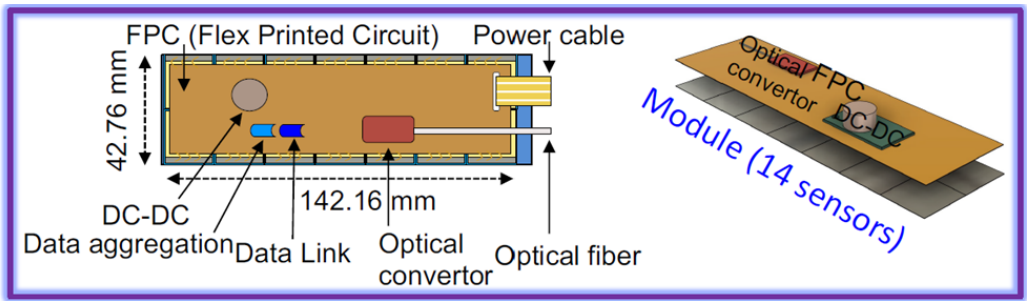


Figure 1.1: Detector module design of the ITK

Each module consisting of 14 sensors are bonded to a Flex Electronics Board (FEB), considering the material budget. The FEB transfers digital signals to the data aggregation chip, then transfers signals to the optical fiber. For error-free data transmission, the FEB uses two ASICs of data aggregation, TaoTie chip and ChiTu chip. The TaoTie chip collects the data from different sensors and transfer it serially. The ChiTu chip collects data from several TaoTie chips. The hit rate is different at different radius. A dedicated buffer is needed in each ASIC to average the rate variation and match the best speed of the e-link drivers transceiver inputs. The optical fibers take the data out of the detector, and connects to the

back-end DAQ. The ChiTu will work at a data rate of 10Gbps which is enough for end cap at the smallest radius. The clock is recovered by CDR in ChiTu. The ChiTu gives 3 choices of output of clock, 40MHz, 160MHz and 320MHz, which will be used in frond end electronics for different detectors.

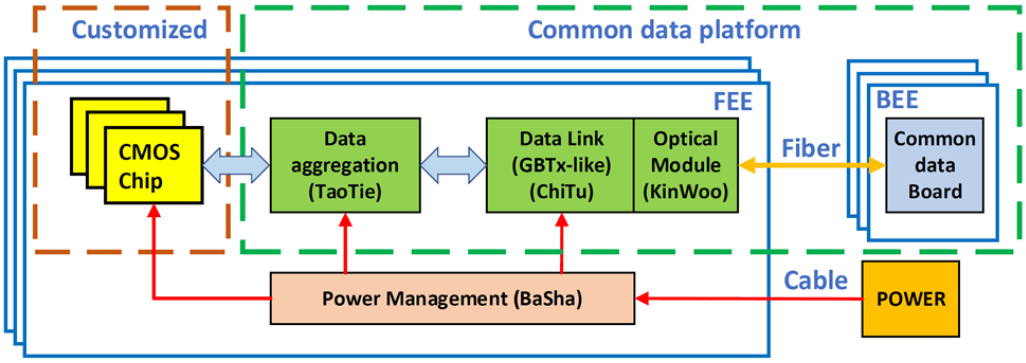


Figure 1.2: Global Framework of the Frontend Electronics

The power for low voltage (LV) and high voltage (HV) is independent for each module, considering the total consumption is 200mW/cm2. There will be 2 DC-DCs on the flex for each module since the current will be more than 10 A with 1.2V power, regarding the margin for efficiency of conversion. The 48V from power crate steps down to 12V at the first stage and to 1.2V at the second stage where the output capability of DC-DC is 10A. A composite cable with a pair of LV, a pair of HV and an optical fiber will be used to make module assembly easy.

For Monolithic CMOS strip, the readout scheme is very similar, even though the hit rate for each channel is higher than pixel in front end electronics.

1.3.2 OTK readout electronics

1.3.2.1 Front-end board

The FE board receives signals from LGAD strips that are processed by six OTKROC ASICs. No need of AC coupled thanks to the internal coupling design. to the ASIC using 150V-rated capacitors that isolate the circuit from the large leakage current and protect the ASIC from being damaged by the bias voltage in case of LGAD failure. The OTKROC ASIC is powered by a single 1.2 V supply. This voltage is regulated and filtered by the DC-DC BaSha ASIC. The BaSha delivers up to 10A current, which is sufficient for the operation of 8 OTK ASICs. The 2 slides of sensor (4cm*104cm) share one FE board, on which has 2 BaSha ASICs and 16 OTKROC ASICs. In the baseline design, the distribution of the LGAD bias voltage is provided by external bias channels, each channel serving a LGAD module. Each bias channel has two HV wires transmitted over the services cables. The HV wires for each module are independent. The LV wires are connected by shunt cables between two neighbor FE boards. The FE board interfaces to the Concentrator Card through board side-to-side connectors transferring the following signals:

1. Clock: sixteen ChiTu e-clocks (43.3 MHz), one per OTKROC ASIC ;
2. Data readout: 1 up E-links (320 Mb/s) per TaoTie connecting to ChiTu on the CC;
3. Configuration: one down E-link (43.3 Mb/s) for OTKROC configuration shared by sixteen OTKROCs;
4. Sync/reset: one down E-link (43.3 Mb/s) for OTKROC resync/reset shared by sixteen OTKROCs;
5. Monitoring: provision for sixteen temperature sensors per FE board (sensor and electronics temperatures).
6. Power and ground.

Each FE board is served by 2 DC-DC converters providing 1.2 V. In order to have a more stable and precise regulation of the analog power supplies and to reduce the switching noise introduced by DC-DC, filter with passive components will be used. The aggregation chip TaoTie provides up to 16 upstream links (1.28 Gbit/s) and up to 16 clocks (43.3 MHz), and 16 downstream links (43.3 Mbit/s). This allows each FE board to receive a dedicated clock from the ChiTu and to transmit data over one dedicated uplink to one ChiTu. The sixteen OTKROCs in the FE board share two downstream links used to provide the OTKROCs with configuration, synchronization. In order for various OTKROCs to share the

configuration downlinks, the configuration protocol includes a 4-bit address. Each OTKROC chip is given its 4-bit address though dedicated ID pins in the chip, which can be connected to a jumper or hardwired in the PCB. To implement reliable reception of the downstream links from the TaoTie, the OTKROC chip can use either the falling edge or the rising edge of CLK to latch the input signals.

1.3.2.2 Concentrator card and power distribution

The Concentrator Card is designed to interface the system readout with four FE boards. Its location with respect to the sensor modules, cooling bar, and FE boards on the barrel or endcap tray. The CC uses the ChiTu to provide an interface between E-links and an opto module. Each opto module has a single channel receive and a single channel transmit. The command downlink (receive) will be at 2.771 Gb/s and the data uplink will be at 11.093 Gb/s. The average rate of each data link from the FE board is 500 Mb/s. This translates to an aggregate rate of about 2 Gb/s, which can be transmitted by one ChiTu at its lower output bandwidth of 5.542 Gb/s. Another important feature of the ChiTu is to ensure the precise clock distribution, received from the downlink, to the front-end system, achieved by the high frequency clock noise filter in the PLL. The power is distributed from the DC-DC converter module BaSha, which is a step-down converter module with a radiation tolerant ASIC. To power the CC components as well as the FE cards, two other kinds of converters are needed. The BaSha1 converts 48 V to 12V on CC. The BaSha2 converts 12V to 1.2V for frontend ASIC on FE board, or 3.3V for VCSEL driver on CC. For the full channel capacity, we will use two BaSha's for reliability on FE.

1.3.2.3 Slow control and monitoring

The ChiTu provides a set of slow control and monitoring features, I2C master controllers, JTAG master controller, programmable and bidirectional IO ports, memory-like bus master controller with data and address. The preliminary of slow control and monitoring functions are following:

1. Slow Control bits
   (a). powering control bits
   (b). configuration bits of frontend ASIC
2. Monitor
   (a). DC-DC status
   (b). ASIC status
   (c). temperature on FE
   (d). temperature on CC
   (e). leakage current of LGAD

1.3.2.4 Clock distribution

The distribution of a precise clock to the front-end is a major requirement for OTK. The clocks in the backend system are recovered from the ChiTu down links. The clock is synchronized to the 43.3MHz frequency bunch crossings rate. In order to achieve the target timing performance, the clock distribution system should have less than 15 ps rms link-to-link jitter over all clock distribution links. For instance, a 50 ps timing performance obtained from the sensors and readout electronics would be degraded by 2.2 ps by a clock distribution system with 15 ps rms jitter. The high frequency clock noise is expected to be filtered by the PLL in the ChiTu. Low frequency clock jitter and possible phase instability, in particular arising from temperature variations or low frequency response of the clock chain, will require special attention.

1.3.2.5 OTK readout ASIC

This section describes the required performance, design, and latest prototype testing of the ASIC chip, which will have 128 readout channels in future. The main challenge in the design of this ASIC is a high time resolution for time measurement and charge resolution for position, in order to match the excellent performance of the LGAD. The time contribution comes mainly from the jitter and the time walk. The most critical aspect concerning the jitter is the design

of the analog front-end electronics, which are composed of a transimpedance amplifier followed by a shaper and a fast discriminator. The measured time-of-arrival (TOA) and time-over-threshold (TOT) are digitized using two time-to-digital converters (TDCs), and stored in a local memory at the channel level. The TOT can be recognized as charge because the charge is related to the time over a certain threshold. The charge resolution is determined by time resolution and TOT width. The contribution of time walk will be addressed by applying a correction based on the fact that the variations in the TOA of the pulse are related to the TOT. The ASIC common digital part is composed of clock generator and alignment, slow control configuration and data transimission. A prototype chip has been produced and will be tested so far: OTKROC, integrated 8 channels, with the preamplifier and the discriminator, TDC and digital components. The chip will be test in the end of 2024.

The requirements imposed by the data taking conditions, the sensor and the targeted performance are presented first in Section 3.1. The ASIC architecture is described in Section 3.2, first going through the single-channel architecture and then the entire ASIC. Section 3.3describes in detail the design of the single-channel readout electronics, followed by the description of the ASIC common digital part in Section 3.4. The radiation tolerance is described in Section 3.5 and the power distribution in Section 3.6 The performance results obtained so far in test bench and test beam are described in Section 3.7. The description of the monitoring can be found in Section 3.8. Lastly, a brief account is given of the future steps towards the completion of the design and testing of the ASIC in Section 3.9.

1.3.2.5.1 General requirements The requirements of the ASIC can be divided into two types. On one side the considerations regarding the operational environment of the ASIC, its powering and electrical connections. These requirements are summarized in Table 3.1. The second group concerns the ASIC performance, driven by the targeted time resolution. A summary of these requirements is presented in Table 3.2.

i) The target for the electronics is to be able to read out signals from 16 fC up to 50 fC throughout the lifetime.

ii) Each readout channel needs to match the sensor strip, with a pitch of 100μm. It will be capable of handling up to 5μA leakage current from the sensor.

iii) The electronics jitter is required to be smaller than 30 ps for an input charge of about 16 fC, that is smaller than intrinsic dispersion of LGAD. A detector capacitance of about 4 pF is considered. The TDC bin size for TOA measurement should be less than 30 ps, thus the contribution from TDC will be negligible. The time walk should be smaller than 10 ps over the dynamic range after correction.

iv) The charge measurement is applied by TOT measurement. A resolution of 1.6 fC is necessary for a special resolution of 10μm. The bin size for TOT will be the same as TOA, thanks to the reusing of delay chain.

v) The TOA and TOT information are transferred to the data acquisition system, therefore integrating the protocol of data aggregation is necessary.

vi) The charge generated by MIP will be shared by adjacent strips, it should be possible to set the discriminator threshold for small enough values of input charge. The minimum threshold (4 fC) should provide an efficiency above 95% for an input charge of 16 fC. The cross-talk between channels should be kept below 10 %, to enable the possibility to set such low thresholds.

vii) The ASIC will have to withstand high radiation levels. The expected radiation levels have been presented before, considering a safety factor for the electronics leading to a maximal TID of ? MGy

Table 1.2: Geometrical, environmental, electrical and power requirements for the OTK ASIC

Voltage	1.2V
Channel	128
Channel pitch	100 μm
Power dissipation per area (per ASIC)	300mW/cm2
e-link driver bandwidth	320 Mbps, 640 Mbps, or 1.28 Gbps
Temperature range	40 C to 40 C
TID tolerance	1.0 MGy

The values given for the noise, minimum threshold and jitter have been specified considering a detector capacitance

Table 1.3: Performance requirements for the OTK ASICC

Maximum leakage current	5μA
Single channel noise (ENC)	10000 e = 1.6 fC
Cross-talk	10%
Threshold dispersion after tuning	10%
Maximum jitter	30 ps at 16 fC
TDC contribution	30 ps
Time walk contribution	10 ps
Minimum threshold	4 fC
Dynamic range	16 fC–50 fC
TDC conversion time	23 ns

Cd = 4 pF.

1.3.2.5.2 Data transmission bandwidth requirements The required bandwidth of the readout e-link of each ASIC strongly depends on the radial region it covers at barrel or endcap, as shown by the distribution of the average number of hits per ASIC in Figure ?. The number of bit per hit is 48 as described in Section ?. Each module consisting of 2 slides of sensors, and each sensor needs 8 ASICs to readout. 16 ASICs are on one FE board, and are connected to a aggregation chip TaoTie. 4 FE boards connect to a Concentrator Card (CC) via flex cables and connectors. The CC transfers digital signals from the flex cables to optical fibers connected to the back-end DAQ. A dedicated buffer is needed in each ASIC to average the rate variation and match the best speed of the ChiTu transceiver inputs:

1. The largest average hit rate at small radius does not exceed 20 hits per ASIC and per event, equivalent to a rate of 500 Mbps (not including header). In the current design a bandwidth of up to 1.28 Gbps was considered for the innermost radius ASICs.
2. For the barrel, taking into account a considerable safety margin, a 160 Mbps bandwidth can be used. For the innermost radius ASICs at endcap, a 640 Mbps e-link driver is needed.

1.3.2.5.3 ASIC architecture Building on the preliminary results of LGAD, an ASIC, the Out Tracker Read-Out Chip (OTKROC), is proposed to be developed in a CMOS technology. OTKROC includes 128 channels. The height of each channel should be less than 100um, which matches the pitch of the LGAD strip. Each channel in OTKROC has a preamplifier, a discriminator, and a time-to-digital converter (TDC) for the Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements. The preamplifier and discriminator are most critical parts for the contribution of jitter. The TOT is used to calculate the charge as well as to correct the time walk due to the charge Landau distribution in LGAD. The power consumption of OTKROC must stay below 2.5 W per chip, which means 20 mW per channel, constrained by the system cooling capacity. This value translates to a power budget of 15 mW for the front-end analog readout circuits in each channel. The time resolution of the Out Tracker is determined by the LGAD sensor and OTKROC together. The LGAD sensor has a jitter of about 40 ps due to non-uniform charge deposition. The OTKROC contribution should be below 30 ps to achieve 50 ps overall time resolution per hit. The Most Probable Value (MPV) of the charge from the LGAD sensor is around 16 fC. Considering the charge sharing with adjacent strips, the expected operating range of the charges is 8–50 fC. Due to such a small signal from the LGAD sensor, the analog readout circuits, including the preamplifier and the discriminator, dominate electronics' jitter contribution and are critical for the Out tracker precision timing performance.

1.3.2.5.4 Preamplifier The preamplifier consists of two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower (M3) as the second stage. The bias current of the input transistor (M1) has two components: the constant current IB1 is small due to that the VGS of M2 should not be too large. The transistor M2 and its gate voltage Vb set the DC operating point of M1. Vb is the replica bias voltage from IB1. The gain and bandwidth depend on the Gm of transistor M1. Most of the current of M1 is provided by a tunable IB2. The feedback resistor Rf is programmable to adjust the gain of the preamplifier. The load capacitance CL of the first stage is also programmable to optimize the bandwidth. The drain current IB3 of M3 is generated by a resistor. The gain of the first stage and the second stage are

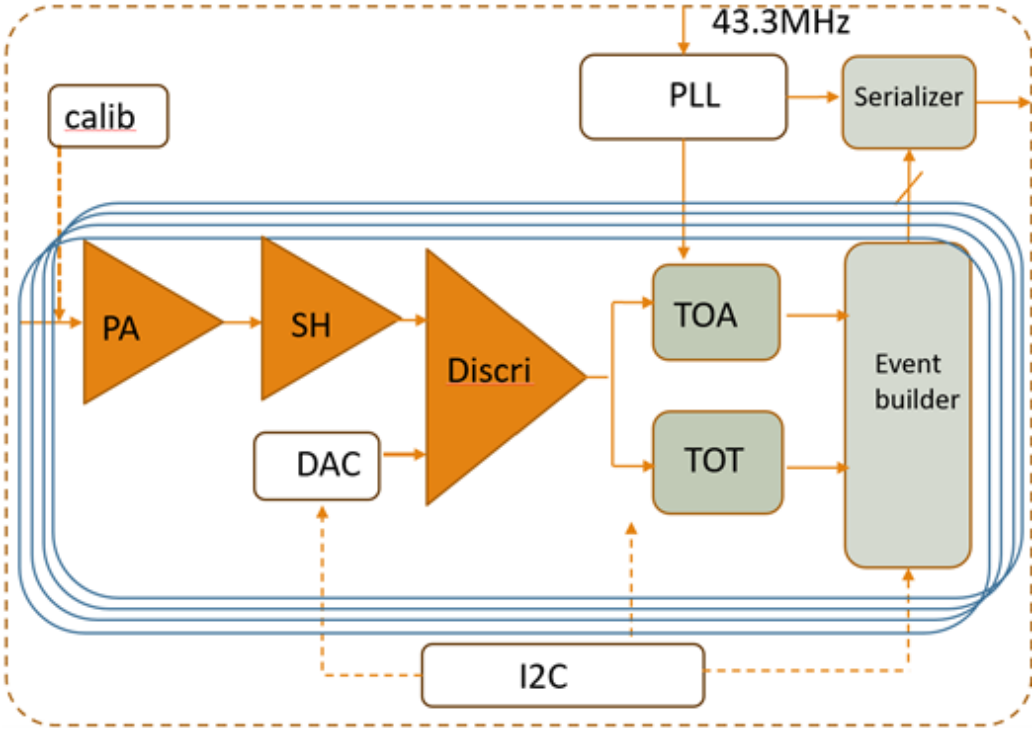


Figure 1.3: Single-channel readout electronics

negative and positive, respectively. Since the preamplifier's input signal is a negative pulse, the output signal is a positive pulse, whose rise edge is the leading edge and falling edge the trailing edge. Both the leading and trailing edges of the preamplifier should be considered. A faster leading edge can be achieved with a higher bias current of M1 and a smaller load capacitance of CL. When the IB2 is biased to its highest value, the preamplifier output's leading edge time can be set to several 1ns with a bandwidth of 400MHz. Small load capacitance leads to a fast leading edge but introduces more noise because of the large bandwidth. Therefore, the load capacitance can be selected to fine-tune the jitter. The default setting is to use the smallest load capacitance. The time constant, the product of the total capacitance Cs and the input impedance Rin, determines the trailing edge time of the preamplifier output. The input impedance should be considered because the 4 cm strip is a transmission line to a signal with a leading edge of 1 ns. The input impedance Rin is given by the feedback resistance Rf divided by the open-loop gain. The open-loop gain depends on the bias current. Thus, Rf is programmable with four settings to adjust the gain, the trailing edge time of the preamplifier output and input impedance. Based on the simulation with LGAD signals, a default feedback resistor will be selected. The bias current IB2 allows different trade-offs between the power consumption and the timing performance. A larger signal slew rate (dV/dt) and a faster rise time of the preamplifier output tr can be achieved at a higher bias current, and thus the better performance is expected.

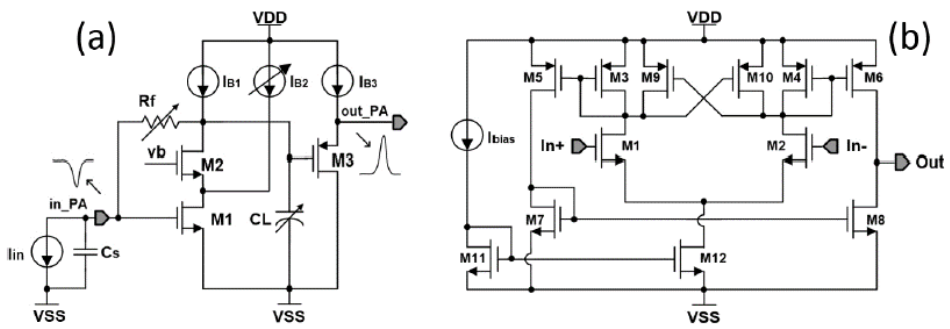


Figure 1.4: OTKROC schematic

1.3.2.5.5 Discriminator The discriminator consists of three stages of fully differential amplifiers, a comparator, and an internal buffer. The three stages of amplifiers receive the small input pulses, and generate the larger pulses comfortable for the comparator. The overall gain for three stages of amplifiers will be 20-40 dB with a bandwidth of around 400 MHz. The comparator discriminates the differential input at the crossing point with programmable hysteresis. The internal buffer delivers the digital output to the following circuits. The internal buffer is composed of two CMOS inverters and relieves the loading pressure. As shown in figure ?, the comparator has two stages: The first stage is a common-source differential amplifier of high gain with the MOSFET pair M1 and M2. The loads is comprised of a transistor pair M3 and M4, which are diode-connected PMOS. M11 and M12 provide the bias current with a source current Ibias, shared with the three-stage amplifiers. The first stage digitizes the differential input at the crossing point with a tunable hysteresis. The hysteresis is used to alleviate ringing due to noise and generated by the transistors M9 and M10. The second stage converts the differential output of the first stage into single-ended. The leading edge of the discriminator output provides the TOA, while the trailing edge, combined with TOA, provides the TOT. The discriminator threshold is connected to the inverting input and set by an internal 10-bit DAC. The DAC is comprised of a global 6bit DAC and a local 4 bit DAC in each channel. Since the preamplifier's baseline varies for different channels with temperature, bias setting, and irradiation. The DAC output range is from 0.6 to 1 V with an LSB (Least significant bit) of 0.4 mV. A reference voltage generator provides a 1 V reference voltage to the DAC. To minimize the DAC noise contribution to threshold, a RC filter is added to the DAC output.

1.4 Global architecture (Wei Wei)

1.4.1 Consideration on readout strategy (Wei Wei)

As a next-generation large collider experiment electronics system, to design all front-end electronics subsystems according to a unified system specification, to ensure that their data interfaces, power interfaces, etc., are supplied in a uniform manner, and furthermore, to make the backend electronics able to receive data, perform slow control, and configure the front-end electronics of each subdetector in a unified interface, and further communicate with the TDAQ system, will significantly enhancing the unity of the electronics system. This will not only facilitate the unified design and management of different subdetector systems but also enable the entire electronics system to be designed with a certain degree of maximized commonality. That is, based on the different scales of subdetectors, achieving modular design of subdetector electronics can be relatively easy by simply increasing the number of common generic modules accordingly.

To achieve this design style, it is necessary to first determine the overall strategy of the electronics and TDAQ systems. In other words, it is essential to clarify whether the electronics and TDAQ systems adopt a front-end trigger scheme or are based on a front-end triggerless readout scheme.

Table 1.4: Comparison of the FEE-Triggerless readout and Trigger readout strategy

Characteristics	FEE-Triggerless	FEE-Trigger	Superiority
Where to acquire trigger info	On BEE	On FEE	
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	FEE-Triggerless
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	
Maturity	Mature but relatively new	Very mature	FEE-Trigger
Resources needed for algorithm	High	Low	
Representative experiments	CMS, LHCb, . . .	ATLAS, BELLE2, BESIII, . . .	

Table 1.4 provides a general comparison of the two typical trigger readout schemes. It can be seen that the front-end trigger-based approach is relatively traditional. In this method, while the front-end electronics of the detector process the

detector signals, they also need to extract key information usable for triggering from the detector signals and send it to the trigger system. At the same time, detector data needs to be cached in the front-end electronics. Once the trigger system receives the key information, it generates trigger decision information based on the physics model and corresponding trigger algorithms, which is then sent back to the front-end electronics. The front-end electronics compare the cached data with trigger decision information to extract valid physical events and send them to the backend electronics, which further routes them to the data acquisition system.

On the other hand, the backend trigger-based approach involves digitizing the detector signals in the front-end electronics and directly transferring them to the backend electronics for caching. The trigger system only communicates with the backend electronics, and the extraction of detector valid events is done solely in the backend electronics and trigger system. The comparison in Table 1.4 shows that these two main electronics frameworks have their own advantages and disadvantages without a clear superiority. In typical applications, they are supported by various large particle physics experiments such as CMS, LHCb, as well as ATLAS, BELLE2, BESIII, respectively.

The traditional front-end trigger scheme effectively eliminates detector background, reduces pressure from data transmission bandwidth, but also increases the demand for front-end electronics data caching capacity. It usually allows only short trigger delays, requires faster trigger decision speeds, and simpler trigger algorithms. On the other hand, the front-end triggerless readout method reduces the design complexity of front-end electronics by eliminating trigger-related logic. However, since detector background and valid events are both read out together, it increases the pressure on front-end data transmission. Nevertheless, with improved processing capabilities and cache space in the backend electronics compared to the front-end electronics, the front-end triggerless readout scheme can also implement relatively complex trigger algorithms. This reduces the requirements for trigger delay and trigger system design, making pure software triggering possible. In China's collider spectrometer experiments represented by BESIII, the front-end trigger-based approach is commonly adopted. Non-collider experiments represented by JUNO and LHAASO generally explore front-end waveform sampling schemes, but overall, the implementation of trigger algorithms still follows relatively traditional approaches such as data compression and detector information extraction.

Considering the physical goals and project timeline of CEPC, the electronics-TDAQ framework based on front-end triggerless readout scheme has been selected as the reference strategy for the electronics system of CEPC. At the same time, the traditional framework based on front-end trigger readout will serve as a backup plan for the electronics system. This choice is made based on the following considerations:

i) Considering that CEPC will serve as a discovering machine, choosing a front-end triggerless strategy can retain the maximum possibility of exploring new physics, as all raw information from the detector, including background and signals, will be fully read out. Once a front-end trigger is adopted, the trigger strategy will typically be fixed at some extent, usually based on known physics processes, potentially leading to the abandonment of unknown physics processes. Additionally, because front-end triggerless electronics do not require pre-condition judgments, they are also well-suited for future detector upgrade planning, usually only requiring upgrades to the signal processing and readout capabilities of the front-end electronics to meet the new requirements of the detector; in contrast, if a front-end trigger strategy is adopted, new trigger strategies may need to be considered, potentially leading to a redesign of the front-end electronics.

ii) Based on the above considerations, the triggerless strategy at the front-end will also effectively accelerate the process of ASIC iteration and qualification. Under this strategy, the front-end ASIC only needs to consider information related to detector detection and background, and provide output data rates, then all key interface parameters will be determined. On the other hand, ASICs based on front-end trigger strategy also need to consider related on-chip trigger algorithms, trigger information output, and trigger-compliant readout designs, which are often difficult to finalize in the early stages of detector overall design, inadvertently increasing the number of ASIC design iterations significantly. The introduction of new digital module design in front-end ASICs will also increase the risk of potential bugs. Considering the possible construction timeline of CEPC, rapidly completing the design, iteration, and qualification of ASICs, and completing the prototype design of the detector within a limited time frame, is undoubtedly the most suitable strategy for achieving the engineering goals of CEPC.

iii) The triggerless front-end electronics readout framework also maximizes the versatility of the electronics system

design. Due to the unified interface between front-end electronics and back-end electronics of different sub-detectors under this framework, a common data interface design can be adopted to achieve the transmission of front-end data to back-end electronics. This data interface does not need to consider the specific trigger inputs and outputs of different sub-detectors, but only the common high-speed data transfer characteristics, clock distribution characteristics, slow control, and BCID, etc. Furthermore, in this framework, trigger-related algorithms will only be implemented in the FPGA devices of the back-end electronics and trigger system, and the online programmable feature of FPGAs allows their algorithms to be adjusted as needed, achieving detector independence. This also allows the back-end electronics and trigger system to be implemented in a similar manner with common back-end PCBs and common trigger PCBs. It is only needed to scaled the number of common PCBs according to the data volume of different sub-detectors to meet the readout requirements of all sub-detectors. This greatly simplifies the overall design and management of the electronics system, allowing the electronics of different sub-detectors to be unified in a top-down manner, without the need for customized designs of the electronics system for different sub-detectors as in traditional front-end trigger schemes.

iv) The key premise that can be achieved by the triggerless scheme is that the readout capability of the front-end electronics is sufficient to read out all data, including background and critical detector information. As shown in Table 1.1, based on the preliminary design of the front-end ASICs of various sub-detectors and the background evaluation of the MDI system, the expected data rates of the common data interface corresponding to detector module are generally below 8Gbps. Considering the use of balanced encoding for high-speed data transfer, even with the relatively large overhead of 8b10b encoding, the output data rate is within 10Gbps. Referring to the commonly used lpGBT interface chips, this data rate falls within the typical interface capabilities using optical fibers as the transmission medium. Even for typical high data rate detectors represented by vertex detectors and electromagnetic calorimeters, the data interface corresponding to the optical fiber channels can be increased by using MTX module, without significantly increasing the interface size (it can be referenced in Section 1.5.1). This will allow the maximum possible data rate of the detector module to reach 40Gbps, equivalent to an effective data rate of 32Gbps. Even considering the future High LumiZ working environment, there is ample capacity and flexible upgrade room in the readout capability. This makes the adoption of a triggerless readout scheme at the front-end feasible under the necessary conditions.

1.4.2 Baseline architecture for the Electronics-TDAQ system (Wei Wei)

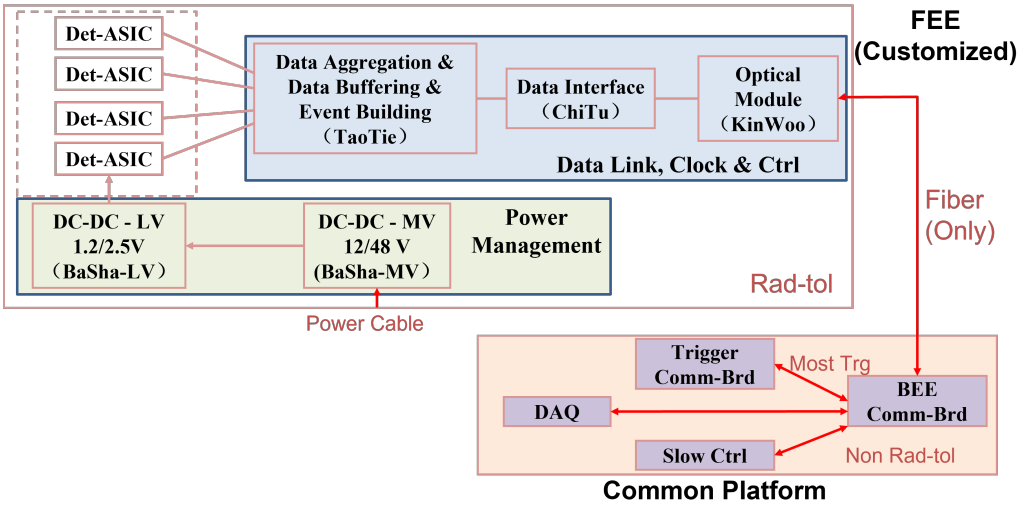


Figure 1.5: Global Framework of the Electronics-TDAQ System of CEPC

Figure 1.5 presents the electronic system architecture based on the considerations above, which is built on a front-end triggerless readout scheme. The electronic system can be divided into two main parts: customized front-end electronics and a common platform. Customized front-end electronics are designed according to the specific requirements and layout of

each subdetector system, as described in the corresponding sections. However, to maximize versatility, only the front-end readout ASIC responsible for triggerless readout of detector signals and backgrounds is fully customized. The data interface and power supply systems following it are implemented based on a common platform. The data interface platform initially receives multi-channel relatively low-speed data from the front-end ASIC by the data aggregation chip TaoTie, aggregates it into high-speed serial data, encodes the data through the data interface chip ChiTu, and finally converts the high-speed electrical data flow from ChiTu into optical signals using the optoelectronic module KinWoo. The optical signals are then transmitted through optical fibers to the common back-end electronics, completing the front-end data transmission chain. The detailed design of this part will be discussed in Section 1.5.1. The front-end power module efficiently converts external high-voltage power supplies into the required power voltages for the front-end chips, with detailed design covered in Section 1.5.2. According to the previous plan, the back-end electronics and trigger system can be implemented using a common PCB approach, which is scalable based on the data volume of different subdetector systems to achieve the overall design. Within this framework, all trigger signals are transmitted between the common back-end board and the common trigger board, allowing flexible trigger algorithms to be implemented based on the physical objectives.

The benefit of dividing the electronics system into customized front-end electronics and a common platform is that the front-end electronics can be fully ASIC-based, achieving the goal of radiation tolerance design. By transmitting front-end data through optical fibers to the back-end electronics, the common platform can be placed in shielded environments further away from the collision point, enabling the utilization of high-performance commercial devices without the need for radiation tolerance considerations.

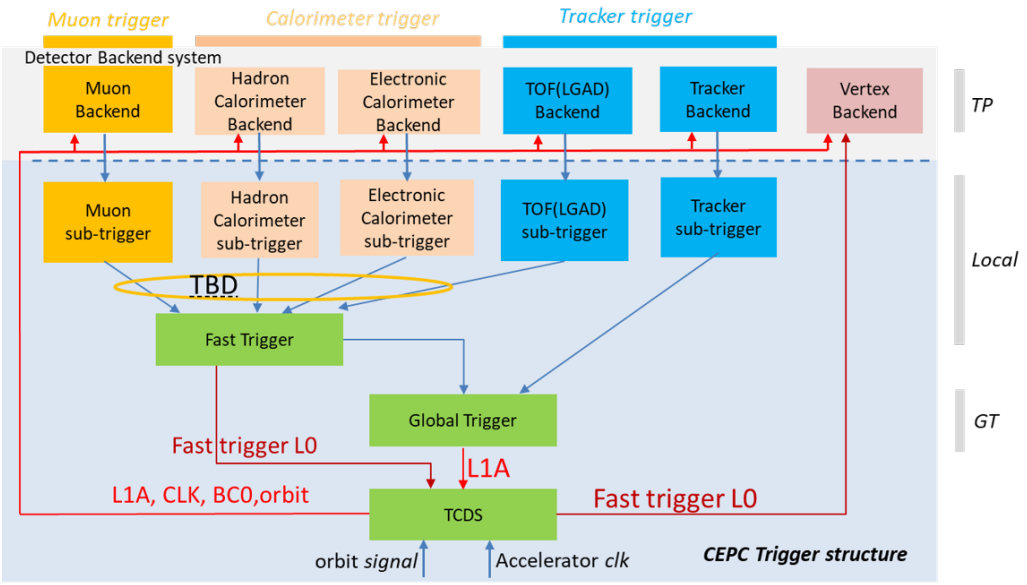


Figure 1.6: Backup Plan for the Global Framework of the Electronics-TDAQ System of CEPC

As a backup plan for triggerless front-end readout, it is a reasonable choice compared to the traditional front-end trigger readout scheme, as shown in Figure 1.6. With the continuous optimization of detector design and MDI background assessment, it is possible that the final detector background will exceed the rated transmission capability of the common data interface. In this case, the front-end electronics can still be gradually adjusted to return to the backup plan of front-end trigger readout. The specific plan is as follows:

i) When the detector background data rate exceeds the transmission capability of the fiber interface in the preliminary plan, additional fiber channels can be added to the MTX fiber interface, with each effective data rate of 8Gbps, to achieve a maximum data interface transmission capacity of 32Gbps.

ii) When the data rate levels of certain detector modules still exceed the above data rate limits, advanced data compression algorithms can be deployed in the front-end ASIC chip, such as extracting key information about hit clusters in the track and reducing redundant timestamp information output and so on, thereby reducing the data rate levels at the front end.

iii) When the above optimization schemes still cannot meet the data transmission requirements, adding a Fast Trigger

interface to detectors with data transmission bottlenecks (typically the Vertex Detector) can be considered, targeting only this specific detector to return to the traditional trigger mode: the front-end chip first buffers the detector signals and background data; in order to limit the front-end chip buffer space to a reasonable range, the trigger system needs to generate relatively rough fast trigger arbitration information as quickly as possible and send it to the front-end chip through a dedicated channel; after the front-end chip receives the trigger signal, it compares the buffered data with the fast trigger information, and finally transmits the preliminary arbitrated data to the back-end electronics. This approach can effectively reduce the front-end data rate, but it will require a relatively reasonable fast trigger algorithm based on detector optimization and physical objectives. Further details on this part will be discussed in the relevant sections of the trigger system.

1.5 Common Electronics interface

1.5.1 Data interface (Di Guo, Xiaoting Li, Jingbo Ye)

1.5.1.1 General requirements and overall architecture

Table 1 Requirements

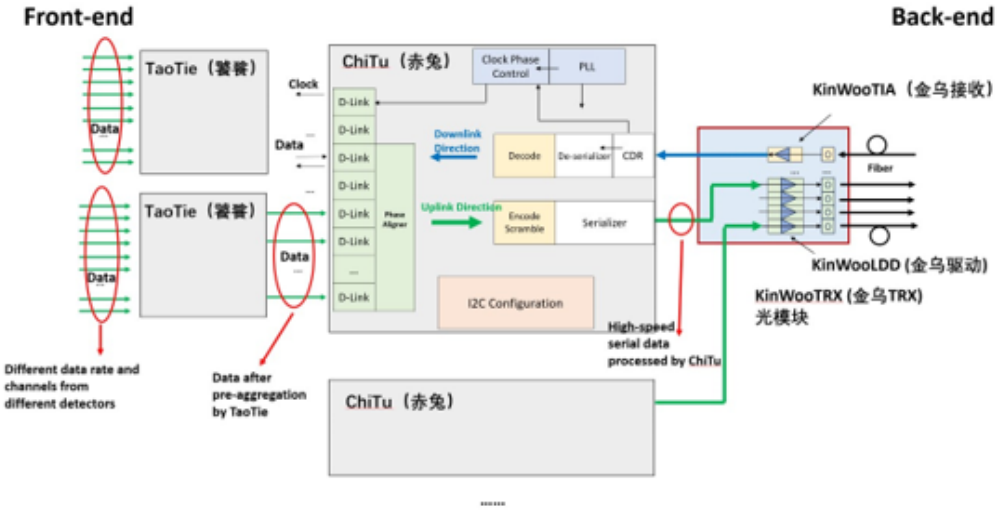


Figure 1.7: Overall architecture of the data interface

Figure 1.7 shows the overall architecture of the data transmission interface, comprising four ASICs and an optical module. The ASICs include TaoTie, ChiTu, KinWooLDD, and KinWooTIA, while the optical module, KinWooTRX, consists of four KinWooLDDs, four KinWooTIAs, and VCSEL and LD arrays. TaoTie functions as a data pre-aggregation ASIC for multiple channels of readout electronics in different sub-detectors. ChiTu serves as a bi-directional data transceiver with both an uplink and a downlink. The uplink receives data post pre-aggregation, performs encoding, serialization, and transmits the data to KinWooTRX. The downlink receives clock and slow control signals, performs de-serialization, decoding, and transmits data to blocks on-ChiTu and others off-ChiTu. KinWooLDD and KinWooTIA are optical drivers and receivers designed specifically for the VCSEL and LD arrays, respectively. They will be integrated and assembled within the optical module.

1.5.1.2 Optical data transmission ASICs

1.5.1.2.1 TaoTie: Front-end data pre-aggregation TaoTie employs a self-compatible scheme to handle a variety of data channels and rates from front-end sub-detectors. Basically, each TaoTie can serialize a maximum of 16 channels into 1 channel, with configurable modes allowing for 2, 4, or 8 channels to be serialized into 1 channel. Moreover, an N-stage TaoTie can serialize 16N channels into 1 channel. Based on the current requirements, it is likely that 2 stages will be

sufficient. The ultimate serial output data rate should align with the input data rate requirement of ChiTu, which is 1.3856 Gbps based on the 43.3-MHz system clock.

1.5.1.2.2 ChiTu: Bi-direction data interface ChiTu primarily comprises a flexible high-precision clock system, a high-speed serializer, de-serializer, data builder, configuration capabilities, and monitoring. The 8-channel data at 1.3856 Gbps received from TaoTie is processed by D-links in ChiTu. It undergoes alignment by phase aligners, encoding, DC-balancing by a data builder, serialization to a data rate of 11.0848 Gbps, and is ultimately transmitted to KinWooTRX.The high-quality clocks imperative for the serializer are generated by an LC phase-locked loop (PLL), which can also offer several configurable output frequencies and phases externally. The de-serializer in ChiTu receives control signals, including fast command, at a data rate of 2.7712 Gbps. The circuit recovers data and clock signals through an integrated clock data recovery (CDR) mechanism.

Table x. Operation modes (Data rate supports)

1.5.1.2.3 KinWooLDD: VCSEL array driver KinWooLDD is a four-channel vertical-cavity surface-emitting laser (VCSEL) driver. Each channel mainly comprises an input equalizer stage, a pre-driving stage, and an output-driving stage. The pre-driving stage is composed of four stages, with two stages sharing an inductor to enhance bandwidth beyond 10 GHz. The output driver receives fast wide-swing differential signals from the pre-driver and converts them into single-end current to drive the VCSEL. This design enables achieving a transmission data rate of up to 14 Gbps in a 55-nm technology, meeting the current data transmission requirement of the CEPC (11.0848 Gbps per fiber). To increase the driving bandwidth further, active-feedback and feed-forward equalizer (FFE) pre-emphasis techniques can be implemented in the pre-driver and output driver, respectively.

1.5.1.2.4 KinWooTIA: VCSEL receiver KinWooTIA is a four-channel photodiode (PD) receiver with a data rate capability exceeding 2.7712 Gbps or 5.5424 Gbps per channel for standard and enhanced requirements, respectively. Each channel consists primarily of a transimpedance amplifier (TIA), limiting amplifier (LA), and driver stage.

1.5.1.2.5 KinWooTRX: Optical module KinWooTRX is an optical module consisting of a KinWooLDD, a KinWooTIA, a four-channel VCSEL array, a four-channel PD array and a carrier board for the optocoupler devices. The height requirement is xxx mm.

1.5.1.3 Prototype performance

Prototype circuits have been developed to assess functionalities and performance. Figure x.2 illustrates the block diagram of the BDTIC (bi-direction transceiver integrated circuit) chip, which is a prototype design of ChiTu. Figure x.3 presents the test platform comprising a test board with a wire-bonded BDTIC die, a clock board, power supplies, an oscilloscope, a spectrum analyzer, a bit error rate tester (BERT), and a computer. Figure x.4 shows measured performance including jitter and phase noise performance of the PLL (as shown in (a) and (b)), jitter and phase noise performance of the CDR recovered clock (as shown in (c) and (d)), and eye diagrams of the serializer and de-serializer (as shown in (e) and (f)). The results indicate that the building blocks meet the characterization requirements of ChiTu.

1.5.1.4 Clock blocks (PLL, CDR, Phase aligner. . .)

1.5.1.4.1 SerDes blocks

1.5.1.4.2 Optical data interface

1.5.1.4.3 Periphery blocks (SPI, I2C. . .)

1.5.1.4.4 Irradiation tests

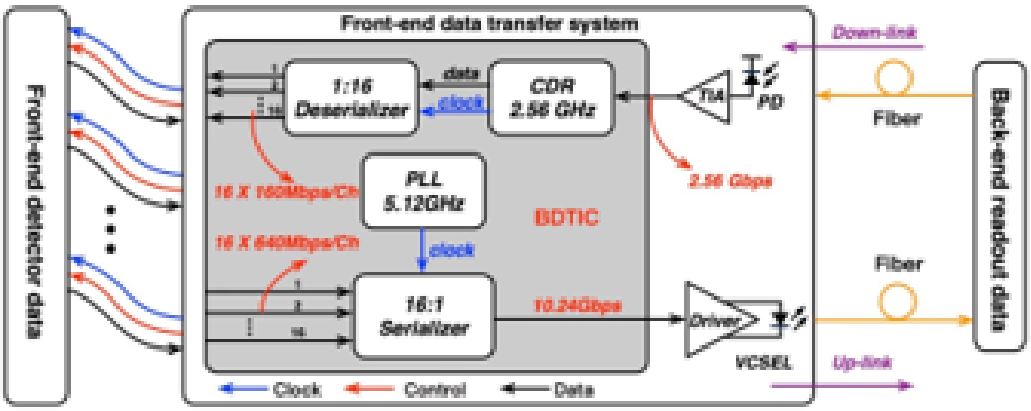


Figure 1.8: Block diagram of the prototype BDTIC chip

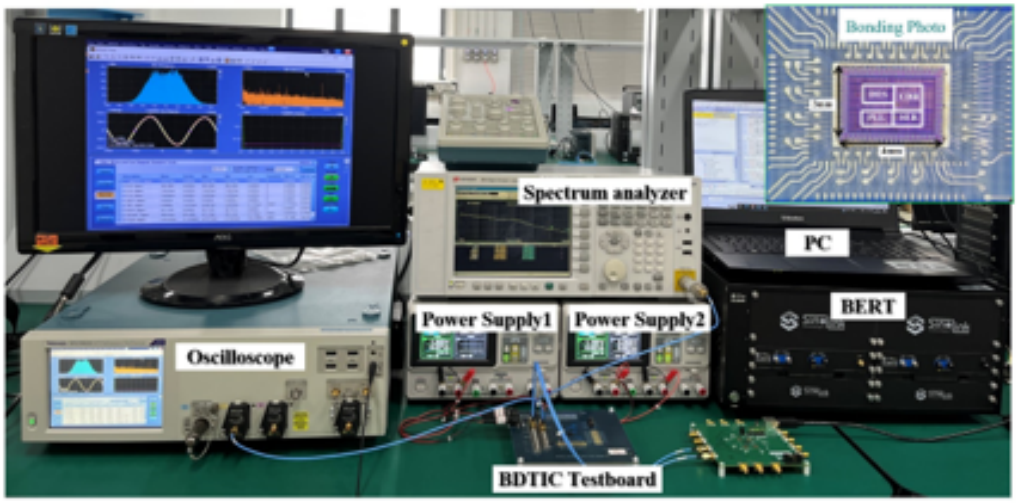
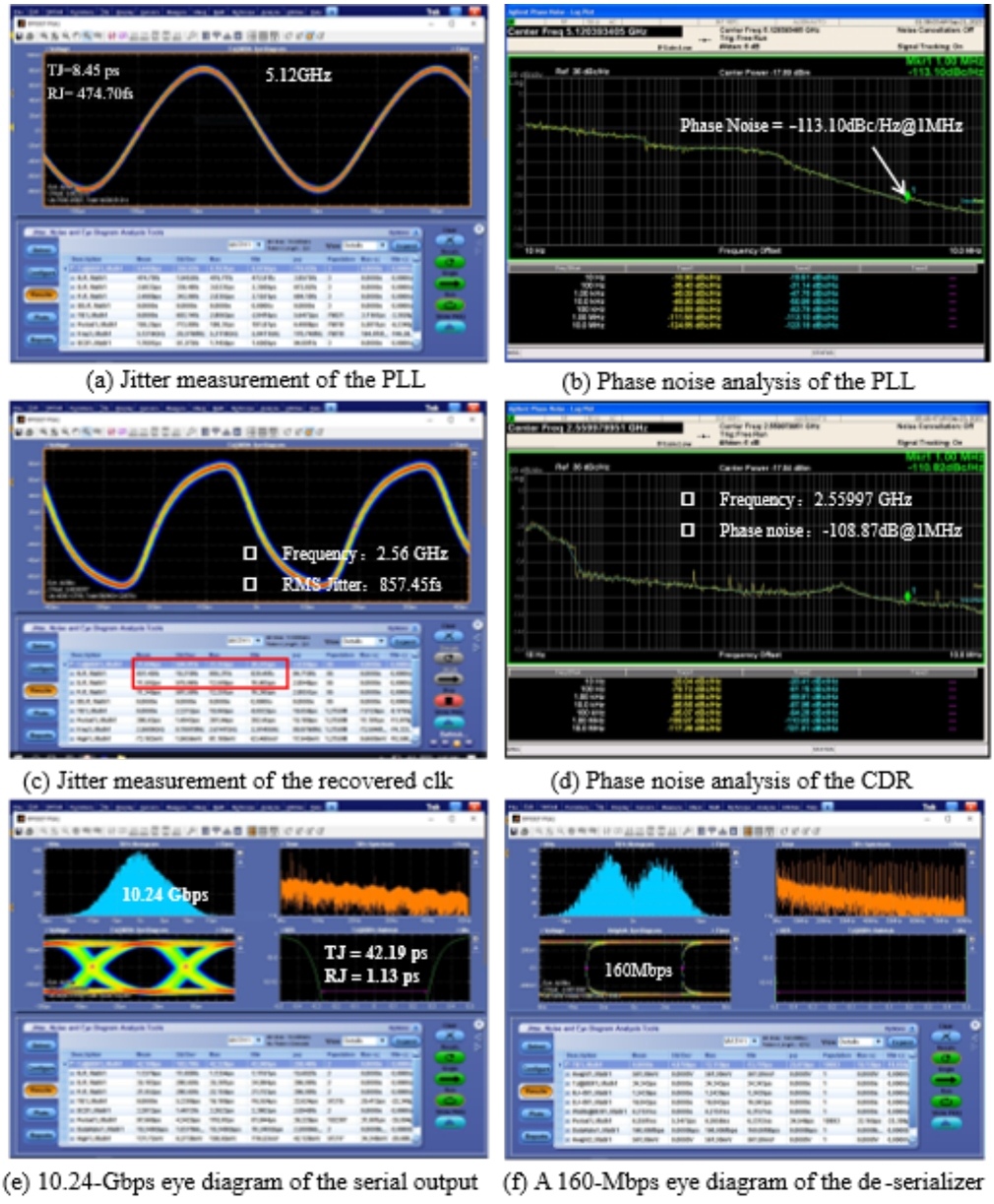


Figure 1.9: Test platform of the BDTIC chip



(a) Jitter measurement of the PLL (b) Phase noise analysis of the PLL

(c) Jitter measurement of the recovered clk (d) Phase noise analysis of the CDR

(e) 10.24-Gbps eye diagram of the serial output (f) A 160-Mbps eye diagram of the de-serializer

Figure 1.10: Performance measurements of the BDTIC chip

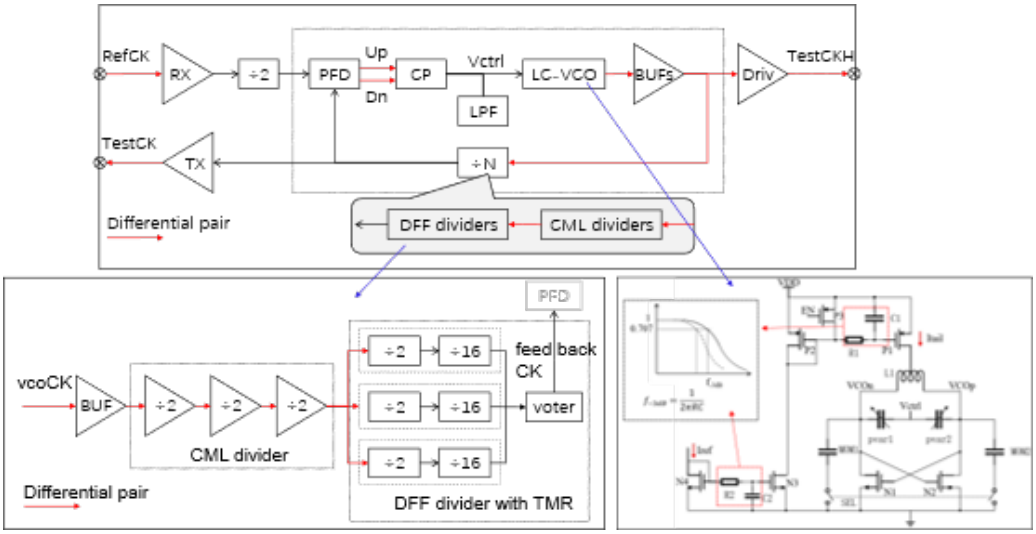
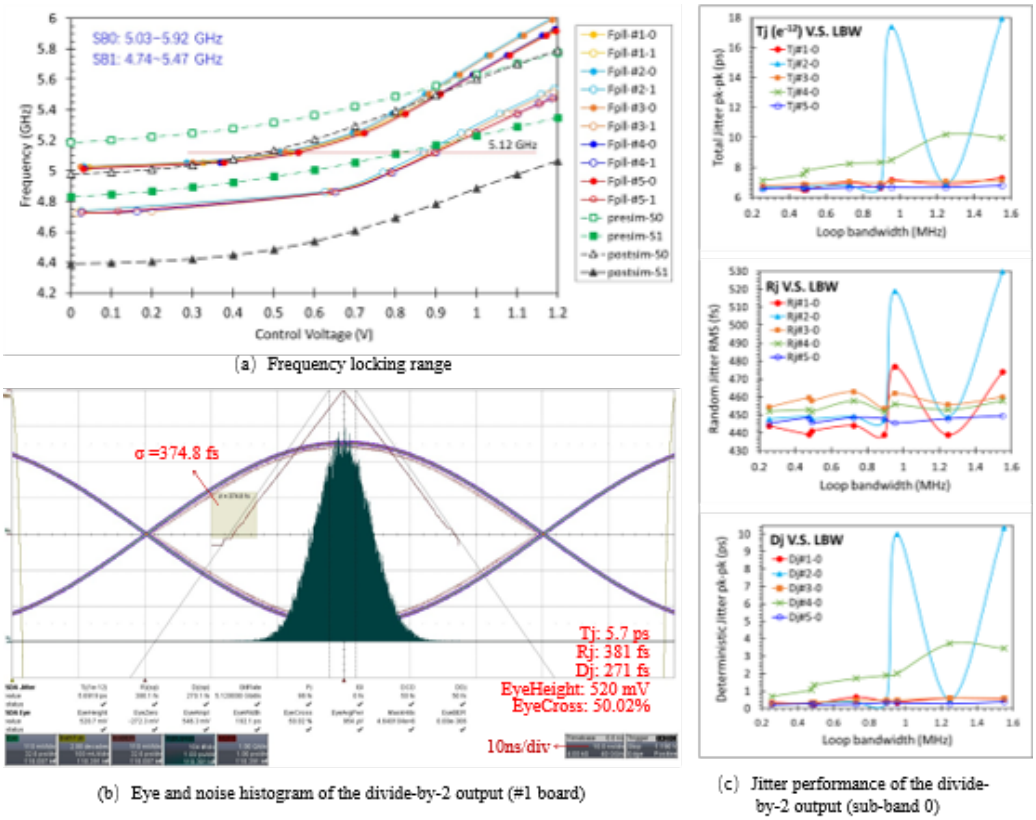


Figure 1.11: PLL schematic



(a) Frequency locking range

(b) Eye and noise histogram of the divide-by-2 output (#1 board)

(c) Jitter performance of the divide-by-2 output (sub-band 0)

Figure 1.12: PLL schematic

1.5.1.5 . . . Package? Power consumption?

1.5.1.6 Roadmap towards production

1.5.2 Power module (Jun Hu, Jia Wang, Jingbo Ye)

1.5.2.1 Power supply distribution

1.5.2.1.1 Power supply distribution overview The power supply is a crucial element in electronic systems, as it has a direct impact on their overall performance and functionality. Figure 1 provides a visual representation of the power distribution scheme for the CPEC low-voltage supply system.

In the electronics room, which does not necessitate radiation and magnetic protection, both the COTS (Commercial Off-The-Shelf) AC-DC power supply and a custom-designed DC-DC converter are housed. The DC-DC converter is specifically engineered to step down the voltage from 110V to 48V, supplying the necessary power for various components within the system.

To support the frontend detectors, lower voltage levels are required, specifically 1.2V for the analog readout chips and 2.5V for the digital transmission chips. These low voltages are critical for the operation of the frontend boards, which form part of the detector readout electronics. These boards are typically installed in environments that are subject to radiation and magnetic, making it essential for them to not only receive appropriate power levels but also to be designed and shielded to withstand the challenging conditions posed by radiation exposure. Ensuring proper power distribution and voltage regulation in these environments is vital for the reliable operation of the detector systems and, ultimately, for the accuracy of the data they collect.

We will implement a two-stage DC-DC conversion architecture to efficiently manage voltage levels for our system.

In the first stage, the Basha48 module will receive a 48V input from the long cable that extends from the electronics room. This module is responsible for stepping down the voltage to 12V. The Basha48 module will be strategically installed near the end cap, reducing the length of cable that must carry high voltage, thereby minimizing potential voltage drop and

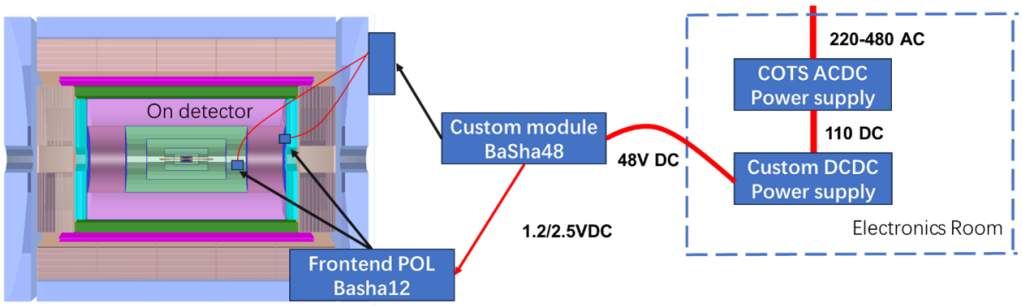


Figure 1.13: CEPC low-voltage power supply distribution

ensuring efficient power delivery.

In the second stage, the 12V output from the Basha48 module will be delivered to the frontend board via finer, more manageable cables. On the frontend board, the Basha12 module will further convert the 12V supply into the specific lower voltages required for the operation of the frontend detectors, namely 1.2V for the analog readout chips and 2.5V for the digital transmission chips.

This two-stage conversion approach not only optimizes the efficiency of power distribution but also allows for a compact design that minimizes radiation exposure to sensitive electronic components in the frontend. It ensures that the necessary voltages are precisely regulated, maintaining the performance integrity of the detector readout electronics while adapting to the challenging environmental conditions present in radiation-prone areas.

Figure 1.14: test power module?

1.5.2.1.2 COTS power supply Since the first two stages of the power supply are installed in an environment free from radiation and strong magnetic fields, commercial power supplies can be procured. In order to enable power control, the power supply must provide the following interfaces to the DCS system:

i) On/Off Control Interface: A simple input to allow the DCS to turn the power supply on or off.

ii) Voltage Adjustment Interface: An adjustable output voltage interface that lets the DCS set the required voltage

levels.

iii) Current Monitoring Interface: An output that provides real-time current readings to the DCS for monitoring purposes.

iv) Temperature Monitoring Interface: An interface to relay temperature data to the DCS, allowing for effective thermal management.

v) Fan Speed Control Interface: The ability to control and adjust fan speeds based on system requirements to ensure proper cooling.

These interfaces will facilitate seamless integration with the DCS, ensuring effective monitoring and control of the power supply operation.

1.5.2.1.3 Basha DC-DC conversion module To ensure that the power management module operates stably under radiation levels and provides a consistent voltage for the frontend electronics to meet the requirements of the CPEC experiment, we need to study the key technologies for radiation-hardened power modules and design dedicated radiation-hardened power management modules. Specifically, this includes:

Power management modules provide energy for electronic devices and serve as a cornerstone for the proper operation of these devices. Currently, commonly used power management modules are DC-DC converters, which, as the name suggests, convert direct current to direct current. These are primarily categorized into buck converters, boost converters, and buck-boost converters. Among them, buck converters are one of the most prevalent topologies in DC-DC power circuits, characterized by high efficiency and high power density. They represent critical components in power systems for various detectors within the CEPC, primarily responsible for reducing high-voltage power supplied via high-pressure transmission to the lower voltages required by frontend electronics. The use of high voltage and low current for power transmission can reduce the number of cables, minimize voltage loss, and enhance the power efficiency of the detector system. However, in buck converters, key modules such as the reference, pre-buck, and on-chip LDO (Low Dropout Regulator) are susceptible to radiation effects, which may lead to level drift and circuit failures. Therefore, it is crucial to implement specific radiation-hardening measures for different modules.

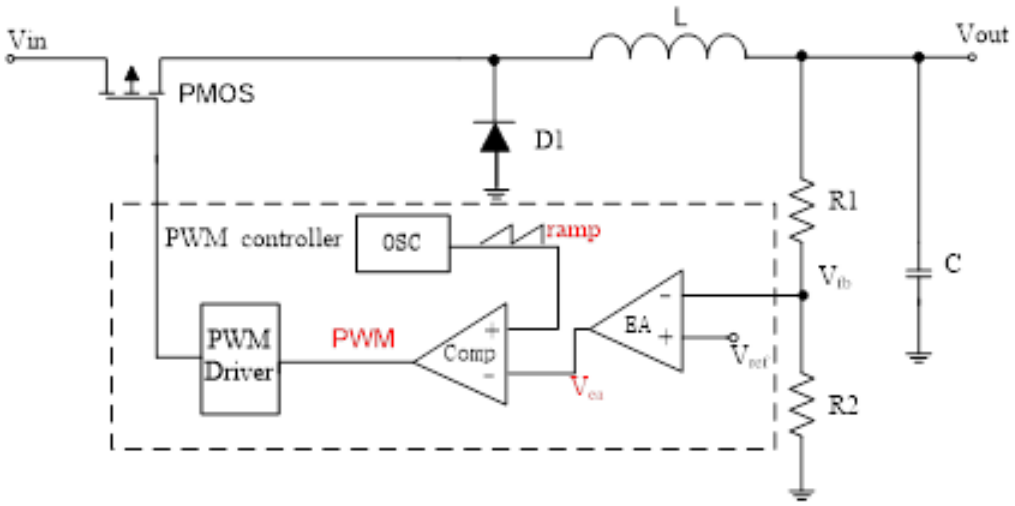


Figure 1.15: Schematic of the DC-DC Controller

Since the buck-type DC-DC converter is located within the detector and is subjected to high radiation and magnetic field intensity, magnetic-core inductors cannot be utilized. Additionally, due to area and space constraints, the energy storage inductance values are relatively low. However, the frontend electronics impose stringent requirements on power noise performance, necessitating a sufficiently low ripple voltage. Traditional methods, which involve increasing inductance values to reduce ripple voltage, are no longer feasible. Instead, the ripple voltage can only be minimized by increasing the switching frequency. The proposed DC-DC controller aims to operate at switching frequencies exceeding the MHz range. Furthermore, the radiation environment created during detector operation can induce soft errors or even hard failures, such as burnout, in silicon-based circuits. Hence, the designed DC-DC controller must withstand both ionizing

and non-ionizing radiation effects.

This project will define the design criteria for the DC-DC voltage converter based on the typical power requirements of frontend electronics circuits. Building on research and a review of current literature regarding radiation-resistant buck-type DC-DC voltage converters, a study will be conducted on the structure of the controller system. The focus will be on parallel output current capabilities, high switching frequency, and efficient circuit structures, along with specific circuit implementation methods. System-level modeling and simulation will be employed to optimize the controller's system architecture. On this foundation, research will delve into key circuit modules, analyzing the switching losses of each module to ensure that the power system maintains an efficiency above 85%. Additionally, protection circuits for overheating, overcurrent, overvoltage, and undervoltage, as well as auxiliary circuits for power status indication, will be developed to ensure that the voltage converter can promptly cut off power to protect itself and its load modules during abnormal operating conditions.

The design of the circuit and layout will simultaneously consider radiation-hardening methods. Specific studies will be undertaken on radiation-sensitive components, such as bandgap references, error amplifiers, and switch timing controllers, focusing on TID (Total Ionizing Dose), SET (Single Event Transient), and SEL (Single Event Latchup) hardening strategies. Verification of the designed circuits will incorporate approaches such as fault injection. Finally, research on radiation testing methods for the DC-DC voltage converter will be conducted, designing TID and SEE radiation testing methods for the buck-type DC-DC voltage converter based on existing radiation testing standards.

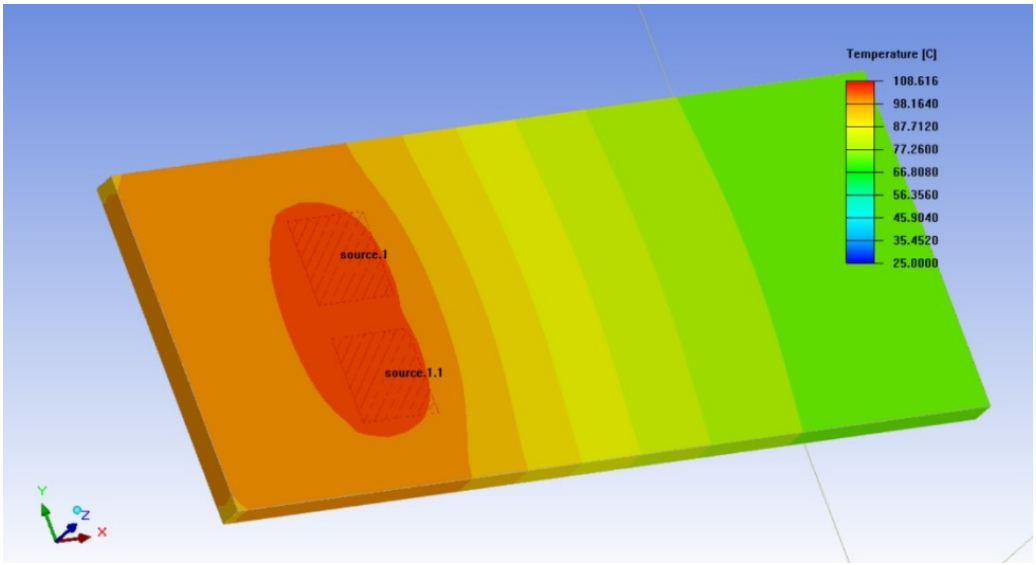


Figure 1.16: Heat Simulation Result of the DC-DC Module

1.5.2.1.4 Cable, connector

1.5.2.1.5 Power interface According to the requirements of the frontend chips of the detector, the power supply module needs to provide a high-quality 1.2V power output. In addition, the data transmission chips require a separate 2.5V digital power supply. The basic parameters are as follows:

The basic structure of the designed module is shown in the figure. The output signals include:

1.6 Alternative scheme based on Wireless communication (Jun Hu)

1.6.0.1 Technology study

1.6.0.1.1 Traditional Wi-Fi Solutions Traditional Wi-Fi solutions operate primarily in the 2.4 GHz and 5 GHz frequency ranges. Their key advantages include a mature technology and widespread adoption, with the most common standards for wireless local area networks defined by the IEEE in the 802.11 series—commonly referred to as Wi-Fi.

	Vertex	Pix Tracker	Si Strip	TPC	TOF	ECAL	HCAL
Detector for readout	CMOS Sensor	HVCMOS	Si Strip	Pixel PAD	Strip-LGAD	SiPM	SiPM
Main Func for FEE	X+Y	XY + nsT	X	E + nsT	X + 50psT	E + 400psT	E + 400psT
Channels per chip	512*1024 Pixelized	768*128 (2cm*2cm@25um*150um)	128	128	128	16	16
Voltage @chip	1.2V@65nm	1.2V@55nm (HVCMOS Pixel)	1.2V@130nm	1.2V @65nm	1.2V@55nm (TDC)	1.2V@55nm (TDC)	1.2V@55nm (TDC)
Power @chip	200mW/chip	<200mW/cm2 <0.8W/chip	336mW/chip	35mW/chip	<20mW/ch <2.56W/chip	15mW/ch	15mW/ch 160~320mW/chip
chips@module	8~29@ladder 4~25@layer	14	9~22@ladder 48~299@sector	1115	22(barrel) 11-23@sector(endcap)	1000ch*2	480ch*5pcb (barrel) 5832ch@sector(endcap)
Power @module	2.6~6.8W@ladder 10.4~170W@layer	11.2W	4~8.4W @ladder 23~119W@sector	39.7	56.32W(barrel) 58.9W(endcap)	31W@module	37W@module(barrel) 88W@sector(endcap)
Number of PW module	66	2204	192	496	3780 + 720	480 + 260	5536 + 1536

Figure 1.17: temp table

指标	**额定值**	**实际范围**
输入电压	**48V**	**36V-48V**
输出电压	**1.2V**	**1.2V、2.5V**
输出电流	**10A**	
输出纹波	**10mVpp**	
效率	**85%**	**80%-85%-80%（轻载-额定重载）**
尺寸	**50mmX20mmX6.7mm**	**包括散热和屏蔽**

Figure 1.18: temp table

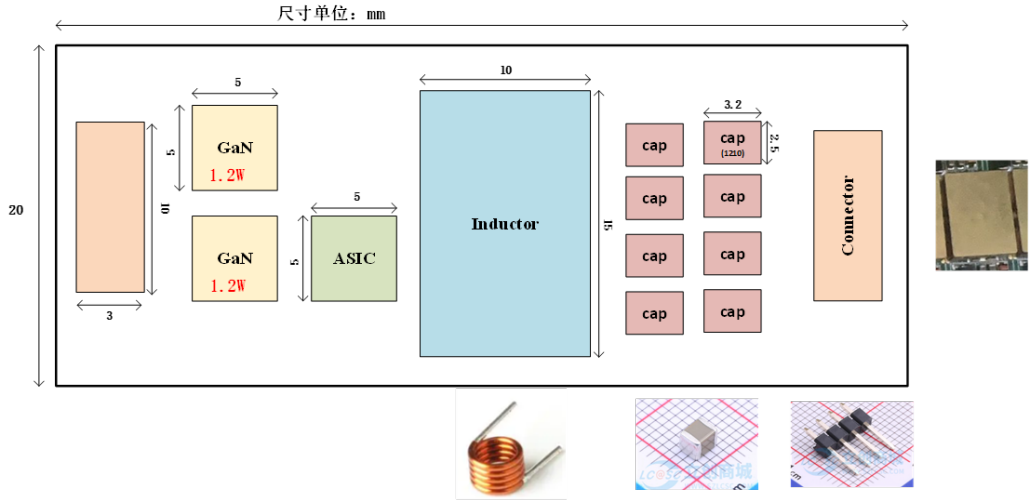


Figure 1.19: title

However, there are notable drawbacks associated with these solutions. The transmission density is limited due to the small frequency range and restricted number of channels available. Additionally, the inability to miniaturize antennas at high power levels further contributes to lower transmission density. Despite these limitations, traditional Wi-Fi is easier to develop and therefore well-suited for applications where bandwidth requirements are not particularly demanding, such as for slow control data and small system testing.

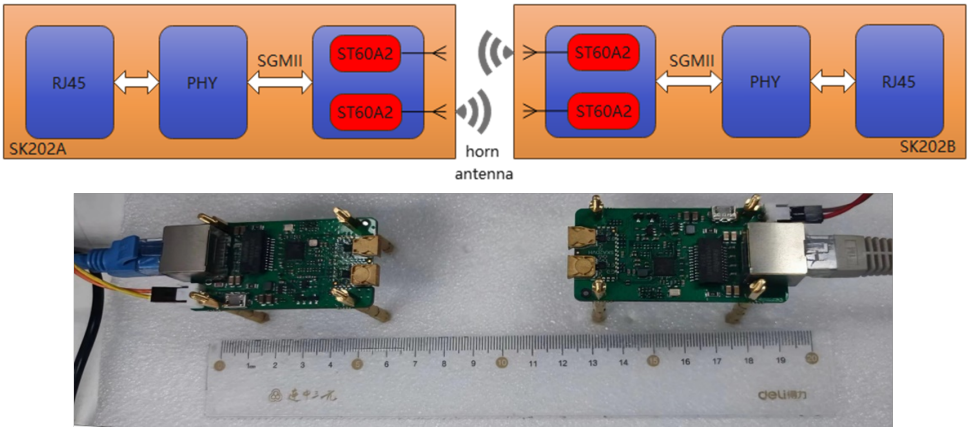


Figure 1.20: Test setup based on Raspberry board

1.6.0.1.2 Millimeter Wave Solutions It is currently popular to classify the frequency ranges as follows: 0.3-30 GHz is considered the microwave band, 30-300 GHz is classified as the millimeter wave band, and 0.1-10 THz belongs to the terahertz band. The transmission technologies for future 6G and Wi-Fi 7 are likely to be based on these two transmission bands. The frequency range represents a significant increase over traditional Wi-Fi, substantially addressing bandwidth issues and providing a theoretically excellent solution. However, higher bandwidth also brings increased power consumption and costs. More importantly, since these technologies are still in the development stage, relevant chips have not yet been commercially promoted on a large scale. The technical difficulties are considerable, and strict technology restrictions from foreign entities present high barriers and costs in manufacturing. At this stage, this project will focus on collaborating with domestic research institutes or large commercial companies, such as Huawei, to explore the possibility of system development using existing or upcoming millimeter wave and terahertz chips.

1.6.0.1.3 Research on Wireless Optical Communication Unlike traditional fiber optic communication, wireless optical communication utilizes air as the transmission medium, loading data onto a light source and directly transmitting

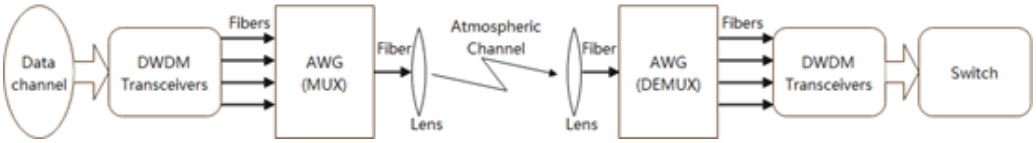


Figure 1.21: title

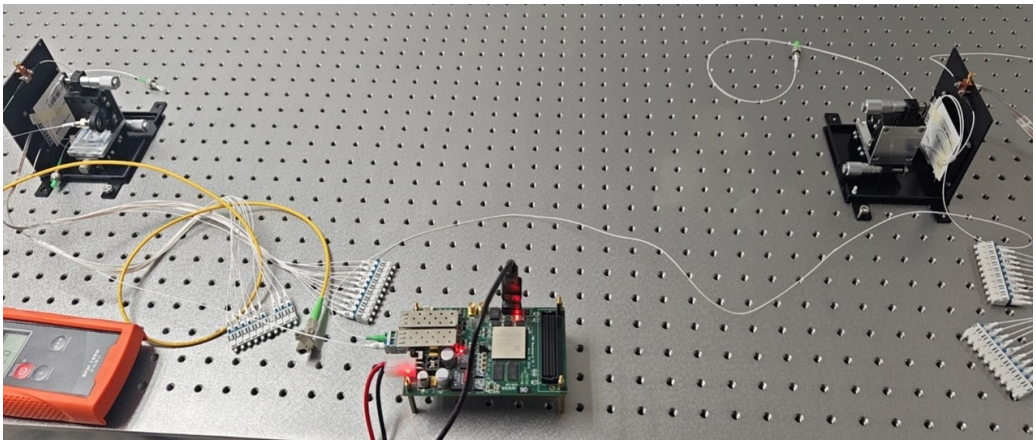


Figure 1.22: title

information by altering properties such as light intensity, phase, and polarization. Based on different propagation media frequency bands, wireless optical communication can be subdivided into infrared (IR), visible light (VL), and ultraviolet (UV) communication. Among these, visible light communication is currently the fastest-growing area, with transmission rates exceeding Gbps, which can meet our requirements. Additionally, due to the high directionality of laser channels, natural channel isolation can increase the number of available channels. The main research topics in visible light communication include LED and detector materials, modulation coding, signal processing, and heterogeneous networking.

For a simple visible light communication system, key components include an FPGA, which is the most commonly used programmable device. This enables the development of basic network transmission protocols, and some models also feature high-speed serial transceivers (serdes), making them suitable for prototype validation. As for the light sources, LEDs and lasers are commonly employed in visible light communication systems. LEDs emit light through the principle of spontaneous emission, serving as incoherent light sources with narrow modulation bandwidth but wide divergence angles. Conversely, lasers emit light through stimulated emission, allowing for higher bandwidth suitable for high-speed long-distance transmission, although they require precise alignment. Both light sources have unique characteristics, each suitable for specific application scenarios.

Regarding detectors, commonly used types include PIN and APD detectors, as well as image sensors. Generally, PIN and APD detectors are favored in high-speed visible light communication systems, while image sensors are employed in low-speed, multi-input, and multi-output visible light communication systems. According to the properties of semiconductor PN junctions, LEDs can also be utilized as detectors. In this research, a laser combined with an APD detector is planned to be used as the optoelectronic device.

1.7 Clocking systems (Jun Hu)

The clock system needs to fulfill two primary functions:

1. Provide a Reference Clock for Detector Electronics : This clock will serve as the baseline frequency for sampling, time measurement, and energy measurement across all the detectors.
2. Offer Absolute Timestamping for Detectors : It is crucial for the trigger system to receive temporally correlated physical data. Drawing from the experiences of the Daya Bay reactor neutrino experiment, recent advancements have shown that integrating precise timing information is essential for the effective operation of the experiment.

1.7.0.1 White Rabbit Technology

White Rabbit technology, initiated by CERN and GSI in 2008, utilizes synchronized Ethernet to achieve frequency distribution across multiple nodes. It employs precision time protocol (PTP) for time-stamping synchronization and harnesses all-digital dual heterodyne phase detectors to enhance synchronization accuracy to sub-nanosecond els. This technology offers an excellent solution for the timing system requirements of the Jiangmen neutrino experiment:

1. Synchronized Ethernet : This can provide a low-jitter clock as the operational clock for the frontend electronics.
2. Phase Difference Measurement and Compensation : This will ensure that all nodes' operational clocks reach sub-nanosecond phase alignment accuracy.
3. Precision Time Protocol : It will facilitate the alignment of time stamps for the frontend electronics.
4. External Reference Integration : The system can incorporate rubidium clocks and GPS as external reference frequencies and timestamps for Coordinated Universal Time (UTC).

This state-of-the-art clock system will significantly enhance the performance and accuracy of various detector operations in the neutrino experiment.

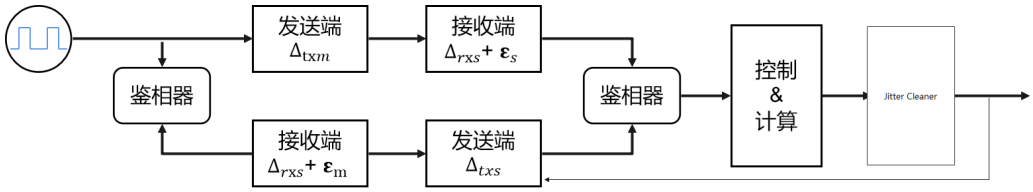


Figure 1.23: title

1.7.0.2 system main clock

1.7.0.3 Center clock generator

1.7.0.4 Clock fanout

1.8 Power system (Jun Hu)

1.9 Backend Electronics (Jun Hu)

The backend electronics system plays a pivotal role in the overall data acquisition process by receiving raw detector data from the frontend electronics. Once the raw data is received, the backend electronics is responsible for performing initial data processing and compression. This processing not only prepares the data for further analysis but also generates trigger signals that are essential for the trigger system's operation. The connections between the backend electronics system and other interfacing systems are depicted in Figure 2.

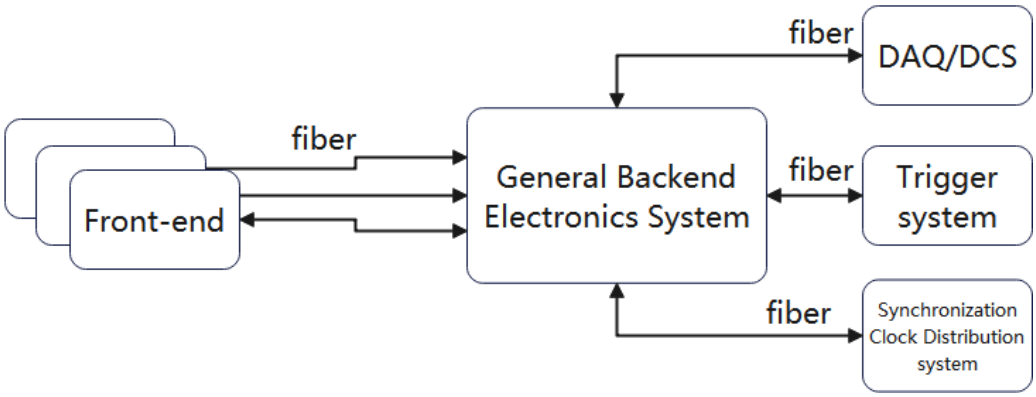


Figure 1.24: General Backend electronics system connection

The trigger signals, once generated, are forwarded to the trigger system to facilitate the triggering process. Concurrently, the backend electronics system caches the raw data for a specified duration, allowing it to maintain access to the data even as decisions are made. After a predetermined delay, the trigger system provides the backend electronics with the final trigger decision. Utilizing this information, the backend can intelligently select the relevant data from its buffer based on the final trigger criteria. Subsequently, the chosen data is packaged appropriately and sent to the Data Acquisition (DAQ) system for comprehensive analysis and storage. Furthermore, the backend electronics system transmits status monitoring and control signals back and forth with the Data Control System (DCS), ensuring effective monitoring and control of both the frontend detectors and the backend electronics.

In addition to data handling, the backend electronics system also communicates with the synchronization clock distribution system. This interaction is crucial for ensuring that clock and timing information remains synchronized across all components, enabling precise data acquisition and processing.

All of these connections are established using optical fiber connections, which provide the necessary high-speed, high-bandwidth communication required for efficient data transfer in a high-throughput environment. This choice of communication medium not only enhances the speed of data transmission but also mitigates issues related to electromagnetic interference (EMI) and allows for the necessary distance between components in radiation-sensitive areas.

1.9.0.1 Backend Electronics Hardware Design

The backend electronics system is engineered around the XTCA (Advanced Telecommunications Computing Architecture) racks, optimizing both functionality and scalability. Each rack is designed to accommodate two ATCA (Advanced TCA) crates, which in turn house ten general backend electronics boards per chassis. This layout allows for the efficient allocation of space, with the remaining capacity utilized for optical patch panels, power supplies, and other auxiliary equipment.

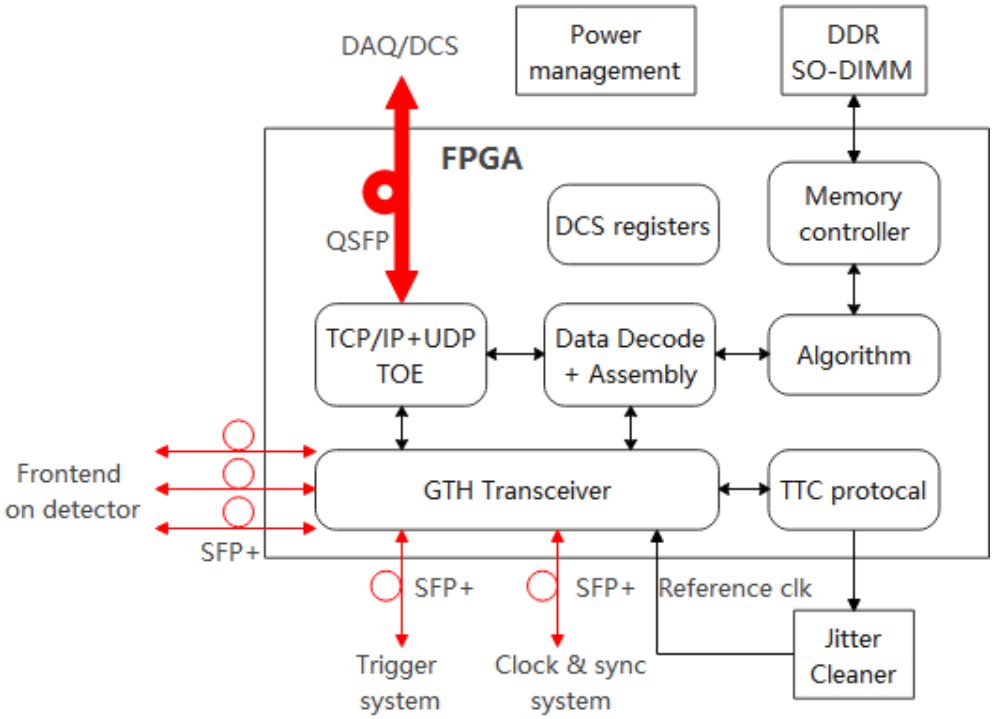


Figure 1.25: General backend board structure

The hardware components of the custom backend electronics are illustrated in Figure 2, and they primarily consist of the following key sections:

1. FPGA: Serving as the core processing unit of the backend electronics board, the FPGA (Field Programmable Gate Array) is responsible for controlling and executing the majority of the backend electronics functions.

2. Clock Jitter-Cleaner: This component ensures that timing signals are free from jitter, maintaining signal integrity across high-speed data connections.
3. DDR Memory: Dynamic Random-Access Memory (DDR) provides necessary memory resources for data buffering and temporary storage during processing.
4. Power Management: This section manages power distribution to ensure that all hardware components receive stable and adequate power.

From preliminary evaluations conducted with the frontend electronics, it is estimated that the fiber optic line rate for data transmission to the backend electronics will be 10 Gbps. To accommodate this high data throughput, a custom communication protocol will be implemented. Additionally, connections to the trigger system and the clock distribution system will also utilize fiber optic links that operate at the same 10 Gbps line rate. In contrast, communication with the DAQ (Data Acquisition) and DCS (Data Control System) will leverage 40 Gbps QSFP+ optical modules to enable robust and high-speed connectivity.

These requirements create stringent demands on both the speed and the quantity of high-speed serial transceivers integrated into the FPGA. Furthermore, the FPGA will be tasked with performing initial processing on the raw data, necessitating a considerable level of processing capability to handle the data rates effectively.

To ensure that our system meets these operational criteria, we have conducted a comparative analysis of the performance specifications of several widely-used FPGA models currently available on the market. The results of this comparison are summarized in Table 1, leading us to initially select the XC7VX690T-2FFG1158C as our preferred FPGA model. This choice is based on its ability to satisfy the high-speed communication requirements and processing demands of the backend electronics system, ensuring efficient operation and data integrity in a high-throughput environment.

1.9.0.2 FPGA Firmware Algorithm Development

Based on the functional requirements of the backend electronics system, several key functional modules will be implemented in the FPGA, as illustrated in Figure 2:

1. Data Interfaces and Communication High-speed data communication will be facilitated through the GTH transceivers integrated within the FPGA, supporting a multichannel transmission bandwidth of at least 10 Gbps. The communication protocols will be designed to accommodate various upper-layer protocols in accordance with system specifications. Specifically, the frontend data will be packaged and transmitted using a custom protocol akin to lpGBT, necessitating the implementation of appropriate unpacking logic within the FPGA to effectively interpret this data. Additionally, for communication with the DAQ and DCS systems, the standard TCP/IP protocol will be utilized, which requires the FPGA to implement a hardware protocol stack to maximize communication efficiency and throughput.
2. Data Processing and Packaging The FPGA will be responsible for categorizing and processing the incoming raw data based on channel and timing information. This involves assigning the data to the corresponding digital signal processing algorithms for further refinement and analysis to generate the required trigger signals. Upon receiving a trigger signal, the FPGA will select the relevant valid data, efficiently package it, and transmit it according to a predefined data structure, ensuring that the information is organized and ready for subsequent stages of handling.
3. Digital Signal Processing Algorithms Once the FPGA receives the raw data, it will implement a variety of processing algorithms tailored to the specific type of detector in use. For instance, tracking detectors may require the implementation of cluster-finding algorithms, while calorimeters will focus on extracting timing and energy information. In scenarios where considerable noise is present, fast filtering algorithms may be deployed to enhance the signal-to-noise ratio. Additionally, real-time processing algorithms will facilitate the proactive acquisition of key information from physical events. This capability significantly improves the efficiency of the system's triggering mechanisms, reduces trigger latency, and alleviates the workload on both the DAQ and offline processing systems.
4. Clock Synchronization Technology In high-energy physics experiments, effective clock synchronization is crucial as it coordinates the timing across multiple channels, detectors, and the data acquisition system to ensure data consistency and accuracy. By researching and developing clock synchronization technology tailored to fiber optic transmission systems, it is possible to transmit both data and clock signals through a single fiber optical cable. This

approach significantly minimizes the required number of optical cables and reduces overall system complexity.

5. DDR Controller Considering the need to buffer raw data until the final trigger signal is received from the trigger system, the backend processing module will incorporate a sufficiently large DDR memory. The FPGA will manage the timing control for reading from and writing to the DDR memory, ensuring that data integrity is maintained and that no data is lost during the buffering process.
6. Slow Control Registers The backend electronics system must be responsive to monitoring and control commands originating from the slow control system. Acting as a communication bridge between the backend and the frontend detectors, the FPGA will handle the parsing, forwarding, and responding to slow control commands. This functionality ensures that the system remains manageable and that any necessary adjustments can be made in response to operational conditions or changes.

By implementing these functional modules within the FPGA, the backend electronics system will be equipped to handle the rigorous demands of high-speed data acquisition and processing while maintaining reliability and efficiency in a high-energy physics experimental environment.

1.9.0.3 Prototype performance

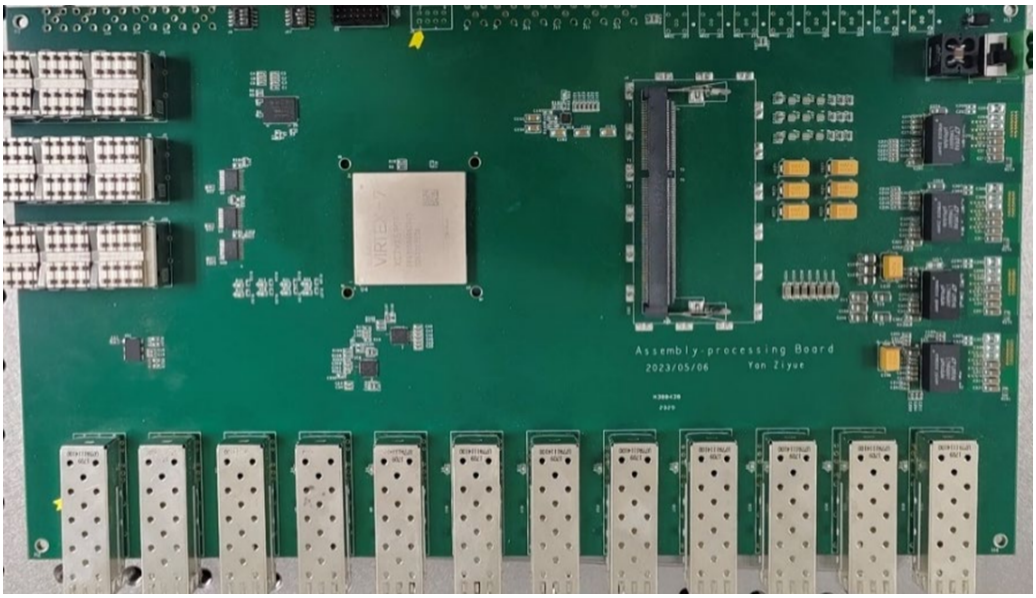


Figure 1.26: title

The physical overview of the data aggregation processing board is presented in Figure 4-14 (a), while the distribution of components on the board is illustrated in Figure 4-15 (b). The board is equipped with twelve SFP+ interfaces and two QSFP+ interfaces, which are utilized for connecting the GTH transceiver modules of the FPGA. These interfaces serve as the communication pathways for data transmission between the data aggregation processing board and the upper computer, as well as the readout system that encompasses multiple readout channels.

The GTH transceivers offer higher data rates and improved performance compared to GTX transceivers, making them suitable for applications that demand higher data transmission bandwidth. Additionally, the board is equipped with a 204-pin DDR3-SODIMM , which is intended for large data buffering during the algorithm processing phase. This configuration ensures that the board can efficiently manage the substantial data flow necessary for effective data aggregation and processing.

1.10 Consideration on Electronics Crates & Cabling (Wei Wei, Zheng Wang)

The overall spatial requirements of the electronic system for the counting room are an important interface between electronic and mechanical systems, and also relate to the planning of the underground hall. To this end, this section

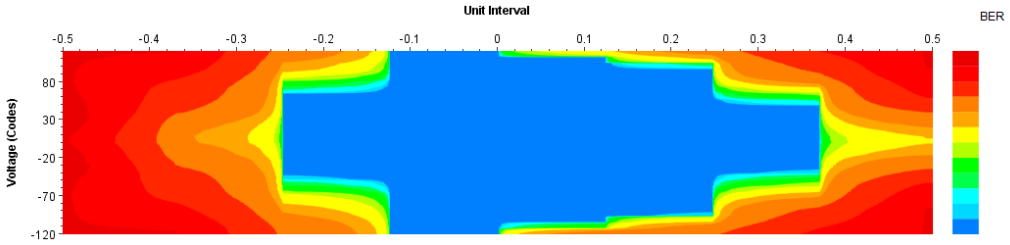


Figure 1.27: title

will first summarize the overall considerations and design specifications of the electronics system's crates and racks, and further discuss the detailed layout of the front-end wiring of each sub-detector, providing wiring considerations for data transmission, low-voltage power supply, high-voltage power supply, and other aspects. Finally, a summary of the requirements for crates and racks for each section will be provided, along with the preliminary spatial requirements of the electronic system as a whole.

1.10.1 Design Specifications for Electronic System Crates and Racks

The requirements for crates and racks related to the electronic system mainly include data transmission, low-voltage power supply, and high-voltage power supply. As an electronics system designed uniformly from top to bottom, the crates and racks should also be designed and planned according to the same specifications. Since crates and racks are usually based on current industry standards and existing products, we consider using the ACTA industrial standard, which can maintain relative advancement and maturity in comprehensive design for the current and future period, as the standard for rack design. Due to its standard height of 42U, the racks used for backend electronics, electronic power supplies, and detector high-voltage power supplies will consider the maximum load-bearing capacity at this height to determine the number of crates that can be installed in a single rack.

The backend electronics in this section are mainly related to data interfaces. According to the previous chapters, the data rate of a single optical fiber channel is designed to be approximately 10Gbps, with an effective data rate of about 8Gbps. The design of the input data channels for general backend electronic PCBs is set at 16 channels, with a height of 9U. In order to make efficient use of ACTA rack resources, the rear-end electronic crates...

1.11 Previous R&D on Electronics System for Large Particle Physics Experiments (Wei Wei)

1.12 Summary (Wei Wei)

[1]

References

[1] Frank Mittelbach et al. *The LaTeX Companion*. 2nd. Addison-Wesley Series on Tools and Techniques for Computer Typesetting. Boston, MA, USA: Addison-Wesley, 2004.

[2] Tobias Oetiker et al. *The Not So Short Introduction to LaTeX 2ε*. 4.2. 2006.