

Progress of CEPC ref-TDR TDAQ Fei Li

On behalf of CEPC TDAQ Group



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Nov. 26th, 2024, CEPC Detector Ref-TDR Meeting

Progress of TDAQ

TDR draft v0.3

- 13 pages now, partial draft
- HLT/DCS/ECS missing

DCS & ECS meeting

- Nov. 25th (Mon. morning)

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DCS&ECS schema disscussion

Missing requirements of detectors

- https://jupyter.ihep.ac.cn/CwulQi9ESayf4QLUXqbz8A
- -HV
 - TPC/ SiPM per module
- -LV
 - 26116 ch/ 549 crates
- Gas/
 - TPC 8 input/8 output
- Cooling/TH/Others

IOT

Wireless LoRA

Software

- WinCC-OA, EPICS

CEPC Detector Control & Monitoring

Underground Requirements

Number Of Detectors Parameters reqired for control and montoring

Detectors	HV Crates	HV Channels	Gas Monitoring	Cooling	Temp& Humidity	Other
Eg.	10	160	control:10 flow:10 ?	control:10 flow:10 ?	T:20 H:20 ?	
Vertex	x	x	x	х	x	
ТРС	3个9U的SHV机箱	248*2	8 input/ 8output			
ITK-Barrel						

Trigger & Data Rate

- Compress background -> 1% @ L1
- Compress background -> 0.1% @ HLT
- Data size per bunch cross
 - 300Kbytes @ Higgs
 - Unknown @Z
- Event size < 2 Mbyte</p>
 - Occupancy and read out window
- L1 trigger rate
 - 13~120 kHz @ Higgs&low lum. Z
- DAQ data rate
 - Read out: 26~240 GB/s
 - @ Higgs & low lum. Z
 - Storage: 0.3~7.5 GB/s

	Higgs	Z(10MW)	Z(50MW)	W	tt
Luminosity(10E34/cm2/s)	8.3	38	192	26.7	0.8
Bunch space(ns)	346.2	69.3	23.1	253.8	4523.1
Bunch cross rate(MHz)	1.34	12	39.4	6.5	0.18
Raw data rate before trigger (TBytes/s)	0.4	3.6	11.82	1.95	0.048
Physical event rate(kHz)	0.008	13.2	66	0.1	0.002
L1 trigger rate(kHz)	13	120	400	65	2
DAQ readout rate(Gbyte/s)	26	240	800	130	4
High level trigger rate(kHz)	1	25	100	6	1
DAQ storage rate(Gbytes/s)	0.3	7.5	30	1.8	0.3

Backup

TCDS-Trigger Clock Distribution System

TCDS/TTC

- Clock, BC0, Trigger, orbit start signal distribution
- Full, ERR signal feed back to TCDS/TTC and mask or stop L1A

- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD-Data Concentrator and Timing Distribution
- BEE-Backend board Electronic



TDAQ are only responsible for system-level distribution, each system is then responsible for its own internal distribution.

Trigger simulation



Working Plan for TDR

- - 第一周: 事例率 (Cal+Muon), muon tracking
 - 双gamma光子应对策略
 - 第二周:L1算法(Cal+Muon)算法, TDR editing
 - 第三周: TPC、OTK tracking, low lum. Z background.
 - 第四周: Global trigger start, TDR draft 0.1
 - 12月, TDR draft 1.0
 - HLT algorithm 结果
 - Global trigger
 - trigger efficiency

12.1	Introduction									
12.2	Requirements and Design Considerations									
	12.2.1 Requirements									
	12.2.2 Event rate & background rate estimation									
	12.2.3 Technology survey									
	12.2.4 TDAQ policy consideration									
	12.2.5 TDAQ Interface with electronics									
12.3	Trigger Simulation and Algorithms									
12.4	Hardware Trigger									
	12.4.1 Previous experience on large facilities									
_	12.4.2 System architecture									
•	12.4.3 Common Trigger Board									
	12.4.4 Trigger Control and Distribution									
	12.4.5 Resource cost estimation									
12.5	Software and High Level Trigger									
12.6	Data Acquisition System									
	12.6.1 Previous experience on large facilities	•								
	12.6.2 Overview of System Functionality	•								
	12.6.3 Detector Readout	•								
	12.6.4 Dataflow									
	12.6.5 Network									
	12.6.6 Online Software									
12.7	Detector Control System									
12.8	Experiment Control System	•								
12.9	Summary	•								

Working Plan for TDR



- 11月
 - Hardware trigger structure design for TDR
 - trigger board/ TTC detailing
 - BEE interface
 - basic trigger primitives
- 12月:
 - trigger primitives for each L1 detectors
 - common trigger board structure finalize
 - L1 algorithm deploment design, boards num

Working Plan for TDR

HLT

- 11月
 - 编辑一页的FPGA加速
 - GPU, 概念性描述
 - 离线软件状况

DAQ

- 11月
 - system architecture
 - software layer data flow
 - RDMA/GPU/FPGA/Mem buffer
- 12月
 - Network/hardware
 - Online software

DCS

- 11月

- DCS requirement from each detectors
- framework design

ECS

- _ 11月
 - framework design
 - control network
- 12月
 - IT infrastructure
 - hardware
 - control/computing room
 - monitoring

Findings--revised

- The baseline plan is to transmit the full raw data to the front-end electronics and connect the trigger to the back-end electronics.
 - Transmit the full raw data from front-end electronics(on-detector) to backend electronics(off-detector)
- A hierarchical trigger scheme is foreseen to bring event data rates down from ~3MHz to ~1kHz in ZH running and ~40MHz to ~100kHz at the Z pole.
 - The bunch cross rate in ZH running is about 1.34 MHz when bunch space is 346.2 ns (2.9 MHz) and there is 54% bunch train gap.

Comments

The detailed (bottom-up) design of the TDAQ must await further details on the sub detector design.

- We will closely follow the design of each sub detector. Especially background study and data rate estimation from each sub detectors.
- Work on the trigger primitives is needed to bring the rate down to an acceptable input for the second-level trigger, and to inform further planning for the processing farms in the DAQ design. Should it be needed, a track trigger could provide a powerful additional primitive.
 - More simulation works on trigger primitive and more discussion with physics and detector experts are needed. Track trigger simulation will be next main work.
- High-level triggering will also need to weigh the physics-versus-bandwidth tradeoff for lower-energy events, e.g. from gamma-gamma collisions.
 - We need more study for low-energy events of beam induced background. And few gamma-gamma collisions are included in the available background sample data.

Recommendations

- A simple simulation of sub detector-based trigger inputs using simple, robust algorithms should be prioritized to allow more detailed specification of the requirements for TDAQ hardware and identify areas that need further attention. This should include an appropriate safety factor for beam-related backgrounds.
 - Basic trigger simulation study for each sub detectors are in progress.
 - And the safety factor needs to be discussed carefully.
- Further work should include an evaluation of benefits of implementing a track trigger as a complement to the calorimeter and muon primitives, and to clarify the bandwidth foreseen for gamma-gamma events.
 - We will move forward this after finish simple trigger simulation.

Physical Event Rate

Higgs 240GeV(30MW/50MW)

- BX rate:0.8(1.74)/1.34(2.9) MHz
- Physical event rate: 5Hz/8Hz (Higgs: 0.02Hz)

Z pole 91GeV(10MW/50MW)

- BX rate: 12(14.5)/39.4(43.3) MHz
- Physical event rate: 13.2kHz/66kHz

	Higgs		Z	W	tť		
SR power per beam (MW)	30	30	10 3		30		
Bunch number	268	11934	3978	1297	35		
Bunch spacing (ns)	576.9 (×25)	23.1(×1)	69.2(×3) 253.8(×11)	4523.1(×196)		
Train gap (%)	54	17	17	1	53		
Luminosity per IP (10^{34} cm ⁻² s ⁻¹)	5.0	115	38	16	0.5		
	TEase	XX/	++				
	riggs	Higgs Z W					
SR power per beam (MW)	50						
Bunch number	446	13104		2162	58		
	346.2	23.1		138.5	2700.0		
Bunch spacing (ns)	(×15)	(×1)		(×6)	(×117)		
Train gap (%)	54	9		10	53		
Luminosity per IP $(10^{34} \text{ cm}^{-2} \text{ s}^{-1})$	8.3	192		26.7	0.8		

									pc		
过程	xsection(nb)	百分比	事例率kHz	F	Z	W	•W-	ZH		tt	٦
Bhabha	0.0586	0.001371951	0.068597543	107	9 <u>q</u>						uts
muon	1.5361	0.035963374	1.798168703	10.							[evel
tau	1. 5249	0.035701158	1.78505791	106							ber of
qq	30.6522	0.717633315	35.88166573	105	∕∖.	+					Numl for 5
电子中微子	2.9607	0.069316296	3.465814777		ЛX		W	• W-			
muon中微子	2. 9896	0.069992906	3.499645306	10 ⁴			ß				= 5 × 10 ⁷
tau中微子	2. 9909	0.070023342	3.501167095	ь 10 ³ г	Singi	e Z	Z	Z			
中微子总	8. 9411	0.209330202	10. 46651012	10 ²	ngle V	v/		<u>ZH</u>		tī	-5×10^{5}
总共	42.7129	1	50			^		w	fusion		-
		亮度		101				7	fusion		
30 m w		1.15E+36	4.91E+01	1							-5×10 ³
50 MW		1.92E+36	8.20E+01	Ē	100			250	200	250	400
		I		50	100	150	200	s [GeV]	300	3.0 .	400

Z pole, ref: MC /cefs/data/stdhep/CEPC91/ 2fermions/wi_ISR_20220618_50M/2fermions/ nossihlu

Raw Data Rate

Data rate before trigger

- <1 TB/s @ Higgs</p>
- Several TB/s @ Z
- L1 trigger rate
 - O(1k) Hz @ Higgs
 - O(100k) Hz @ Z
- Event size < 2 MB</p>
 - Related to occupancy and read out window
- Storage rate after HLT
 - <100 Hz(200 MB/s) @ Higgs
 - 100 kHz (200 GB/s)
 @ Z

	Vertex	Pix(ITKB)	Strip (ITKE)	ОТКВ	ΟΤΚΕ	ТРС	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon	
Channels per chip	512*102 4	512*128	1024	12	28	128		8~16				
Data Width /hit	32bit	42bit	32bit	48	bit	48bit	48bit					
Avg. data rate / chip	0.18Gbp s/chip, 1Gbps/c hip inner	3.53Mb ps/chip	21.5Mbp s/chip	2.9Mbp s/chip	38.8Mb ps/chip	~70Mb ps/mod ule Inmost	10kHz/ch	10kHz/ch	5kHz/chann el	5kHz/chann el	10kHz/c hannel	
Detector Channel/modu le	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 module s	11520 chips 720 module s	492 Module	0.96M chn ~60000 chips 480 modules	0.39 M chn	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43,176 chn, 288 modules	
Avg Data Vol before trigger	474.2 Gbps	101.7 Gbps	298.8 Gbps	249.1 Gbps	27.9 Gbps	34.4 Gbps	460.8 Gbps	187 Gbps	811.2 Gbps	537.6 Gbps	24 Gbps	
Occupancy(%)	0.022	0.025	(Strip)	0.35(Strip)	0.0028	0.5	58	0.0	0.038		
Sum	3.2 Tbps = 400GB/s											

Collected from each detectors @Higgs