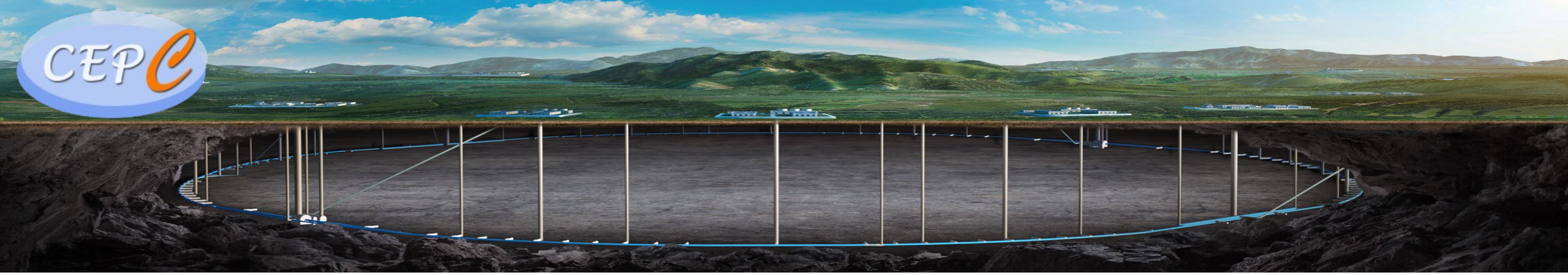


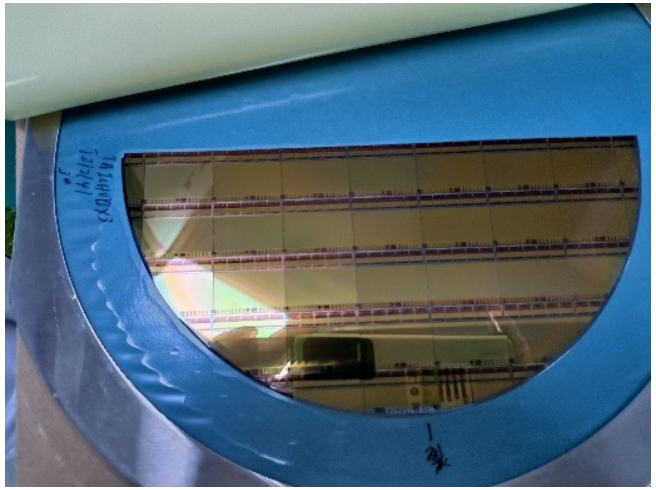
太初芯片测试

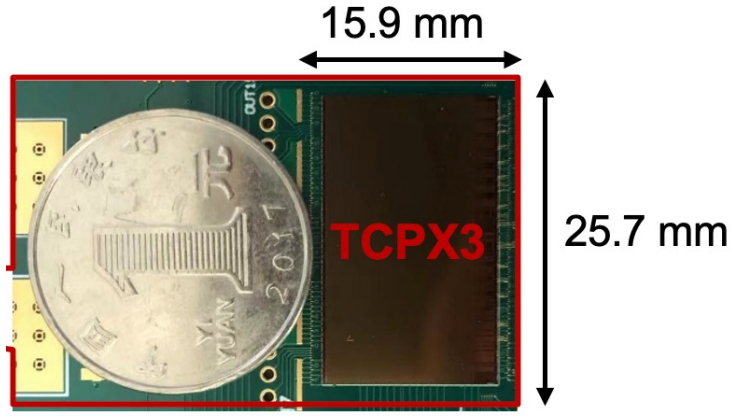
张颖、梁志均

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

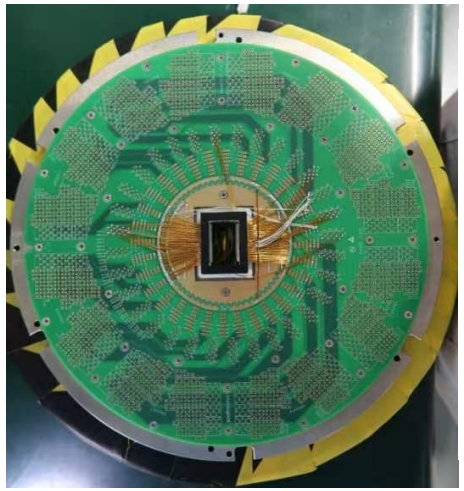
太初3芯片

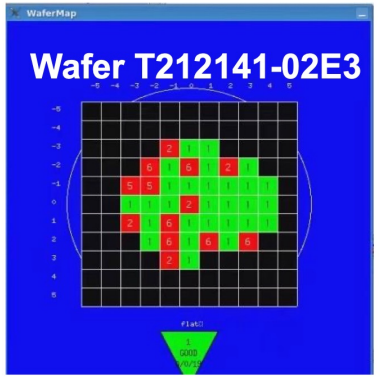
- 全尺寸 CMOS 像素探测器
  - 1024×512 像素阵列 芯片尺寸：15.9×25.7mm
  - 25μm×25微米 像素尺寸
  - 工艺: Towerjazz 180nm CIS process
  - 快速优先级读出，可以用在ZH and Z runs上 (~40MHz clock)





TaichuPix-3 chip vs. coin

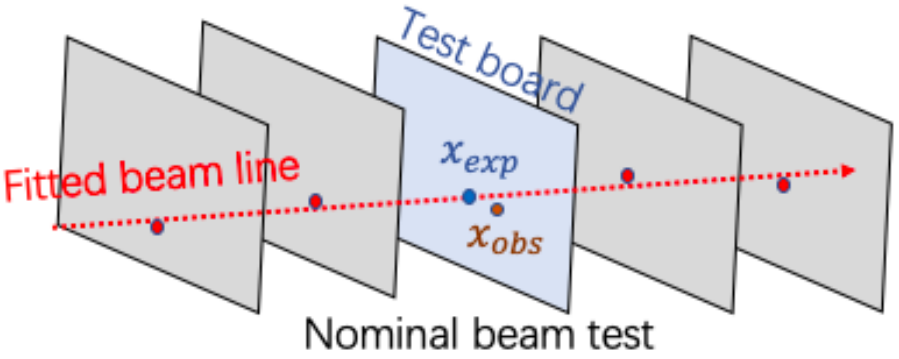




An example of wafer test result

	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

太初束流望远镜： 空间分辨率



- Vertex 探测器项目指标： 3微米空间分辨率
- 目前太初芯片实现指标：
  - 4.5微米 （束流测试），像素尺寸25*25微米

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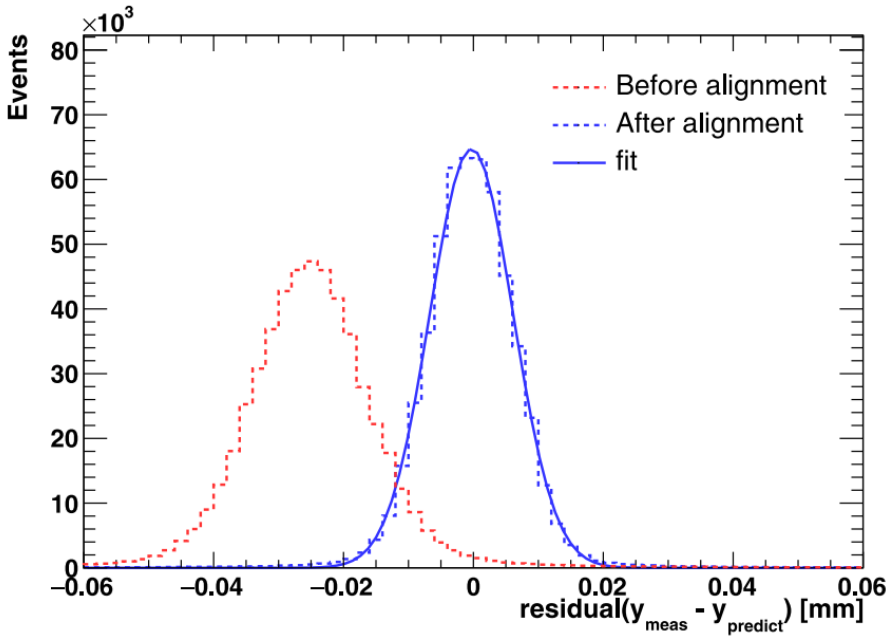
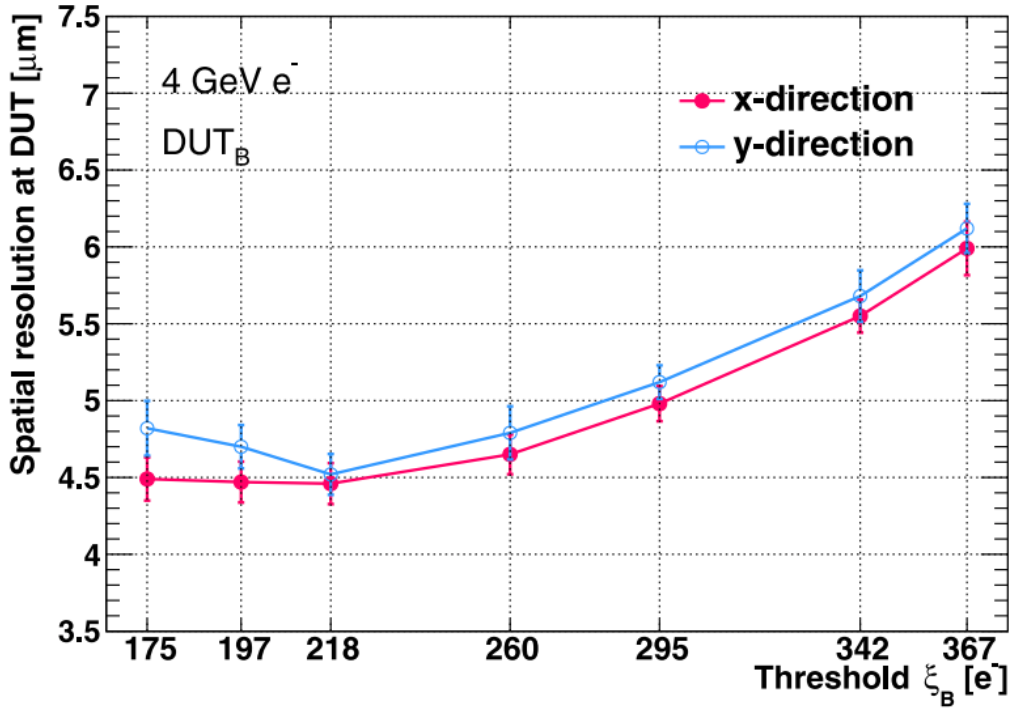
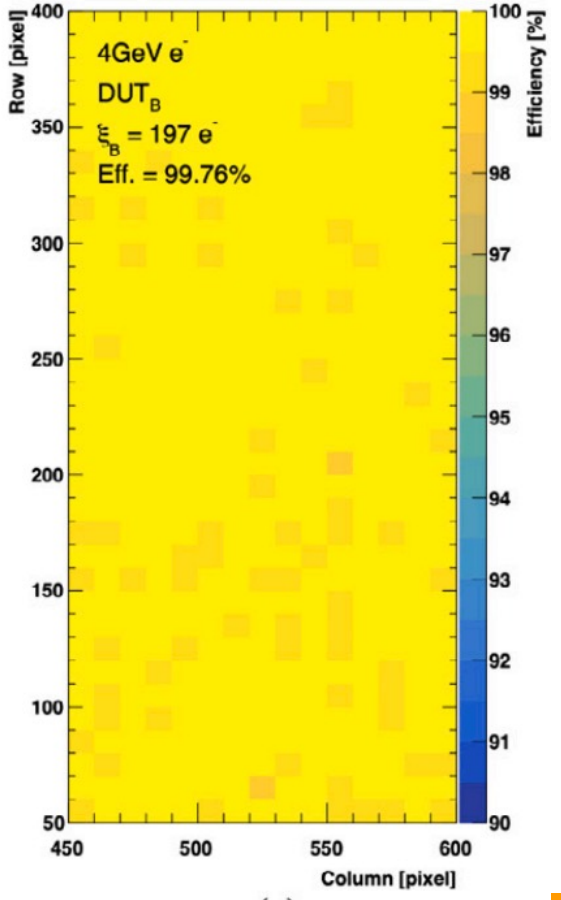
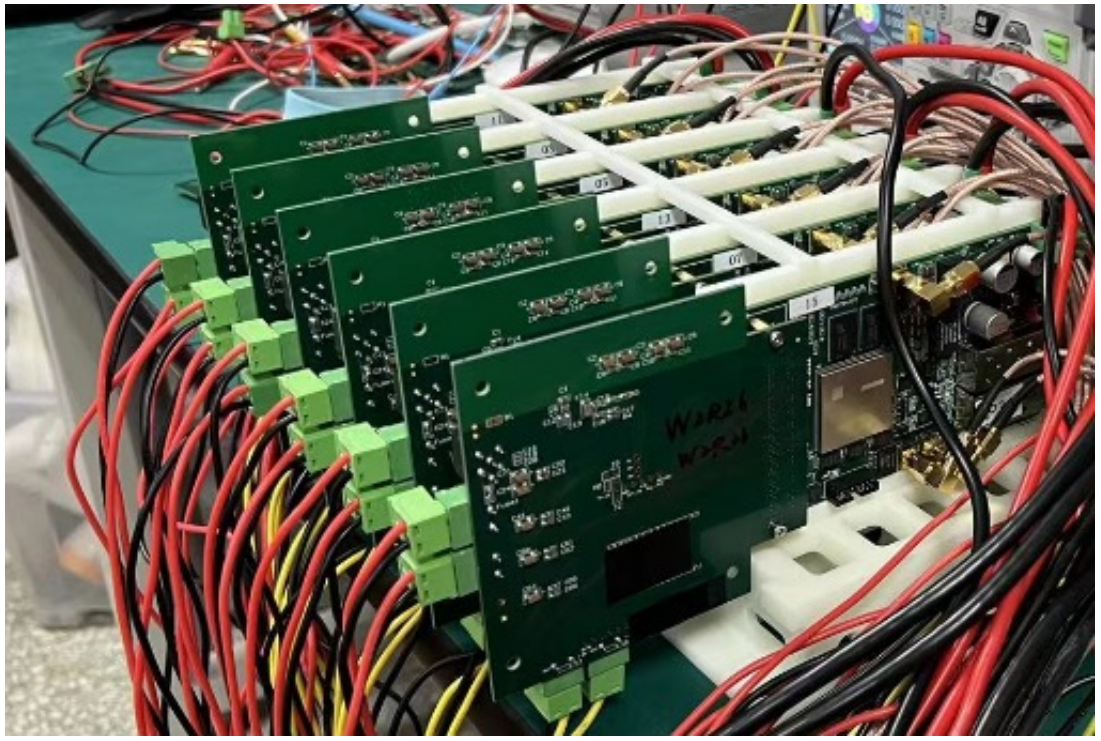


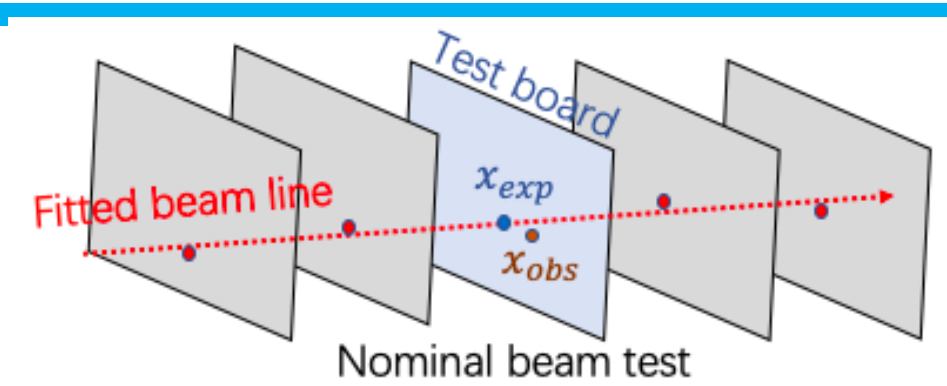


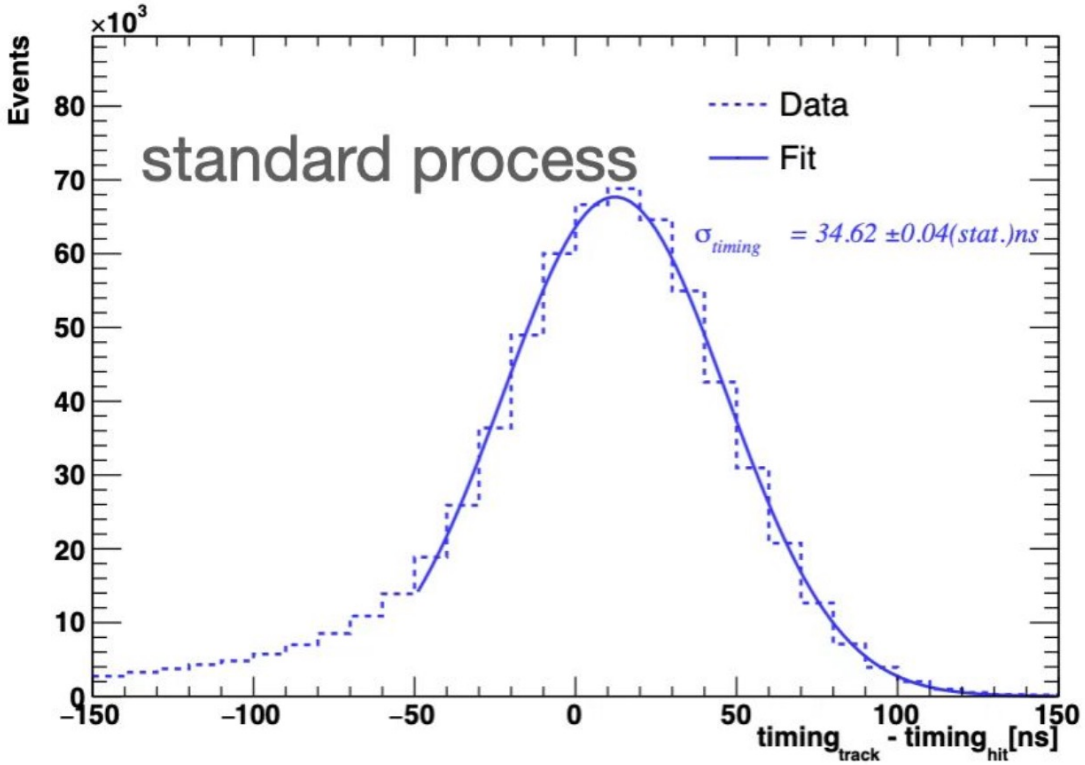


太初束流望远镜： 时间分辨率

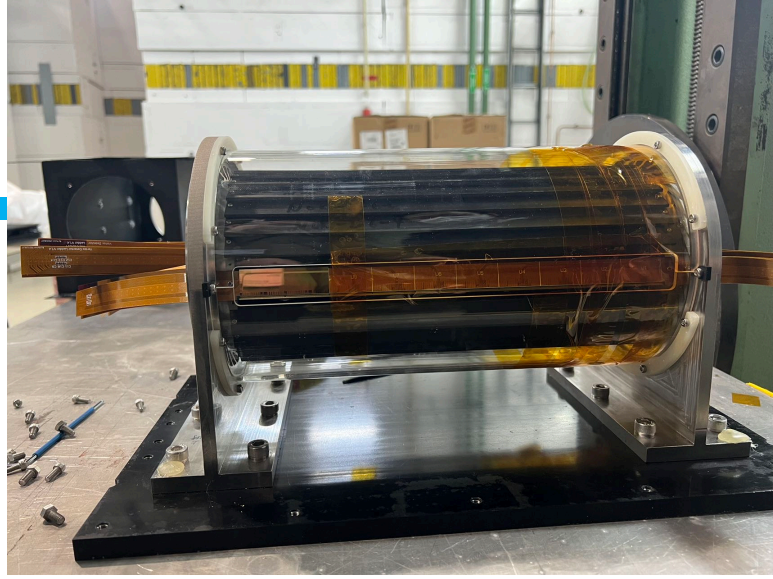
- 项目指标： 好于100ns 时间分辨率
- 目前用太初束流望远镜初步结果
  - 时间分辨率好于50ns，满足指标要求
  - 计划发表文章



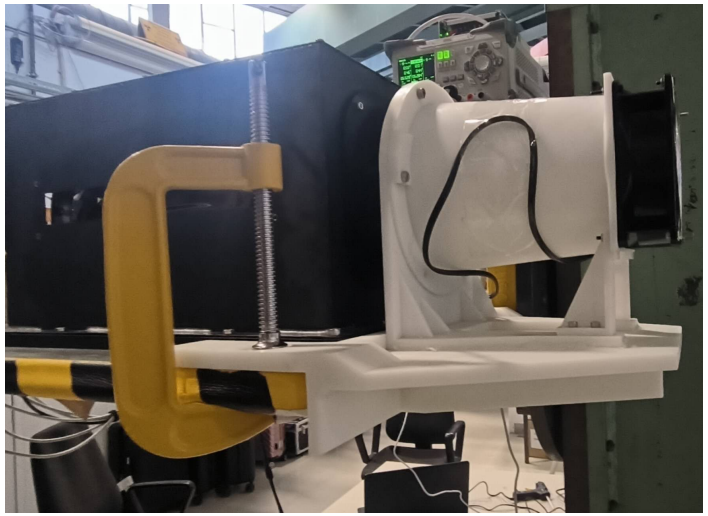




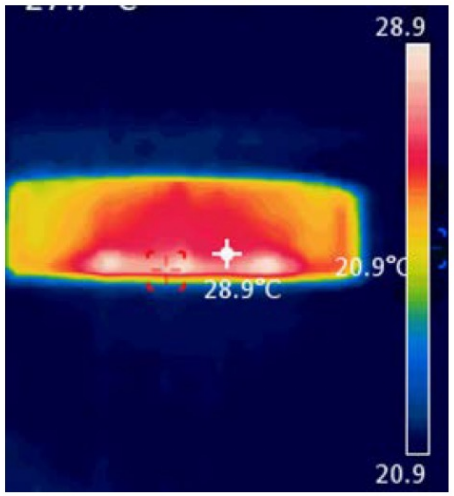
太初顶点探测器原型机：功耗



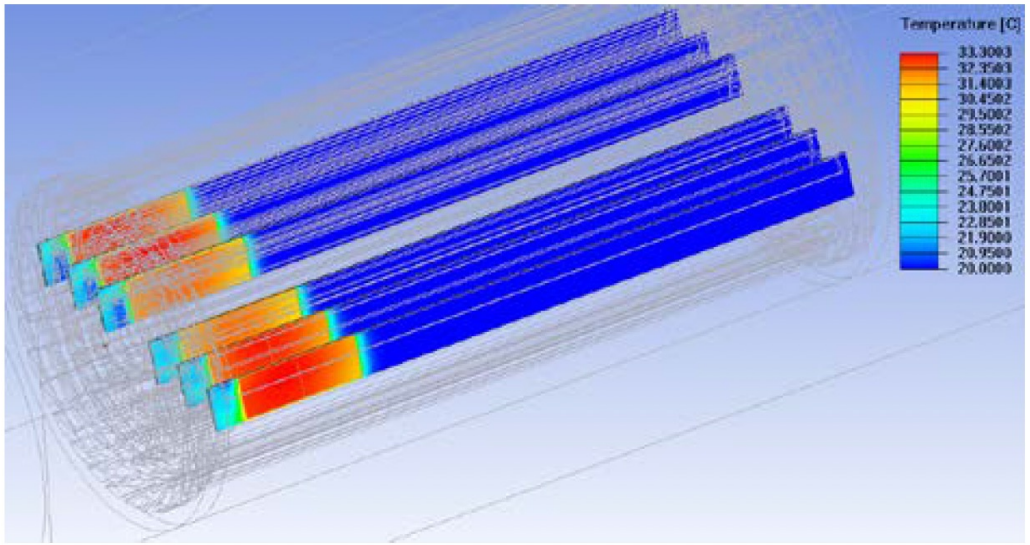
- 项目指标： 低于100mW/cm2 的功耗
- 目前达到指标：60mW/cm2 的功耗@17.5MHz时钟
  - 样机束流测试功耗：60mW/cm2 （@17.5MHz时钟）
  - 验证了风冷设计，温度控制到30度以下，与热模拟符合
  - 风冷带来振动可以控制在微米级，对空间分辨率没有可见的影响



Chip temperature under cooling during beam test: Max 28.9 ℃

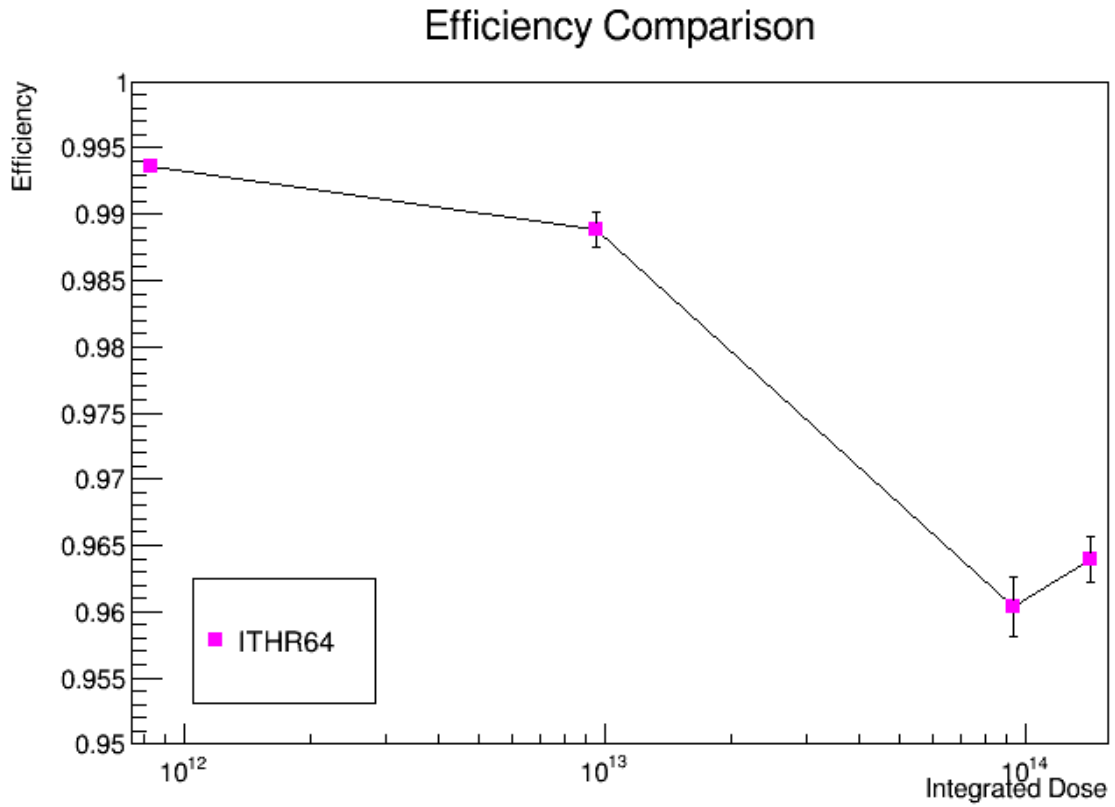


Prototype cooling simulation：Max 33.3 ℃



太初芯片抗辐照性能：

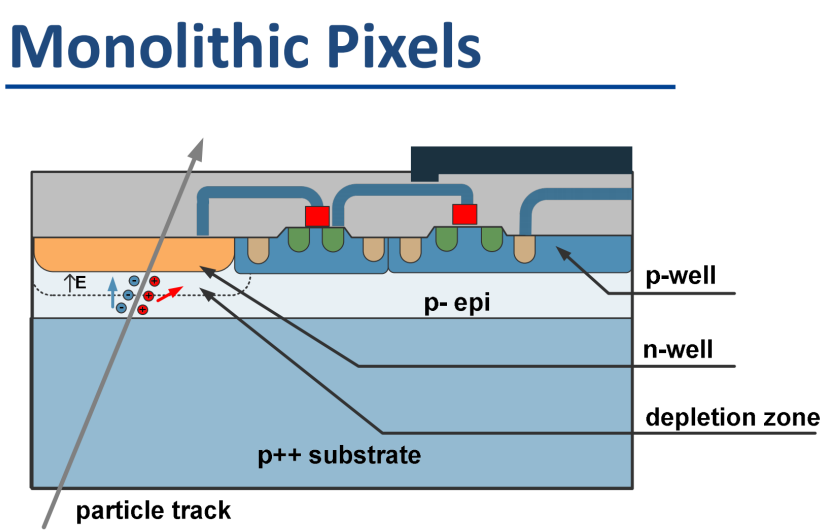
- MOST3项目无指标， CEPC vertex探测器最终需要承受$\mathbf{10^{13}}\boldsymbol{n_{eq}}\cdot\boldsymbol{cm^{-2}}$
- 辐照后束流测试表明
  - 探测效率 >99% @ $\mathbf{10^{13}}\boldsymbol{n_{eq}}\cdot\boldsymbol{cm^{-2}}$ ， 探测效率>95% @ 1.5* $\mathbf{10^{14}}\boldsymbol{n_{eq}}\cdot\boldsymbol{cm^{-2}}$



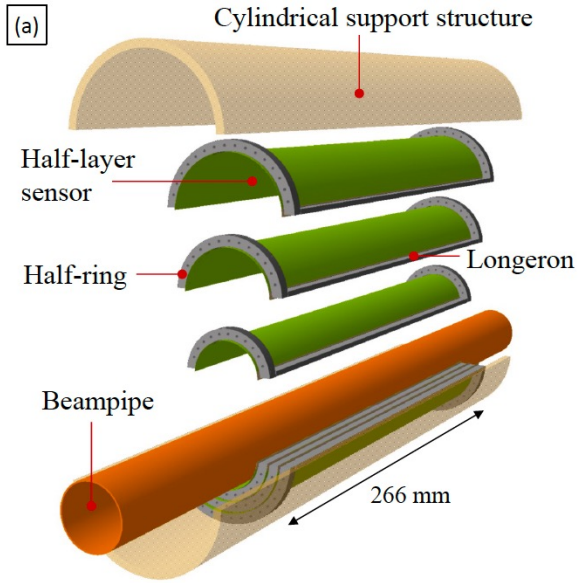
CEPC ref-TDR中的顶点探测器

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder options)
  - Alternative: Ladder design based on CMOS MAPS

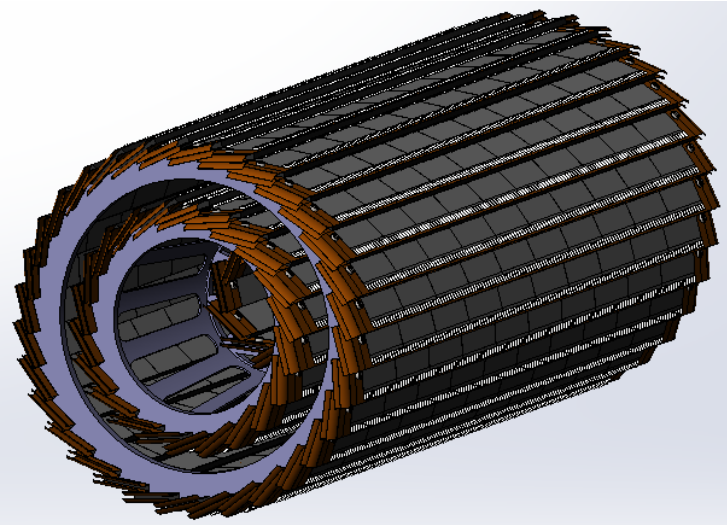
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



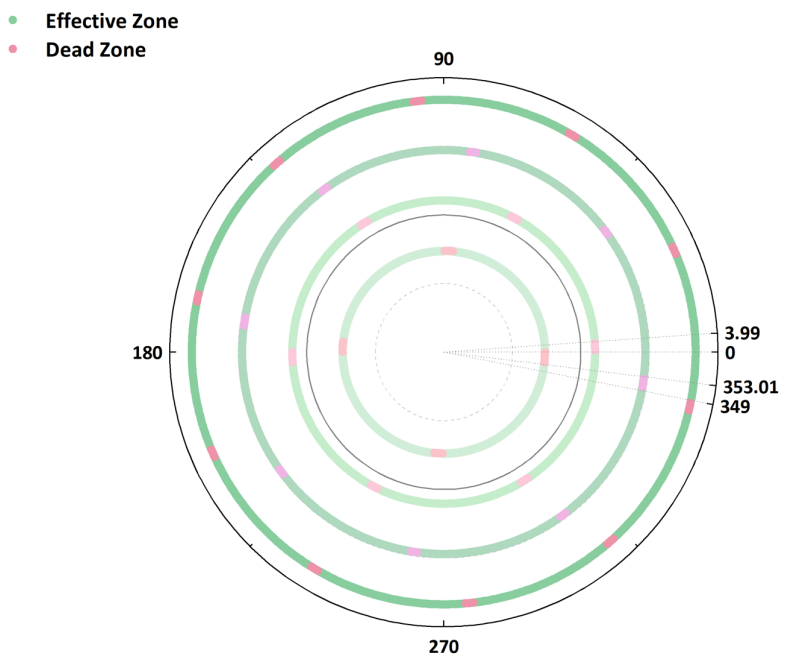
Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

CEPC ref-TDR中的顶点探测器

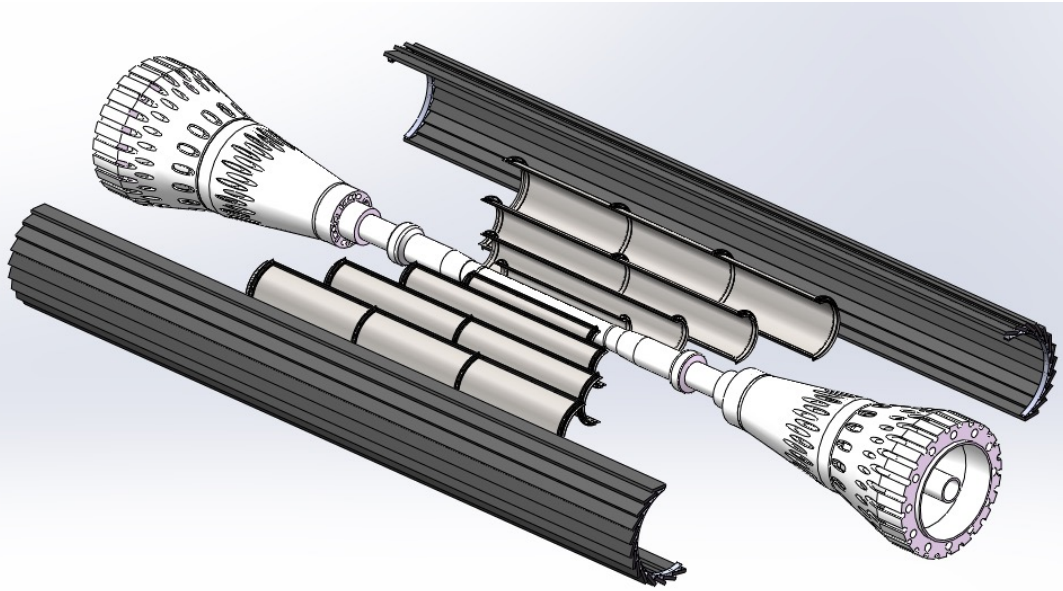
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area

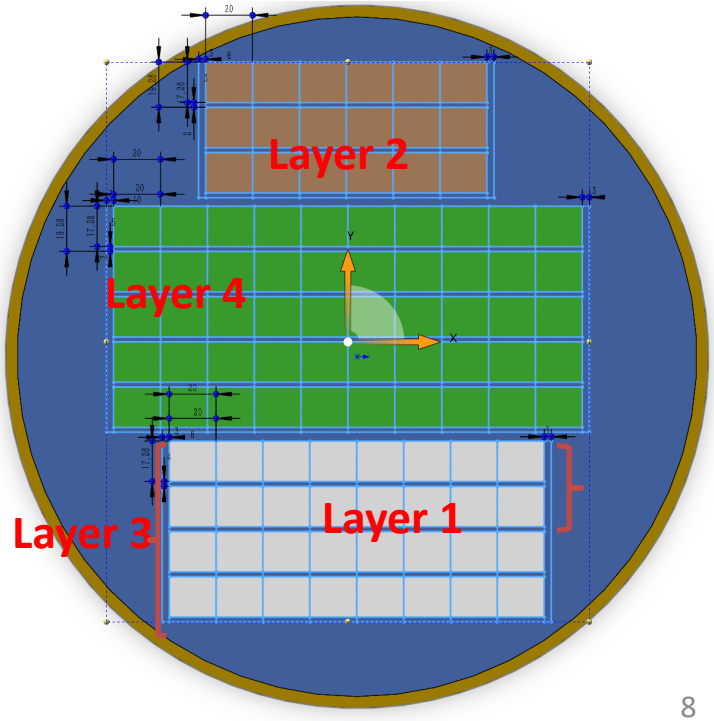


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-40 mm	0.33% X0
Total		0.57% X0

Long barrel layout (no endcap disk)
to cover cos θ<=0.991





CEPC ref-TDR中的顶点探测器计数率

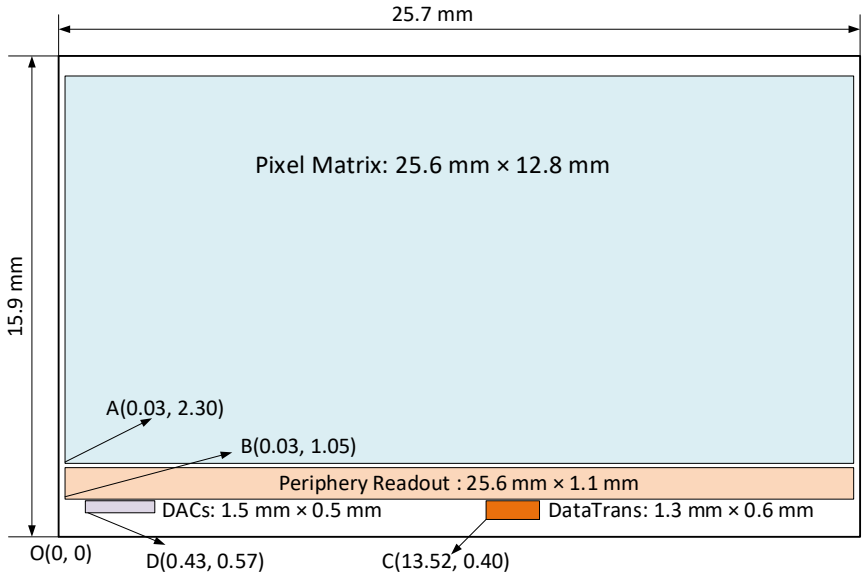
	Hit rate (MHz/cm²)	Data rate@triggerless (Gbps)	Data rate@trigger (Gbps)
Higgs	0.61	0.18	<0.01
W	3.16	0.98	<0.01
Low lumi Z pole	3.9	1.2	~0.1

Hit density from background (from CDR)

- Data rate is dominated by background from pair production
- Estimated based on old version of software
- More details in Haoyu's MDI talk this afternoon
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1.2Gbps per chip for triggerless readout

CEPC ref-TDR中的功耗

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation



	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm^2
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~40 mW/cm^2

总结与讨论

- 太初芯片的时间性能与功耗均达到项目要求
  - 相关测量会尽快发表文章
- CEPC ref-TDR中的顶点探测器设计基于65nm CIS工艺
  - 是否可以结合MOST3的课题目标与CEPC ref-TDR的研发?
  - 是否可以用65nm工艺研发顶点探测器芯片?
  - 同时满足3微米分辨，100ns时间分辨率和功耗要求

论文发表情况

题目	时间	刊物
Beam test of a 180nm CMOS Pixel for the CEPC vertex detector	**2024**	**Nucl.Instrum.Meth. A 1059(2024)** 168945

2024年学术交流情况：学术交流与会议报告情况

会议名称		地点	时间	报告类型	题目
CEPC EU workshop	梁志均	法国马赛	2024年4月	大会报告	CEPC detector and physics overview
Pixel 2024	张颖	法国斯特拉斯堡	2024年11月	大会报告	CEPC vertex detector R & D status
ICHEP 2024	梁志均	捷克布拉格	2024年7月	分会报告	CEPC vertex detector R & D status
IAS 高能物理年会	梁志均	香港	2024年1月	分会报告	CEPC vertex detector R & D
CEPC workshop 2024	张颖	杭州			CEPC vertex detector R & D status
中国半导体辐射探测器会议2024	张颖	青岛	2024年5月	大会报告	CEPC vertex detector R & D status
核探测器与核电子学年会	李淑琦	青岛	2024年5月	分会报告	用于CEPC顶点探测器的单片式像素探测器原型样机的研制
中国LHC物理年会	梁志均	青岛	2024年11月	分会报告	CEPC vertex detector R & D status

人才培养情况：培养青年人才的情况

- 培养1名博士后，2名博士生
  - 1名博士后（吴天涯）在2024年出站，就业于南昌大学副教授
  - 2名学生博士毕业（李淑琦，严子越），1名硕士（周佳）
    - 李淑琦、周佳获得所长奖学金奖,