国家重点研发计划 “高能量加速器关键技术研究” 项目2024年会

# HVCMOS设计与测试

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2024年11月29日

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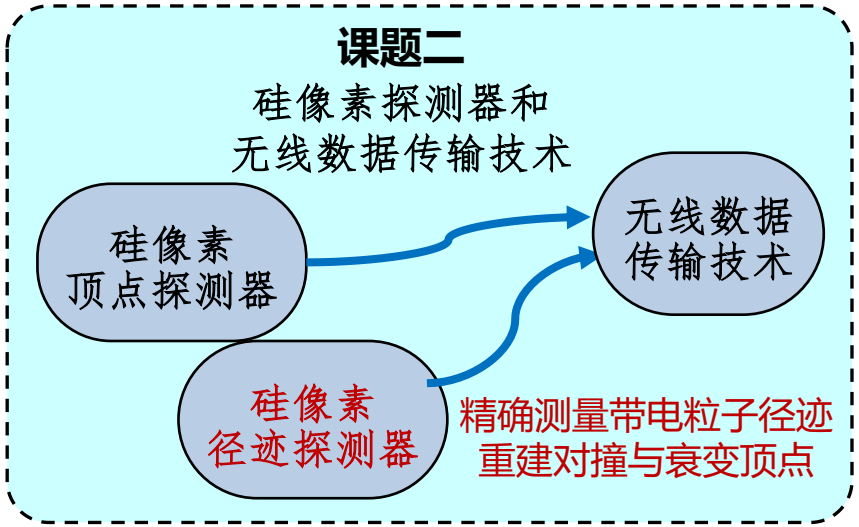
浙江大学
ZHEJIANG UNIVERSITY

# 报告内容

- 研究背景
- 研究进展
- 高压CMOS原理验证芯片：COFFEE2
  - 设计思路
  - 初步测试结果
- 研究计划

# 研究目标

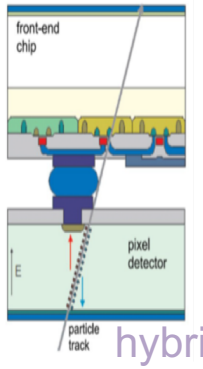
- 针对课题二中“硅像素径迹探测器”，研发新型高压CMOS技术
- 未来高能对撞机上对带电粒子径迹探测需要：
  - 高定位精度 → 精确测量径迹和带电粒子动量
  - 高时间精度 → 以区分高亮度对撞下前后束团对撞
  - 低功耗 → 避免因散热引入不必要的物质量、影响动量分辨性能



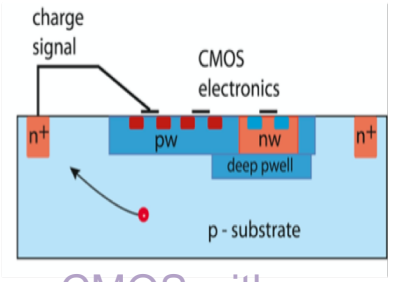

| 参数 | 指标 |
|---|---|
| 位置精度 | 10 μm |
| 时间精度 | 10 ns |
| 功耗 | 200 mW/cm$^2$ |

# 国内外研究现状

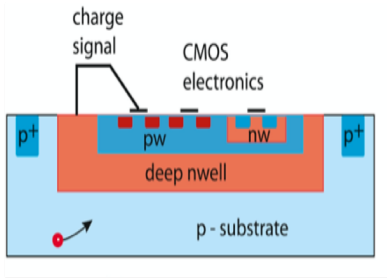
- 高压CMOS是径迹探测理想技术：
  - 利用商业CMOS技术，集成探测器和前端读出，具有良好性价比
  - 良好的抗辐照性能，适用于高能对撞
  - 电荷收集速度快
- 国外高压CMOS技术集中在180nm和150nm工艺制程
  - 应用于Mu3e等实验
  - 尚无能完全满足本项目需求的芯片



hybrid



CMOS with small electrode

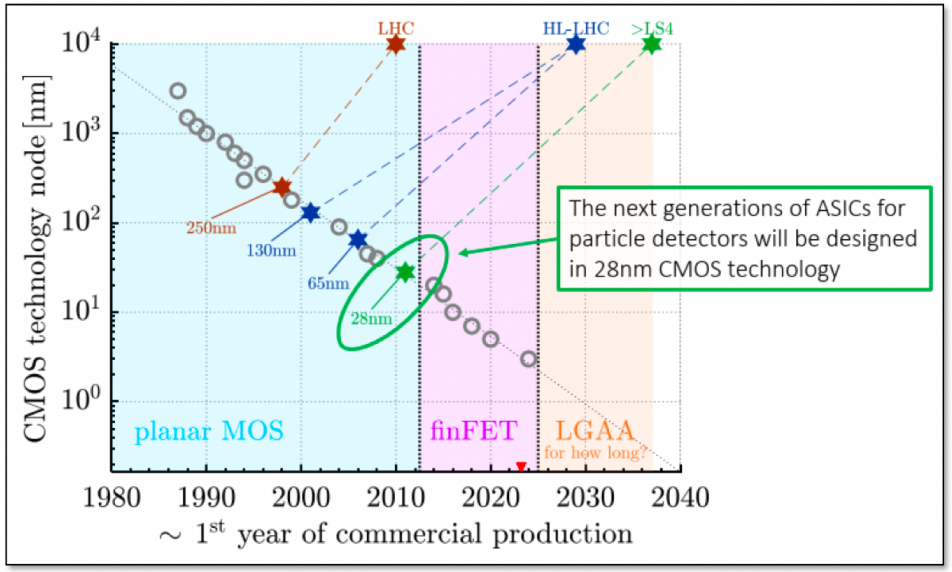


HVCMOS

| Chip | Pixel size [μm²] | Array size | Noise [e-] | Power density [mW/cm²] | Fluence [$n_{eq}$/cm²] |
|---|---|---|---|---|---|
| AMS/TSI 180 nm | | | | | |
| ATLASPix1 | 60 × 50 | 56 × 320 | ~200 | 170 | $1 \times 10^{15}$ |
| ATLASPix3 | 50 × 150 | 372 × 132 | ~60 | ~150 | $1.5 \times 10^{15}$ |
| MuPix10 | 80 × 80 | 256 × 250 | 75 | 190 | |
| MightyPix1 | 55 × 165 | 29 × 320 | | | |
| LFoundry 150 nm | | | | | |
| LF-Monopix1 | 50 × 250 | 129 × 36 | ~200 | ~288 | $10^{15}$ |
| LF-Monopix2 | 50 × 150 | 340 × 56 | ~100 | ~400 | |
| RD50-MPW1 | 50 × 50 | 40 × 78 | | | $2 \times 10^{15}$ |
| RD50-MPW2 | 60 × 60 | 8 × 8 | ~50 | | $2 \times 10^{15}$ |
| RD50-MPW3 | 62 × 62 | 64 × 64 | ~900 | | |
| RD50-MPW4 | 62 × 62 | 64 × 64 | 480 | ~600 | $3 \times 10^{16}$ |
| CACTUS | 1000 × 1000 | 7 × 6 | ~2k | | |

# 为什么要探索先进制程？

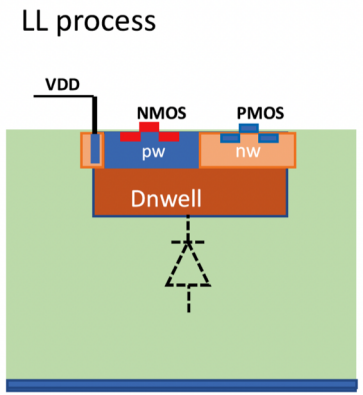
- 本项目计划基于国产55nm先进制程探索高压CMOS传感器芯片
- 先进性驱动
  - 单位面积内集成更高电路密度
  - 实现更复杂功能
  - 同时有望降低功耗
- 可靠性驱动
  - 高能实验研发周期较长，研发时所用工艺在批量生产时可能遇到淘汰停产风险
    - TSI 2023年被收购停止HVCMOS 180nm服务，直接影响Mu3e、LHCb Mighty Tracker等实验生产
  - 国际主流研发依赖国外代工厂！需探索可用的国内工艺
- 欧洲粒子物理战略规划探测器路线把先进制程CMOS研发置于半导体探测器研发首要位置



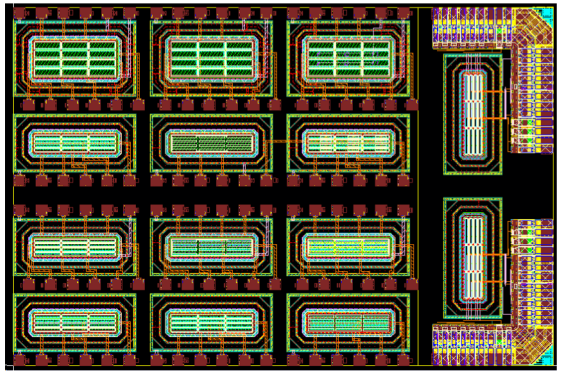

P. Moreira @ CEPC workshop, Oct 2023

# 前期研究基础（COFFEE1）

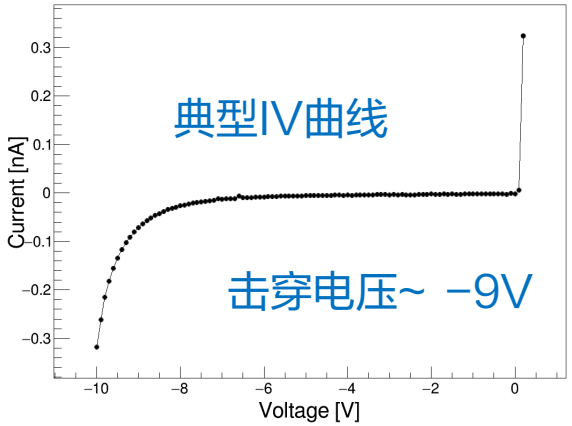
- SMIC 55nm Low-Leakage工艺
  - 非高压工艺，非高阻衬底
  - 存在与HV工艺相似的深N阱结构
  - 2022年提交3mm*2mm MPW流片
  - 初步验证传感器结构

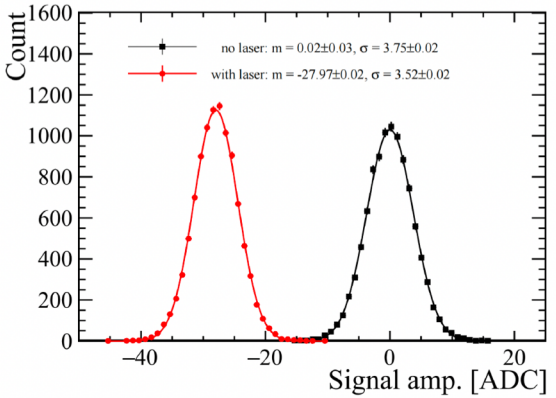



55nm LL工艺
截面示意图



COFFEE1 芯片版图

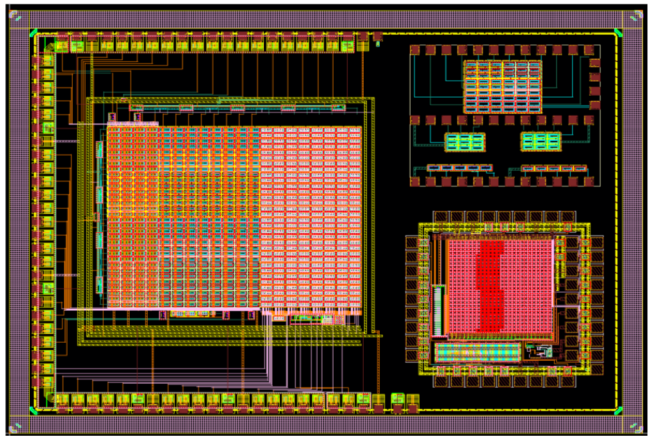


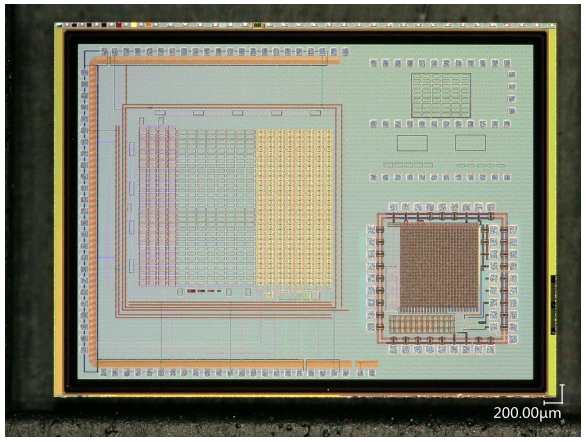

Sensor对激光的信号响应

# 首个高压CMOS原理验证芯片

- 首个55nm工艺高压CMOS原理验证芯片 COFFEE2 提交流片
  - 2023年8月提交 4mm*3mm MPW流片用于初步工艺验证



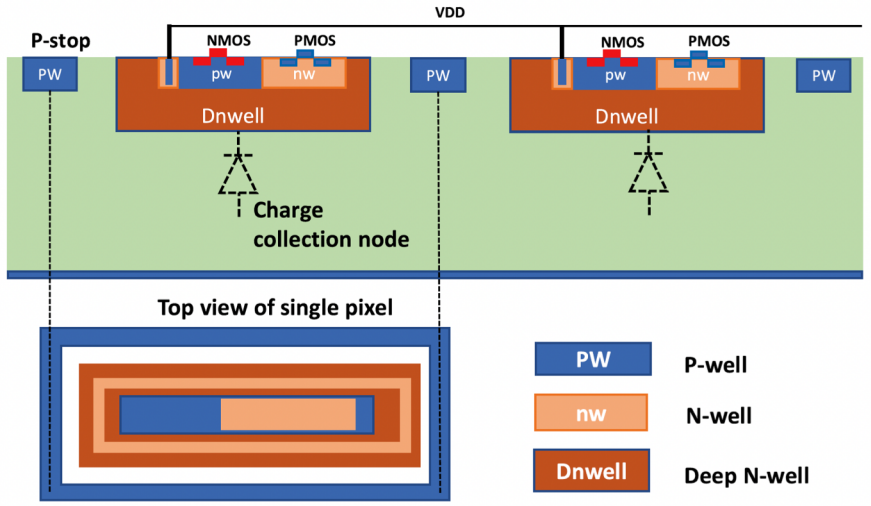
COFFEE2 芯片版图




COFFEE2 芯片版图

COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS



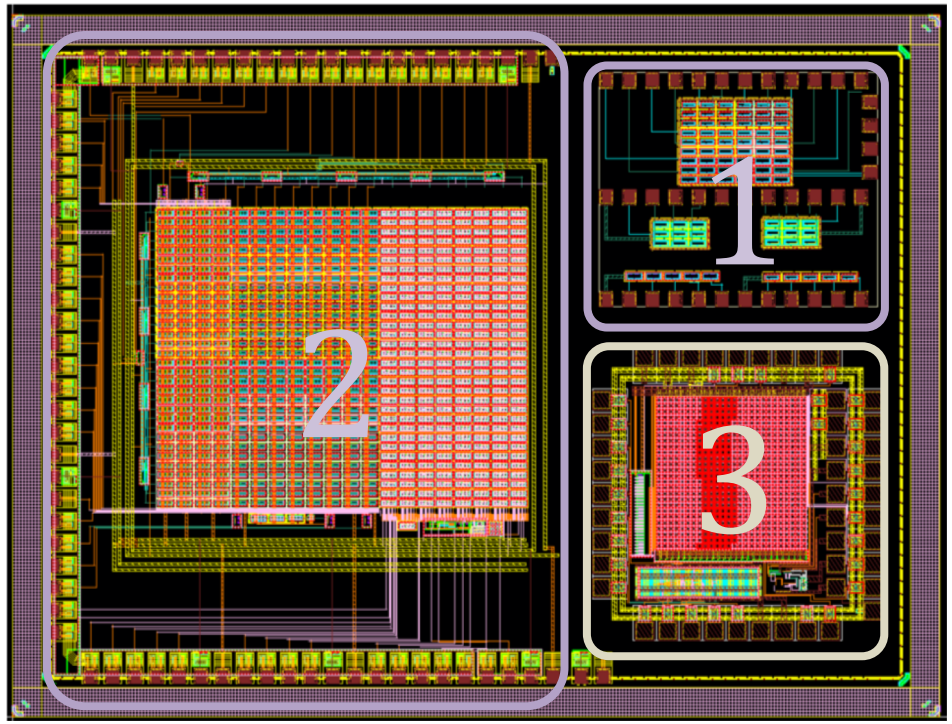

55nm 高压CMOS工艺截面示意图

# COFFEE2 设计

32 × 20 pixel matrix with various diodes and in-pixel amplifier or discriminator designs for process validation

- 34 × 68 $\mu m^2$
- 5/10/15um gap btw pixels
- With/ w.o. p-stops
- 3 versions in-pixel electronics

对应10 um空间分辨率

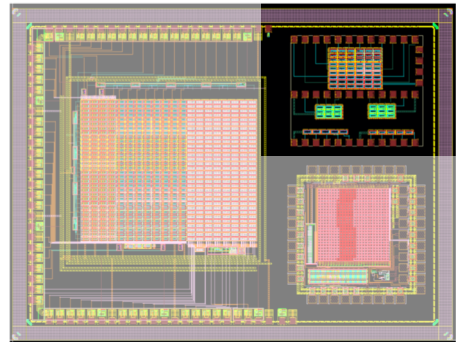


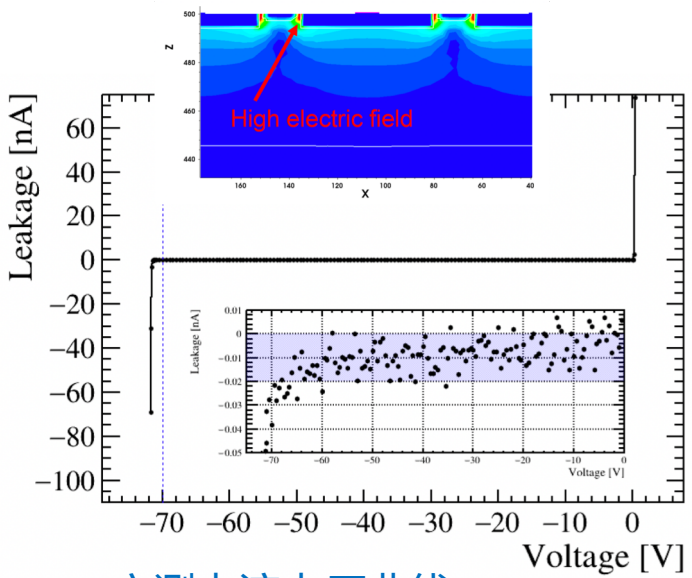

Passive diode arrays, each has 3×4 pixels of size 34 × 68 $\mu m^2$ for study on sensing diode and charge sharing

26 × 26 pixel matrix of 25 × 25 $\mu m^2$ pixels with digital readout periphery for novel electronics structure study

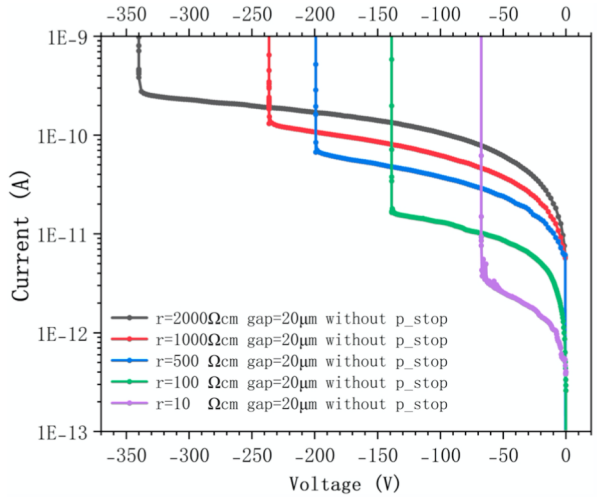
# 传感器主要测试结果

- 击穿电压 – 70V
  - 击穿时尚未达到全耗尽，与仿真结果一致
  - 击穿发生在深n阱边缘（与p阱接触部分）
  - 仿真线上高阻衬底可显著提高击穿电压和耗尽区
- 单个像素电容30-50fF
- 暗电流~0.01nA，$10^{14}\ n_{eq}\ \mathrm{cm}^{-2}$ 辐照后升至~1nA

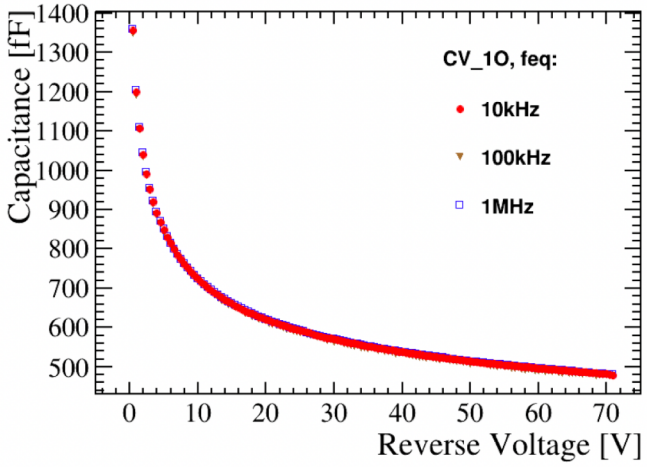





实测电流电压曲线



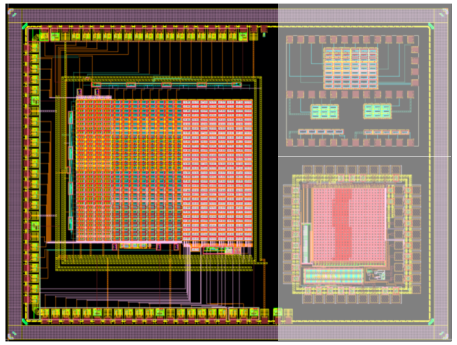

不同衬底阻值IV曲线仿真

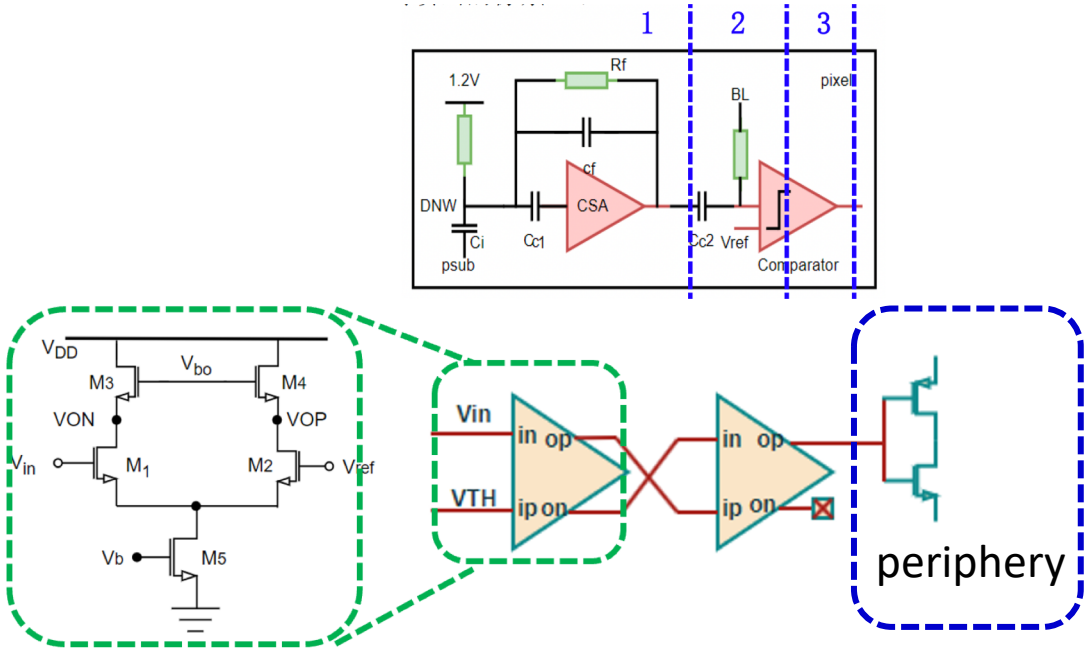


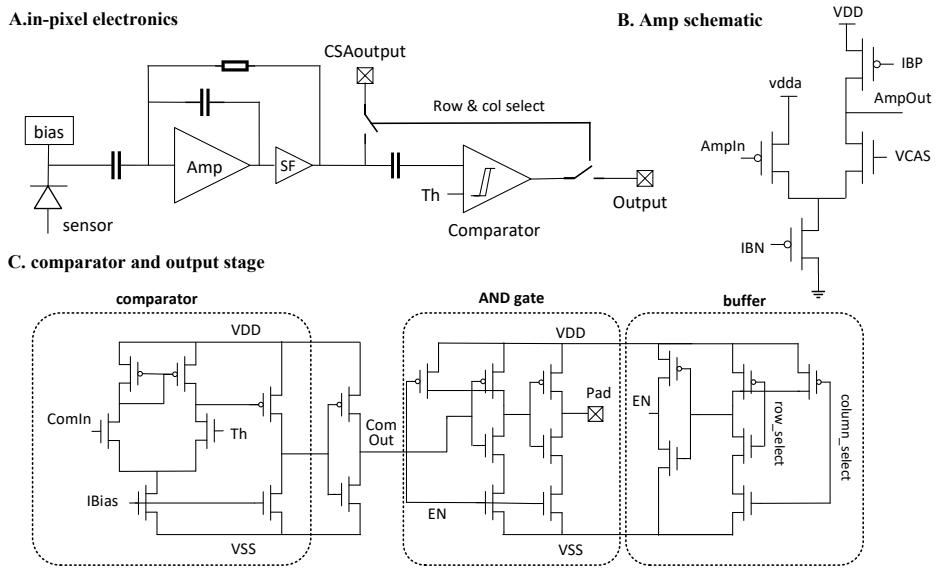

电容电压曲线

# COFFEE2 电路设计

- 三种像素内电路设计：
  - 1 – 仅有放大器
  - 2 – 放大器 + NMOS 比较器 → ADC 在阵列外
  - 3 – 放大器 + CMOS 比较器, 数字化读出
- 通过行、列选通选中一个像素读出

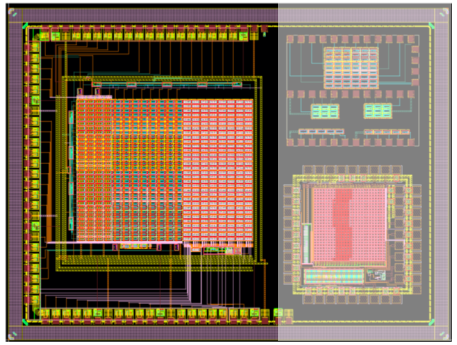




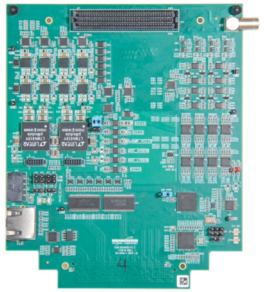
# COFFEE2测试设置

- 读出测试系统：
  - 专用芯片载板 → CaR 测试板 → Xilinx KC705 FPGA → PC



### Control and Readout (CaR) board

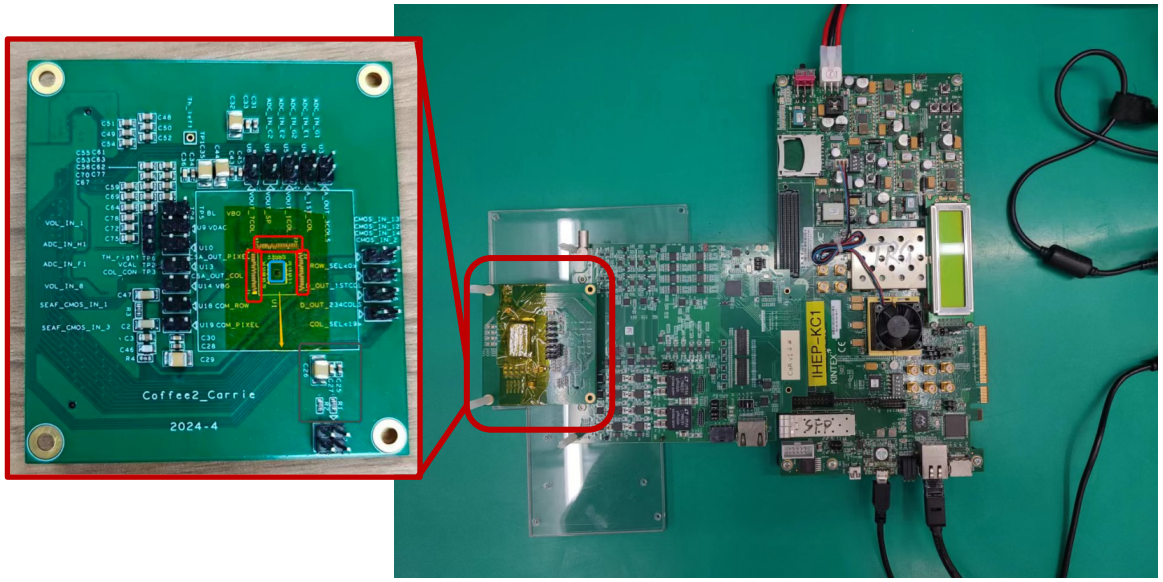
| Feature | Description |
|---|---|
| Adjustable Power Supplies | 8 units, 0.8 – 3.6 V, 3 A |
| Adjustable Voltage References | 32 units, 0 – 4 V |
| Adjustable Current References | 8 units, 0 – 1 mA |
| Voltage Inputs to Slow ADC | 8 channels, 50 kSPS, 12-bit, 0 – 4 V |
| Analog Inputs to Fast ADC | 16 channels, 65 MSPS, 14-bit, 0 – 1 V |
| Programmable Injection Pulsers | 4 units |
| Full-Duplex High-Speed GTx Links | 8 links, <12 Gbps |
| LVDS Links | 17 bidirectional links |
| Input/Output Links | 10 output links, 14 input links, 0.8 – 3.6 V |
| Programmable Clock Generator | Included |
| External TLU Clock Reference | Included |
| External High-Voltage (HV) Input | Included |
| FEAST Module Compatibility | Supported |
| FMC Interface to FPGA | Included |
| SEARAY Interface to Detector Chip | 320-pin connector |

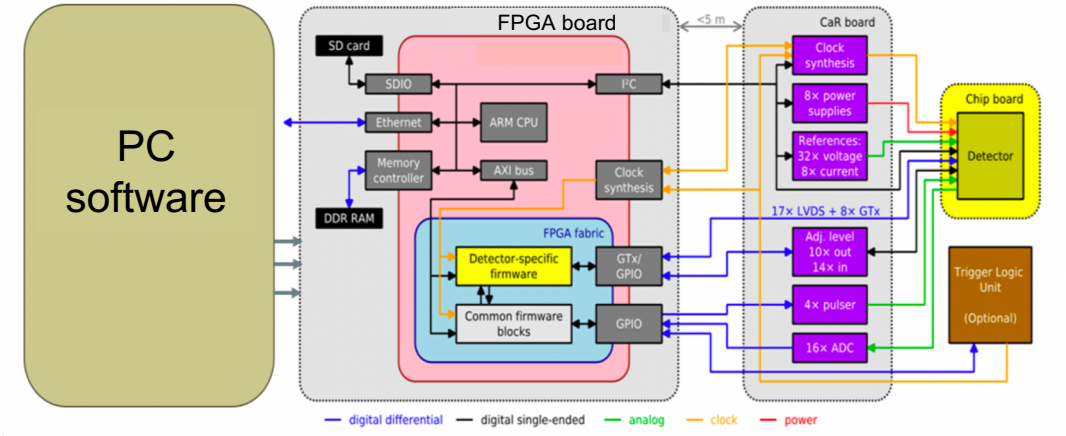


https://gitlab.cern.ch/Caribou/hardware/carboard

Resources for various target applications

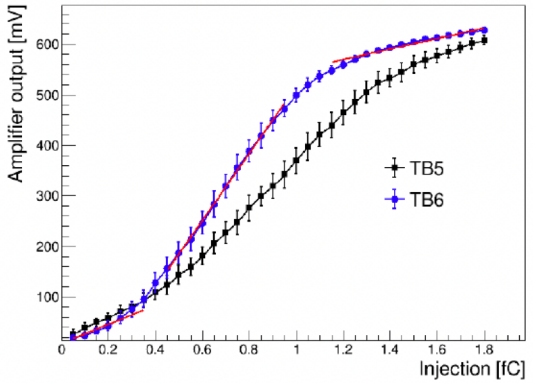
**20 CaR boards v1.4** produced and distributed within RD50 common project

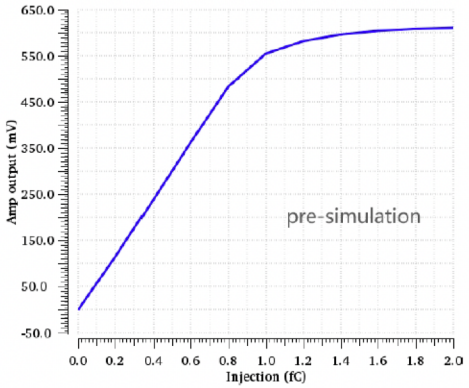


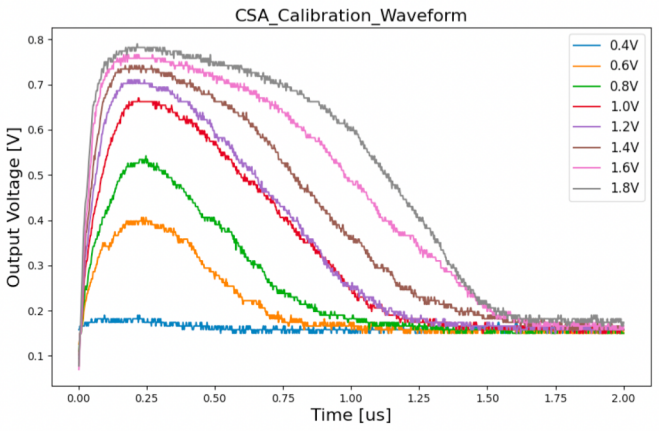
# 电路初步测试结果

- 利用电荷注入功能可研究放大器响应
  - 线性区与仿真基本一致
  - 像素间有不均匀性
- 观察到对激光信号、放射源信号响应

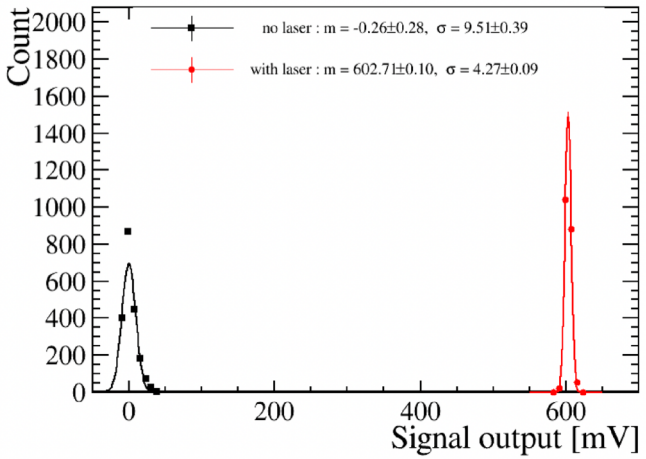


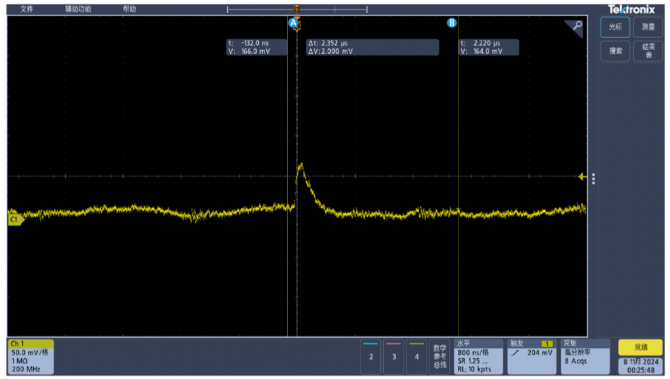

放大器输出幅度与注入电荷量关系（左）实测（右）仿真




放大器输出信号




激光信号响应

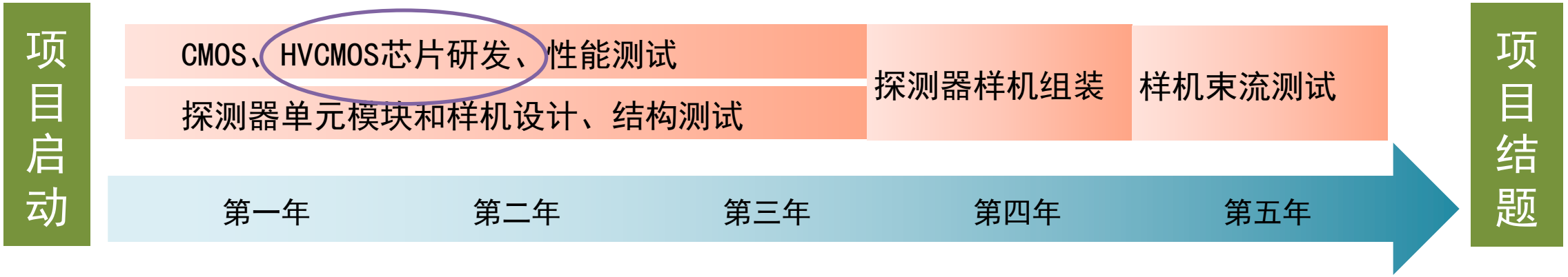


$^{55}$Fe放射源响应

# 研究计划推进

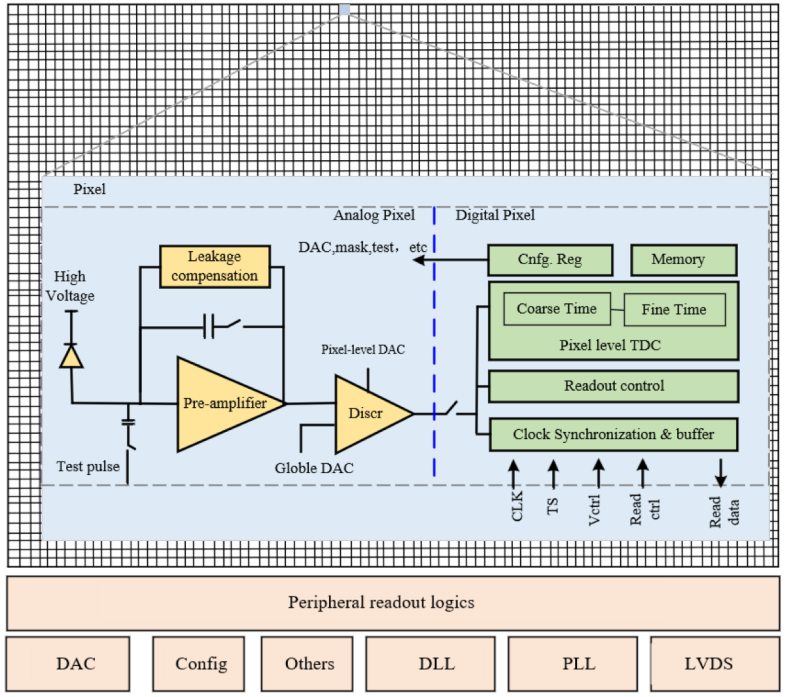
- HVCMOS芯片研发定期召开讨论会
- 未来计划两次小规模拼版流片
  - 验证读出架构
  - 优化电路性能
- 基于测试和芯片性能开展探测器单元模块设计

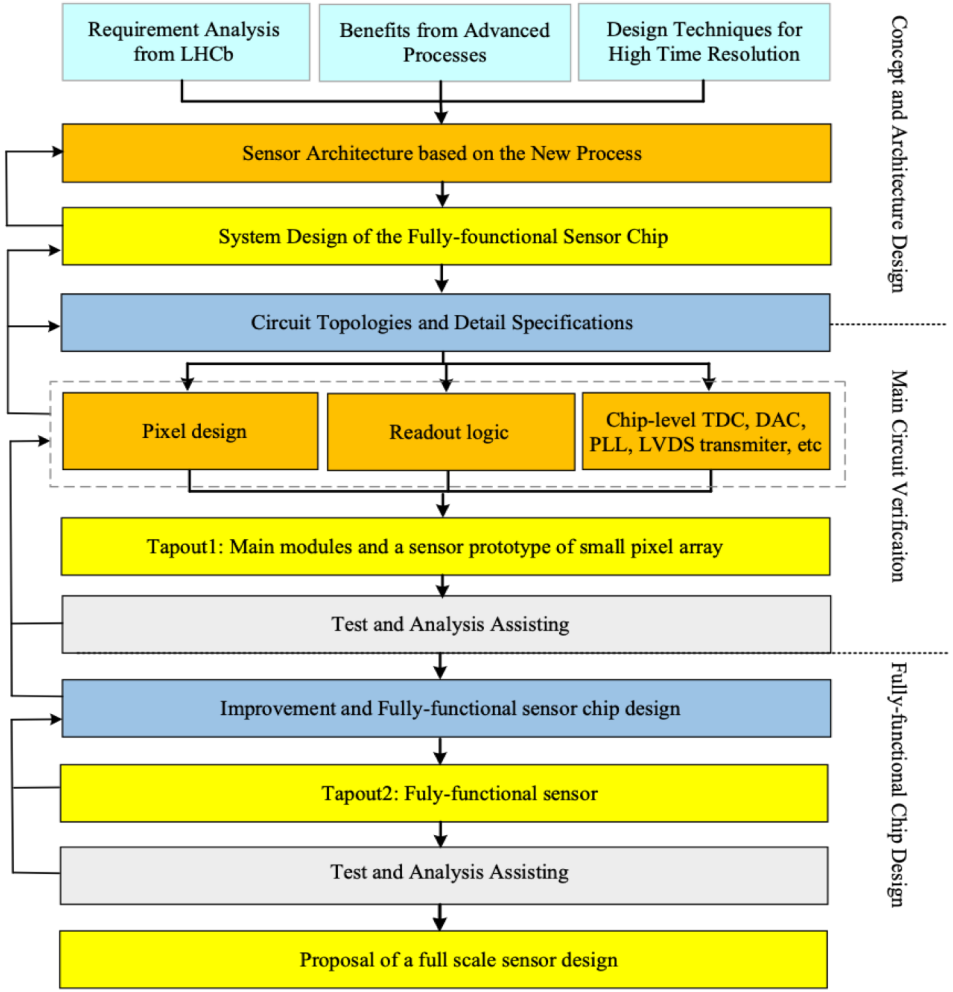
October 2024
Oct 15 HVCMOS meeting
August 2024
Aug 20 HVCMOS meeting
July 2024
Jul 09 HVCMOS meeting
April 2024
Apr 16 HVCMOS meeting
January 2024
Jan 09 HVCMOS meeting
December 2023
Dec 19 HVCMOS meeting



# 设计计划（读出构架）

- 分步骤开展全功能原理验证芯片设计
  - 架构设计 → 关键功能模块验证 → 全功芯片设计
- 新型读出架构
  - 含有像素内TDC的异步阵列读出



# 设计计划（时间分辨）

$$\sigma_t^2 = \sigma_{TW}^2 + \sigma_J^2 + \sigma_{TDC}^2$$

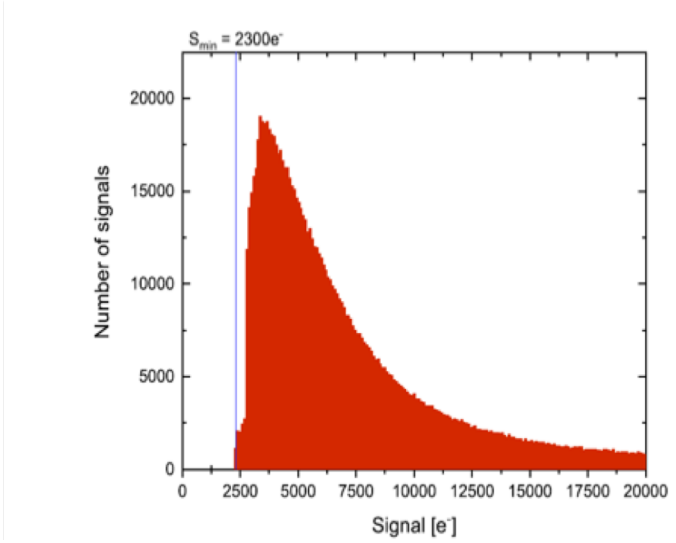
Total timing resolution

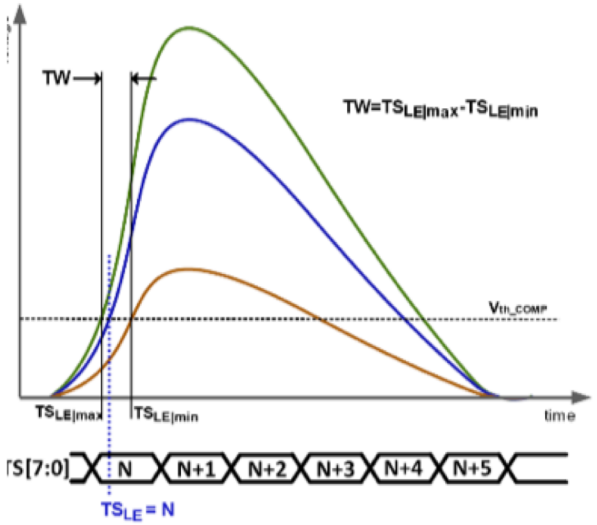
Time walk

Jitter

TDC

- 针对时间不确定性来源，分别优化电路设计



# 发表文章和会议报告

- 文章1篇：
  - Feasibility study of CMOS sensors in 55 nm process for tracking， NIM A 1069 (2024) 169905

- 会议报告7次：
  - 项治宇 @ Chinese LHC Physics workshop, 2024.11 青岛
  - 李一鸣，周扬，邓建鹏，李乐怡 @ CEPC workshop, 2024.10 杭州
  - 周扬 @ 第四届半导体探测器研讨会，2024.05 青岛
  - 李一鸣 @ Hiroshima Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), 2023.12 加拿大温哥华

# 总结

- 首个基于国产55nm工艺原理验证芯片COFFEE2初步测试取得结果，实现工艺验证
- 未来将针对项目指标实现小型像素阵列设计
- 按计划开展研发，已发表1篇文章、多次会议报告