CEPC CMOS Strip Tracker

Xin Shi

On behalf of CMOS Strip Tracker Team

2024.12.06

Ref TDR Progress

- ✓ Add description for electronics
- ✓ Add prospects and plan
- ✓ Add reference to bib file

5.3.1.2 CMOS strip R&D

Responsible person: Xin SHI

Because of its good position resolution, high charge response sensitivity and low material budget, silicon strip detectors are widely used in high-energy physics (HEP) and nuclear physics experiments. Both the past HEP experiments such as Argus, Aleph, CDF and current running experiments at CERN such as ATLAS, CMS, LHCb and ALICE have used silicon strip detectors. In addition, the ATLAS phase 2 upgrade will also utilize the silicon strip as it's main component of the all-silicon tracker, which can be as large as 160 m^2. The sizes of these silicon strip detectors are illustrated in Fig. 5.17. As one can see, with the size of the tracker on the collider increases, the coverage area of the corresponding silicon strip detector enlarged as well. Consequently, silicon strip detectors will be a reliable candidate for future tracking detectors.

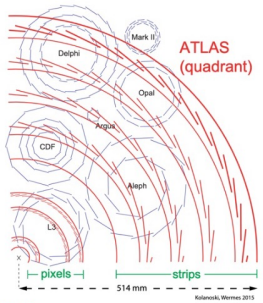


Figure 5.17: The history of strips in HEP experiments and ATLAS ITk strips.

To meet the physics requirement of CEPC Inner Tracker, the high spatial resolution impose challenging pitch si strip detector design and fabrication. To reach less than 10 μm spatial resolution, a pitch size less than 30 μm has achieved, which will be a nightmare for conventional wire bonding process. For example, ATLAS ITk strip wire bo is already reached 4 layers for wires per chip even with just 75.5 μm pitch size, and more than 5000 wires to be on just one strip module, as illustrated in Fig. 5.18. Further more, highly customized silicon sensor fabrication pr relying on a few foundries (in ATLAS and CMS case, only one company is used) to provide large quantities of sensor for more than three years imposes big risk for the project. Apparently, new method to construct the silicon strip de has to be explored.

As the mainstream in the semiconductor industry, CMOS process has been widely used in variety of fields. It pre a natural combination of the active detection sector and readout electronics sector to make them into a monolithic Compared with the CMOS pixel detector, the CMOS strip detector has the advantage of relative simple readout sin readout ASIC only located at the end of strip and there is negligible interference between sensors and ASIC. The

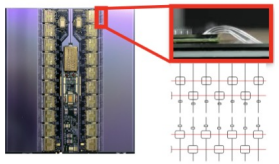


Figure 5.18: The ATLAS Inner Tracker (ITk) strip module assembled at IHEP. The right-hand side shows bonding wires and the bonding pad schematics.

Table 5.3: CSC Parameters (v1.3)

Strip width	10 μm
Strip pitch	20 μm
Strip number/ chip	1,024
Chip size	$2.1 \times 2.3\ cm^2$ (active area: $2.05 \times 2.05\ cm^2$)
Spatial resolution	$\sigma \sim 5\ \mu m$
Time resolution	$\sim 3\ ns$
Power consumption	$\sim 80\ mW/cm^2$
Data size per hit	32 bits (10b BXID, 10b address, 6b TOT + other 6 bits)
Event rate / chip	Maximum ~ 0.25 Gbps
LV / HV	1.8V/ 200V
Wafer resistivity	2k Ω cm
Technology node	180 nm

difference between CMOS strip and CMOS pixel is shown in Fig. 5.19.

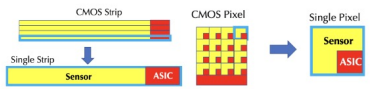


Figure 5.19: The difference between CMOS strip and CMOS pixel.

The first large sized CMOS passive sensor with 4.1 cm strip length and 75.5μm pitch has been fabricated using $3 \sim 5k\Omega$ wafer with LFoundry 150 nm stitching process. The electrical tests with Sr-90 source of the CMOS strip sensor indicates the full depletion can be reached around 30 V for 150μm thickness and the charge collection efficiency reached close to 100%. This confirms the feasibility of CMOS strip sensor as a valid research path. So far, there is no integrated CMOS strip with both sensor and readout ASIC yet.

The ultimate goal for the team is to fabricate a CMOS strip chip (CSC) targeting 20μm pitch, so that a high spatial resolution (less than 5μm), good time resolution (within 5 ns), and high charge resolution (better than 20%) can be reached. The schematic of the CSC chip as well as the CMOS circuit in the periphery is shown in Fig. 5.20 with the chip parameters shown in Table 5.3. The electronics is composed of Amplifier, Shaper, Discriminator, TDC, FIFO, and Serializer, as shown in the CSC1 Design Diagram5.21.

To start with, the team has conducted a comprehensive fast simulation of the minimum ionizing particle (MIP)

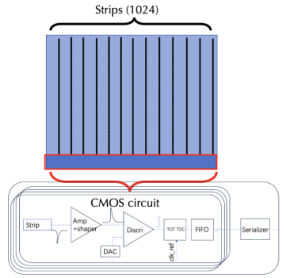


Figure 5.20: Schematic of the CSC chip with 1024 strips on top and the CMOS circuit in the bottom periphery.

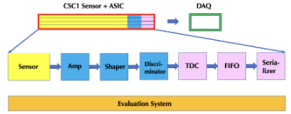


Figure 5.21: Design diagram of CSC1.

and laser response signals for the CMOS Strip Chip utilizing the team developed open-source co simulation workflow inside RASER is sketched in Fig. 5.22. Firstly, a detector geometry is create based on DevSim, in which the electric field and carrier distribution can be calculated. Secondly is generated by Geant4, and the deposited energy is converted into carrier excitation. After th and diffuse, an induced current is generated on the readout electrode, followed by amplification simulated by NGSpice front-end electronics. Finally, With noise simulation, statistical results for ar and dE/dx can be evaluated, allowing for the determination of the detector's time, spatial, and ener

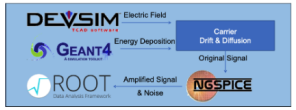


Figure 5.22: Simulation work flow by RASER

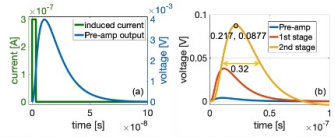


Figure 5.25: Electronics for CSC using the ABCStar as a reference. After injecting 1 fC charge, the signals (a) before and after the Pre-amp, (b) after every stage.

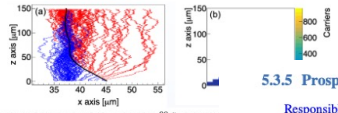


Figure 5.26: Visualization of (a) carrier drift paths after ^{90}Sr injectio

We have developed a strip detector model based on XXX, integrated with a CMOS processing design, as ill in Fig. 5.23, each strip readout is equipped with an n-plus well connected to the cathode, along with two p-stops s neighboring readouts to reduce the charge sharing effect.

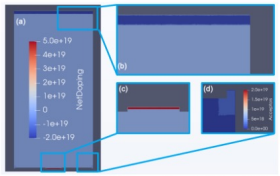


Figure 5.23: Doping profile of (a) the sensor, (b) p-contact (c) n-well, (d) p-stop.

We have evaluated the in-circuit properties of the detector, including the current-voltage (I-V) and capacitance-voltage (C-V) relations. The C-V relationship indicates that the detector reaches full depletion at 30 V. Meanwhile, the I-V relationship shows a relatively mild leakage current of 1uA at operating voltages. These results are shown in Fig. 5.24.

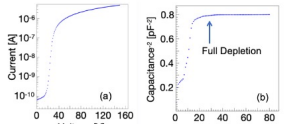


Figure 5.24: Electrical properties of CSC sensor simulation (a) I-V and (b) C-V.

To validate the electronics simulation procedure. we simulated the ATLAS ABCStar amplifier, which consists of three stages: a preamplifier, a first boost amplifier, and a second amplifier with a shaper. This design is with good noise tolerance. The circuit achieves a gain of 87.7 mV/fC, a rise time of 21.7 ns, and a waveform full width at half maximum (FWHM) of approximately 32 ns. These results are consistent with the ABCStar data, which reports a gain of 85 mV/fC, a rise time of 22 ns, and an FWHM of 34 ns, as shown in Fig. 5.25.

Finally, we use both ^{90}Sr as MIP and 660 nm wavelength laser in Geant4 to simulate the response of the detector. The drift paths of the carrier after ^{90}Sr and laser are shown in Fig. 5.26. The current and voltage response of the sensor are shown in Fig. 5.27 and Fig. 5.28 respectively.

5.3.5 Prospects and plan

Responsible person: Qi YAN, Yiming LI, and Xin SHI

Responsible person: Qi YAN, Yiming LI, and Xin SHI

For the sensor technology regarding the HVCMOS process, the priority in the coming few year is to develop a full-functional full-size sensor chip that meets the requirments imposed by the CEPC inner tracker. The development will be performed through a few iterations of chip submissions, including:

- A small pixel array which implement the targeted readout architecture (early 2025);
- One of more small prototypes for performance optimisation (2026);
- A large chip that meets or very close to the production version (2027).

With the small-scale sensor chip key performance will be studied and input will be provided for detector final design and prototyping.

The research and development timeline of CMOS Strip Chip for the next three years is listed in Fig. 5.46 where three versions of the CSC are scheduled to be fabricated. The CSC1 will be mainly focus on the independent CMOS strip sensor and front-end electronics separately. A preliminary reticle design for the CSC1 is sketched in Fig. 5.47. The CSC2 will explore the integration of CMOS strip sensors and circuits together on small area and large pitch. The target of the CSC3 will be the integration of large-area (2cm × 2cm) and narrow-pitch (20μm) monolithic chip.

The prototyping of the detector modules, including the integration process, the supporting and cooling structure will be carried out in parallel to the development of the sensor chips. Small scale sensor chip can already be used to assemble prototypes with sensor, readout and supporting structures as key intermediate steps.

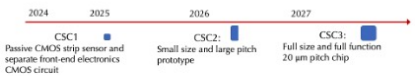


Figure 5.46: CSC Research Timeline.

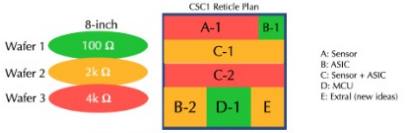
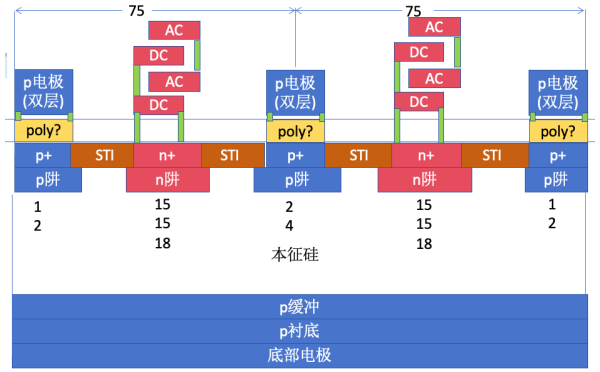
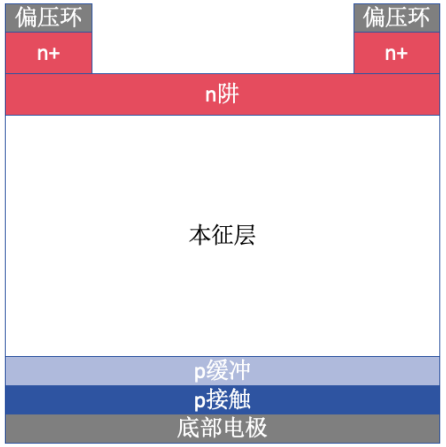


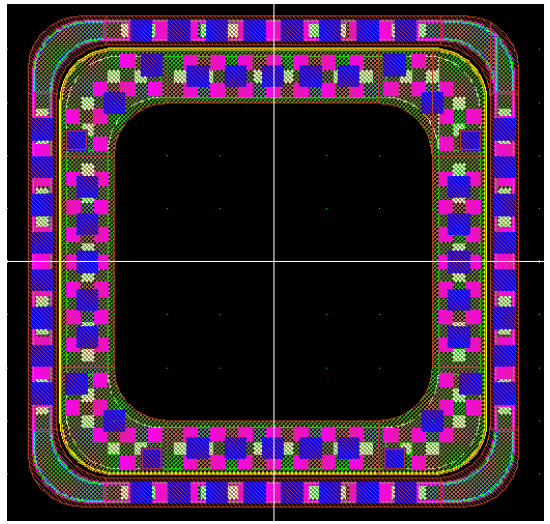
Figure 5.47: CSC1 Reticle Design.

传感器仿真

- 完成 CSC1-A 主传感器设计
  - 间隔75μm， 共256条
  - 小尺寸： 1.05x1.05 道数、条长均减半
  - 大尺寸： 1.05x2.1 仅减半道数
- 完成 mini-diode 设计版图
  - 1x1 cm^2面积
  - 0.8x0.8 cm^2有效探测面积
- 为了保证器件正常工作
  p-stop必须悬空

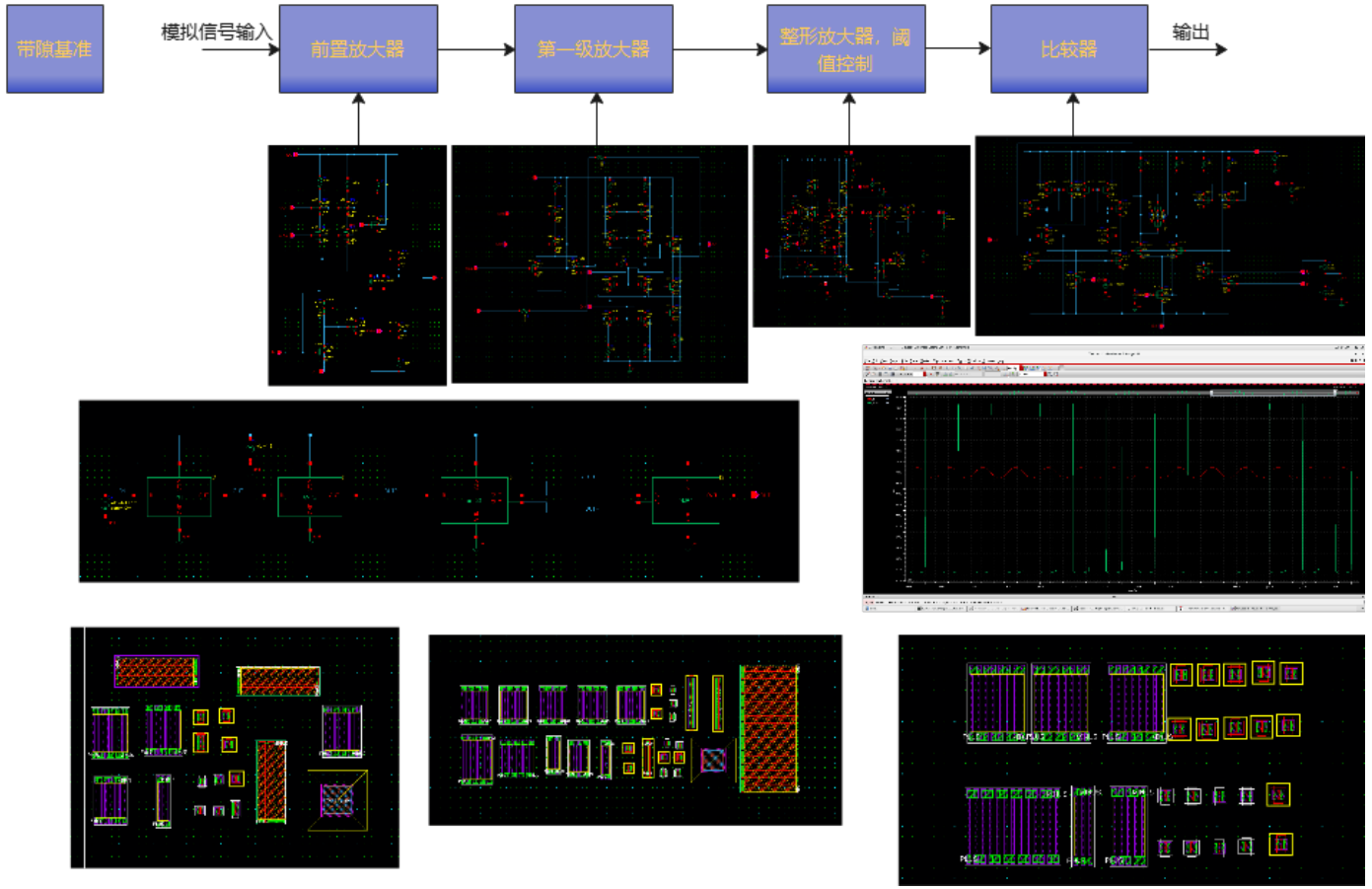




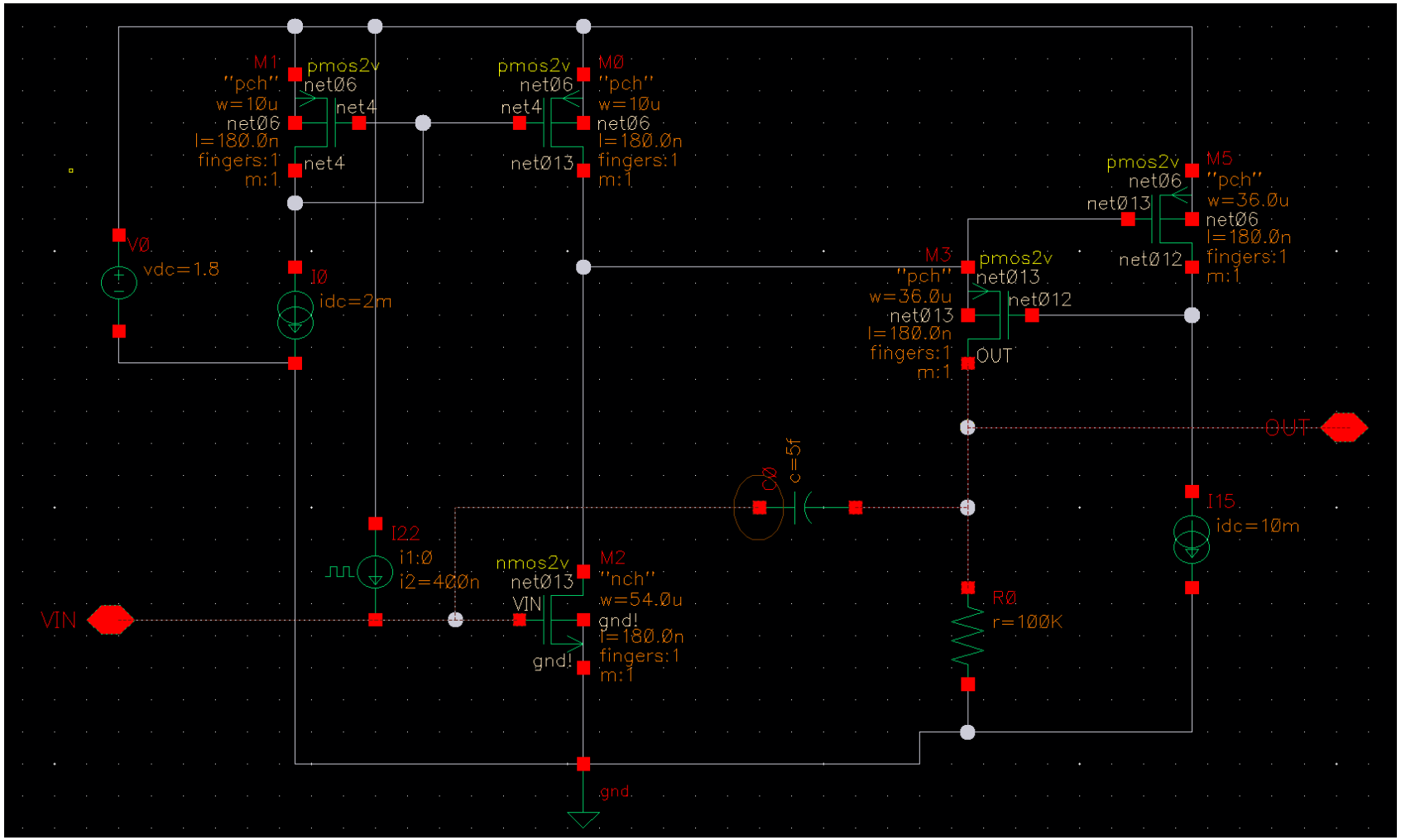


电路仿真进展

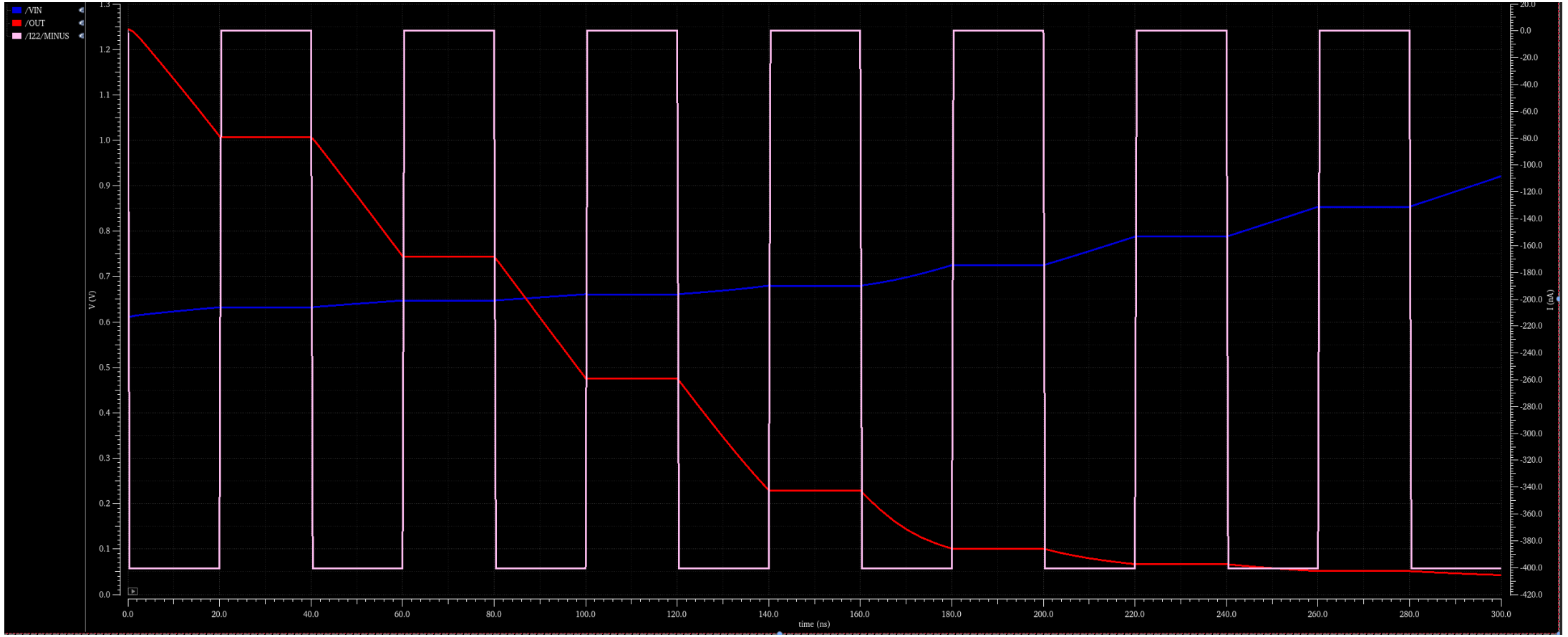
1. 完成了整形放大器，比较器的电路设计，仿真。
2. 完成了 AFE放大器整体仿真。
3. 正在进行版图的布局布图。



CSA 输入电流信号电路

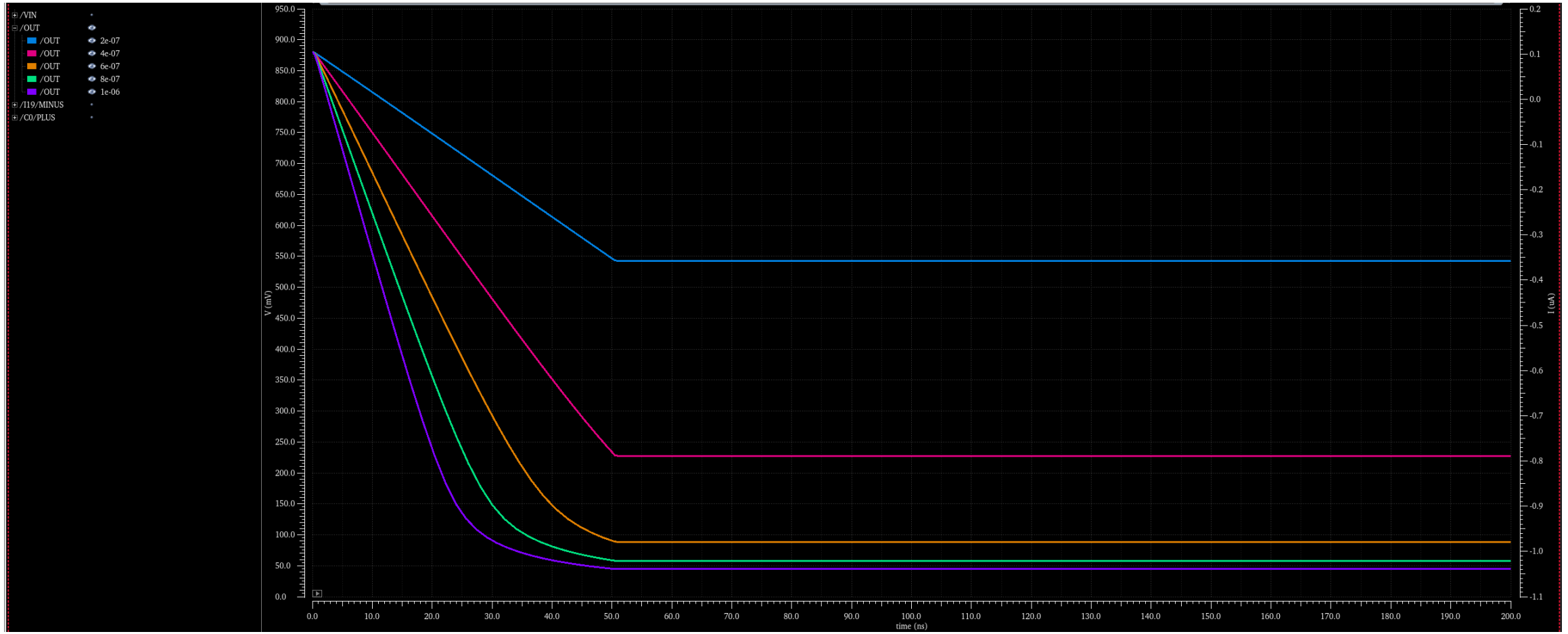


CSA放大效果



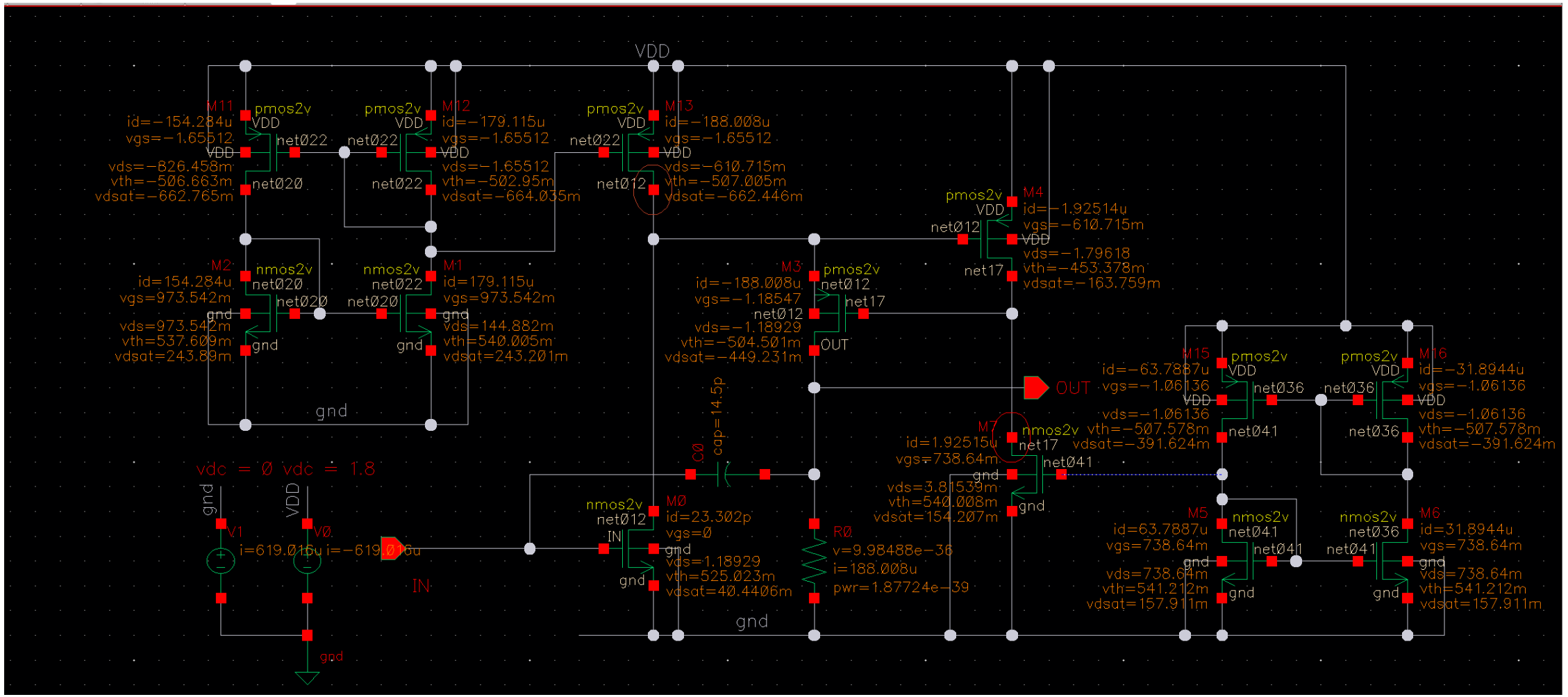
红线代表输入电压，在0ns~180ns范围内，输入电压为600 mV~680 mV之间，电路工作在放大状态，在这范围内输入400 nA的电流信号，输入电压会发生微小的变化（蓝线），输出电压会把输入电压微小的变化放大，产生变化放大的输出电压（红线）。

CSA放大效果

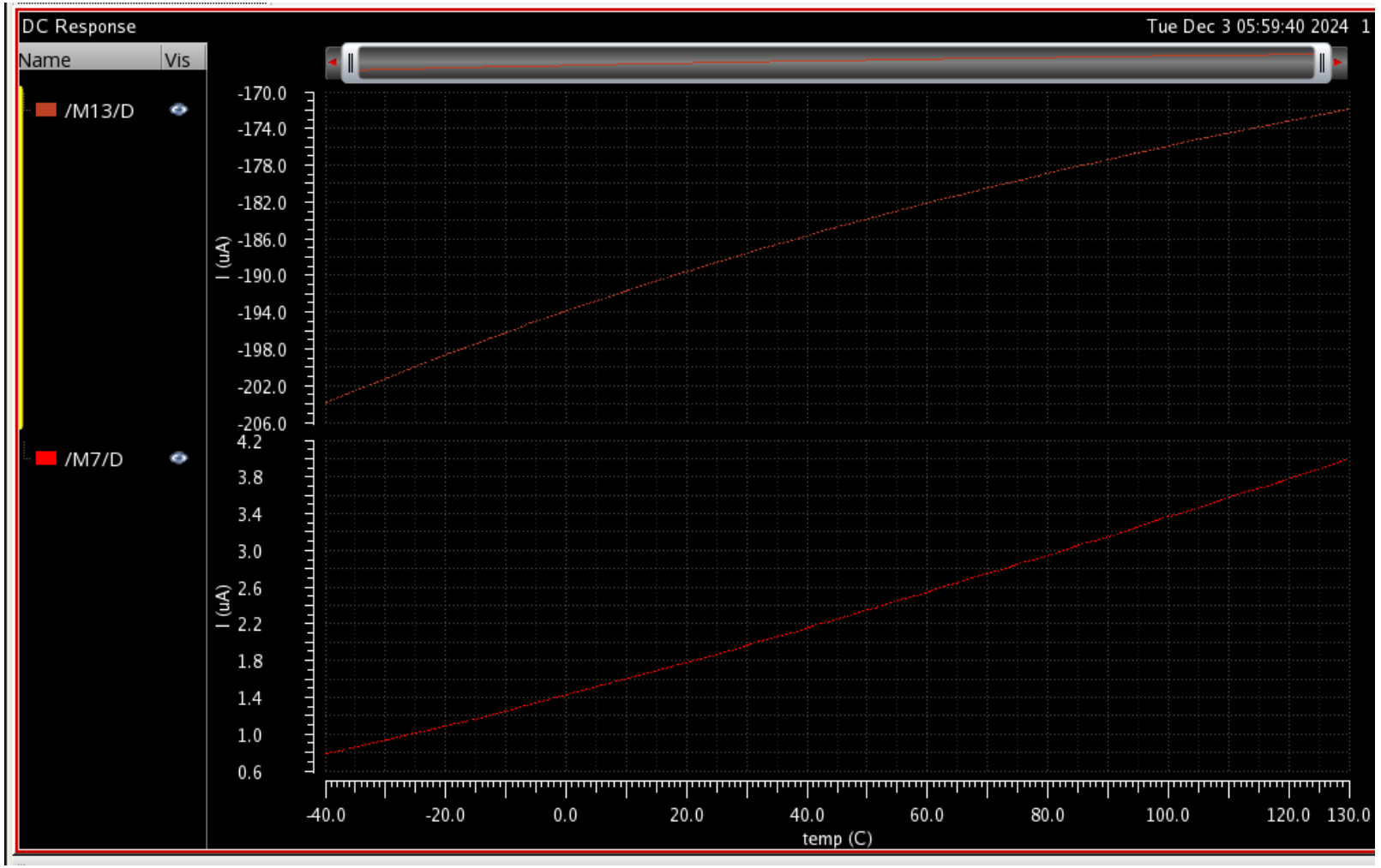


静态工作点工作在640mV，用输入电流I分别等于200nA、400nA到1000nA代表采集到的电荷数量。输出电压随时间的变化关系。

加入电流源电路的 CSA 电路（1）

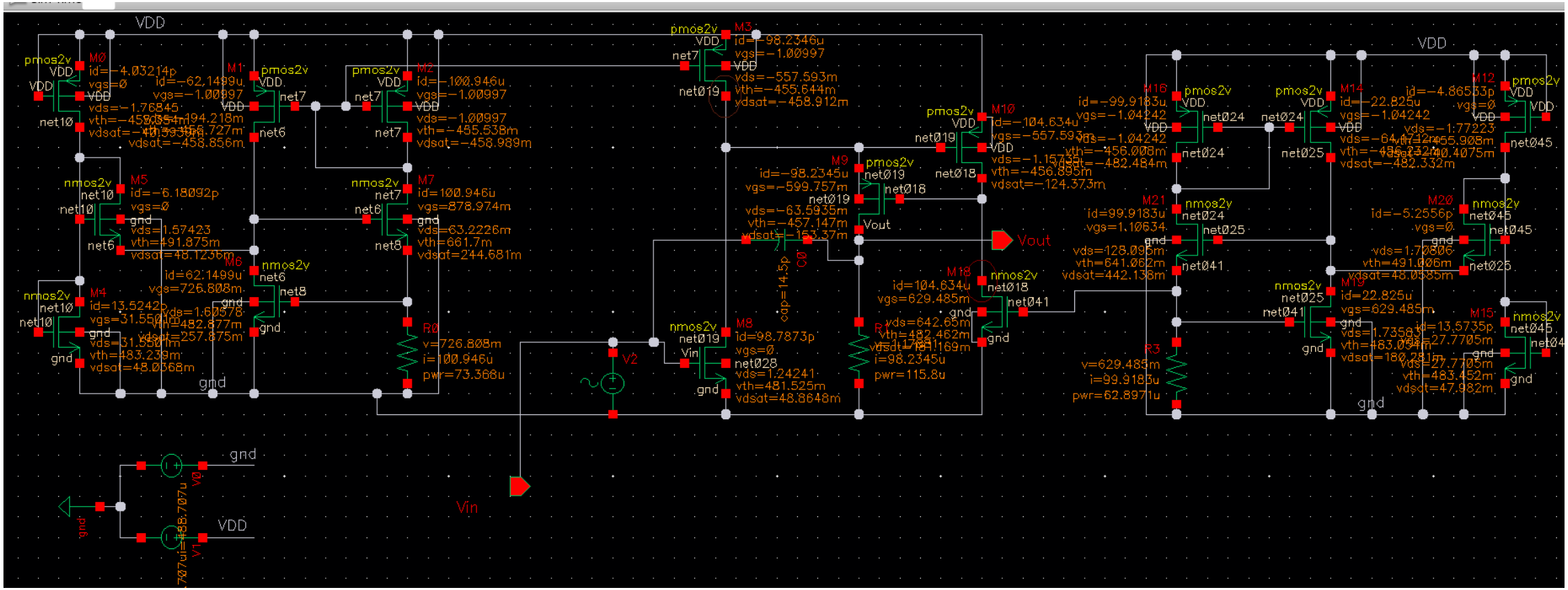


CSA 电路中的电流源电流随温度变化图

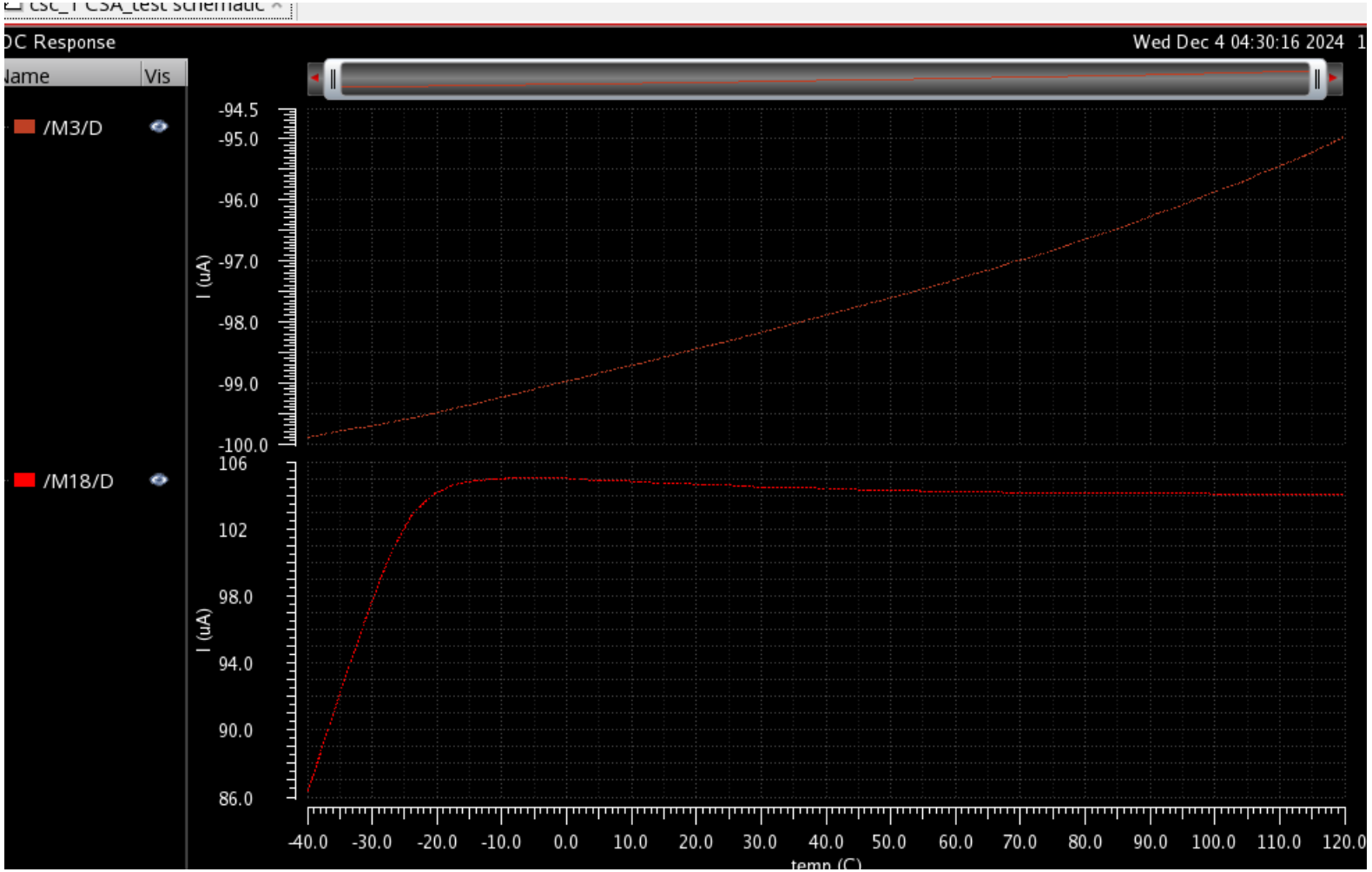


测CSA电路中电流镜输出电流随温度的变化，测得M7和M13的漏极电流随温度变化如左图所示。在-40°C—120 °C温度范围内，M13电流输出范围在204uA-172uA，M7电流输出范围在0.8uA-4uA。

加入电流源电路的 CSA 电路（2）

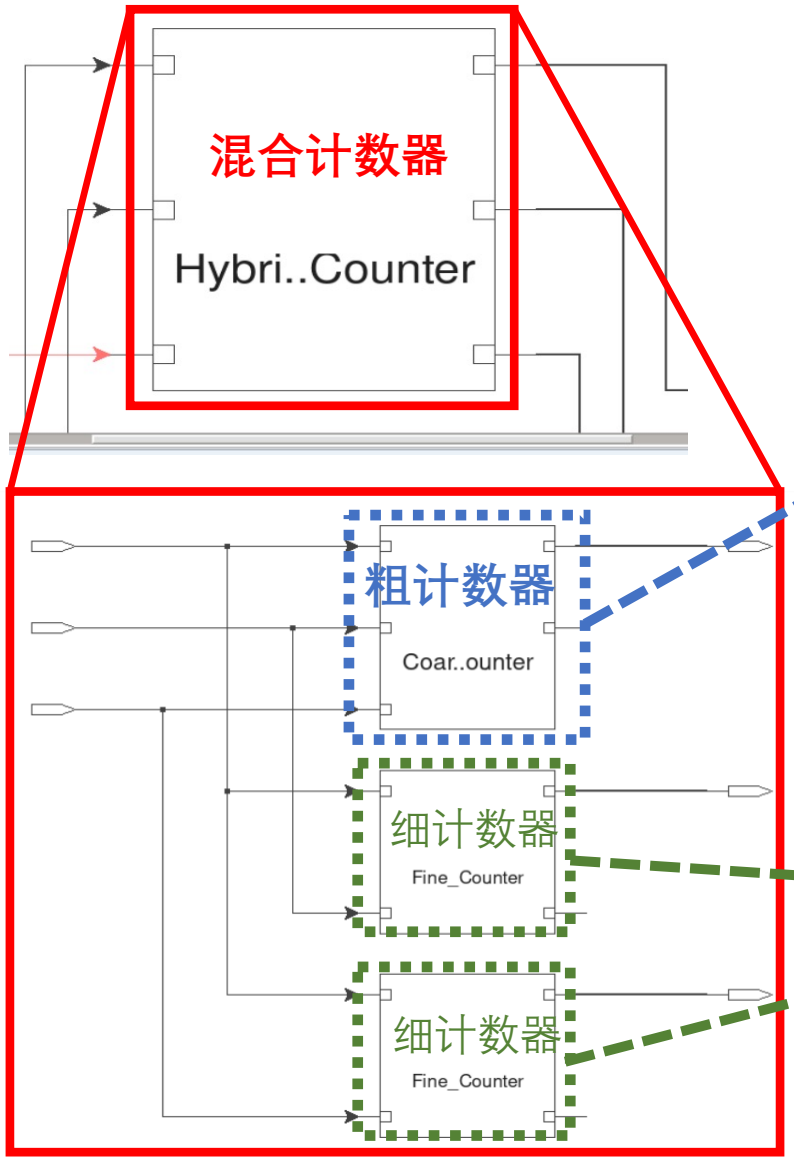


CSA 电路中的基准电流源电流随温度变化图

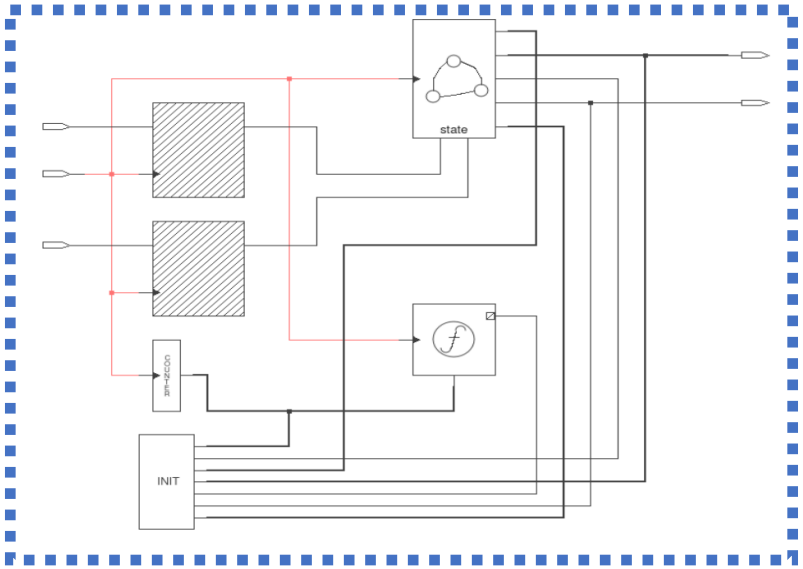


修改后仿真基准电流源输出电流随温度的变化，测得M12的漏极电流随温度变化如左图所示。在-40°C—120 °C温度范围内M3管漏极电流输出范围在 -100uA至-95uA，M18管漏极电流在-20°C—120 °C温度范围内输出较为稳定于101uA至105uA之间

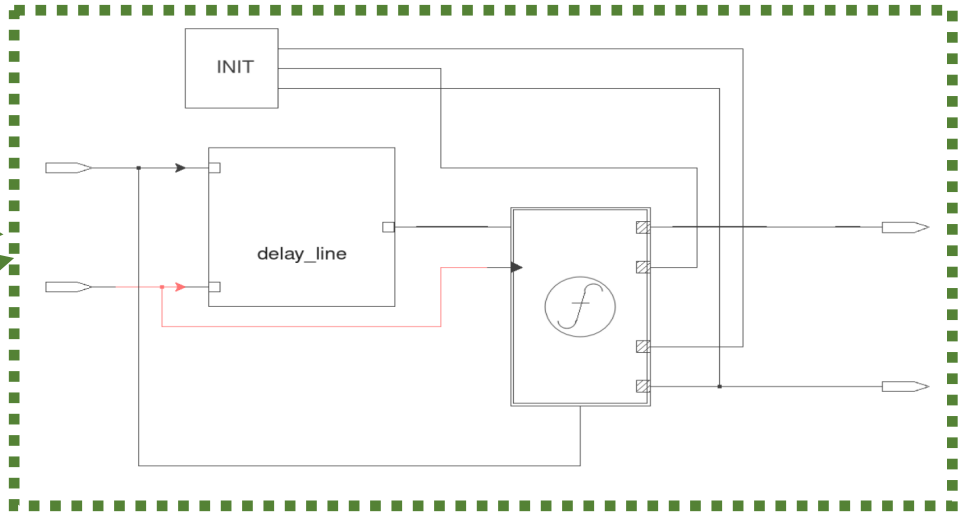
TDC 数字建模



粗计数器：记录从启动信号上升沿到停止信号上升沿之间的时钟周期数。

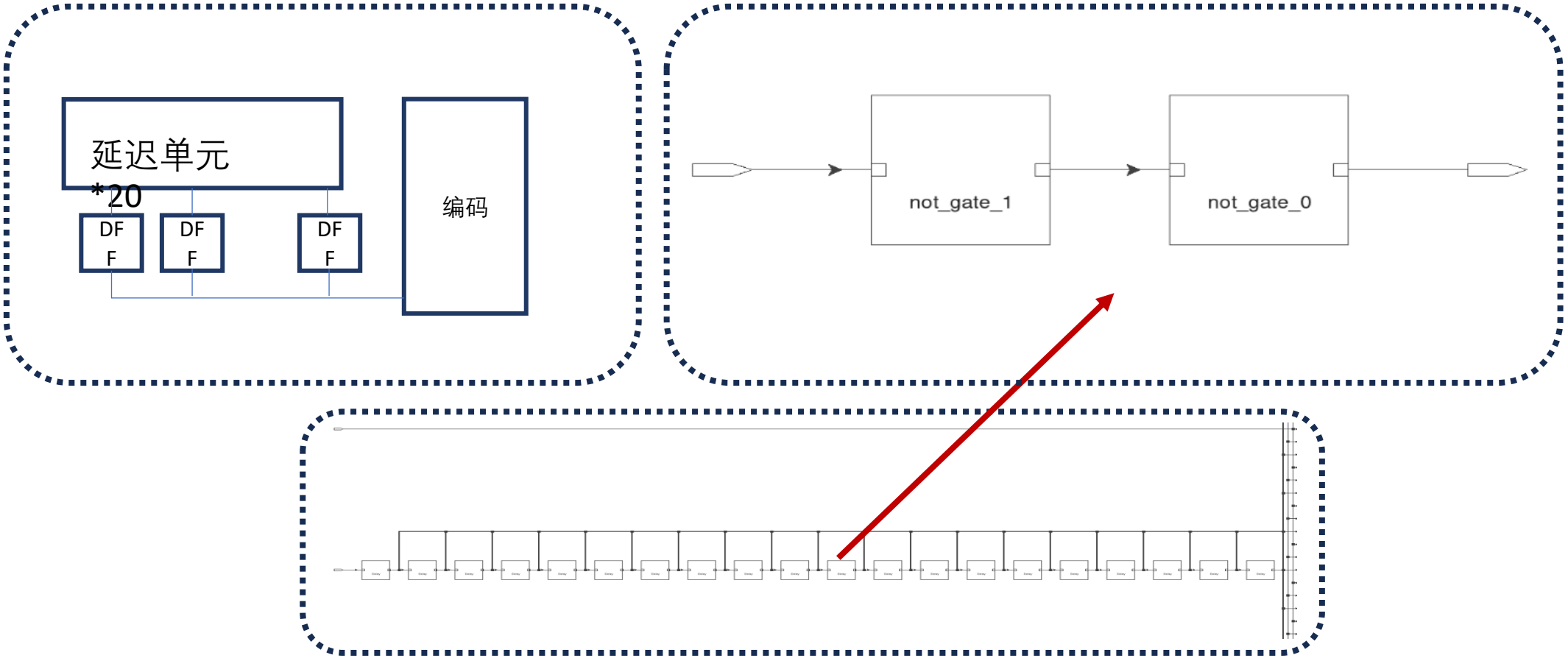


细计数器：延迟链结构，记录启动和停止信号两个上升沿之间的精确时间差。



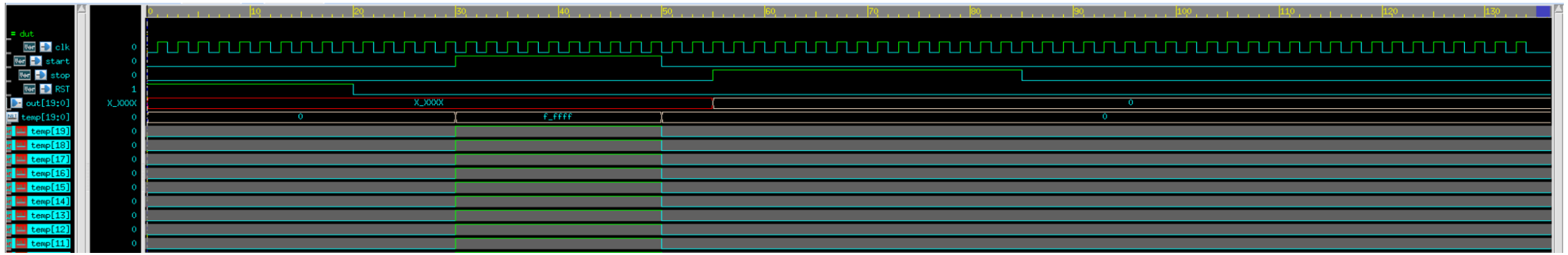
细计数器改进

1.考虑到功耗问题，将延迟单元数量减少为20个
2.重新设计延迟单元 两个非门



前仿真

Start信号与Stop信号上升沿间隔设置为200ns



前仿真功能正确，后续还需要导入工艺库进行后仿真