Summary of the weekly progress

- **Discussion on updated background from MDI on CEPC Day, on ECAL**

Sub-Detectors	Ave. Hit Rate(MHz/cm2)	Max. Hit Rate(MHz/cm²)	Max. Occupancy/BX(%)	Ave. TID(Gy/yr)	
ECal – Endcap	0.011/bar	0.3/bar	0.0008	0.322	Higgs
ECal – Barrel	0.2	2.79/bar	7.03		Low LumiZ
ECal – Endcap	0.35	5.44/bar	9.29		
Ecal – Barrel	1.54/bar	22.3/bar	7.03		High LumiZ With 1MeV th To be optimized
ECal – Endcap	2.84/bar	43.5/bar	9.29		

- **Issue: electronics is unchangeable from Higgs to High LumiZ**
  - **The scheme should be design aiming at the highest request – High LumiZ**
    - **Main difference from the changeable VTXA scheme**
  - **~10kHz vs 350kHz @ 3MHz /bar has a dramatically impact on scheme**
  - **Typically scheme QT measurement (with low power ADC) works for ~10kHz, very challenging for ~350kHz, impossible for 3MHz**
  - **Should consider waveform + continuous ADC + digital processing for Q for > 1MHz**
    - **Leads to high power**
  - **Another potential issue: reliability for over 20years – a repairable scheme is necessary?**

Summary of the weekly progress

- **The VTX data rate also updated according to the latest MDI report (Ying Zhang)**

Detector & Mode	Hit density (Hits/cm2/B	BXRate (Hz)	**Hit density (kHits/cm2/s**	Safe factor	Cluster size	Hit pix rate (k	Hit size (bit/pix)	Chip size (cm2)	Data rate/Taichu3
VTX (Higgs) Ave.	0.37	1.34E+06	490	1.5	3	2205	32	3.27	0.23
VTX (Higgs) Max.			610			2745			0.29
VTX (LowLumiZ) Ave.			1960			8820			0.92
VTX (LowLumiZ) Max.			2300			10350			1.08
VTX (HighLumiZ) Ave.			15640			70380			7.36
VTX (HighLumiZ) Max.			18340			82530			8.64

- **Comment on 3 scenarios with feasibility**
  - **~300Mbps for Higgs: should work with Stitching scheme**
  - **~1.1Gbps for Low LumiZ:**
    - **Stitching scheme: very challenging with power supply, power consumption and transmission, we should try**
    - **Normal ladder: should work from the electronics view, needs smart cooling design**
  - **8Gbps for High LumiZ for phase II**
    - **Major show stopper at current stage, 2.3x higher than CDR**
    - **Impossible for stitching scheme**
    - **MDI optimization is a MUST + normal ladder based + advanced cooling technique**

unique design

Summary of the weekly progress

- **Defined a series of interface parameters for the Data Link system during the discussion of Ref-TDR writing**

32ch x 40 Mbps 或
16ch x 80 Mbps 或
8ch x 160 Mbps 或
4ch x 320 Mbps 或
2ch x 640 Mbps 或 } 1.28 Gbps

32ch x 40 Mbps 或
8ch x 160 Mbps 或
4ch x 320 Mbps 或
2ch x 640 Mbps 或 } 1.28 Gbps

32ch x 40 Mbps 或
8ch x 160 Mbps 或
4ch x 320 Mbps 或
2ch x 640 Mbps 或 } 1.28 Gbps

32ch x 40 Mbps 或
8ch x 160 Mbps 或
4ch x 320 Mbps 或
2ch x 640 Mbps 或 } 1.28 Gbps

TaoTie: input channels vs data rate combination

Capability of ChiTu ASIC		Channel Number	Data/Clock Rate	Notes
Uplink	Payload Data Channels (input)	Maximum 7 channels	1.3867 Gbps/ch	ChiTu can receive and transmit maximum 7 channels of data from TaoTie and front-end. The data rate is fixed to 1.2867 Gbps/ch. Maximum uplink payload transmission capability is 9.7069 Gbps per ChiTu ASIC.
	External Control Channel (input)	1 channel	86.6666 Mbps	ChiTu can transmit one specific channel of 86.6666 Mbps. This channel has specific input pins. The data of this channel is embedded as 2 bits in the uplink frame.
Down-link	Payload Data Channels (output)	Maximum 16 channels	Maximum 346.6666Mbps/ch Minimum 86.6666 Mbps/ch	ChiTu can output maximum 16 channels of data to the front-end with the data rate of 86.6666 Mbps/ch. The output data rate can be configured to 86.6666M, 173.3333M or 346.6666Mbps/ch with the channel number of 16, 8 or 4, respectively.
	External Control Channel (output)	1 channel	86.6666 Mbps	ChiTu can output one specific channle of 86.6666 Mbps. This channel has specific output pins. The data of this channel is embedded as 2 bits in the downlink frame. This data channel is mainly for slow control from back-end.
Provide Clock	(Output)	16 channels	43.3 MHz or 86.6 MHz or 173.3 MHz or 346.6 MHz or 693.3 MHz or 1.3863 GHz	ChiTu can provide maximum 16 channels of clock (differential) to the front-end with configurable frequency from 43.3 MHz to 1.2863 GHz. 2 Channels out of these 16 channels can provide phase adjustment function with a 54.1666 ps resolution for all frequencies.

ChiTu: specification

Output Signal/Clock Specification		Notes
Type	Differential	
Signal Amplitude	200 mV ~ 800 mV differential peak-to peak (@100 ohm differential)	All output data and clock channels in ChiTu provide programmable signal amplitude.
Common Mode Voltage	600 mV	
Data Rate	Maximum 346.6666Mbps Minimum 86.6666Mbps	ChiTu outputs data (downlink) with three configurable data rates : 86.6666M/ch, 173.3333M/ch or 346.6666Mbps/ch. For the specific "External Control Channel" (slow control), the output data rate is 86.6666 Mbps.
Clock Frequency	Maximum 1.3863 GHz Minimum 43.3 MHz	ChiTu can provide clock signals with configurable frequency: 43.3 MHz, 86.6 MHz, 173.3 MHz, 346.6 MHz, 693.3 MHz or 1.3863 GHz.
Coupling	Support both AC or DC coupling	This depends on front-end requirement after considering the signal common voltage and amplitude.
Termination	100 ohm differential resistor	The receiver of these signals needs to provide differential 100 ohm termination.

ChiTu: Driving capability

Summary of the weekly progress

- **Recent progress for the Power System**
  - **COTS module TID test**
    - **Some commercial LDO & DC-DC chips were found survival after 5Mrad**
  - **Basha DC-DC controller design**
    - **Scheme updated, full chip simulation complete**
    - **Discussion on chip technology consideration**

Summary of the weekly progress

- **Joint discussion with accelerator colleagues on running mode and detector clocking related parameters**
- **Running mode confirmed: for Low LumiZ, collision only occurs at 69ns bunch spacing**
- **Ref clock frequency provided from the accelerator: 43.3 MHz is feasible**
- **A rough estimation on power consumption provided, represented by VTX (Ying Zhang)**
  - **Running at new mode, power consumption can be greatly saved**

Table 1 Power estimation of the CEPC Vertex Detector CMOS Sensor
(@65nm CMOS CIS process, 1.2V, Chip size 2.57cm×1.59cm)

	Matrix	Periphery	DataTrans.	DACs	Total Power	Power Density
Case 1	200mW	70mW	32mW	8mW	310 mW	~76mW/cm^2
Case 2	55mW	70mW	32mW	8mW	165 mW	~40mW/cm^2

Progress on Ref-TDR

- A first overlook during the weekly meeting
- Progress for each main chapter of electronics system
  - Introduction ……..100% (Wei Wei)
  - General architecture and Strategy ……100% (Wei Wei)
  - Sub-detector ASIC
    - OTK ASIC ……70% (Xiongbo Yan)
    - SiPM ASIC……TBU with new MDI bkgrd (Huaishen Li)
  - Data Link ……...90% (Di Guo, Xiaoting Li, Jingbo Ye)
  - Power System ……40% (Jun Hu, Jia Wang)
  - Wireless communication ……..80% (Jun Hu)
  - Clocking ……70% (Jun Hu)
  - Backend Electronics ……100% (Jun Hu)
  - Cabling, Crates & Elec Room ……70% (Wei Wei)
  - Previous R&D on electronics system ……..100% (Wei Wei)