应用于CMOS像素探测器的高性能锁相环电路设计

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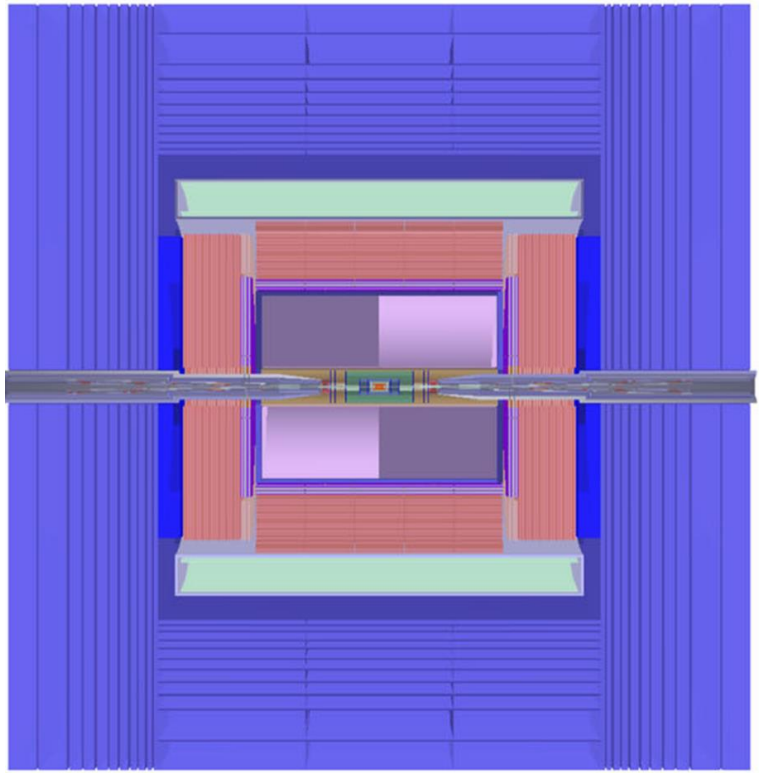
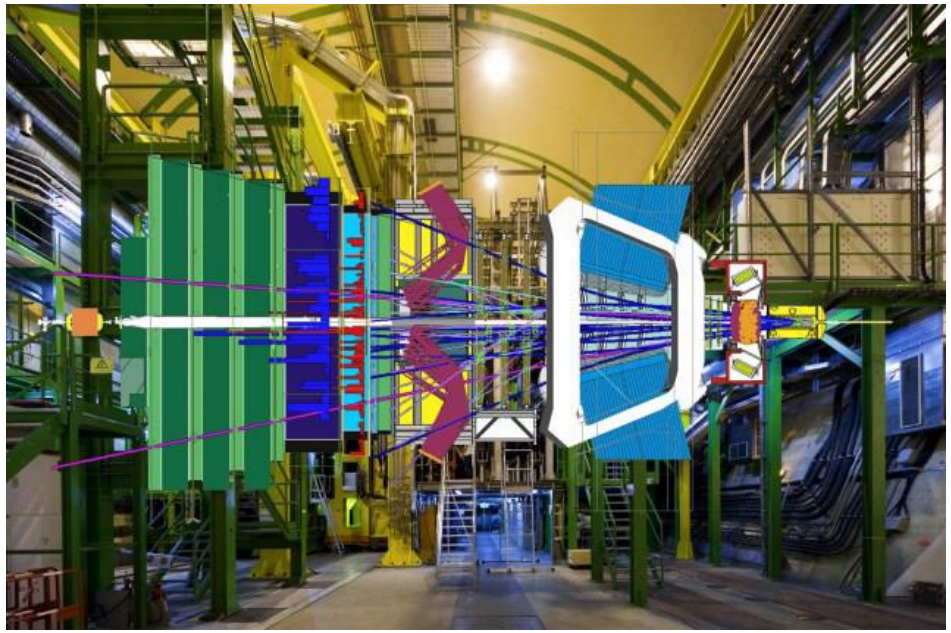
目　录

一、 设计背景

- CMOS像素探测器
  - 高空间分辨率
  - 低功耗



CEPC探测器(r-z方向)

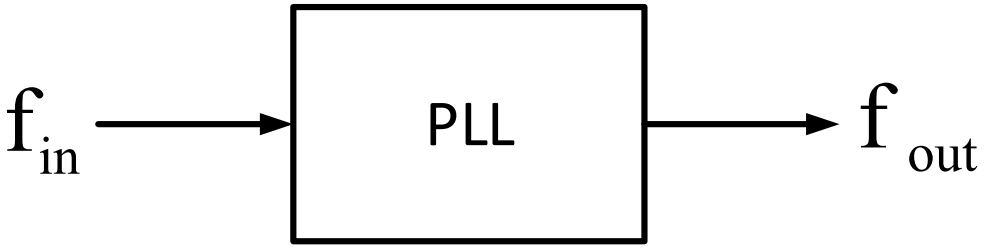


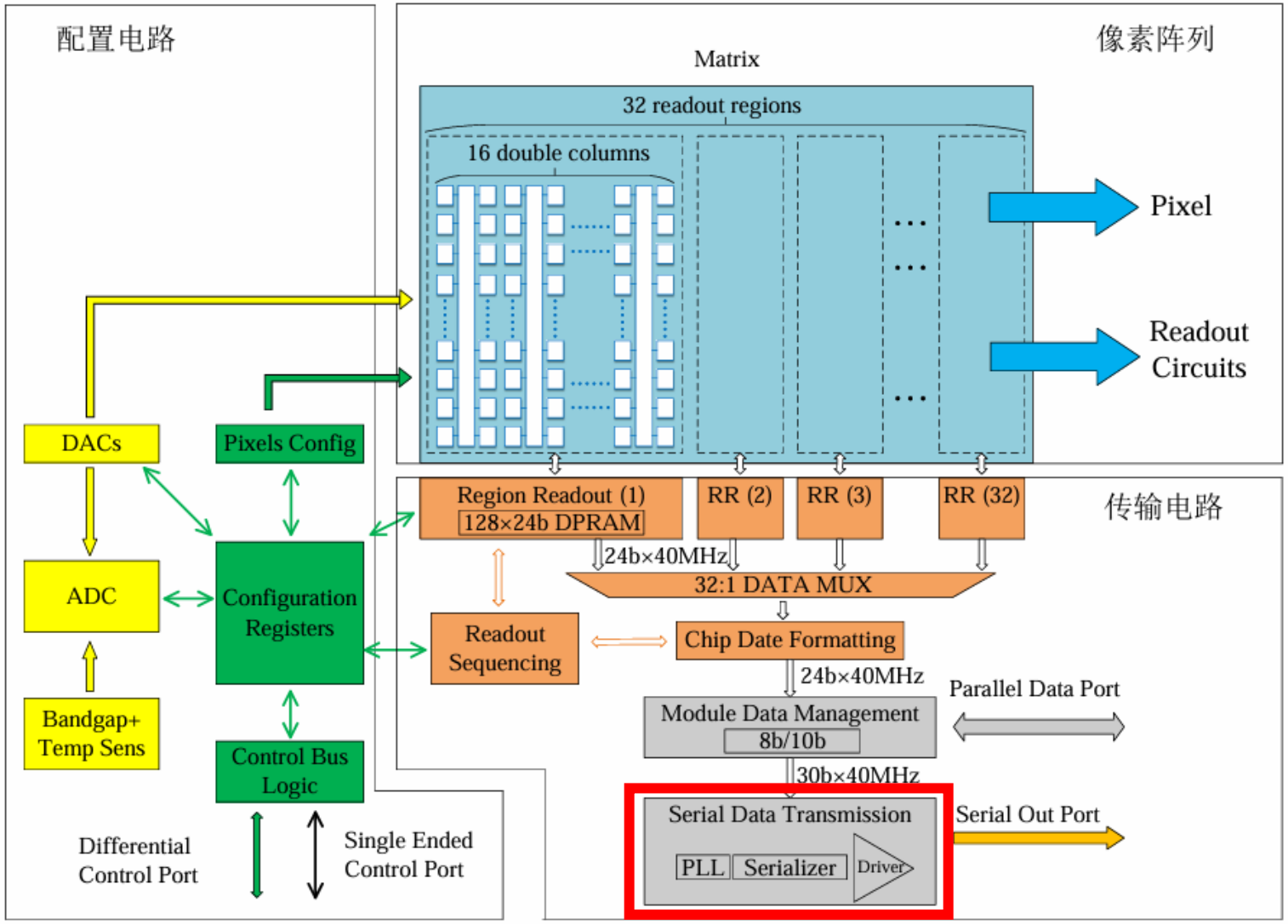
LHCb实验

➢ 锁相环(PLL)

- 时钟同步
- 高速时钟@串行传输电路

$$f_{OUT} = N \times f_{IN}$$





➢ PLL性能需求

- 串行传输速率~1.2 Gb/s → PLL频率 600 MHz

  fin=40 MHz, fout=160M~640M Hz, 倍频值可编程

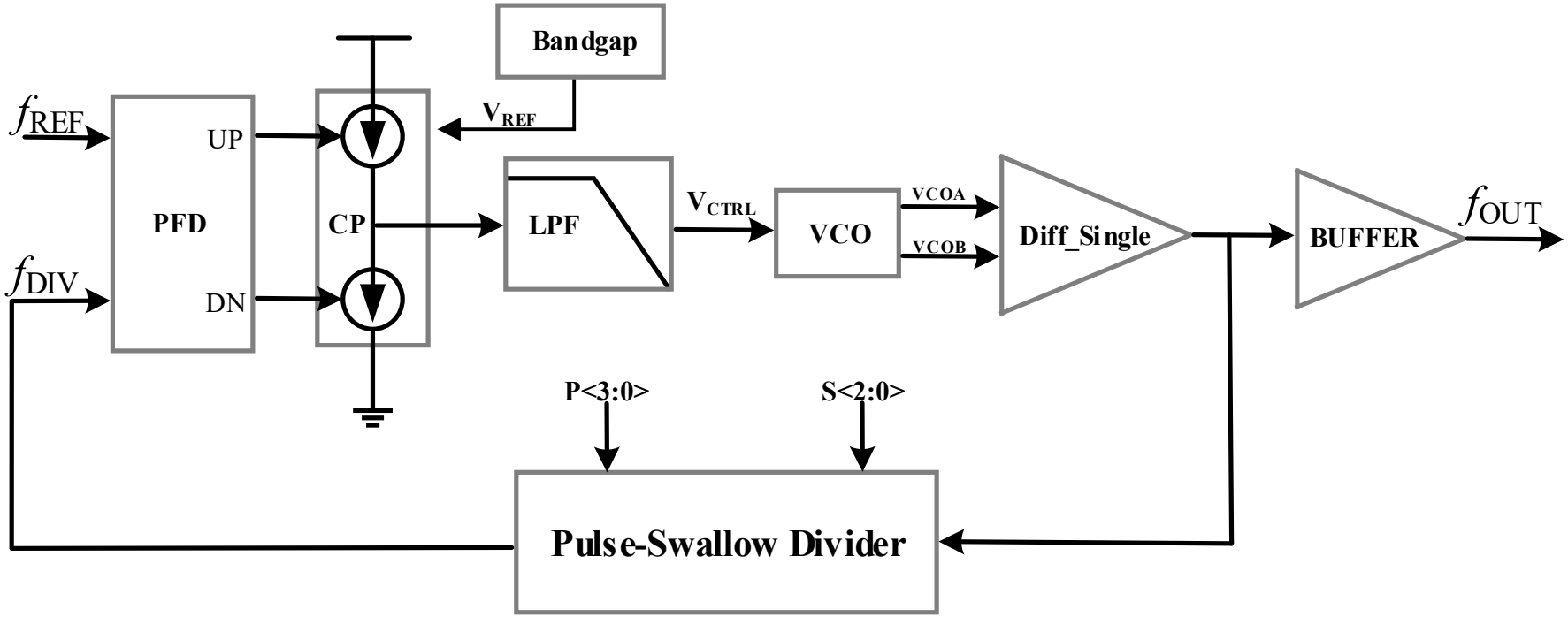
- 低物质量→ 低功耗@55nm, Vdd=1.2V, I↓
- 传输数据误码率→ 抖动↓
- 大探测面积、低成本→ 面积↓

二、 PLL设计

➢ PLL电路拓扑结构：电荷泵锁相环

- 低参考杂散
- 更好的相位噪声
- 快速稳定
- 灵活的环路

参数设计



1. VCO设计

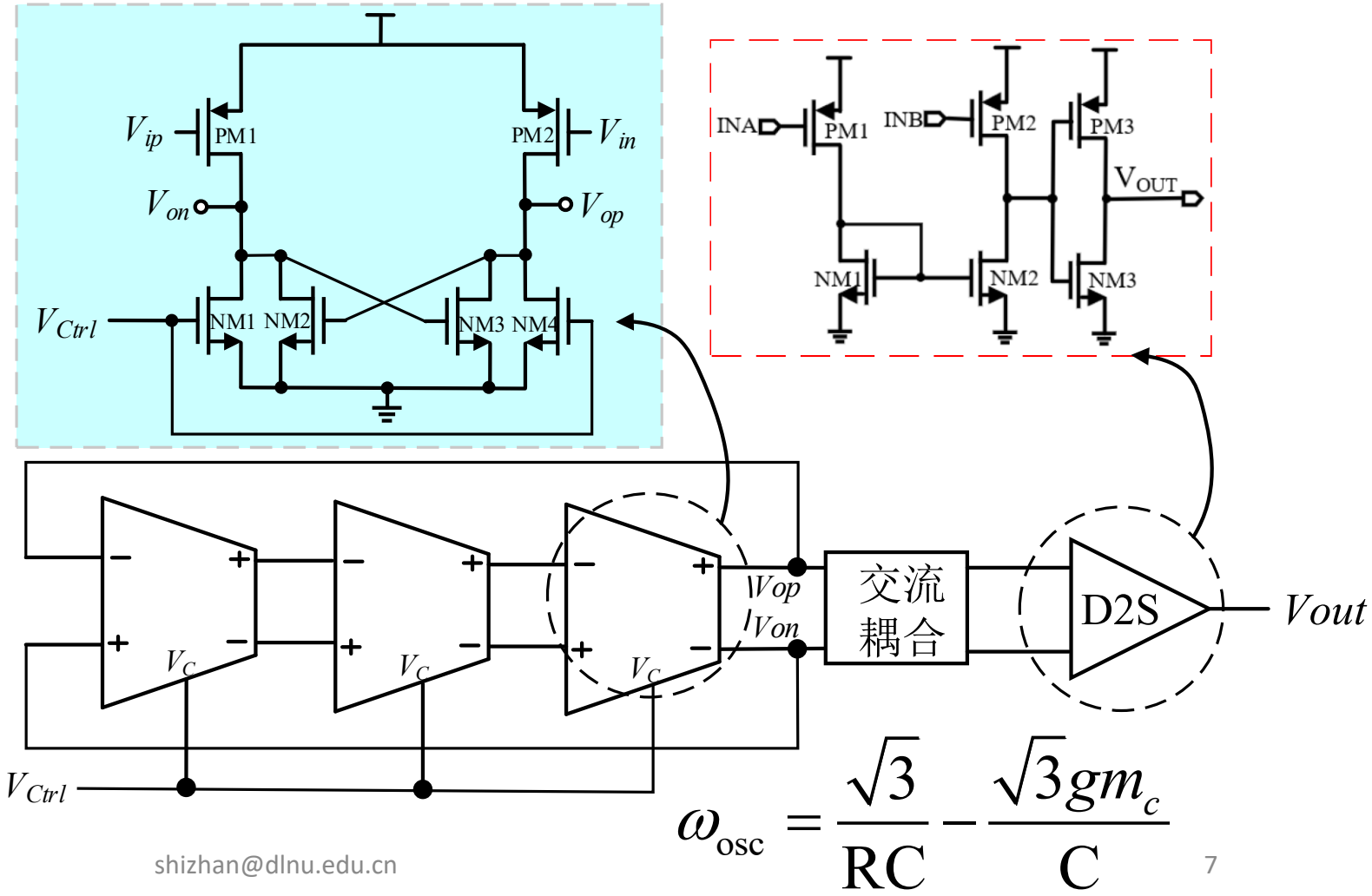
➢ 设计考虑

- 大调节范围，小面积

  →环形振荡器

- 低功耗
  - 3级延时单元
  - 伪差分结构

缺点：噪声较大



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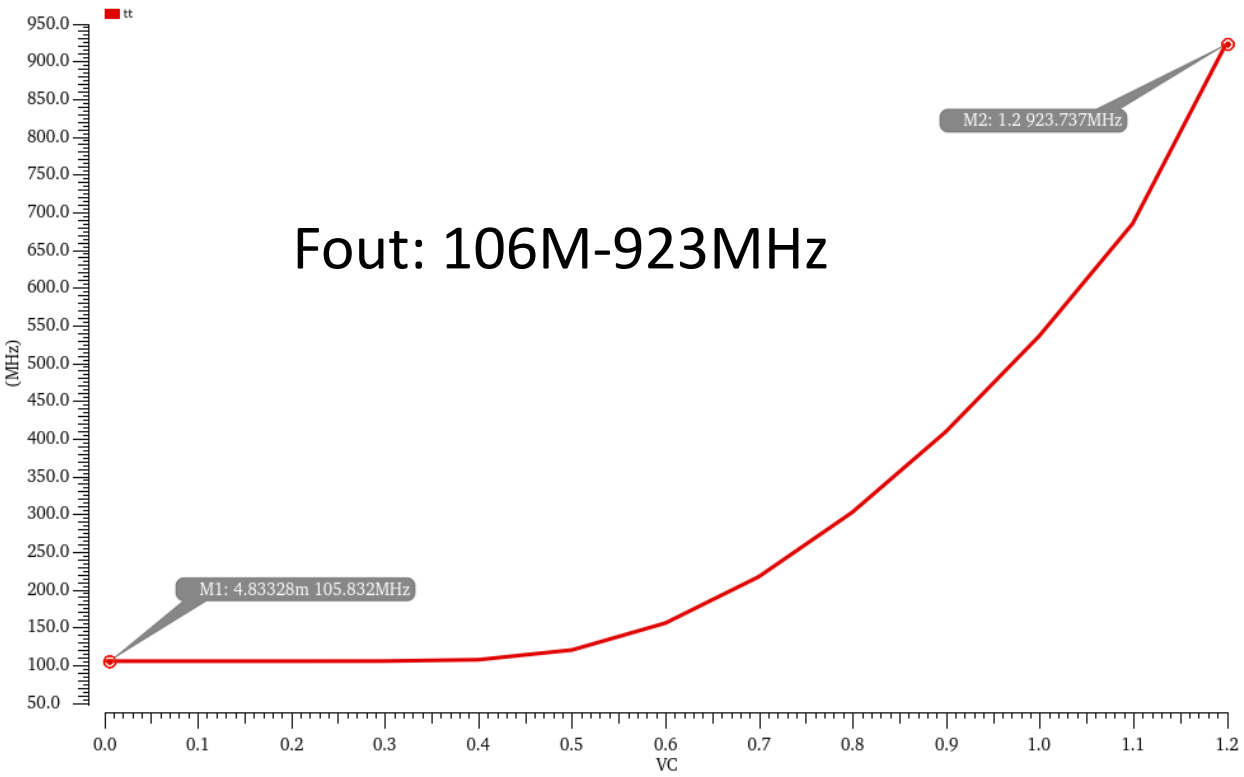
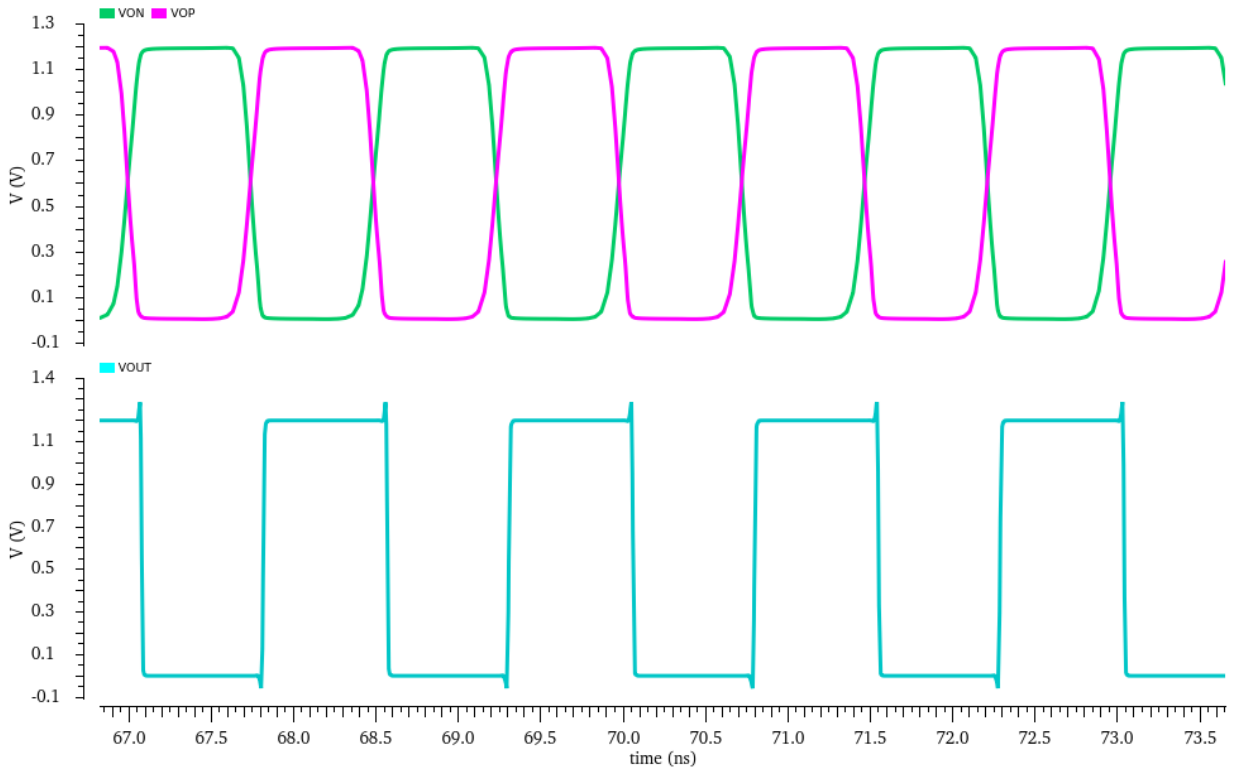


Fout: 106M-923MHz



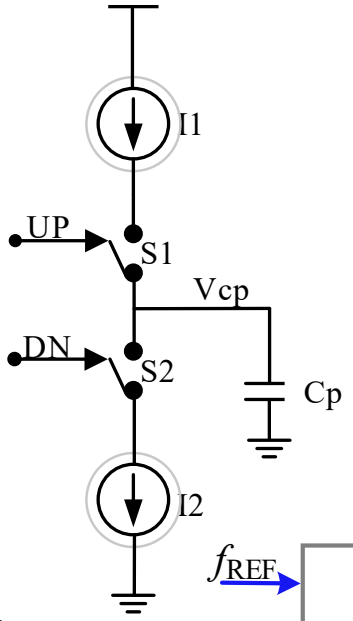
VCO	功耗	相位噪声	K_{vco}/s
160 MHz	0.45 mW	-111.2 dBc/Hz@1MHz	470 MHz/V
320 MHz	0.83 mW	-107.8 dBc/Hz@1MHz	1040 MHz/V
640 MHz	1.62 mW	-104.4 dBc/Hz@1MHz	1490 MHz/V

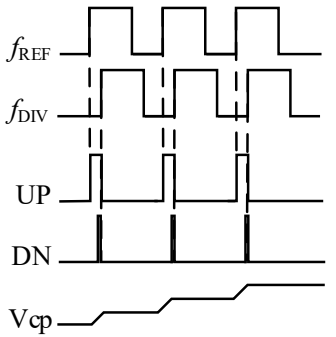
2. 电荷泵(CP)设计

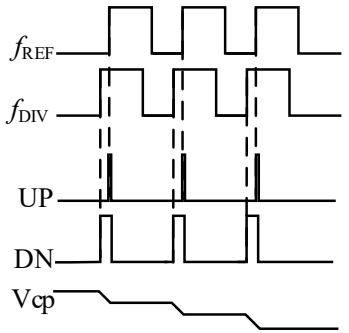
- 设计考虑
  - PLL低相噪→
    CP电流匹配
- 传统CP问题
  - UP和DN电流失配

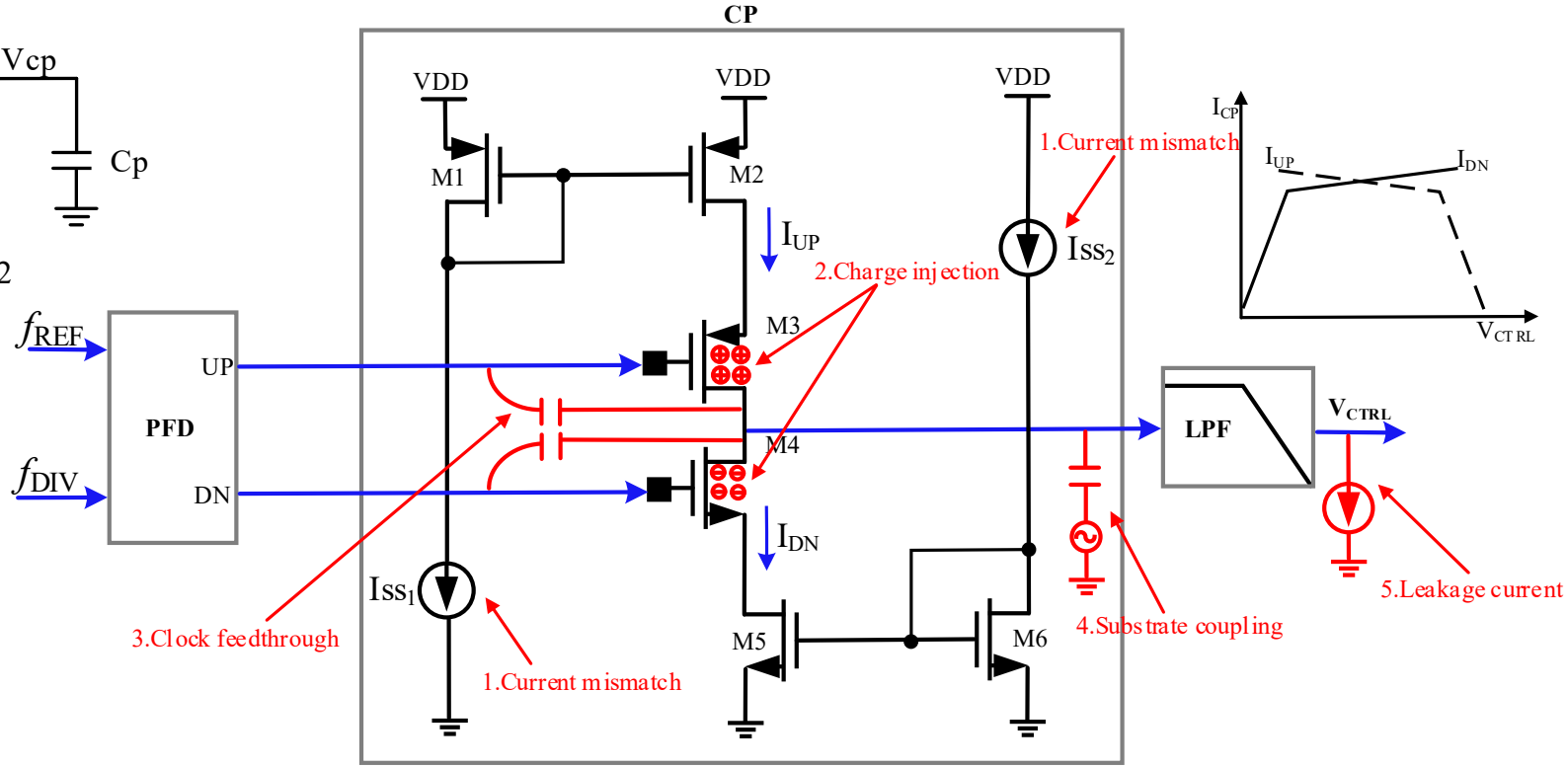
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})$$

  - 电荷注入、时钟馈通





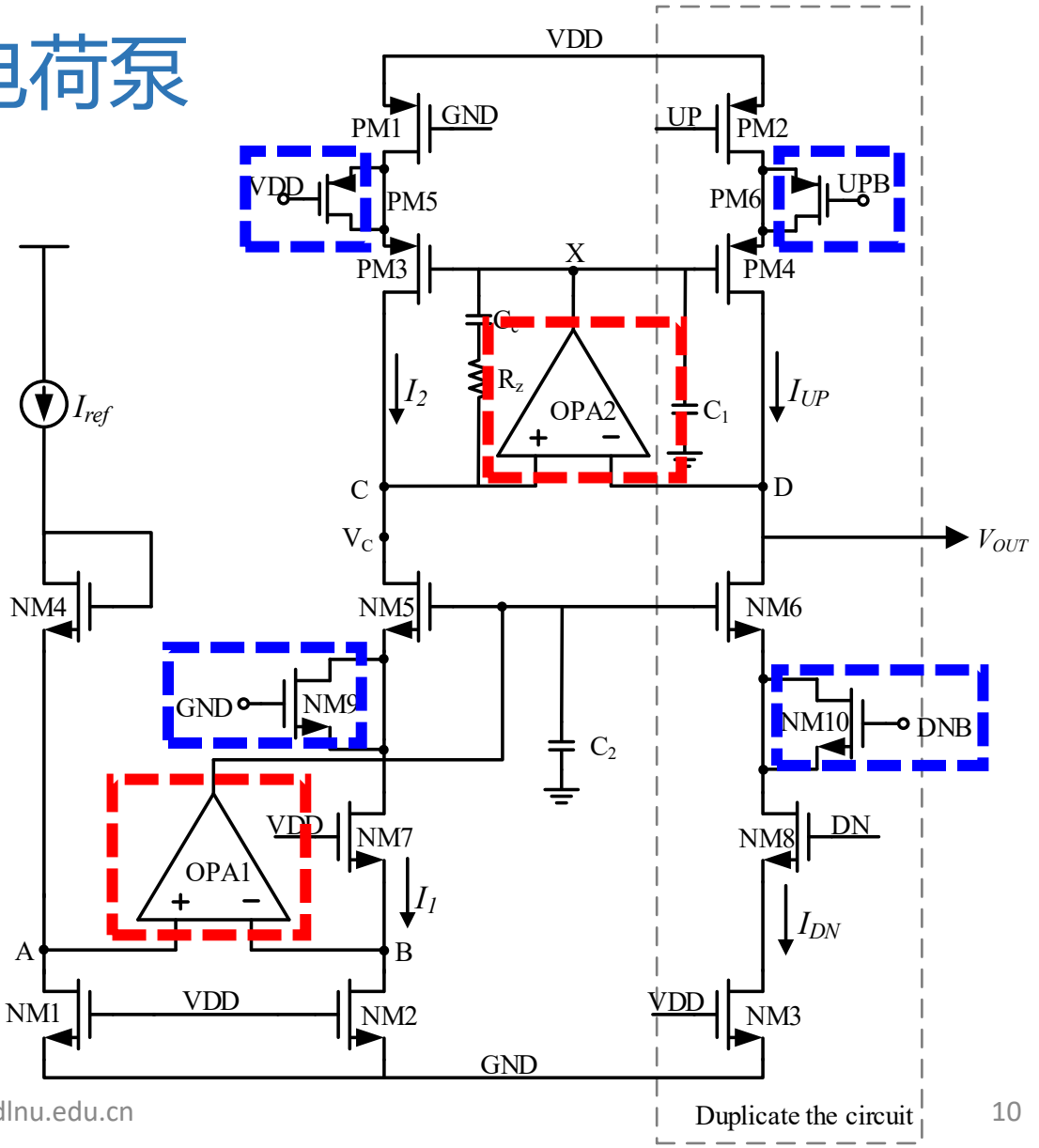




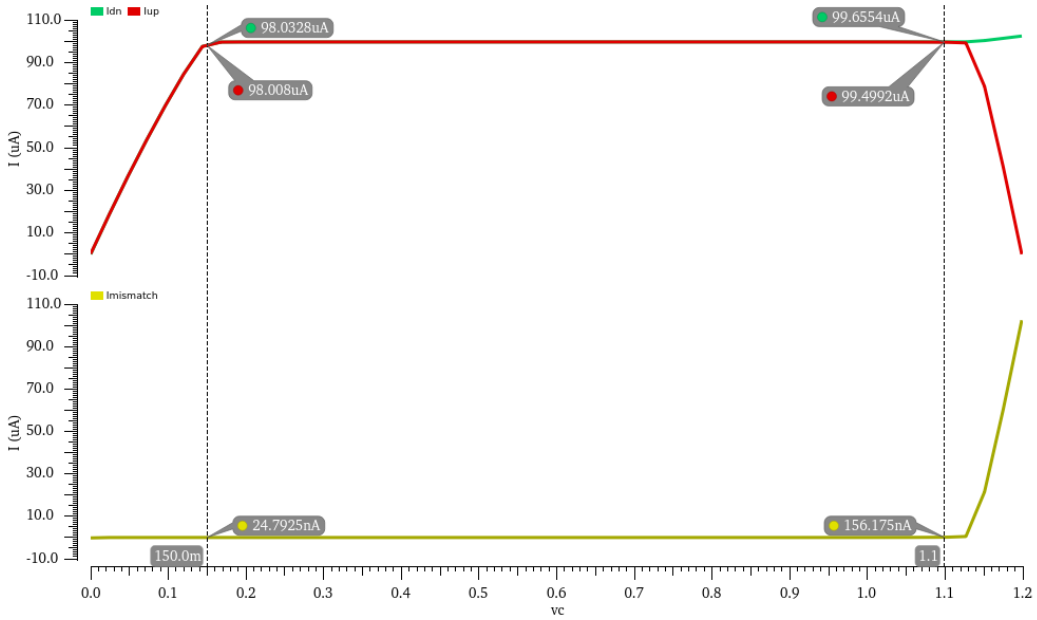
改进电荷泵

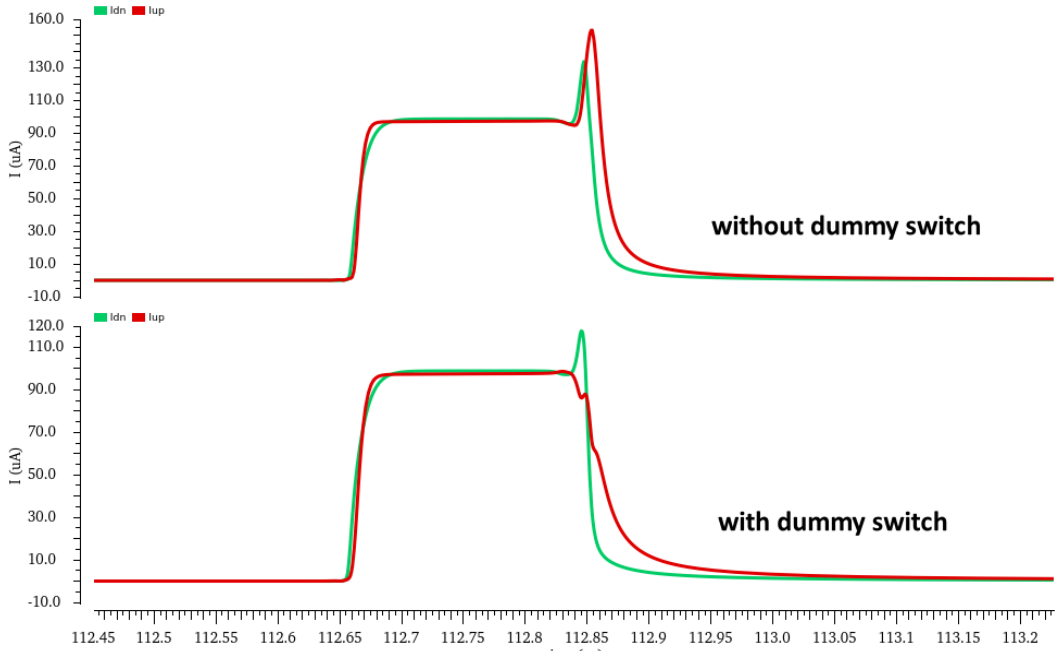
➢ 电路改进

- UP和DN电流失配 →
  提高电流镜输出阻抗→
  校准共源共栅电流镜，
  Vgs相等，Vds相等
- 电荷注入 →
  dummy管



改进电荷泵





CP	功耗	电流失配比(0.15 V~1.1 V)
tt	0.55 mW	0.06%~0.14%
ff	0.65 mW	0.08%~0.16%
ss	0.48 mW	0.05%~0.12%

3. 鉴频鉴相器(PFD)设计

➢ 设计考虑

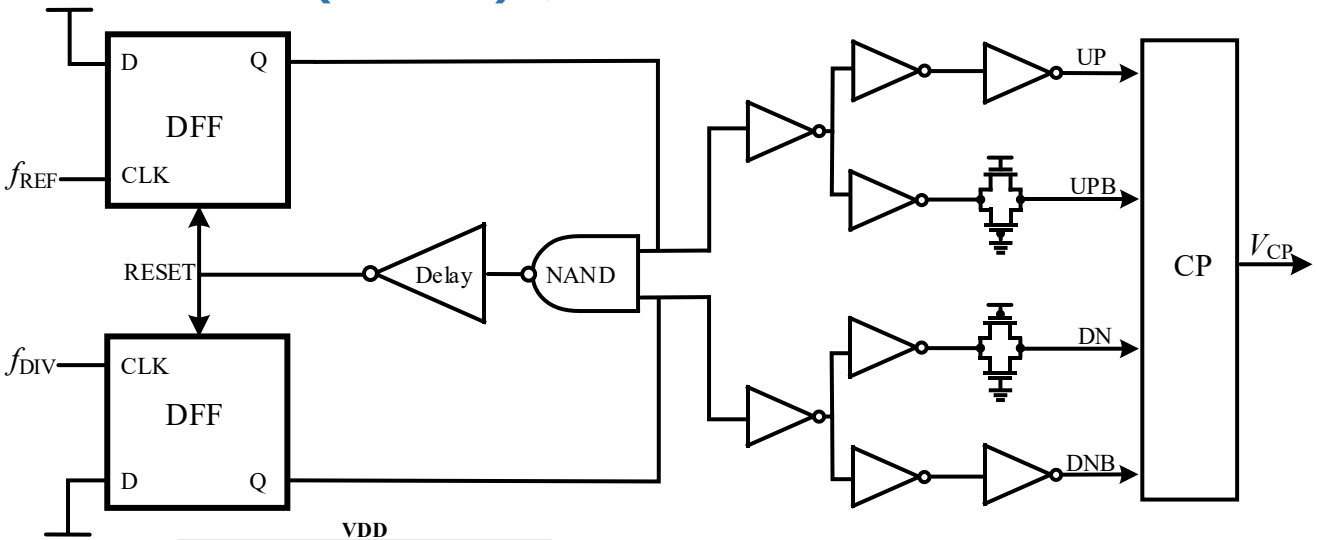
- 减小功耗、面积→

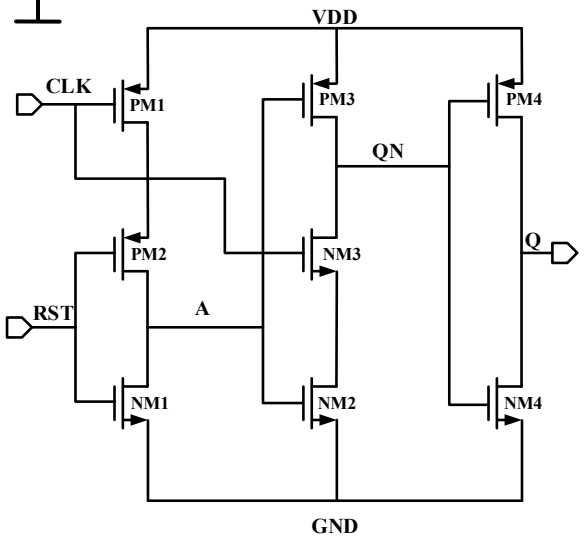
  真单相时钟(TSPC)

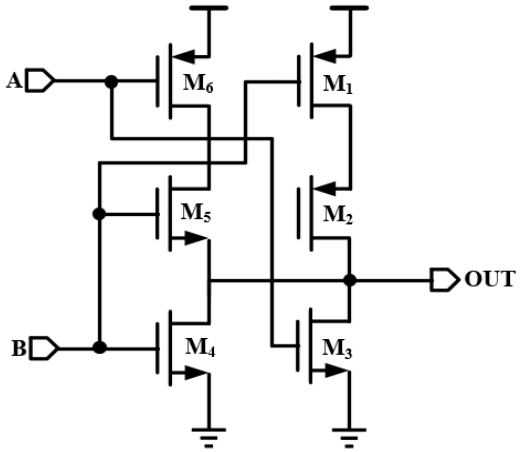
  D触发器

- 相位噪声→时序失配

  →改进与非门





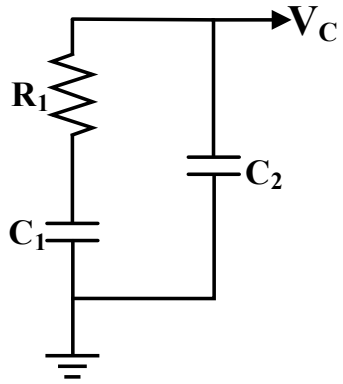


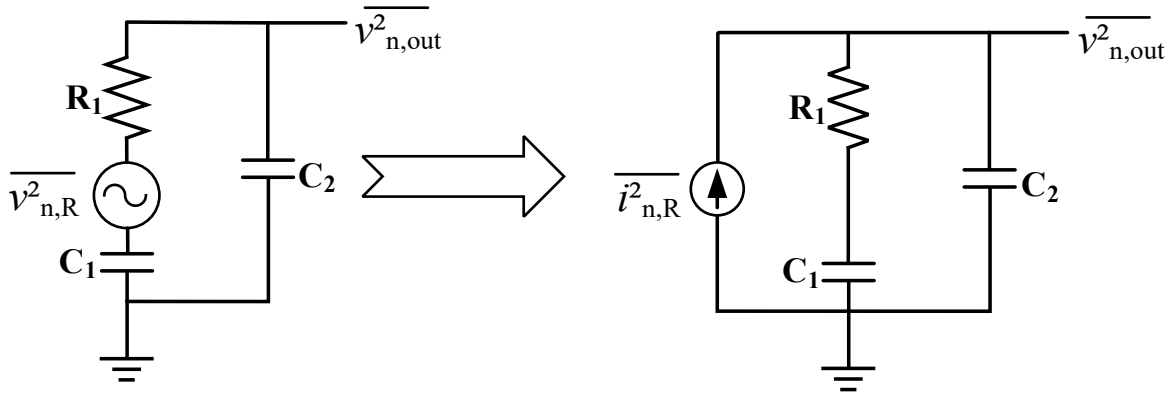
5. 环路滤波器

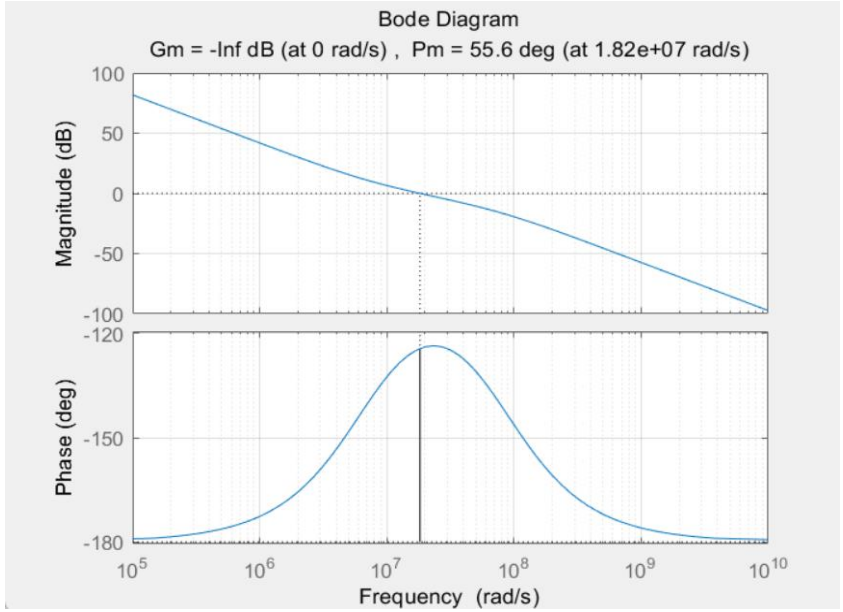
➢ 设计考虑

- 环路稳定性
- 噪声

元件	值
R1	2.1KΩ
C1	67.6pF
C2	6.5pF







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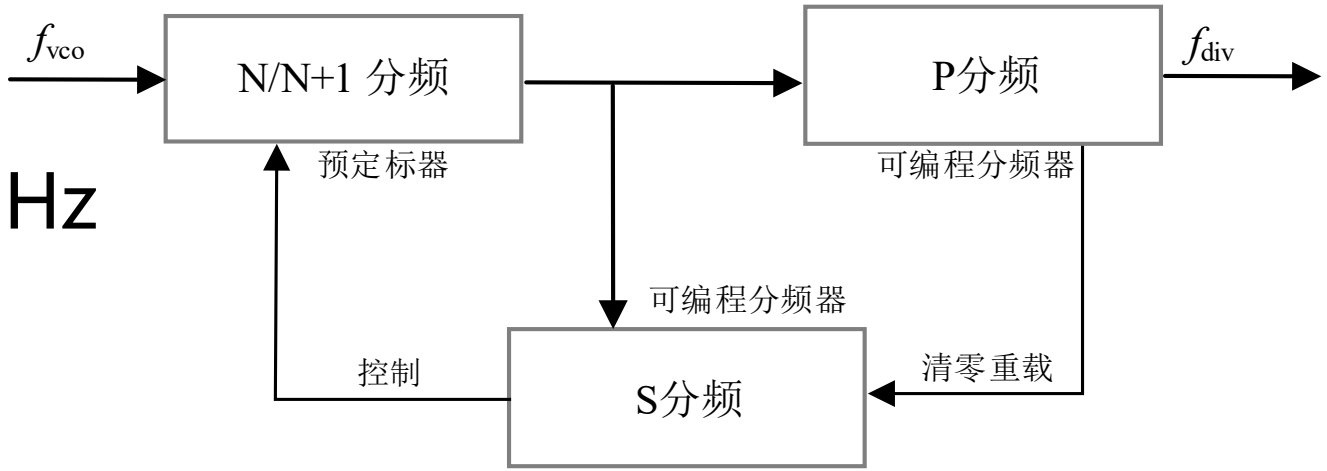
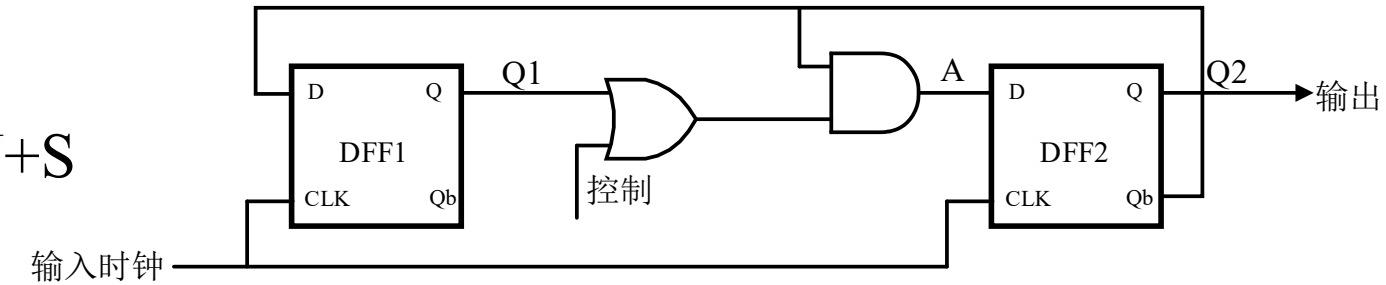
6. 可编程分频器

➢ 设计考虑

- 输入频率：160M-640M Hz
- 输出频率：40M Hz
- 分频比：4-16

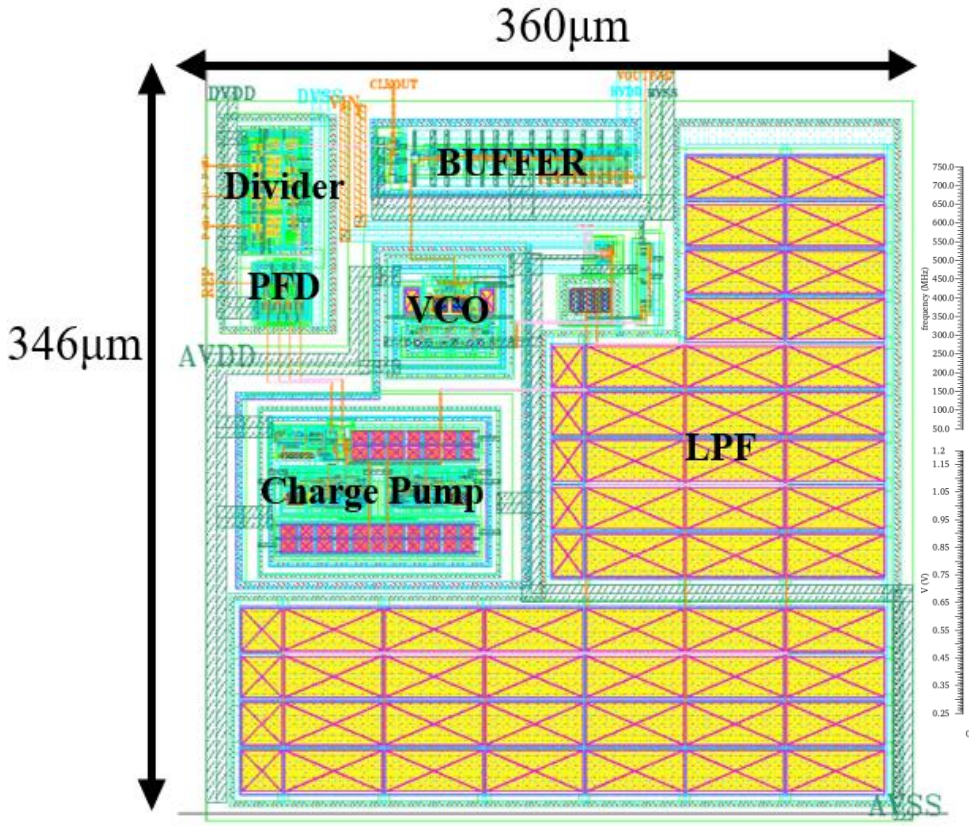


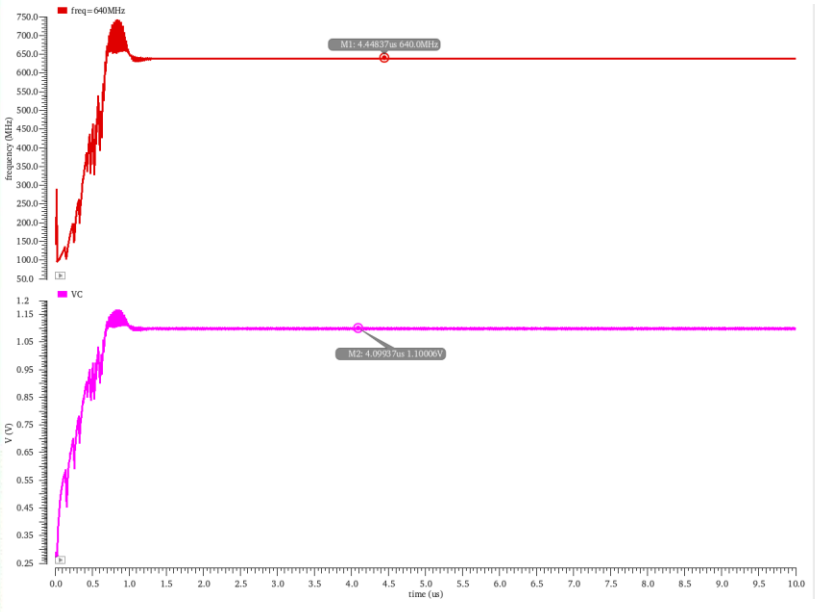
$$S(N+1)+(P-S)N=PN+S$$

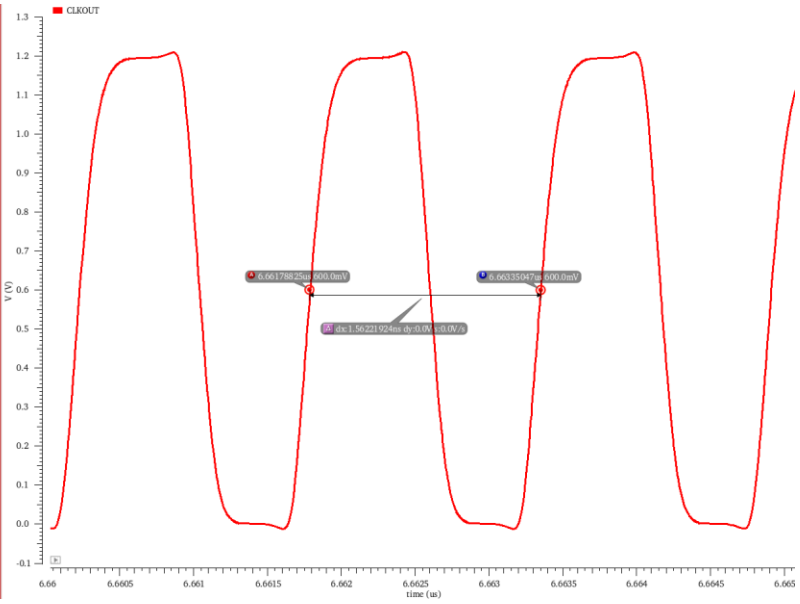


2/3 prescaler

7. 整体后仿真


360μm
346μm
DVDD
DVSS
CLKOUT
VOUTBUF
BUFFER
Divider
PFD
VCO
AVDD
LPF
Charge Pump
AVSS


freq=640MHz
M1: 4.44837us 640.0MHz
VC
M2: 4.09937us 1.1000V
frequency (MHz)
V (V)
time (us)


CLKOUT
V (V)
time (us)

指标	后仿(tt)			[1]	[2]	[3]
工艺	SMIC 55nm CMOS			180nm	55nm	65nm
输出频率	160 MHz	320 MHz	640 MHz	512 MHz	5.12 GHz	1.2 GHz
功耗(mW)	1.68	2.69	**4.05**	8.1	27	0.35
Rms jitter (10K~10MHz)	8.3 ps (1.3 mUI)	4.9 ps (1.6 mUI)	3.2 ps (2.1 mUI)	4.8 ps (2.5 mUI)	0.38 ps (0.19 mUI)	2.9 ps (1.3 mUI)
锁定时间	6.7 μs	5.8 μs	5.3 μs	4.7 μs	2 μs	3.4 μs
芯片面积		**0.125 mm²**		0.28 mm²	1.26 mm²	1.29 mm²
FOM(dB)	-219.4	-221.9	-223.8	-217.4	-234.6	-236

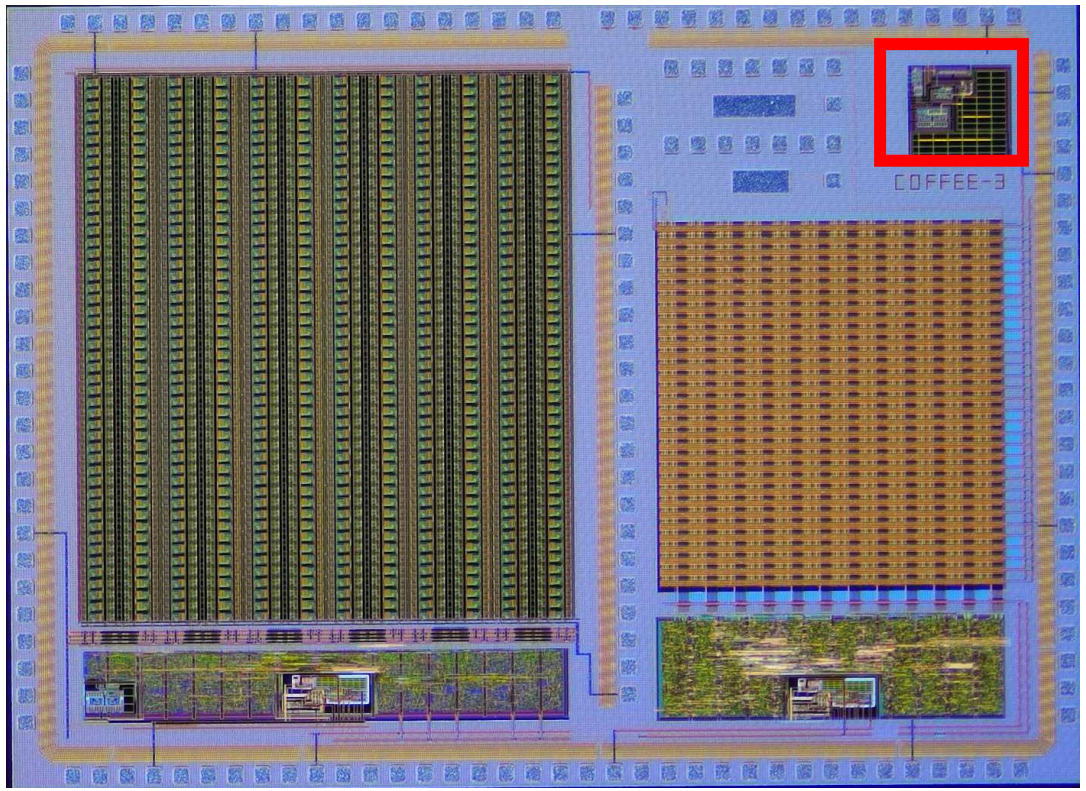
$$\mathrm{FOM} = 10 \cdot \log\left(\frac{\text{Phase Noise} \cdot \text{Power} \cdot f_{\text{ref}}^2}{f_{\text{out}}^2}\right) \quad [\text{dB}]$$

[1] Sun, Hanhan, et al. "A radiation tolerant clock generator for the CMS endcap timing layer readout chip." Journal of Instrumentation. 17.03 (2022): C03038.
[2] Li, Xiao-Ting, et al. "A 5.12-GHz LC-based phase-locked loop for silicon pixel readouts of high-energy physics." Nuclear Science and Techniques 33.7 (2022): 82
[3] Tavakoli, Javad, Hossein Miri Lavasani, and Samad Sheikhaei. "An Ultra Low Power Integer-N PLL with a High-Gain Sampling Phase Detector for IOT Applications in 65 nm CMOS." Journal of Low Power Electronics and Applications 13.4 (2023): 65.

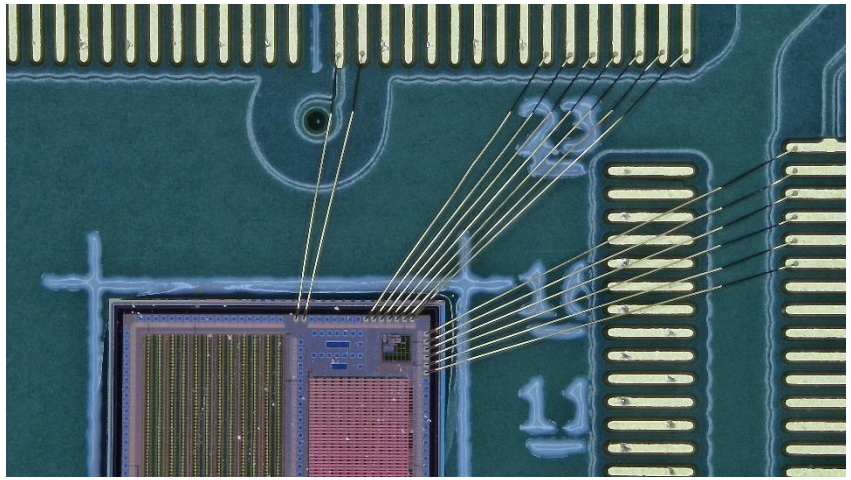
三、 结论

➢ 高性能锁相环设计

- 输入频率40MHz
- 输出频率160M-640MHz（可配置）
- 最大功耗：4mW
- 面积：0.125mm^2

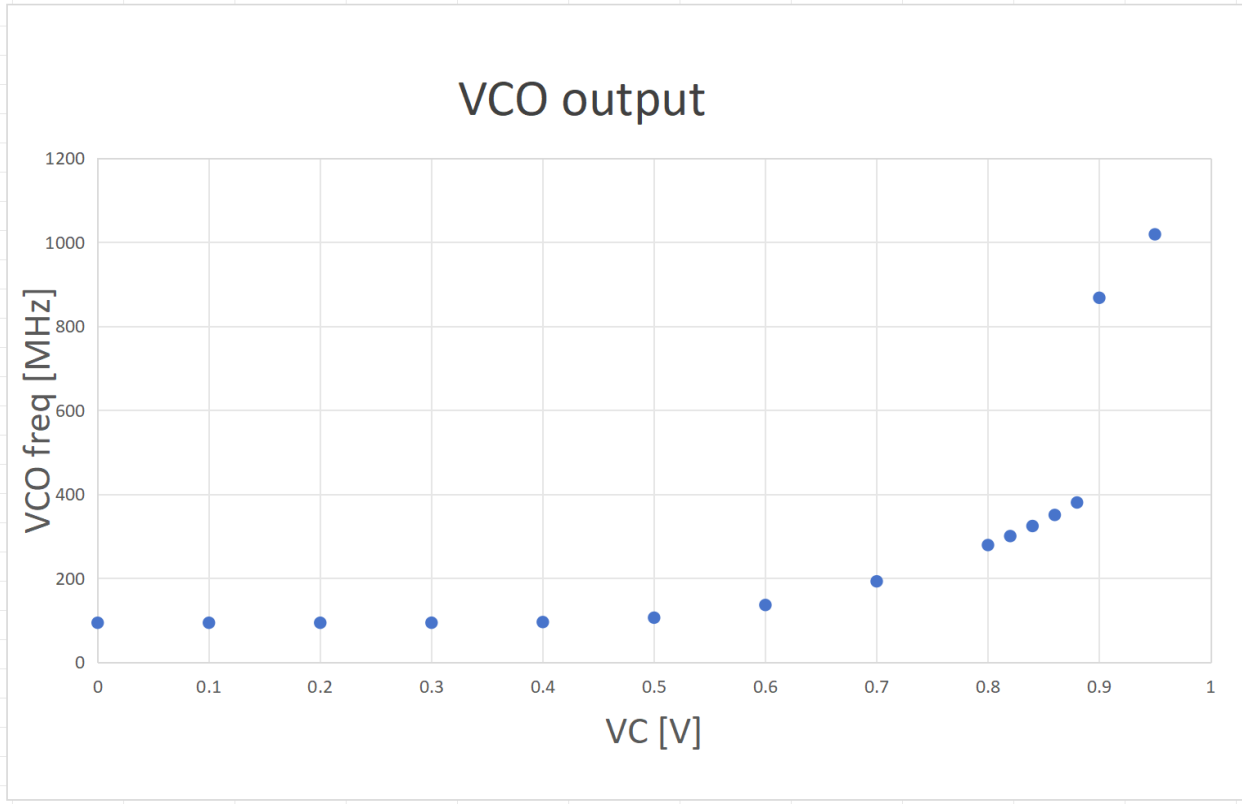


COFFEE3

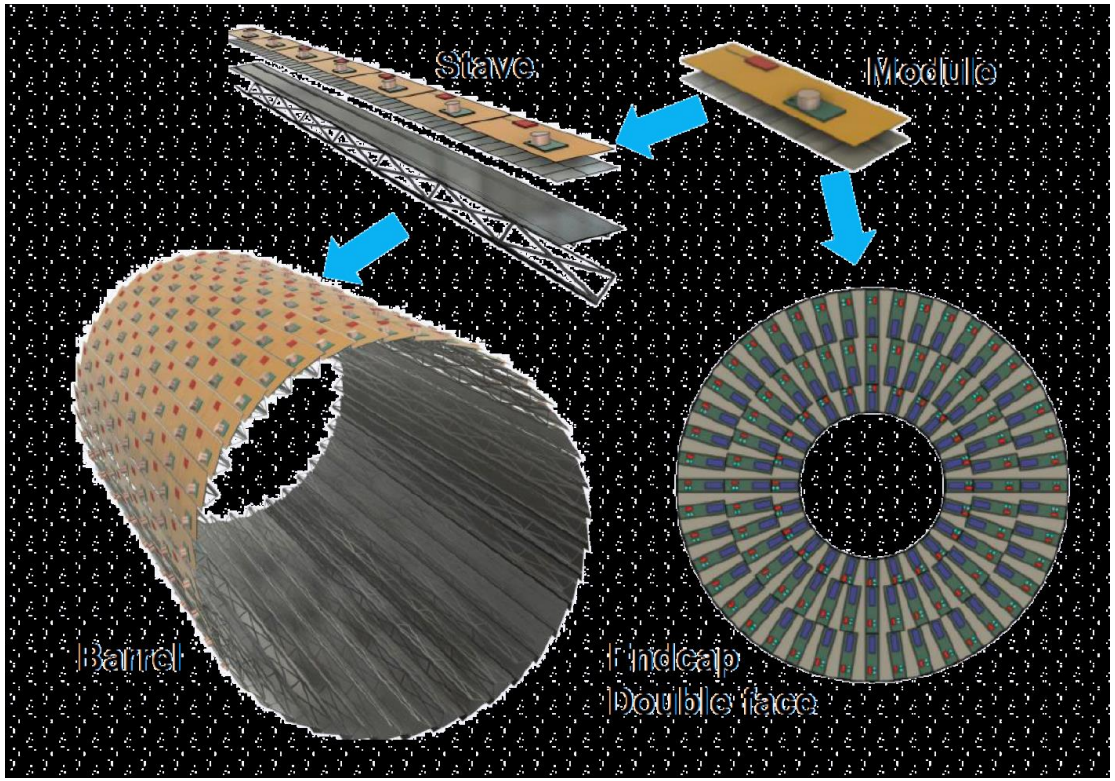


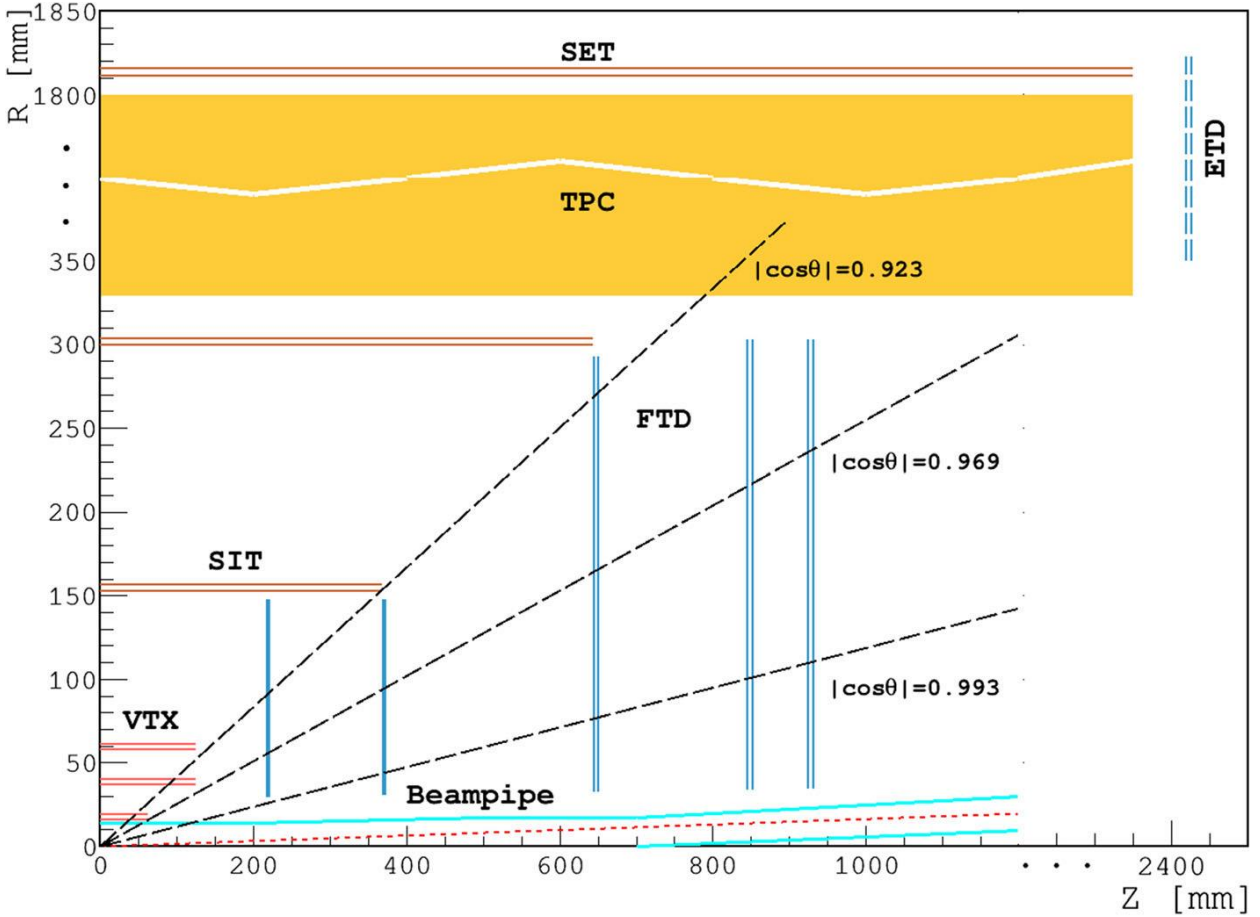
初步测试结果

VC[V]	freq [MHz]
0	93.7
0.1	93.7
0.2	93.7
0.3	93.8
0.4	95.4
0.5	105.8
0.6	136.05
0.7	192.4
0.8	278.8
0.82	300.2
0.84	324.15
0.86	350.5
0.88	380.15
0.9	867.68
0.95	1018.8



感谢大家聆听！





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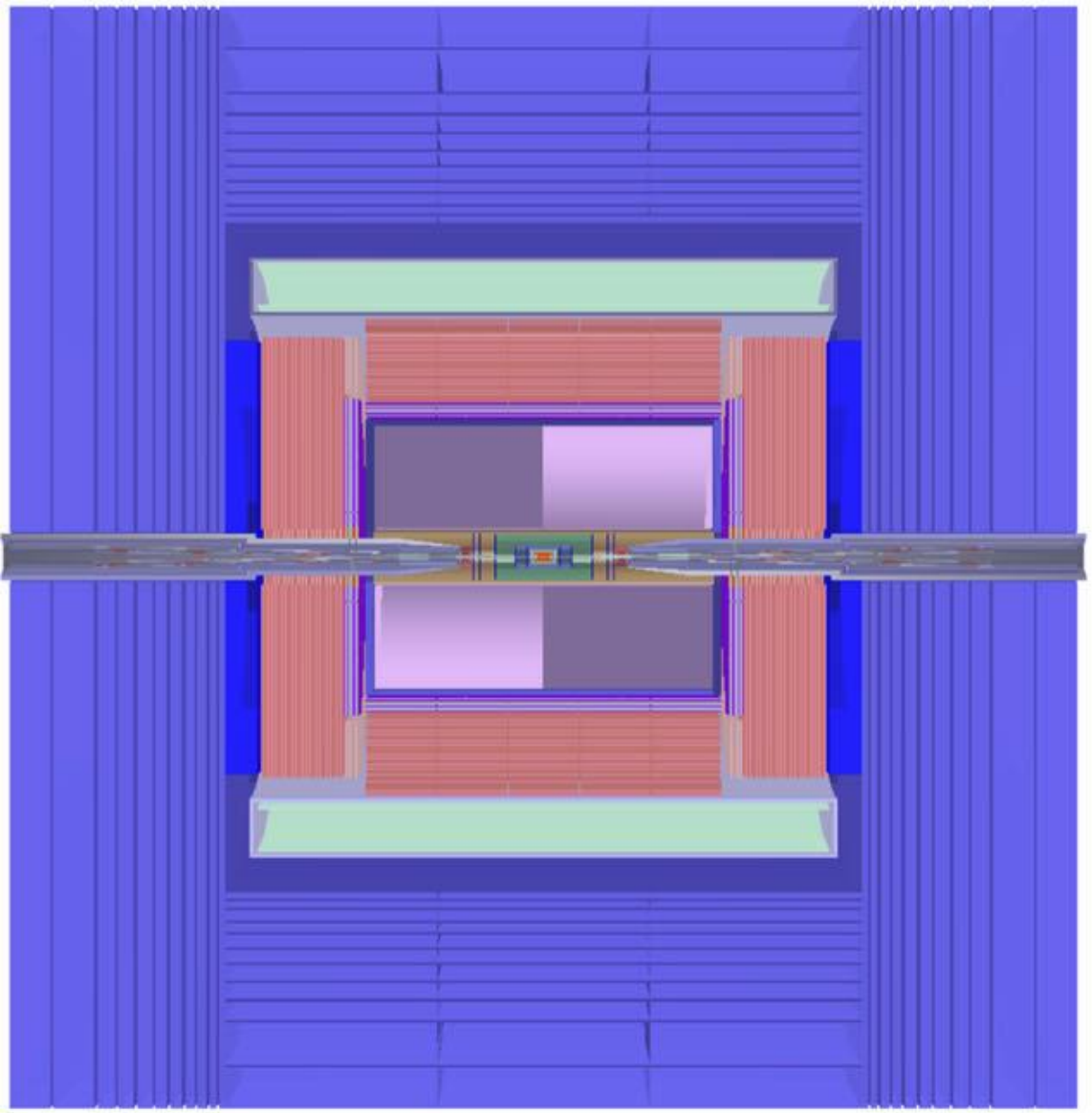
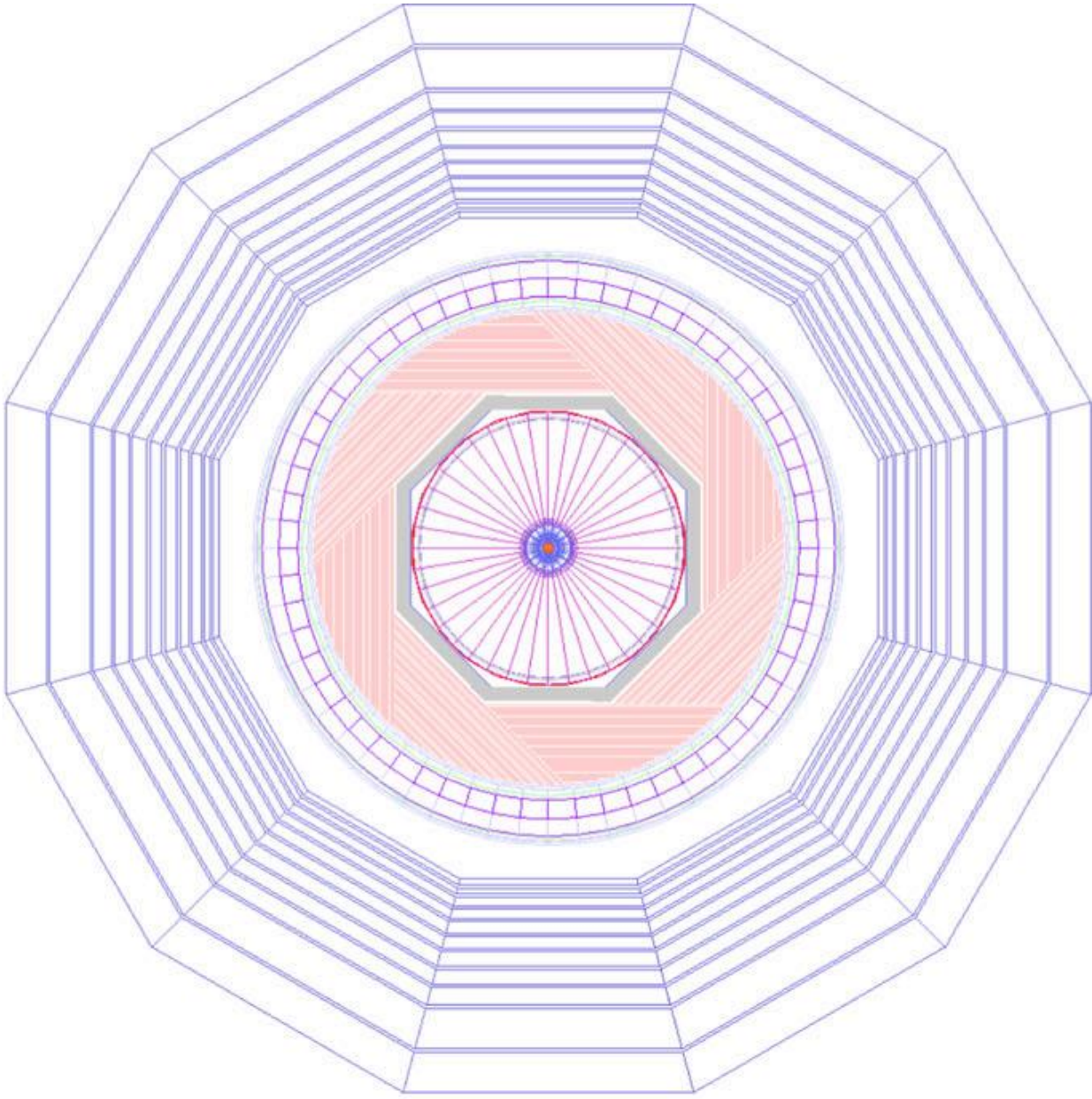
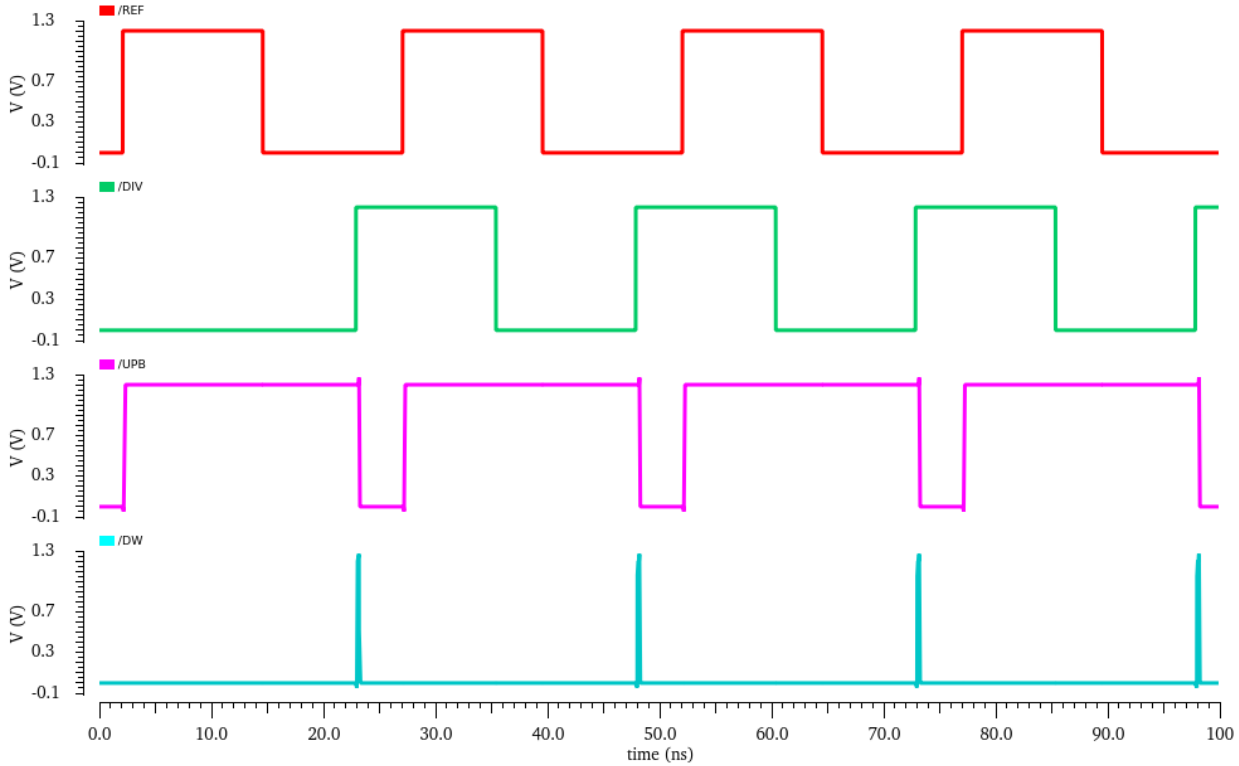
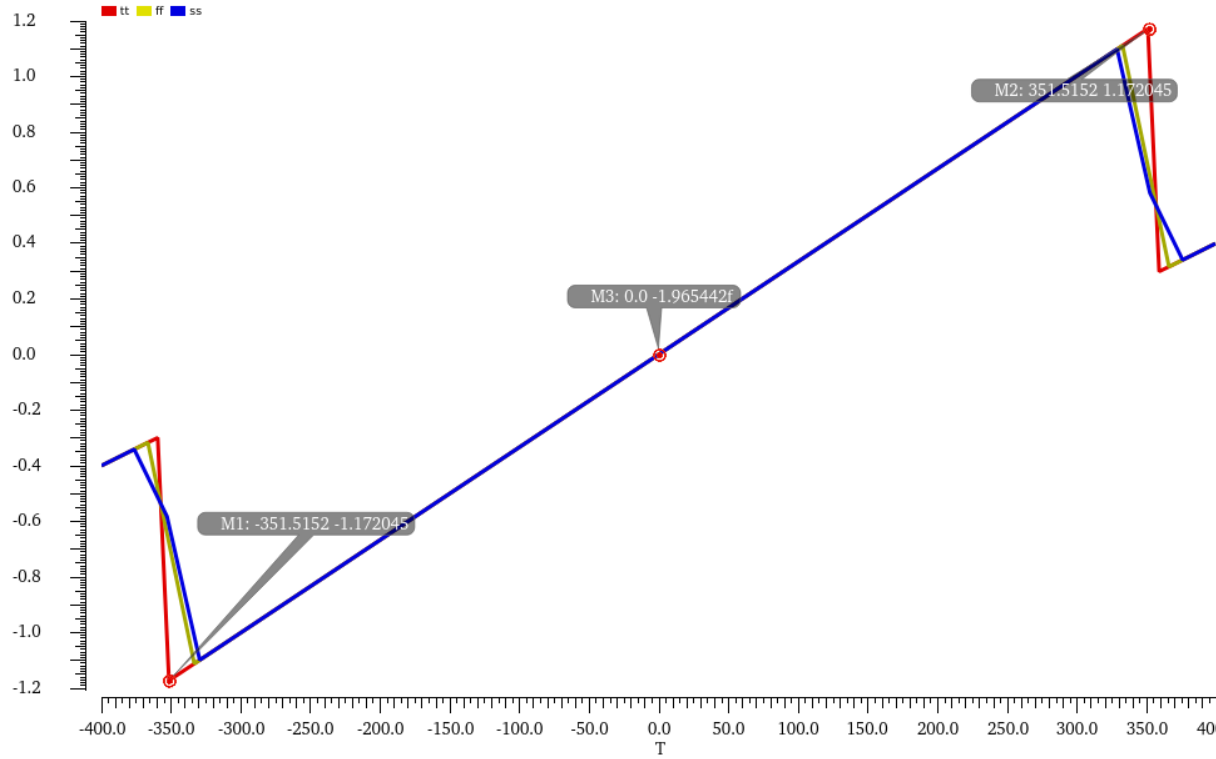


(a) $r - z$ view



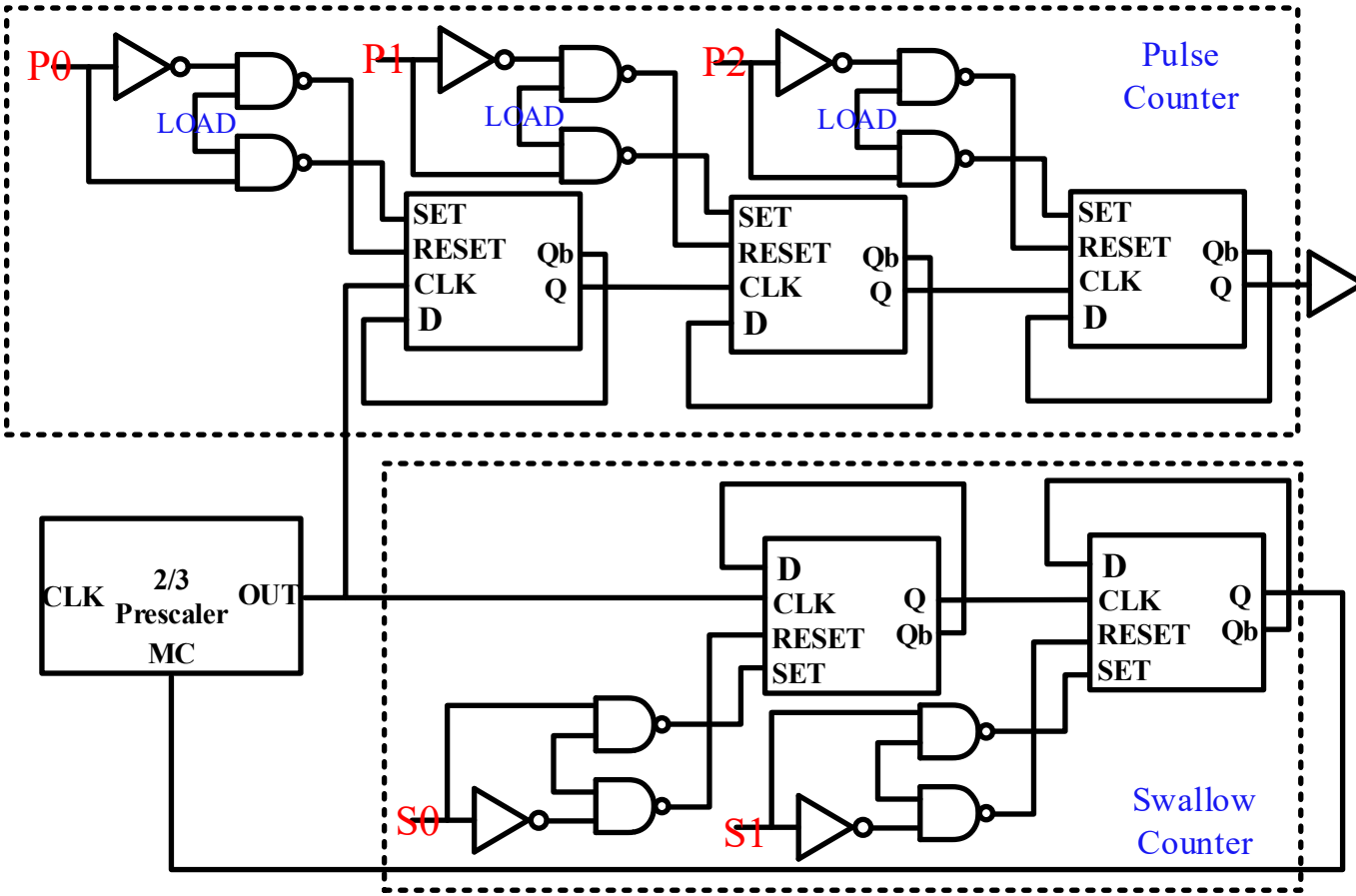
(b) $r - \phi$ view

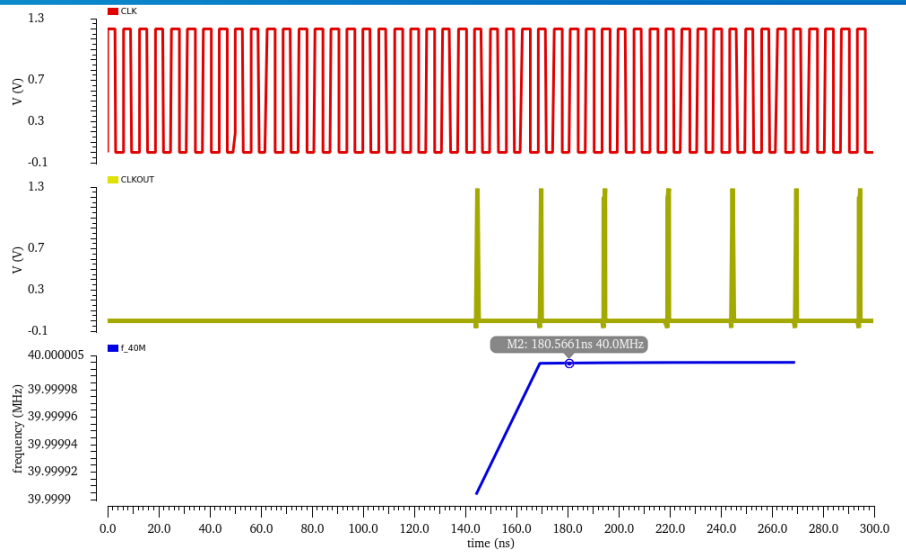




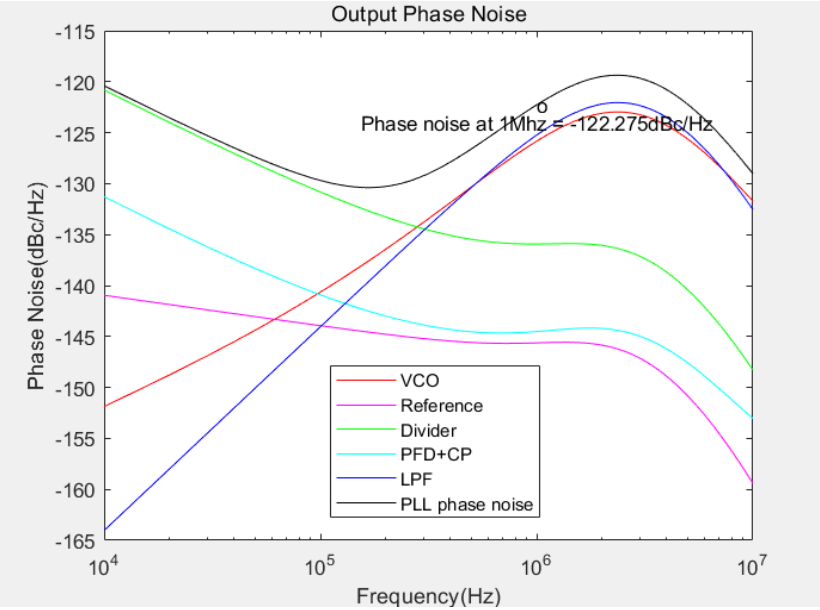
工艺角	功耗	检相范围
tt	0.16 mW	(-1.97π, 1.97π)
ff	0.17 mW	(-1.96π, 1.96π)
ss	0.15 mW	(-1.96π, 1.96π)

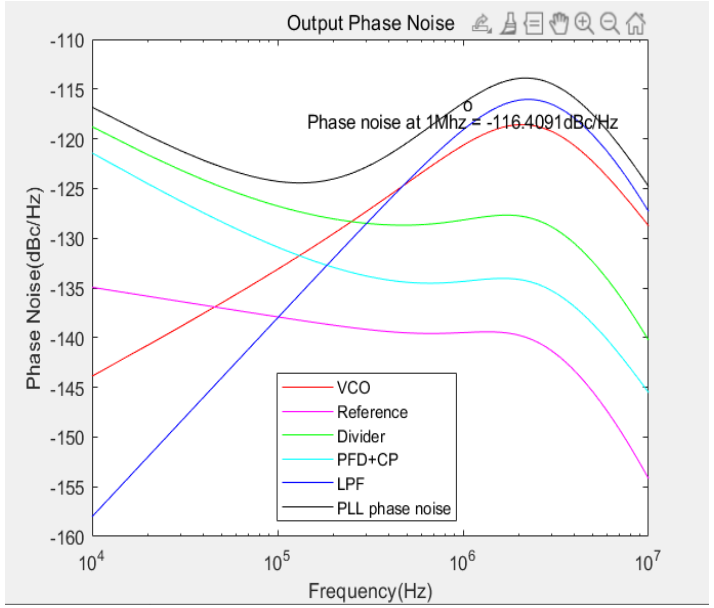
➢ 分频器仿真

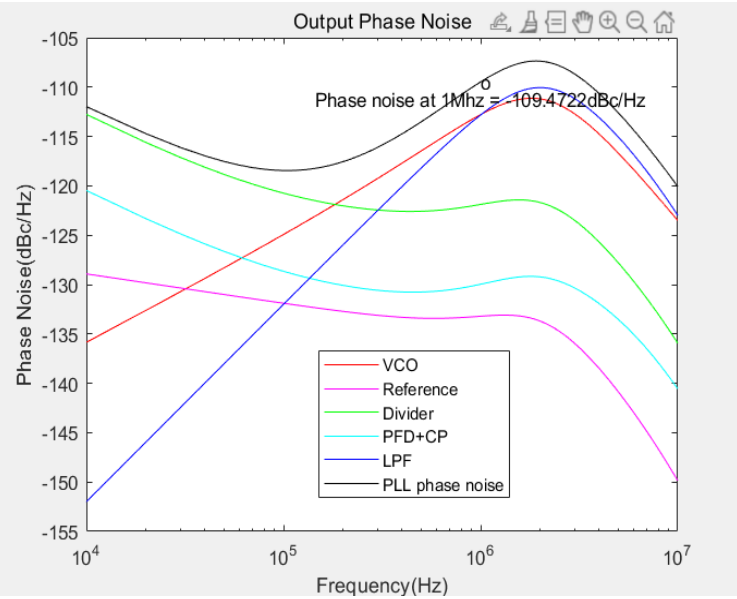




工艺角	160 MHz	320 MHz	640 MHz
tt	0.23 mW	0.28 mW	0.39 mW
ff	0.27 mW	0.32 mW	0.41 mW
ss	0.21 mW	0.26 mW	0.36 mW


Output Phase Noise
Phase noise at 1Mhz = -122.275dBc/Hz
Phase Noise(dBc/Hz)
Frequency(Hz)
VCO
Reference
Divider
PFD+CP
LPF
PLL phase noise


Output Phase Noise
Phase noise at 1Mhz = -116.4091dBc/Hz
Phase Noise(dBc/Hz)
Frequency(Hz)
VCO
Reference
Divider
PFD+CP
LPF
PLL phase noise


Output Phase Noise
Phase noise at 1Mhz = -109.4722dBc/Hz
Phase Noise(dBc/Hz)
Frequency(Hz)
VCO
Reference
Divider
PFD+CP
LPF
PLL phase noise