CEPC CMOS Strip Tracker

Xin Shi

On behalf of CMOS Strip Tracker Team

2024.12.13

Ref TDR Progress

✓ Add more prospects and plan

5.3.5 Prospects and plan

Responsible person: Qi YAN, Yiming LI, and Xin SHI

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For the sensor technology regarding the HVCMOS process, the priority in the coming few year is to develop a full-functional full-size sensor chip that meets the requirements imposed by the CEPC inner tracker. The development will be performed through a few iterations of chip submissions, including:

- A small pixel array which implement the targeted readout architecture (early 2025);
- One of more small prototypes for performance optimisation (2026);
- A large chip that meets or very close to the production version (2027).

With the small-scale sensor chip key performance will be studied and input will be provided for detector final design and prototyping.

The research and development timeline of CMOS Strip Chip for the next three years is listed in Fig. 5.47 where three versions of the CSC are scheduled to be fabricated. The CSC1 will be mainly focus on the independent CMOS strip sensor and front-end electronics separately. A preliminary reticle design for the CSC1 is sketched in Fig. 5.48. Once the devices are fabricated, a detailed evaluation of the macroscopic characteristics such as leakage current and capacitance as

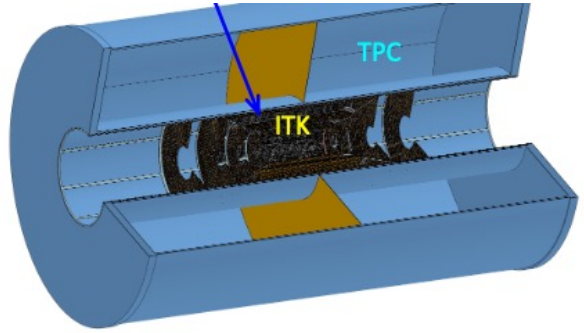


Figure 5.46: ITK installation

the function of bias voltage for the CMOS strip sensor (CSC1-A) will be carried out. In addition, the collected charge of the CSC1-A will be determined for both before and after irradiation. For the readout ASIC (CSC1-B), the initial noise and gain will be investigated utilizing customized testing board.

The CSC2 will explore the integration of CMOS strip sensors and circuits together on small area and large pitch, where the special attention need to be taken in terms of exploring the best strategy to separate the sensor with the active circuits when the sensor is applied high bias voltage. Finally, the target of the CSC3 will be the integration of large-area (2cm × 2cm) and narrow-pitch (20μm) monolithic chip in which a working solution to prevent the cross-talk between each strip need to be consolidated.

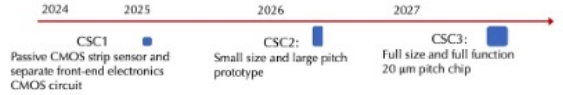
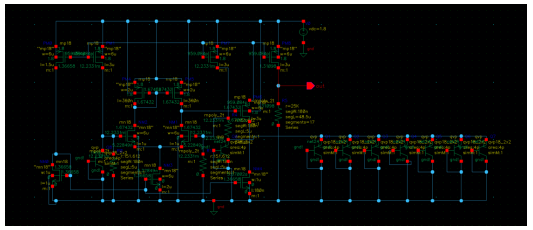


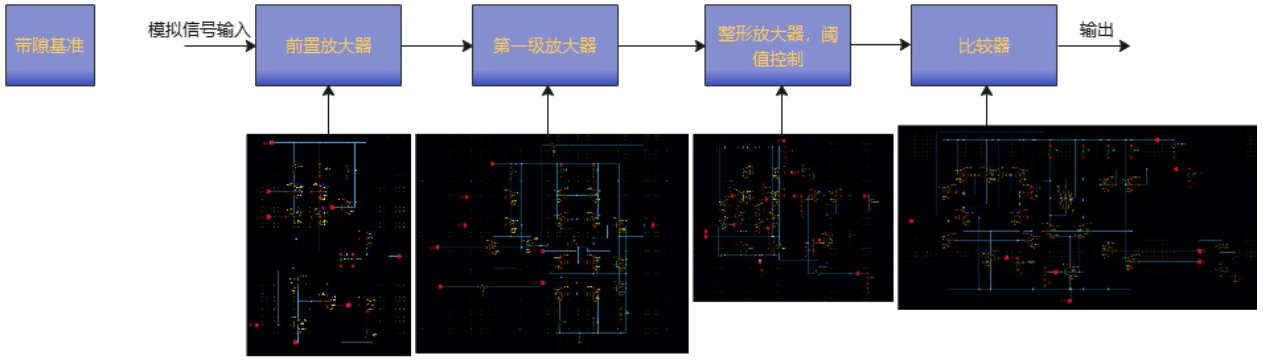
Figure 5.47: CSC Research Timeline.

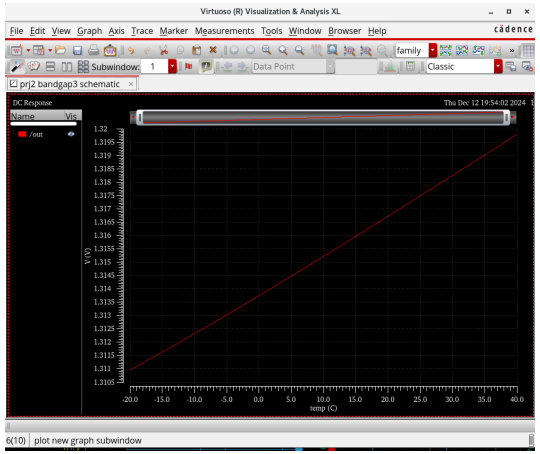
The prototyping of the detector modules, including the integration process, the supporting and cooling structure will be carried out in parallel to the development of the sensor chips. Small scale sensor chip can already be used to assemble prototypes with sensor, readout and supporting structures as key intermediate steps.

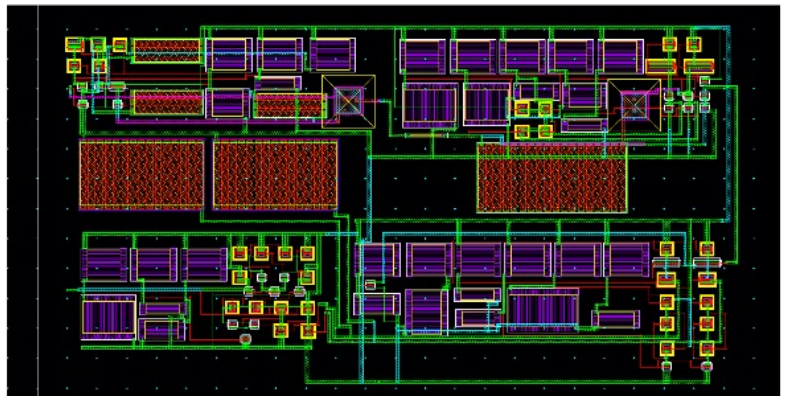
电路仿真进展

1. 完成了AFE部分的前置放大器，第一级放大器，整形放大器，比较器的电路设计，版图设计，前仿真，后仿真等设计步骤。
2. 完成了整体版图的DRC，LVS检查。
3. 完成了带隙基准电路的设计（为模拟电路部分提供基准偏置电流）

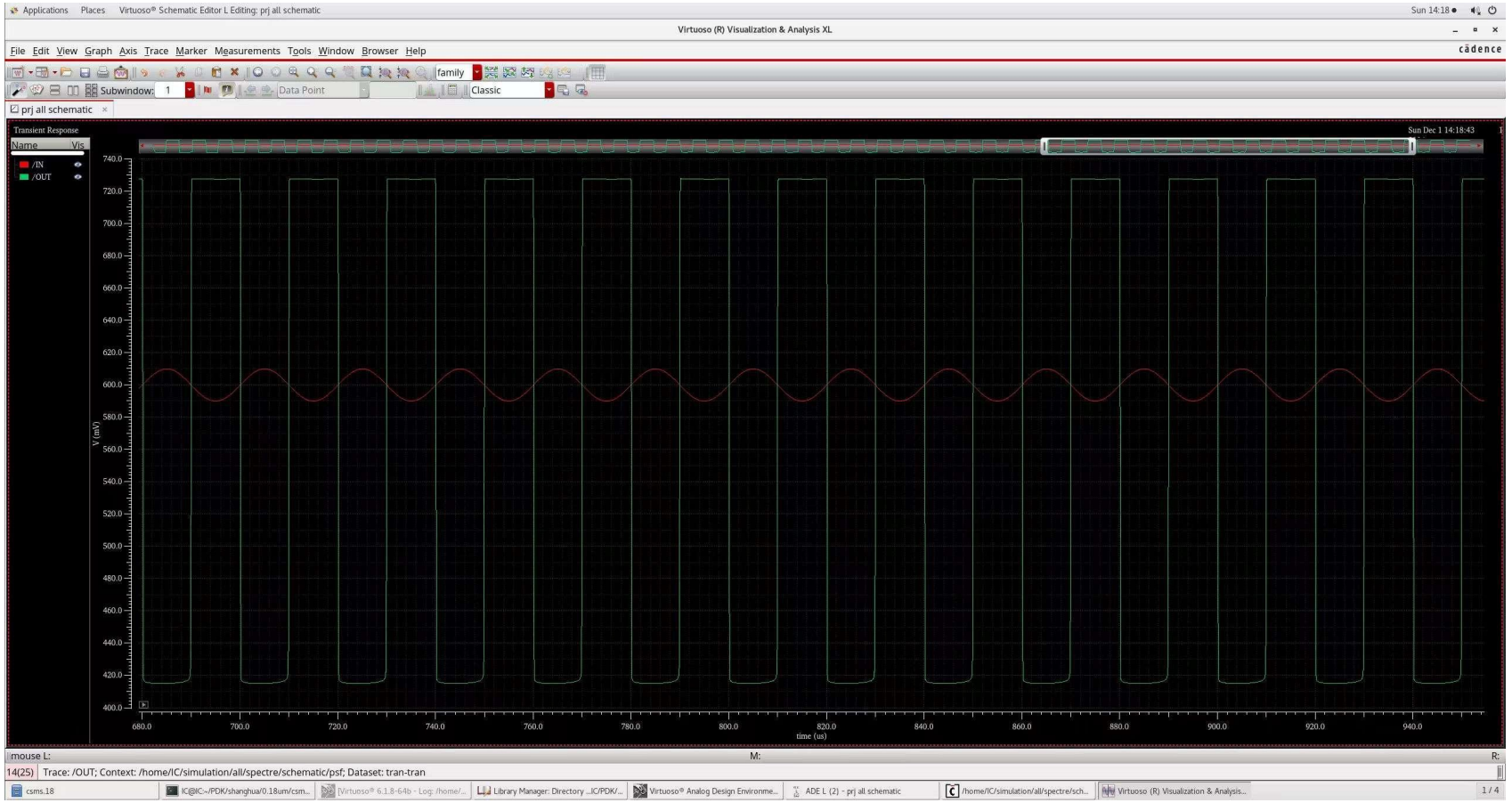






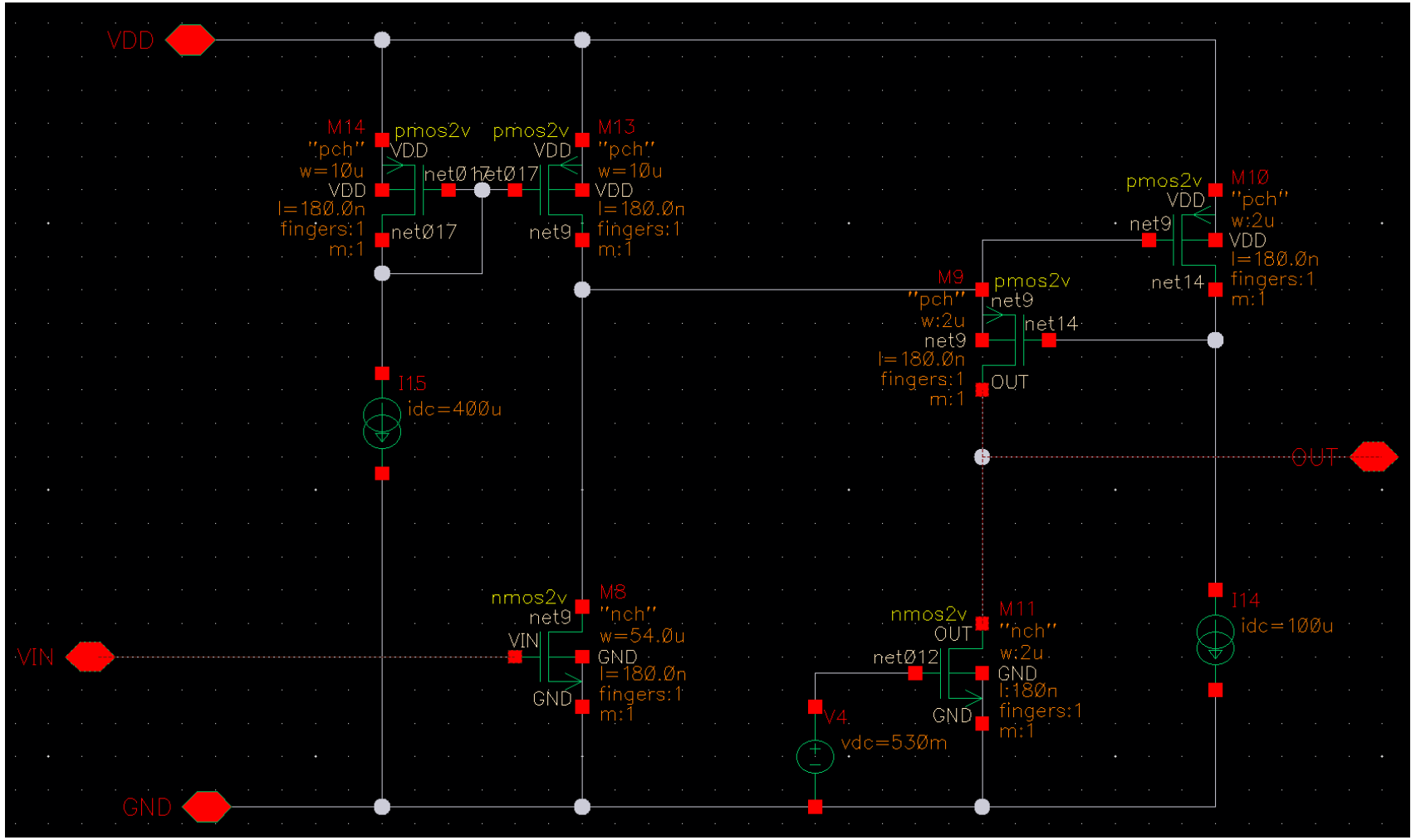


- 从仿真结果可知，此AFE电路，可完成积分，放大，比较等功能，
- 增益、带宽等参数均能满足硅微带传感器的读出需求。



下一步： 完成 Senser + AFE 的版图设计。

CSA 开环电路及参数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M14
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w=10u
VDD
l=180.0n
fingers:1
m:1
pmos2v
VDD
net017
net017
pmos2v
VDD
M13
"pch"
w=10u
VDD
l=180.0n
fingers:1
m:1
net017
net9
I15
idc=400u
M9
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w:2u
net9
l=180.0n
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net9
net14
OUT
pmos2v
VDD
net9
M10
"pch"
w:2u
VDD
l=180.0n
fingers:1
m:1
net14
OUT
VIN
nmos2v
net9
VIN
M8
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w=54.0u
GND
l=180.0n
fingers:1
m:1
GND
nmos2v
OUT
net012
M11
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w:2u
GND
l:180n
fingers:1
m:1
GND
V4
vdc=530m
I14
idc=100u
GND

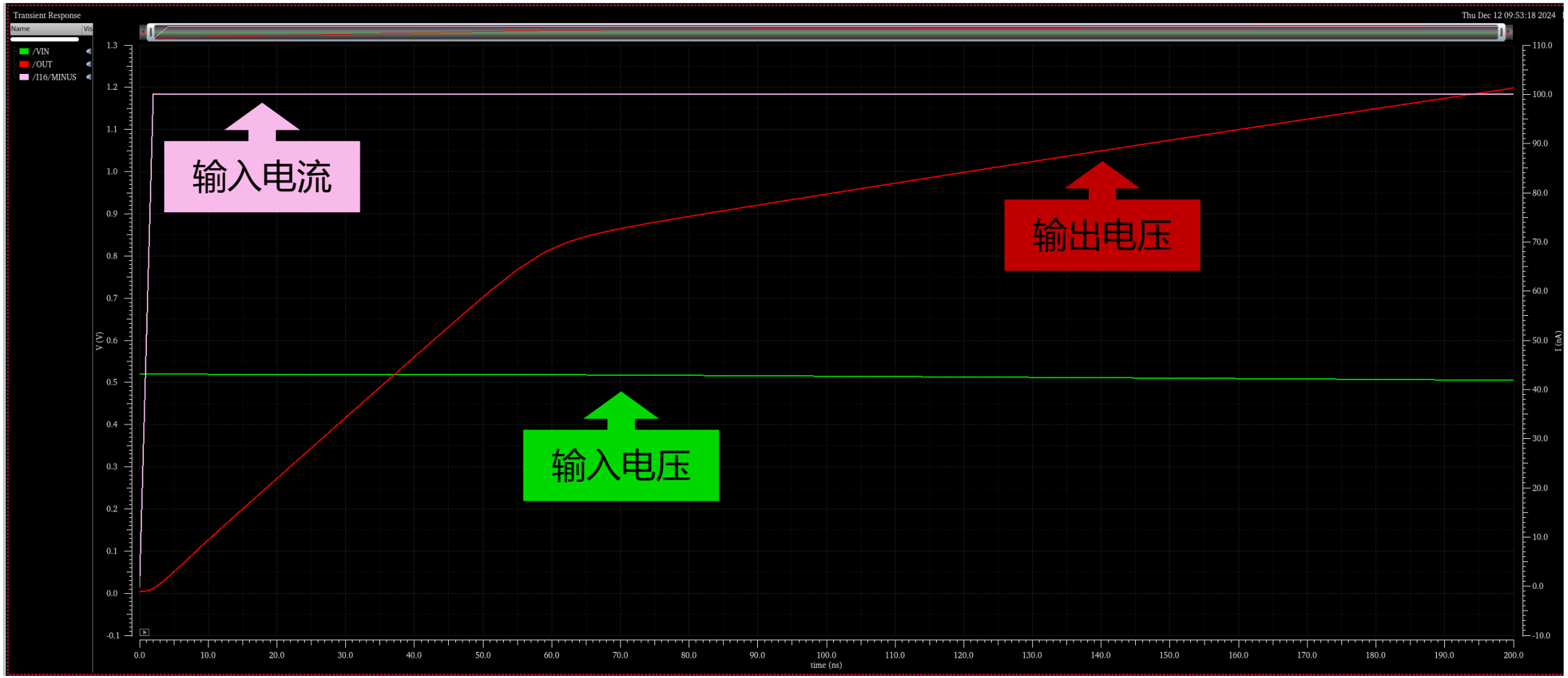
开环AC 仿真

在频率约等于352MHZ时，增益下降3db，相位下降45°，下限截止频率约为352MHZ

闭环 AC 仿真

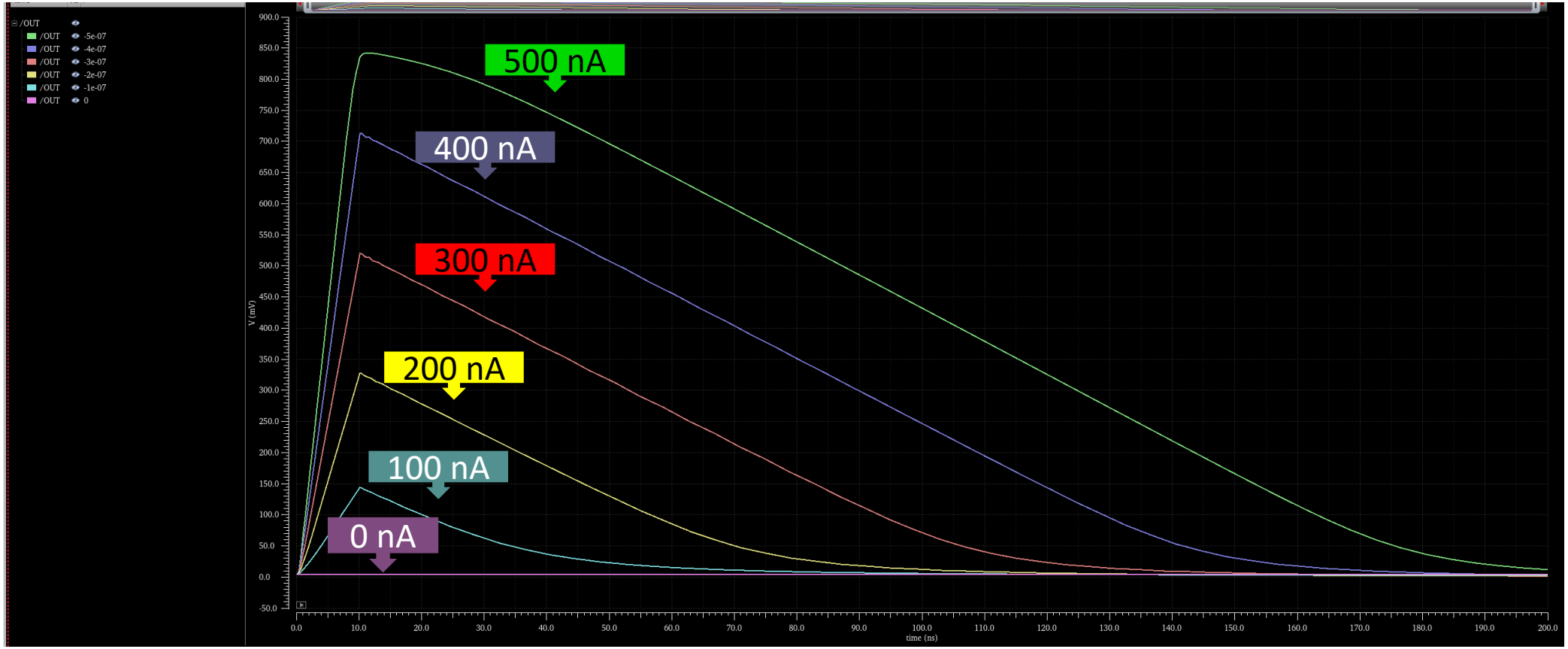
在频率约等于109MHZ时，增益下降3db，相位下降45°，下限截止频率约为109MHZ

CSA 输入电流信号仿真



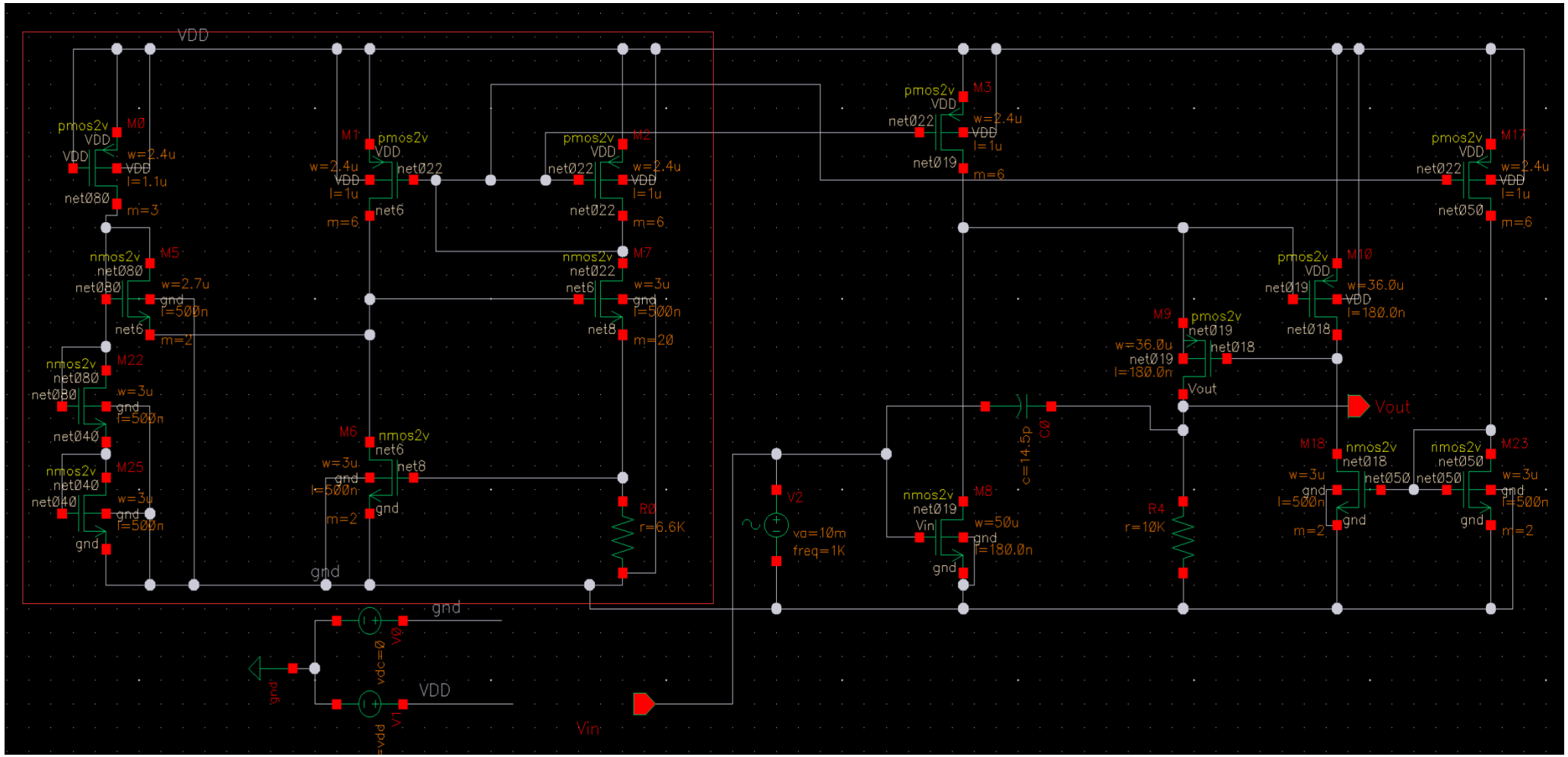
输入电流的大小为88.89nA(代表的电流方向为流出csa电路的方向)。在输出电流的作用下电容开始反向充电，从而导致输入电压微小幅度下降升，输出电压会把输入电压微小的变化放大，产生变化放大的输出电压，在10ns内就可以产生125mV的输出电压幅度变化。

放大效果

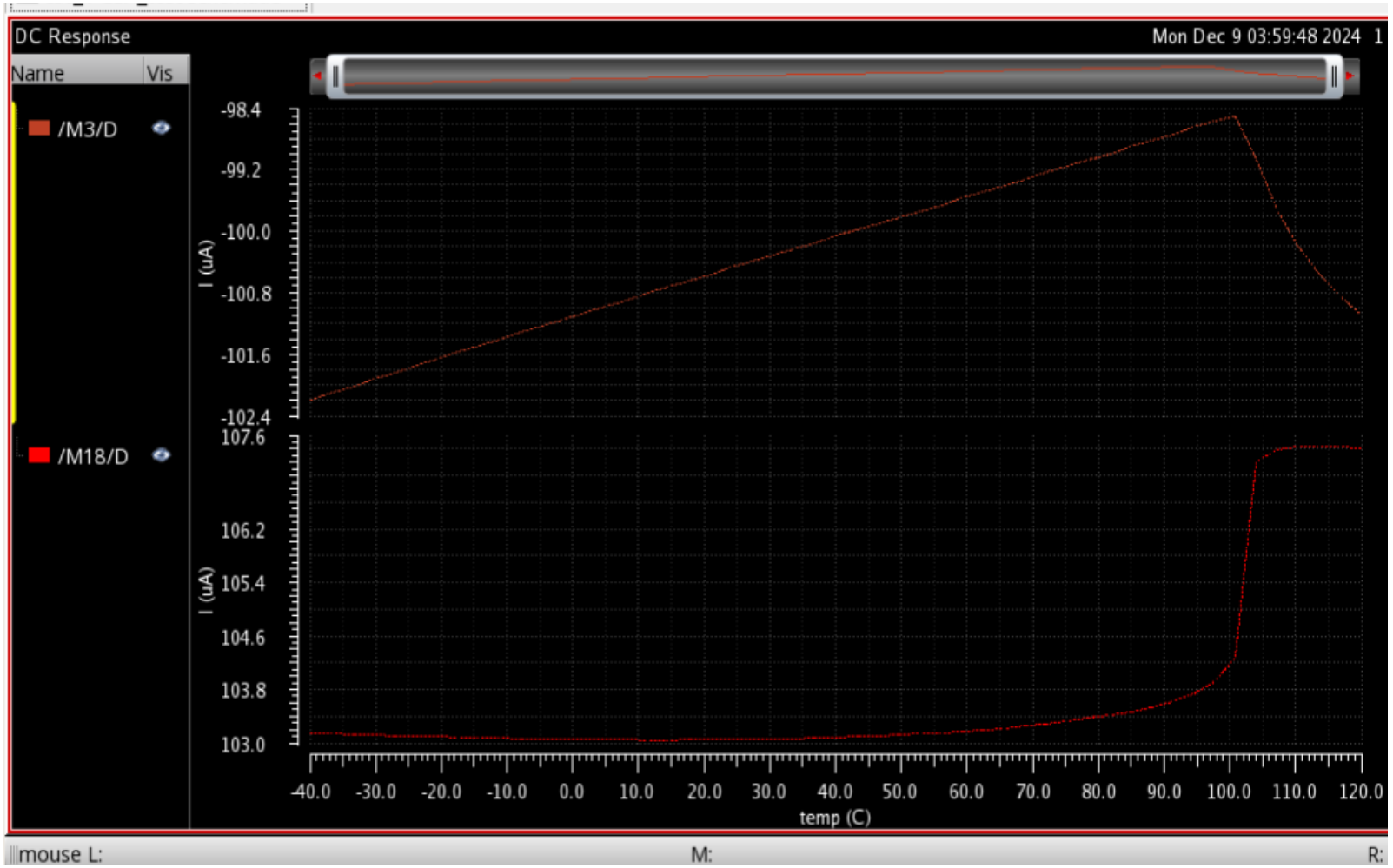


静态工作点工作在520mv，10ns之前进行充电，10ns之后进行放电，恢复静态工作点。用输入电流I分别等于0nA、100na到500na代表采集到的电荷数量。输出电压随时间的变化关系。在较小的输入电流和较短的响应时间内也可以产生比较大的输出电压变化。

CSA 电路中的基准电流源改进电路图参数

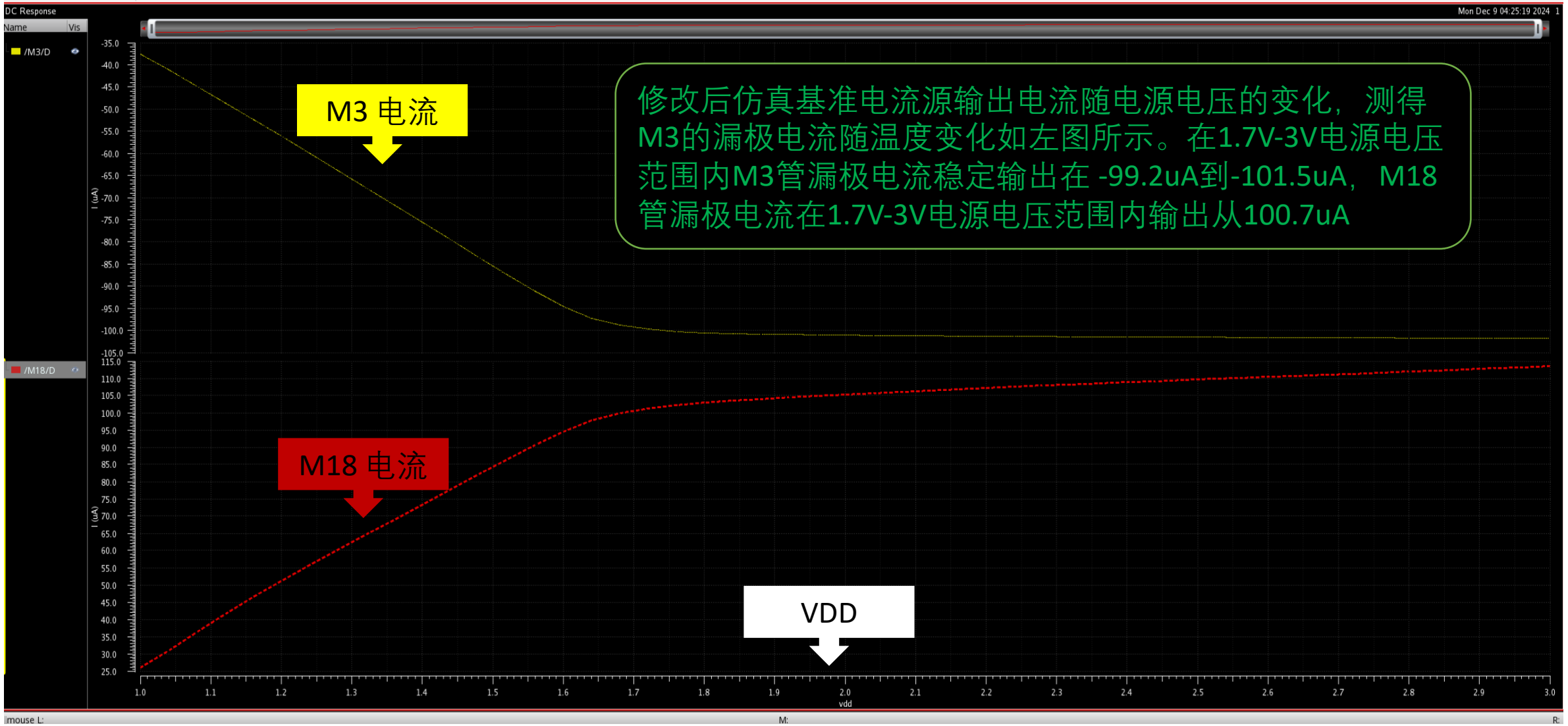


CSA 电路中的基准电流源电流随温度变化图

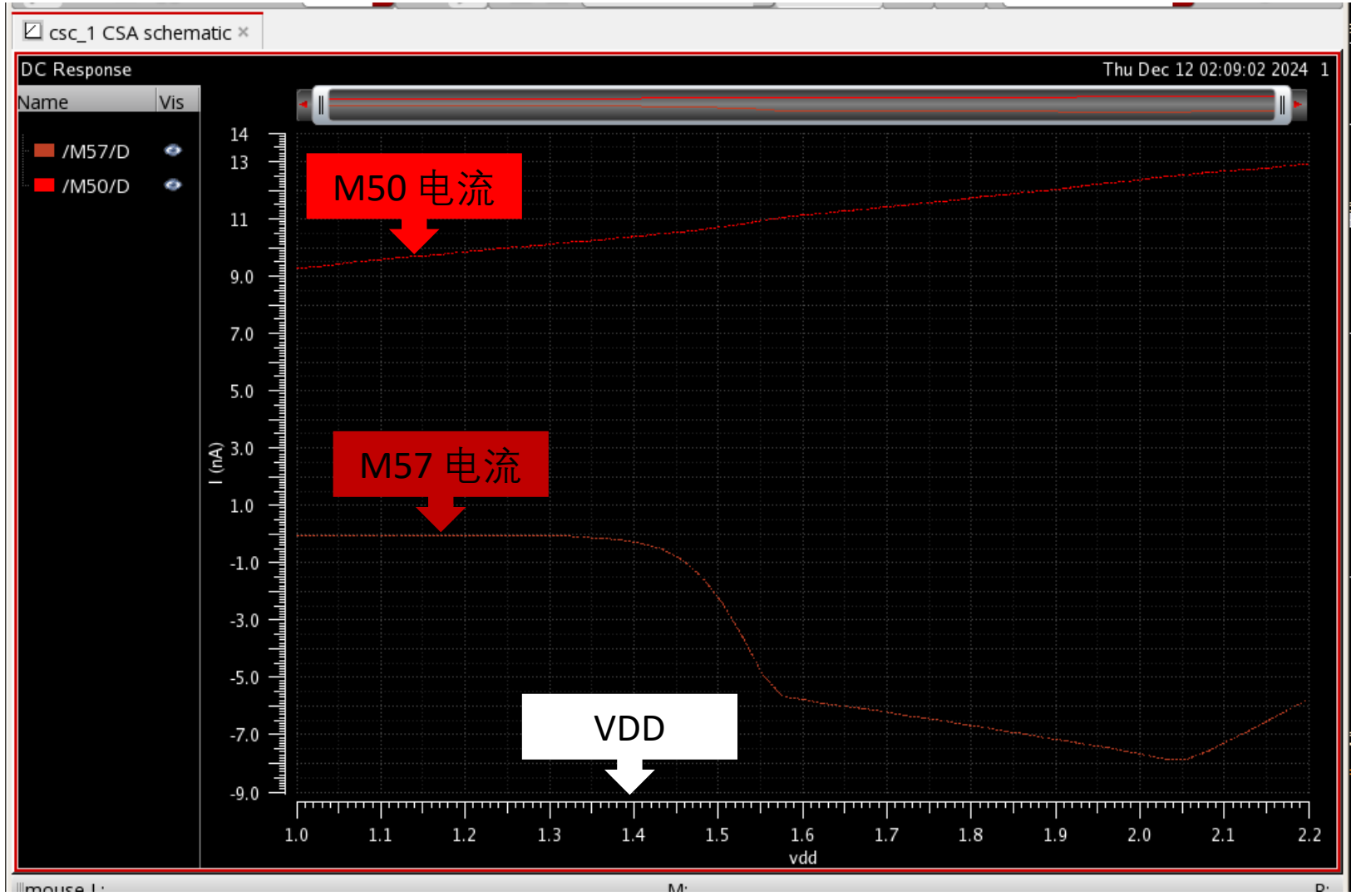


修改后仿真基准电流源输出电流随温度的变化，测得M3的漏极电流随温度变化如左图所示。在-40°C—100 °C温度范围内M3管漏极电流输出范围在 -102.17uA至-98.50uA，M18管漏极电流在-40°C—100 °C温度范围内输出较为稳定于103.06uA至104.20uA之间

CSA 电路中的基准电流源变化

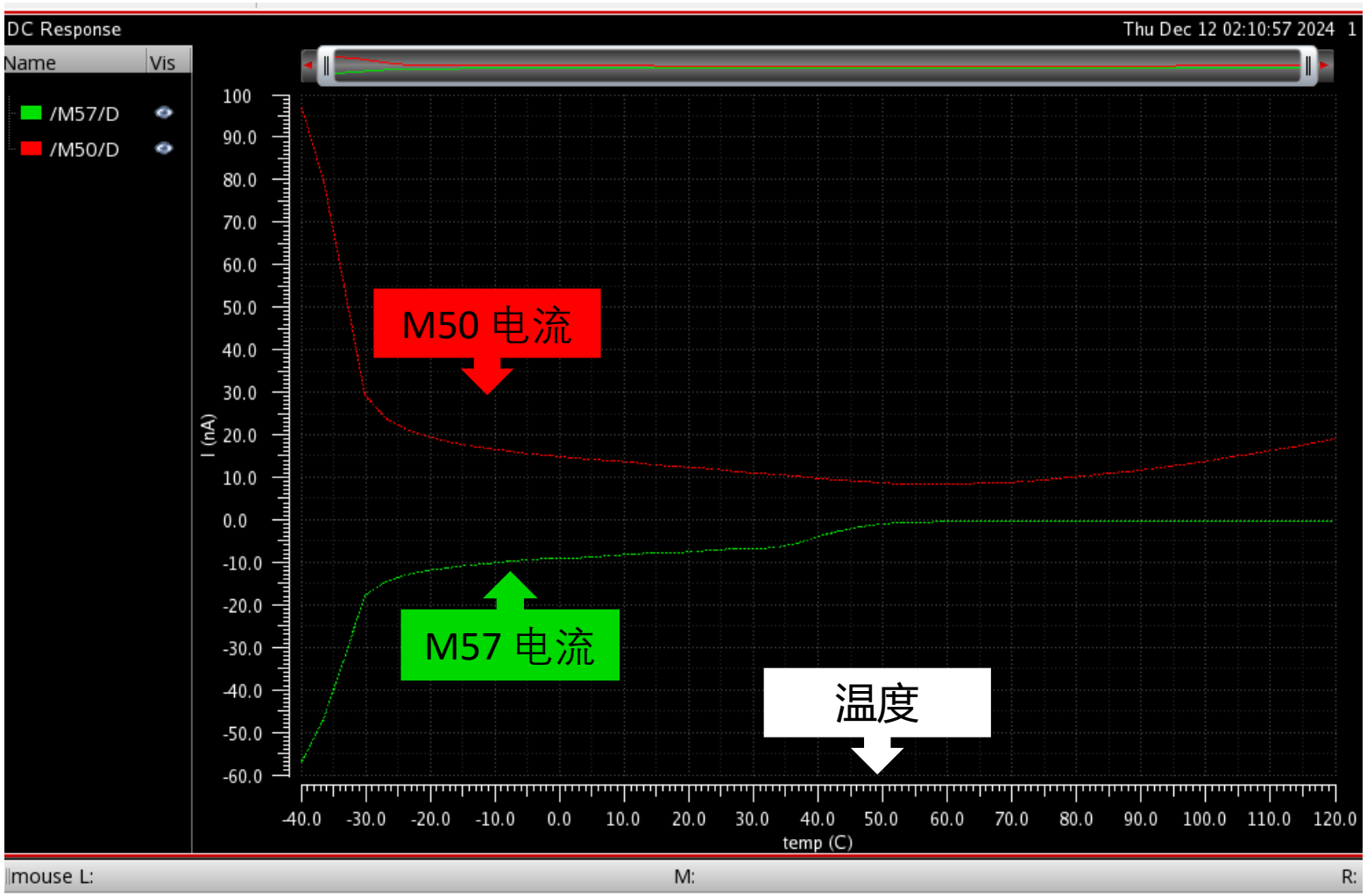


纳安级基准电流源电流随电源电压VDD变化图



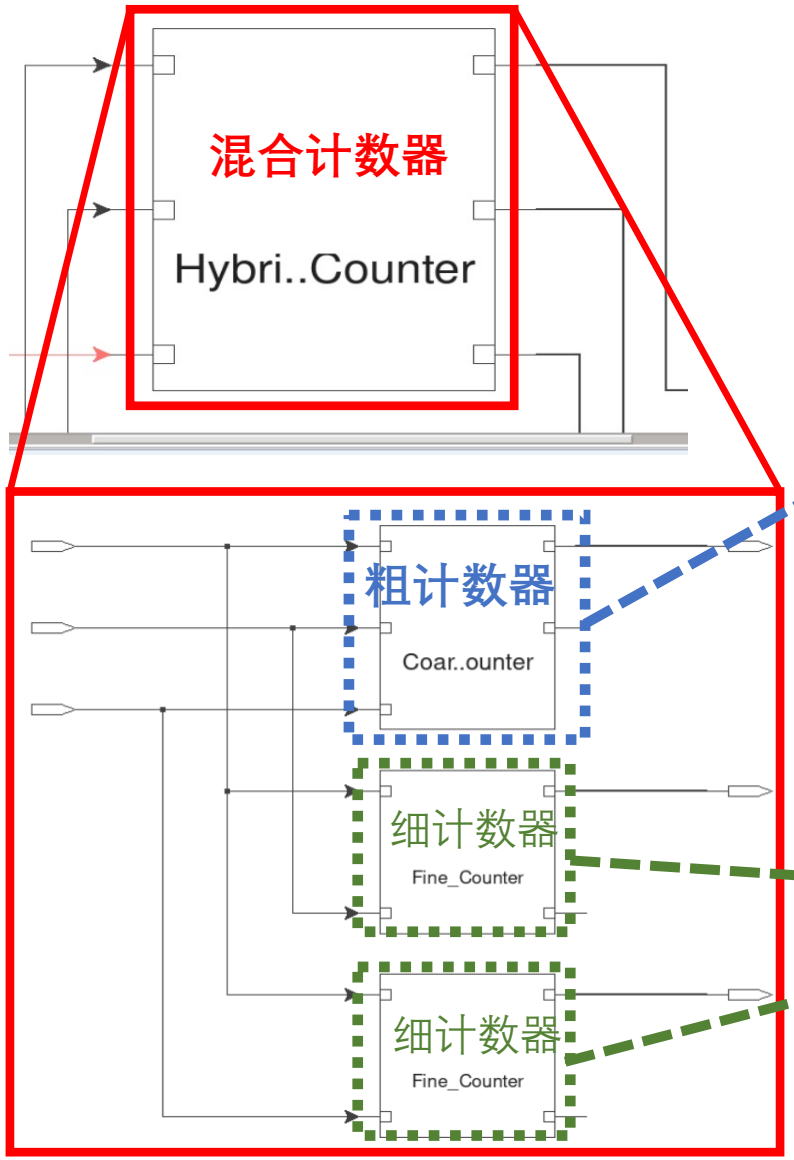
基准电流源输出电流随电源电压的变化，测得M57漏极电流随电源电压变化如左图所示。在1.6V-2V电源电压范围内M3管漏极电流稳定输出在 -5.75nA到-7.67nA，M50管漏极电流在1.7V-2V电源电压范围内输出从-11.17nA到-12.4nA

纳安级基准电流源电流随温度变化图

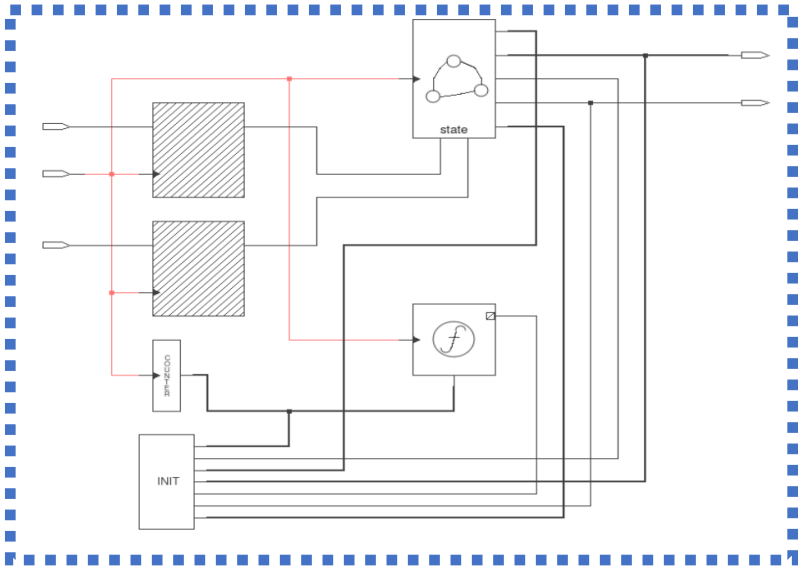


纳安级基准电流源输出电流随温度的变化，测得M57的漏极电流随温度变化如左图所示。在-20°C—120 °C温度范围内M3管漏极电流输出范围在 9nA至20nA，M50管漏极电流在-20°C—40 °C温度范围内输出较为稳定于-11nA至-3.5nA之间

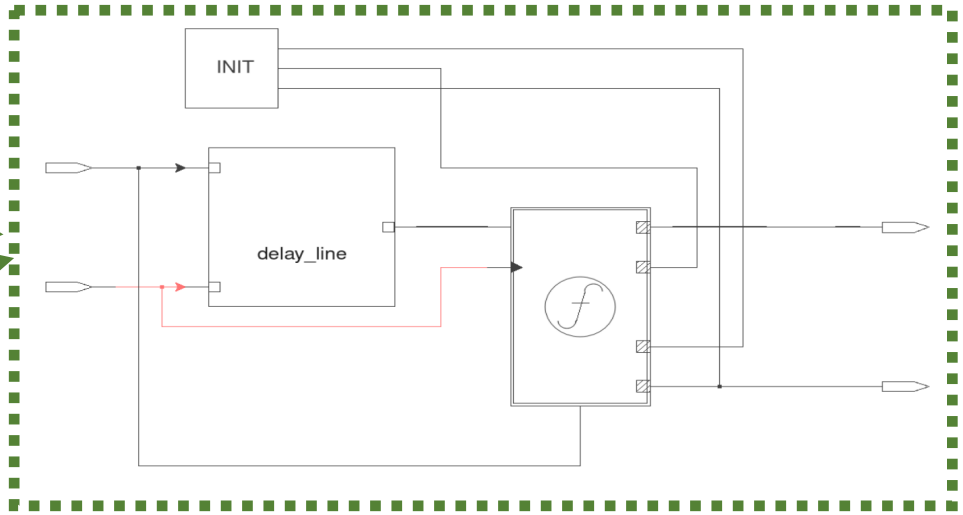
TDC 数字建模



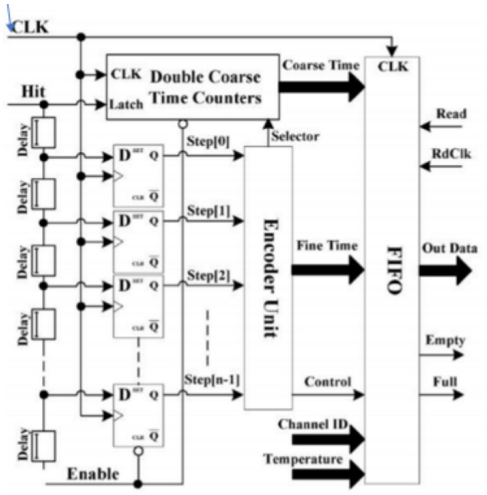
粗计数器：记录从启动信号上升沿到停止信号上升沿之间的时钟周期数。

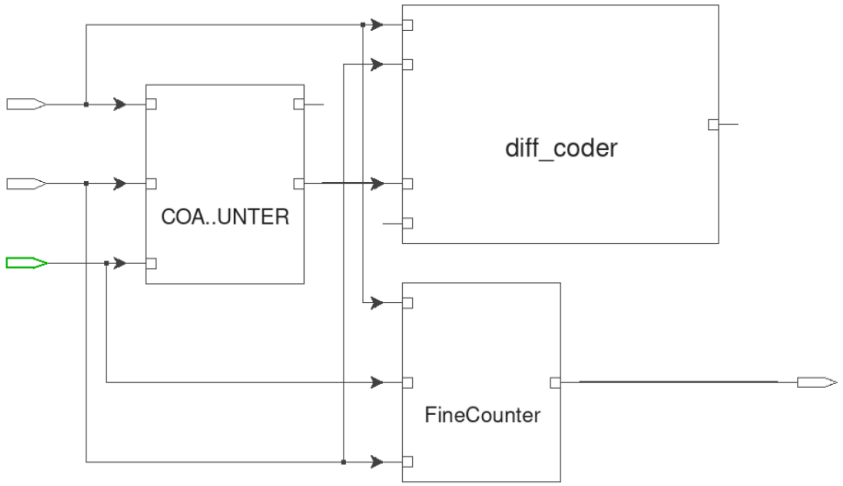


细计数器：延迟链结构，记录启动和停止信号两个上升沿之间的精确时间差。

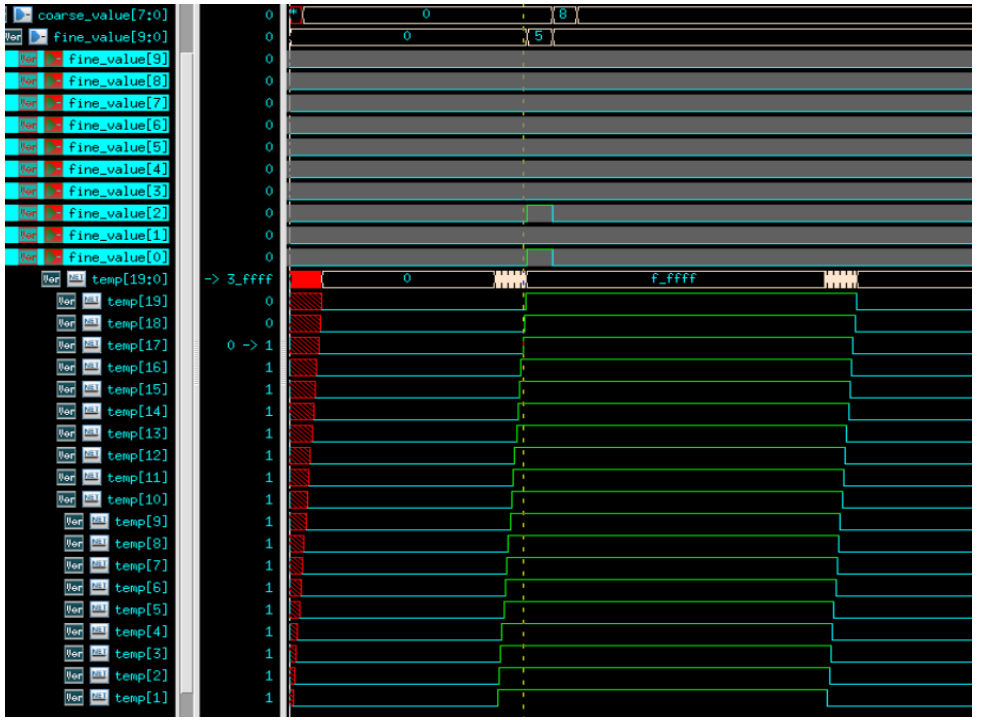


- 对同一时钟和HIT信号进行仿真，验证粗计数器和细计数器同时计数的结果



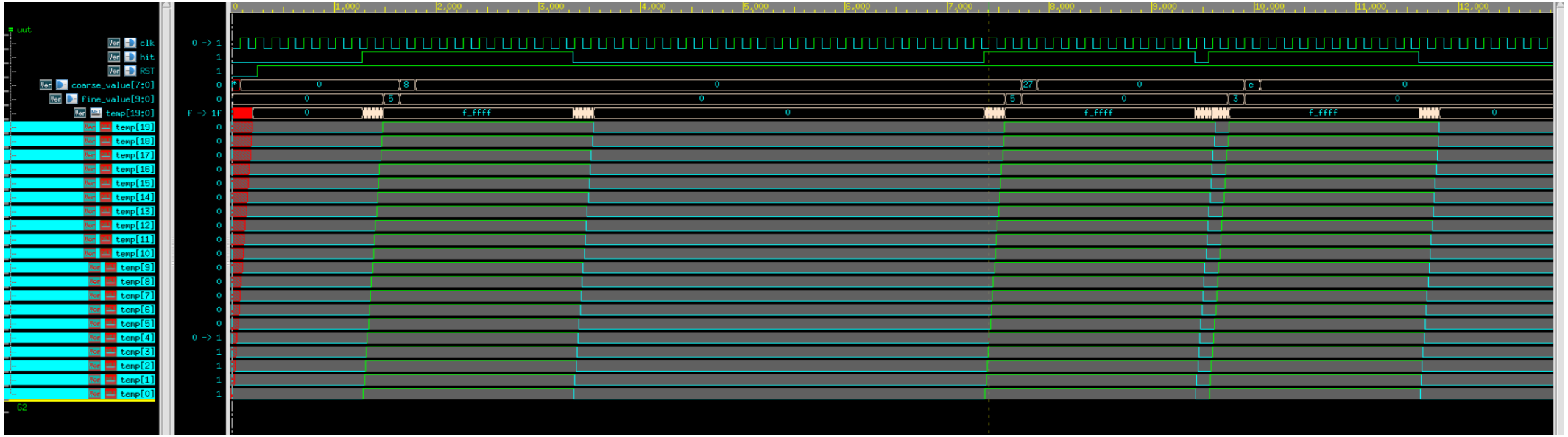


- 对细计数器的输出值进行了温度计编码



模型仿真

时钟周期：20纳秒（ns）



下一步工作：设计FIFO对计数器结果进行输出