SIPM READOUT SMALL SYSTEM

Jie Zhang on behalf of the electronics team

Institute of High Energy Physics, CAS

Institute of High Energy Physics
Chinese Academy of Sciences

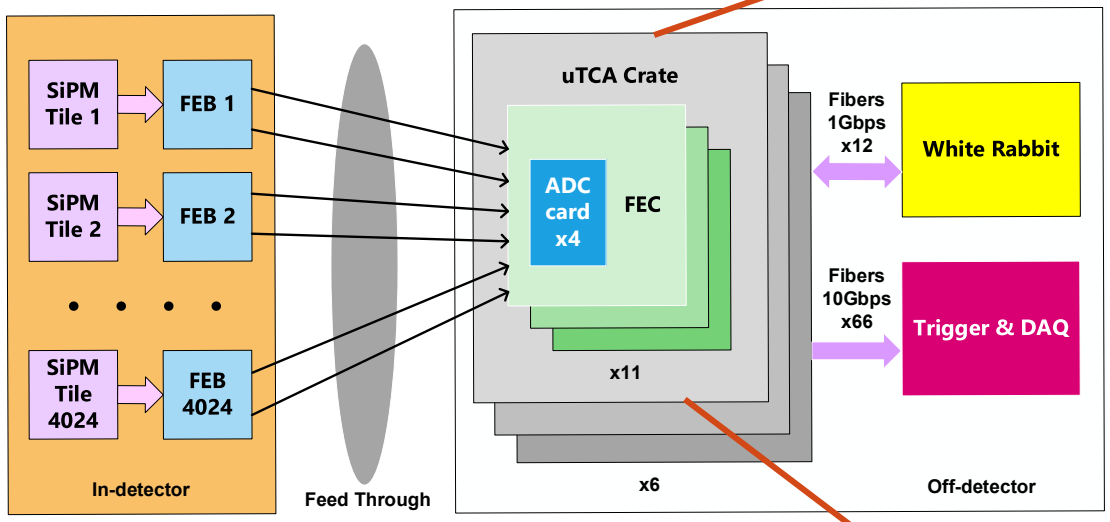
CONSIDERATION

- Up to thousands of channels
- Custom front-end electronics
  - Custom pre-amplifier
    - Single p.e. to ?
    - or TOT
  - ADC or TDC or ADC+TDC
    - Compatible with ASIC scheme or discrete device scheme
    - ADC >=12 bits (SNR, range)
    - TDC <= 20 ps
  - Adjustable multi-channel bias voltage (<200V)
- Universal back-end FPGA readout system
  - White-Rabbit clock synchronization and timing
  - External trigger input for beam or cosmic-ray test
- Universal cable between front-end and back-end
  - Analog or digital signals
  - LV and HV power supply

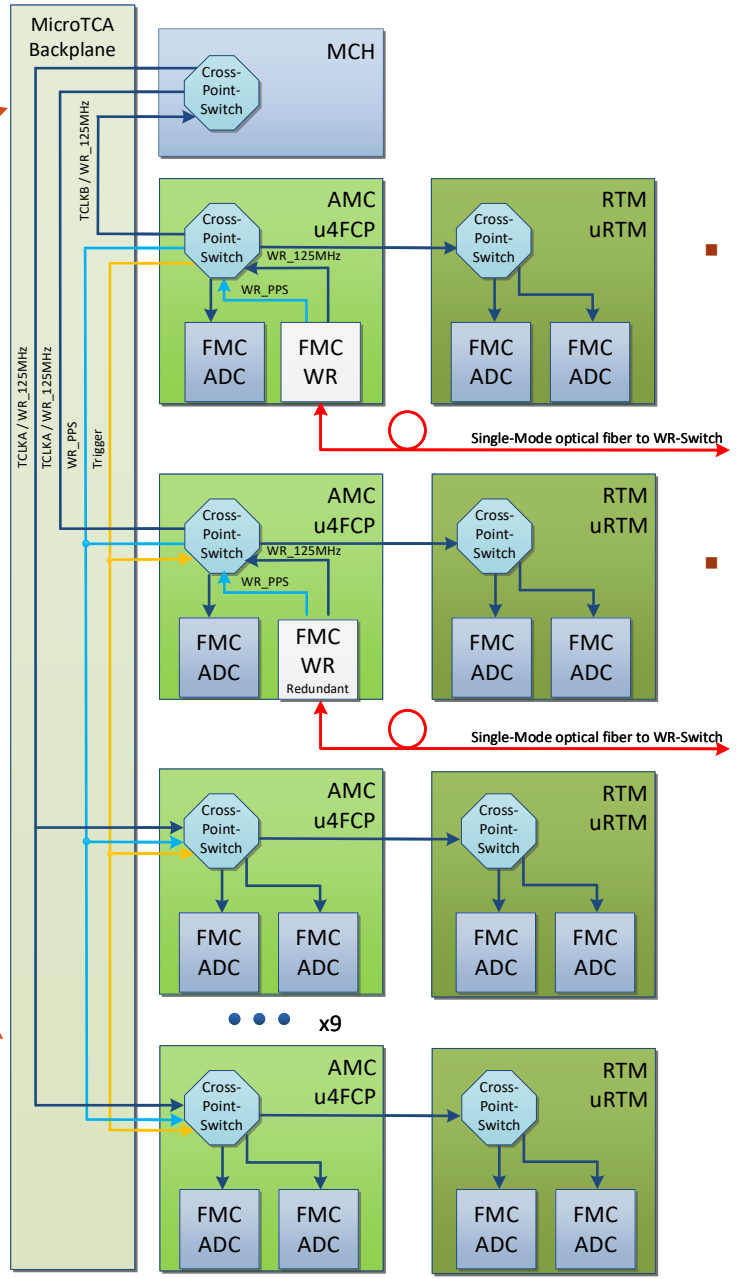
DISCRETE DEVICE SCHEME

Commercial pre-amplifier, ADC or TDC

EXAMPLE:
JUNO TAO READOUT ELECTRONICS



- In-detector
  - Discrete readout: 2 channels/SiPM tile
  - 8064 ch
- Off-detector
  - **6 uTCA.4 crates**
    - Each crate has 12 slots and will be mounted with **11 FEC boards**
      - 9 FEC boards with 4 ADC FMC cards
        - Each ADC FMC card supports 32 channels
      - 2 FEC board with 3 ADC FMC cards and 1 WR FMC card
      - 1 spare slot is reserved for redundancy/debugging
  - 80 FEC under mass-production
    - 66 for CD, 3 for TVT, 11 for spares (**13.75%**)



Block diagram of clock distribution in uTCA crate

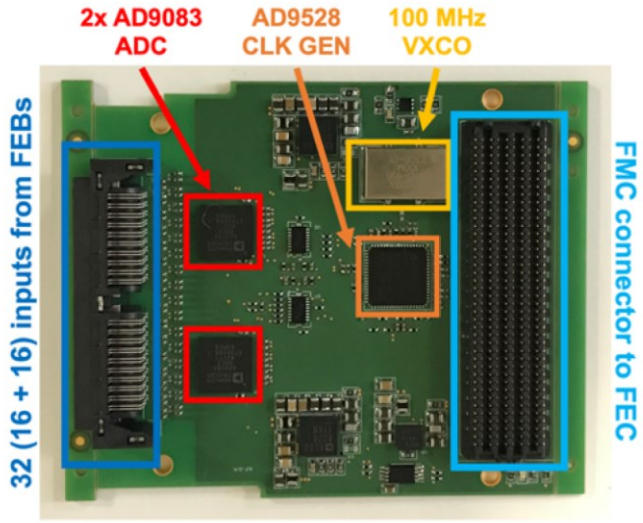
- High reliability consideration in uTCA crate
  - Redundant crate power supplies
  - Redundant WR nodes
- Interface to trigger & DAQ system

Photo of uTCA with FPGA cards

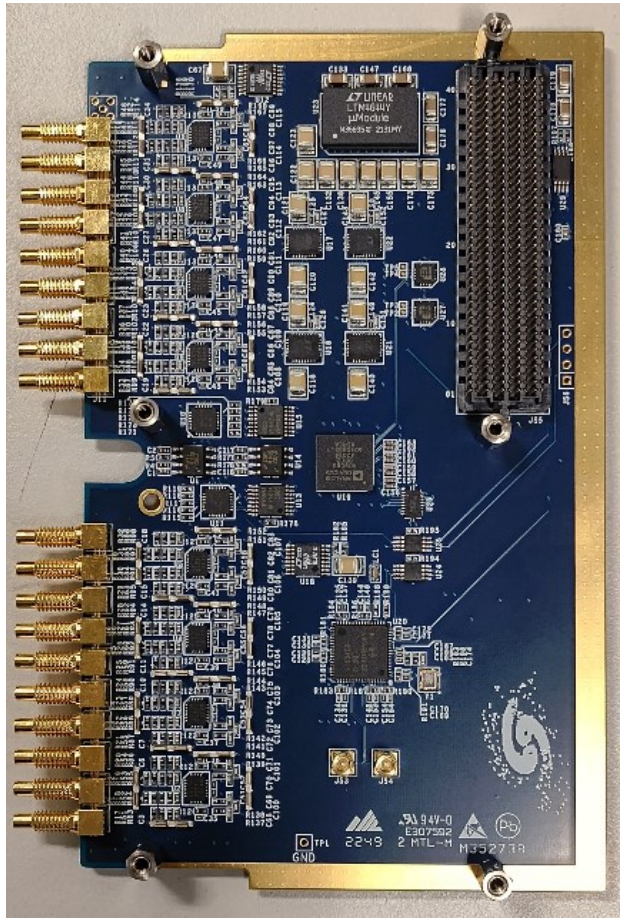
HIGH-DENSITY READOUT

- Samtec high-density connection
  - Up to 128 ch ADC per FPGA board
  - ADC card designed and produced by Roma-Tre
- Status
  - Hardware completed the small system test (60 ch)
    - u4FCP, uRTM, Mini-WR and ADC card
  - Passed PRR, under mass-production
  - Firmware
    - Complete the framework and basic functions, upgrade to 128-channel readout
      - ADC JESD204B interface
      - Q/T calculation
      - Data format
      - Aurora 64b/66b
      - WR timestamp decode
  - Scripts
    - Online configuration through UDP

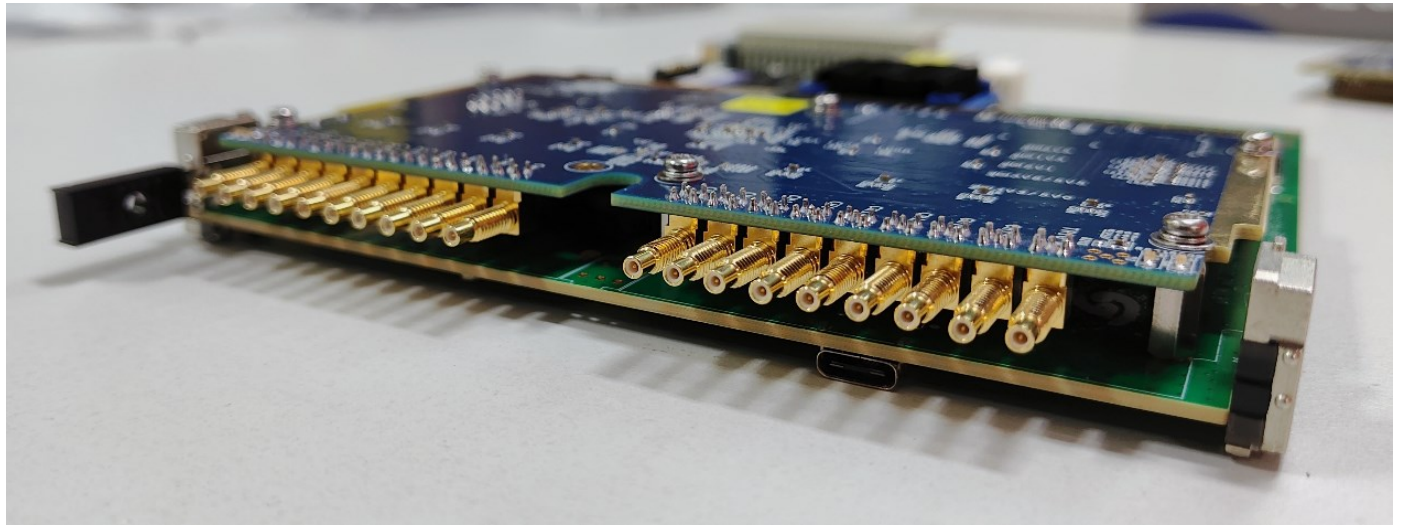
Designed by Roma-Tre



LOW-DENSITY READOUT



- Easy to debug or test
- Coaxial inputs
- 16 ch or 32 ch per FPGA board



ADC FMC board

- 16 single-end channels
- 125 MHz analog bandwidth
- DC coupled analog input
- 12/16-bit Σ-Δ ADC
- Raw sample rate up to 2 GSps

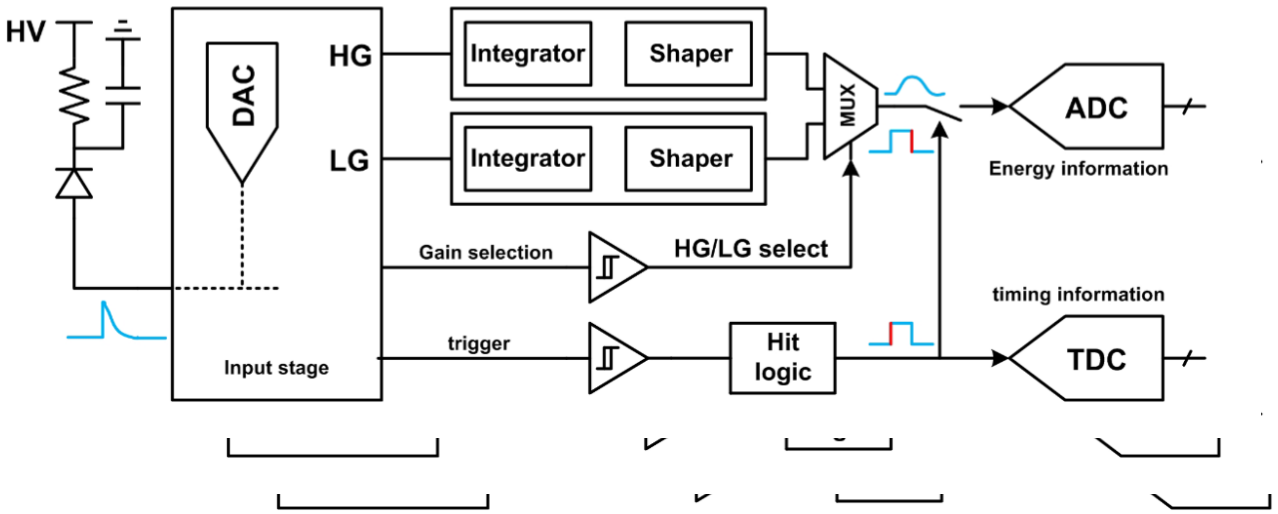
ASIC SCHEME

Put ASIC close to SiPM

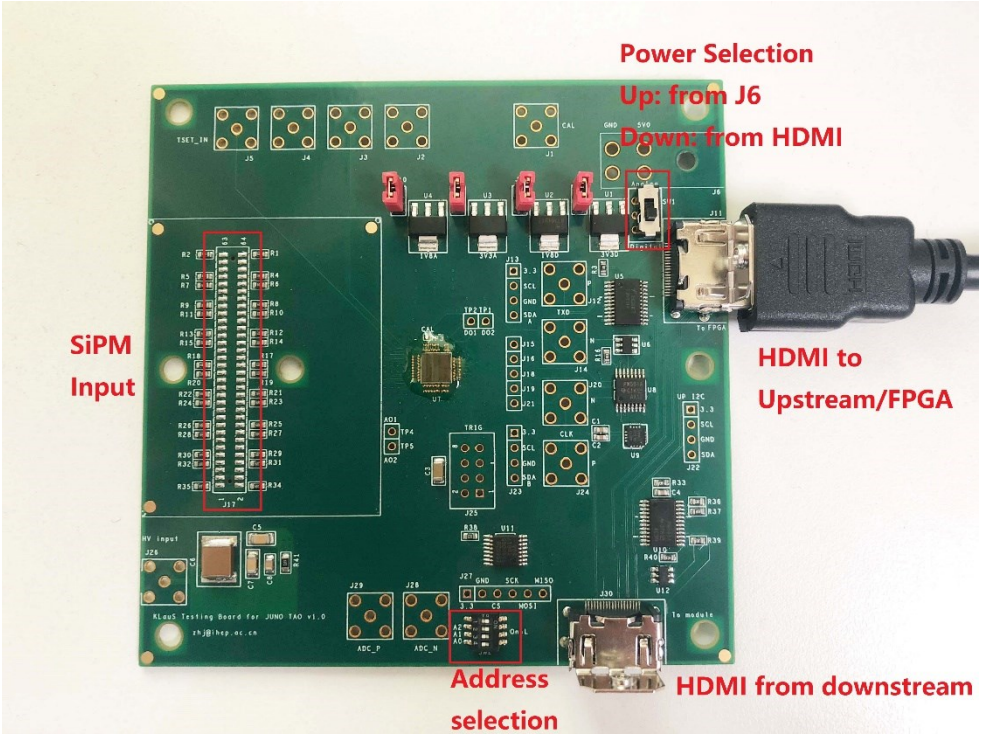
ASIC SCHEME

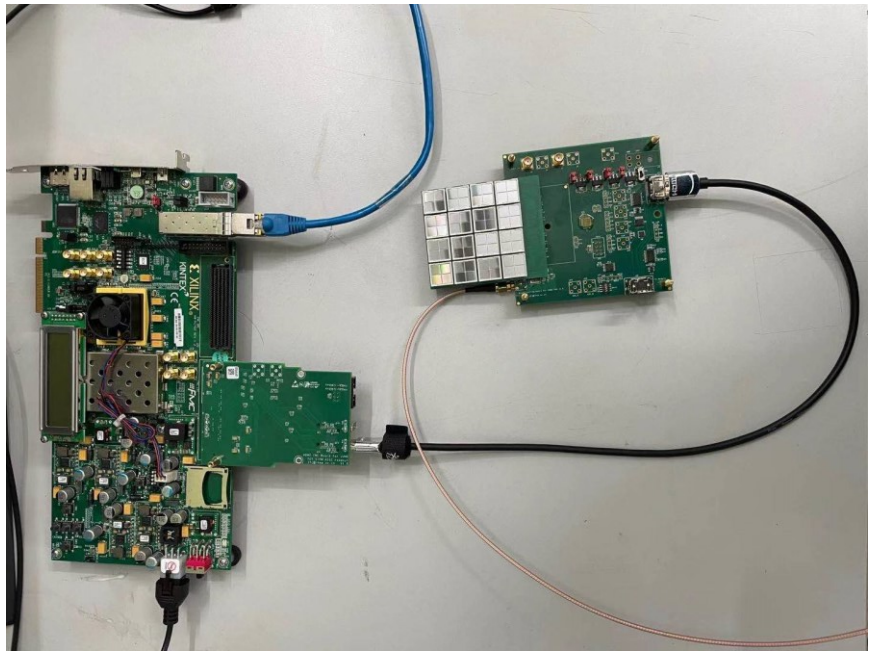
Prototype

- MPT or KLauS
  - Multi-ch inputs
  - ADC+TDC

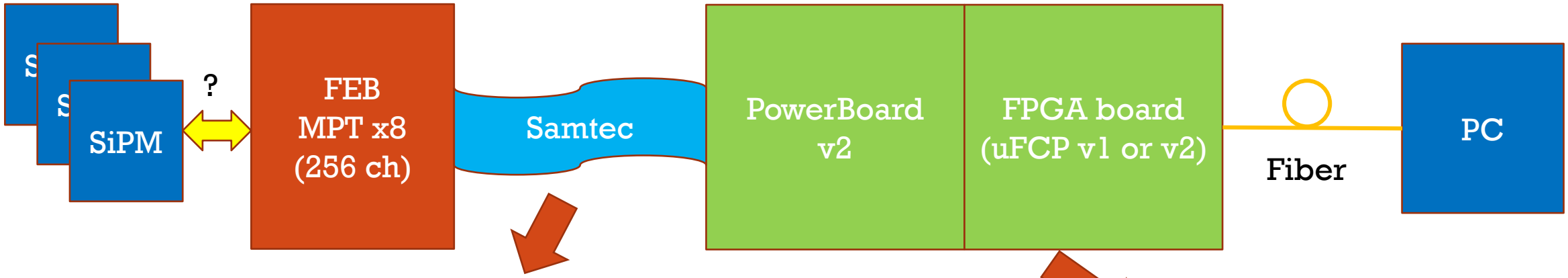


x 36

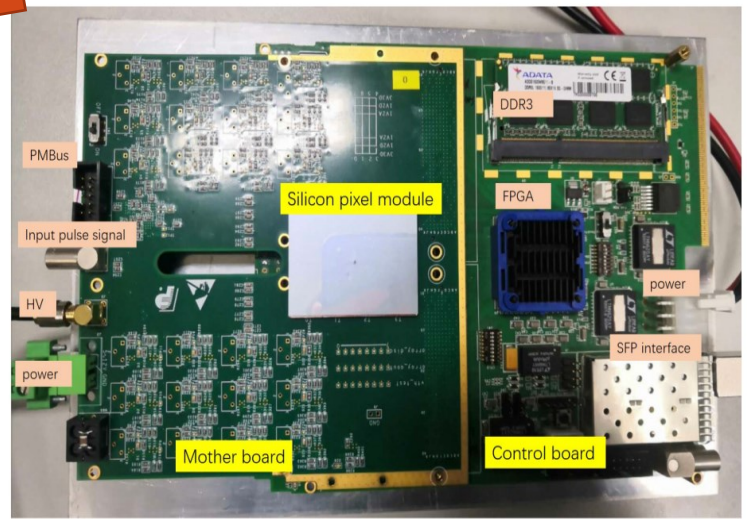




ASIC SCHEME (PLAN)



- Samtec Micro-coaxial cable
  - 32 differential pairs, support up to 32 or 8 MPT ASICs
  - I2C or SPI and GPIO control
  - 16 analog monitor
  - 2 temperature monitors
  - On-line adjustable low-voltage power supply (16 ch)
  - HV line (1 or 2 ch)



BACK-END READOUT SYSTEM

FPGA, MicroTCA, WR, Trigger

Jie Zhang @ IHEP

UNIVERSAL BACK-END FPGA READOUT SYSTEM

- MicroTCA or stand-alone on desktop

Name	Form factor	Controller	Power Supply	JTAG	AMC	RTM
NATIVE-R9	9U, 19”	2 double full-size **NAT-MCH** with 1 **NAT-MCH-RTM**	6 double full-size **NAT-PM**, two of them as Rear Power Module	**NAT-JSM**	12 double mid-size	12 double mid-size
NATIVE-C8	8U, 19”	2 double full-size **NAT-MCH**	3 double full-size **NAT-PM**	1 double compact-size JSM module	10 single mid-size **or** 12 double mid-size	None
NATIVE-R5	5U, 0.5x 19”	1 double full-size **NAT-MCH** with **NAT-MCH-RTM**	1 double full-size **NAT-PM**	None	6 double mid-size + 1 double full-size	6 double mid-size + 1 double full-size
NATIVE-C5	5U, 0.5x 19”	1 double full-size **NAT-MCH**	1 double full-size **NAT-PM**	None	6 double mid-size + 1 double full-size AMCs	None
NATIVE-R2	2U, 19”	1 double full-size **NAT-MCH** with **NAT-MCH-RTM**	1 double full-size **NAT-PM**	1 single mid-size **NAT-JSM**	5 double mid-size + 1 double full-size	5 double mid-size

R2

C8

R9

R5

R5

C5

uFC Series Board

Plan

uFC v2
- Xilinx Kintex-7 28nm 7K325T
  - 0.32 Million System Logic
  - 840 DSP
- PCIe2.0 x4
- 8GB DDR3 800MHz SDRAM ECC
- (8+2)*10G High-Speed Serial Links

u4FCP v1
- Kintex Ultrascale+ 16nm KU11P
  - 0.65 Million System Logic
  - 2928 DSP
- 4*PCIe4.0 x4 + PCIe4.0 x8
- 2*16GB DDR4 1200MHz SDRAM ECC
- 4*40G/100G High-Speed Serial Links

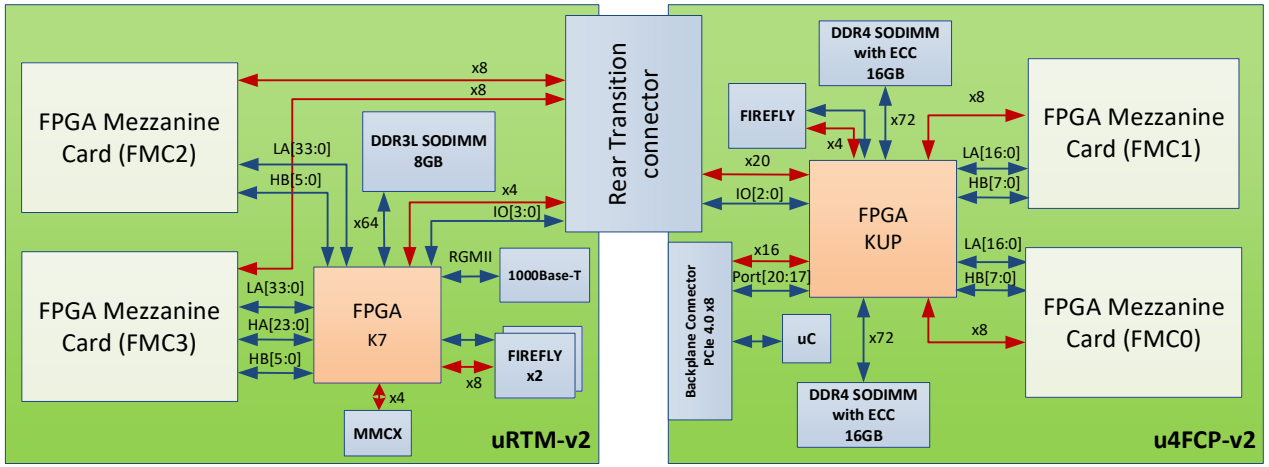
u4FCP v2
- Kintex Ultrascale+ 16nm **KU15P**
  - 1.14 Million System Logic
  - 1968 DSP
- SAMTEC Firefly x3 + PCIe4.0 x8
- 2* 16GB DDR4 1200MHz SDRAM ECC
- 8*40G/100G High-Speed Serial Links

u4FCT
- Virtex Ultrascale+ 14 nm/16 nm **VU13P**
  - 3.78 Million System Logic
  - 12288 DSP
- SAMTEC Firefly x3 + PCIe4.0 x8
- 2* 16GB DDR4 SDRAM ECC
- 12*40G/100G High-Speed Serial Links

Name	Instance Specs						
	Status	FPGA	Memory	FMC	NVMe	PCIe BW	Network
uFC v2	Ready	7K325T	8GB	HPC x2	-	2 GB/s	10GbE
uFCP v1	Ready	KU11P	2*16GB	HPC x4	4*(up to 4TB)	8 GB/s	40/100GbE
uFCP v2	Under Mass-production	KU15P	2*16GB	HPC x4	-	8 GB/s	40/100GbE
uFCT	Plan	VU13P	2*16GB	HPC x2 (FMC+) HPC x2	-	8 GB/s	40/100GbE

Ref1: Zhang, J., et al. (2023). TNS **70(6): 935-940.**
Ref2: Zhang, J., et al. (2019). TNS **66(7): 1169-1173.**

FPGA BOARD (AMC+RTM)



- uRTM-v2
- u4FCP-v1

u4FCP & uRTM:

FPGA-based MicroTCA compatible AMC board

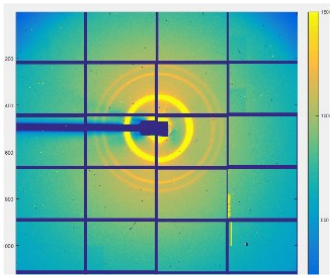
- For generic system control and data acquisition in HEP/HEPS experiments
- Conceived to serve a mid-sized system residing either
  - inside a **MicroTCA** crate or
  - **stand-alone** on desktop with high-speed optical links or Ethernet to PC
- HPC FMC sockets
  - Provide additional clock signals, user-specific I/O and high-speed transceivers that can be used to extend the connectivity as well as the I/O bandwidth
- The red lines are high-speed serial links connected to the gigabyte transceivers (GTY/GTH/GTX) of the FPGA. The blue lines are the general input/ outputs connected to the High Performance (HP), High Range (HR) or High Density (HD) banks of the FPGA.
- More details:
  - https://github.com/palzhj/u4FCPv2

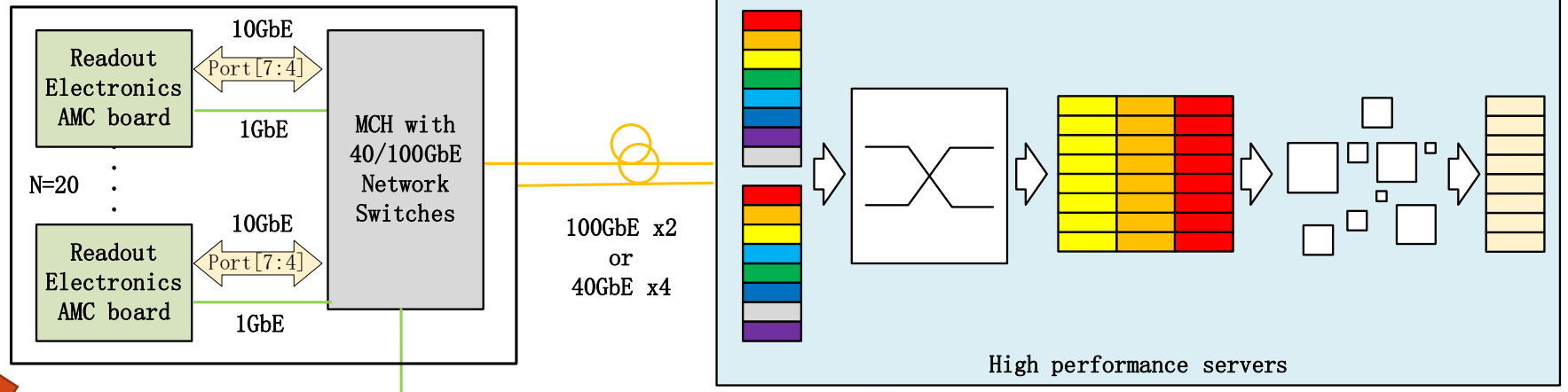
FMC CONNECTION

- Although the FMC standard defines LA, HA, HB and DP differential ports, only parts of them are connected to FPGA due to limited IO resources. The table below summarizes the connections of FMC

FMC	HPC							
	LPC							
	LA[16:0]	LA[33:17]	DP[0]	DP[9:1]	HA[16:0]	HA[23:17]	HB[16:0]	HB[21:17]
FMC0	HP bank (1.0V~1.8V)	-	1 GTY	7 GTY	-	-	HD bank (3.3V), 8 ADC Channels	-
FMC1	HP bank (1.0V~1.8V)	-	1 GTY	7 GTY	-	-	HD bank (3.3V), 8 ADC Channels	-
FMC2	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	1 GTH	7 GTH	-	-	HR bank (2.5V), 5 ADC Channels	-
FMC3	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	1 GTH	7 GTH	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	HR bank (2.5V), 5 ADC Channels	-

ELECTRONICS SYSTEM ARCHITECTURE





To be upgrade with internal switch

On-detector

FPGA AMC board

- Front-end Electronics Control
- Clock Synchronization
- Monitoring
- Data Acquisition

FPGA accelerator cards x2

Off-detector

- High-speed network
- High-speed storage
- High-performance computing
- FPGA
  - Data aggregation
  - Data sorting
  - Data compression
  - Real-time algorithm

Use the MCH with 40/100GbE switch to replace the commercial network switch

- More compact

Options:

- NAT, NAT-HUB-E (wait to deliver)
- Vadatech, UTC056-500-212-110 (under test)

CLOCK SYNCHRONIZATION AND TIMING

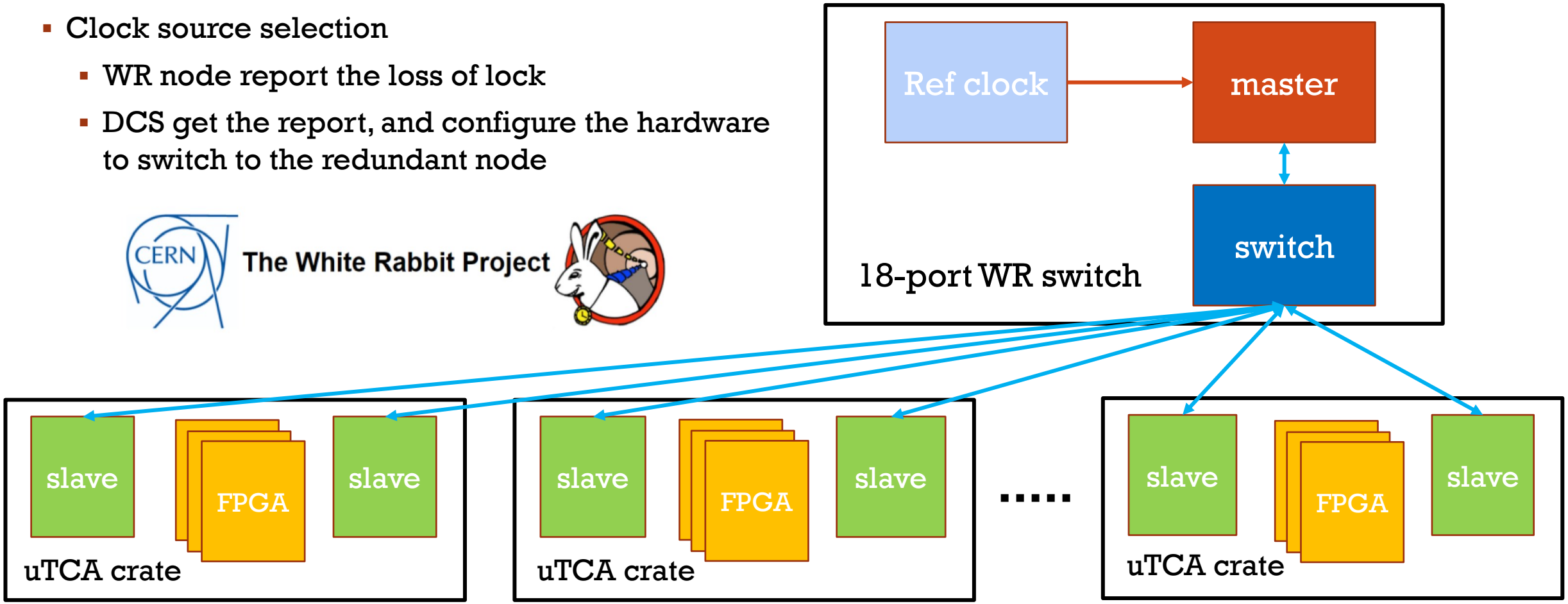
WR(White Rabbit)

Jie Zhang @ IHEP

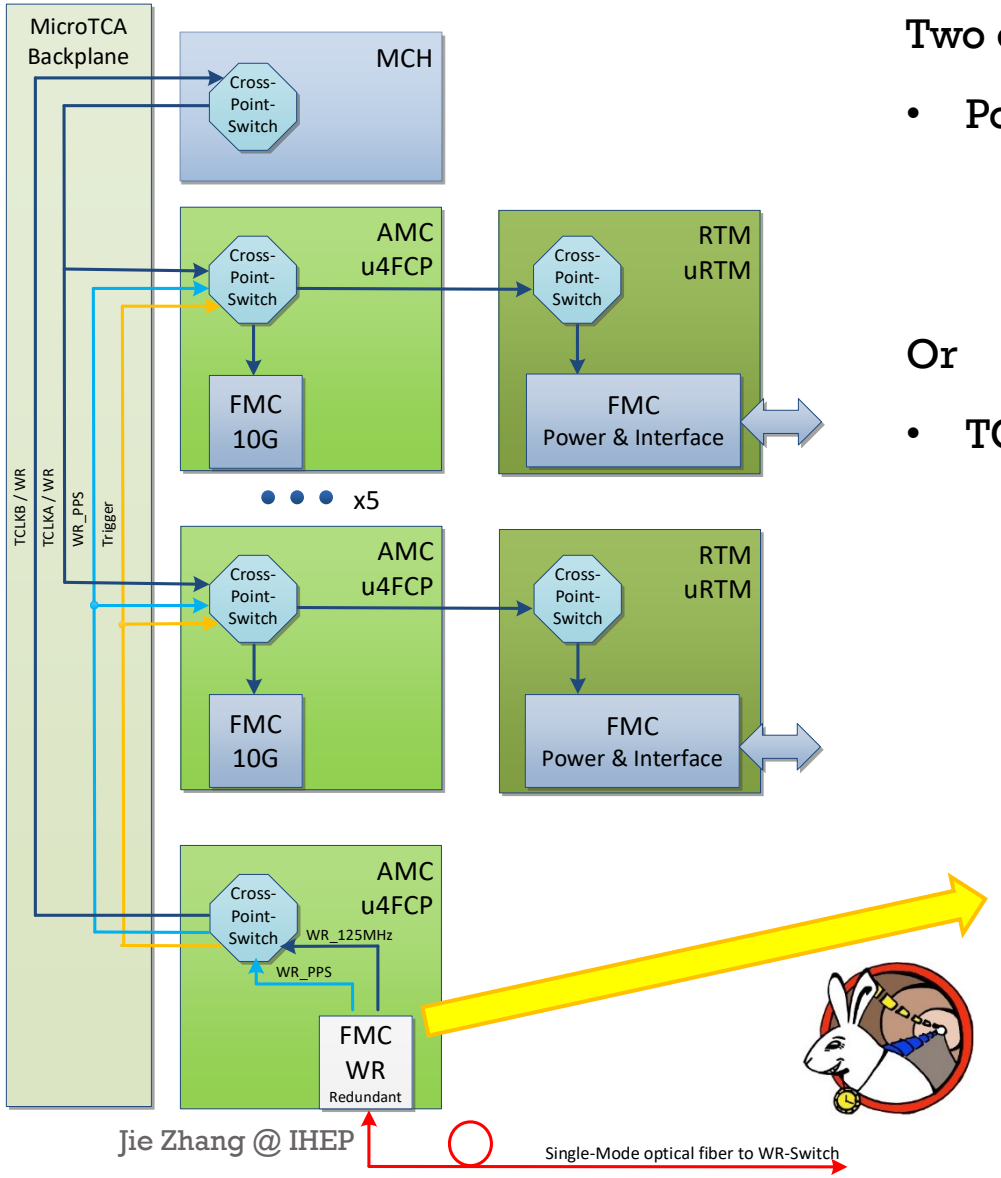
CLOCK REDUNDANCY CONSIDERATION

- Due to the life limit of fiber optic transceivers, we plan to use a redundant WR clock
- Each uTCA crate has two WR slave nodes
- Clock source selection
  - WR node report the loss of lock
  - DCS get the report, and configure the hardware to switch to the redundant node

CERN The White Rabbit Project

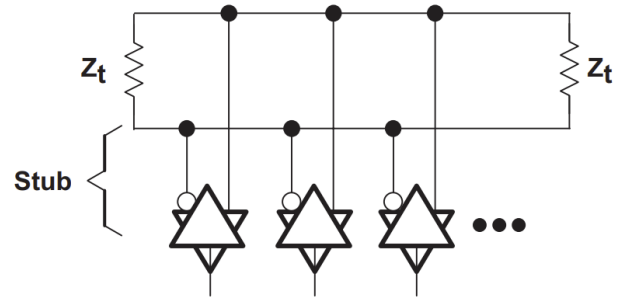


CLOCK DISTRIBUTION IN MICROTCA



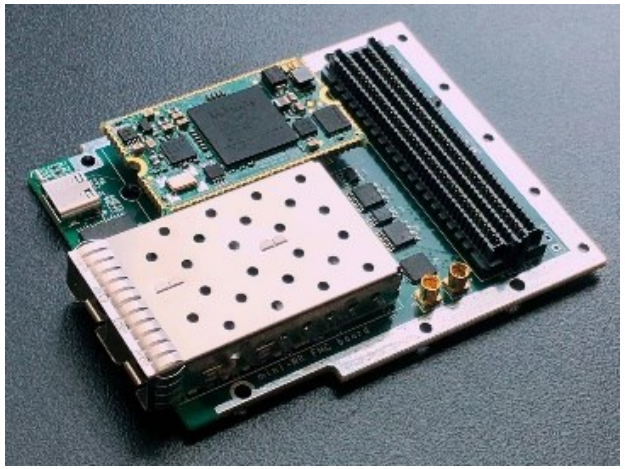
Two clock allocation schemes inside the crate

- Port 17 ?
  - Native R9 crate with WR Support
  - MLVDS multi-drop connection



Or

- TCLK ?
  - TCLKB (slot12)-> MCH (NAT-MCH-PHYS80) -> TCLKA (slot1-11)



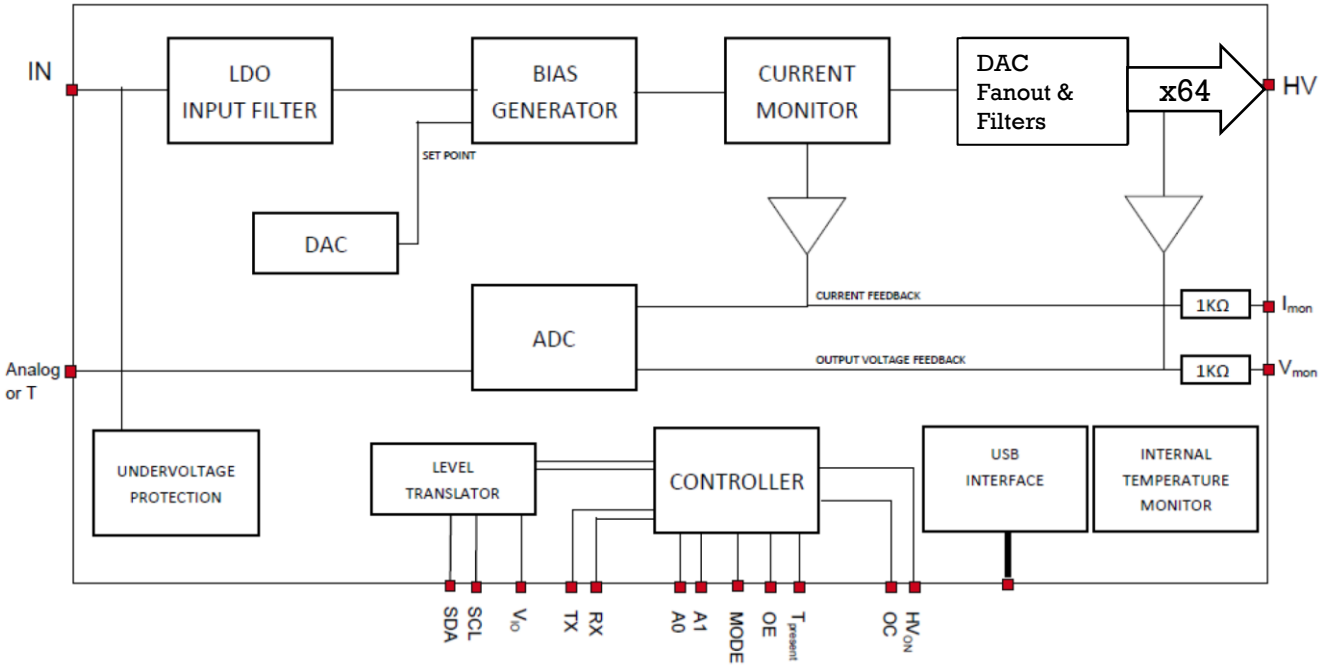
Mini-WR FMC for System-level clock synchronization

BIAS VOLTAGE

Multi-channel, each channel independent adjustable

ADJUSTABLE MULTI-CHANNEL BIAS VOLTAGE (PLAN)

- MicroTCA card mechanics
  - 64 ch outs
    - 2 x 64 pin IDC connectors
  - up to 200V/ch
  - up to 550uA/ch
  - 2 x 14bit DAC chips
  - Output voltage monitor (24bit ADC)



HARDWARE STATUS

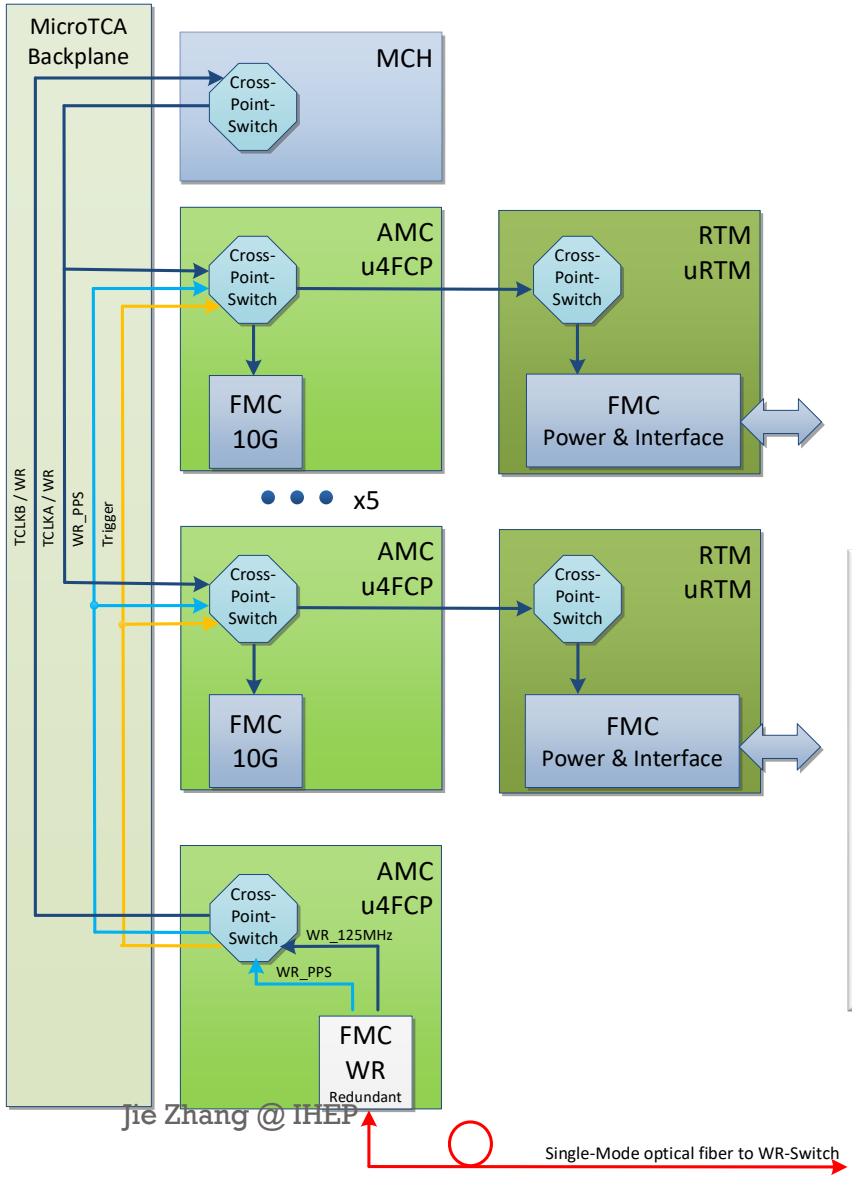
	Name	Status
ASIC scheme	FEB (Front-end board) with 8 MPT ASIC (256 ch)	Not started
	Powerboard v2	Ready
Discrete device scheme	FEB with pre-amplifier	Prototype
	ADC card low-density (16 or 32 ch)	Ready
	ADC card high-density (128 ch)	Under mass-production by Roma-Tre
Back-end	FPGA board (uFCP v1 and uRTM v2)	Ready
	FPGA board (uFCP v2 and uRTM v2.2)	Under mass-production
	FPGA board (uFCT and uRTM v2.2)	Not started
	WR node	Ready or on-shelf product
	External trigger node	Ready
Bias voltage	64 ch bias voltage(<200V)	Not started

SUMMARY

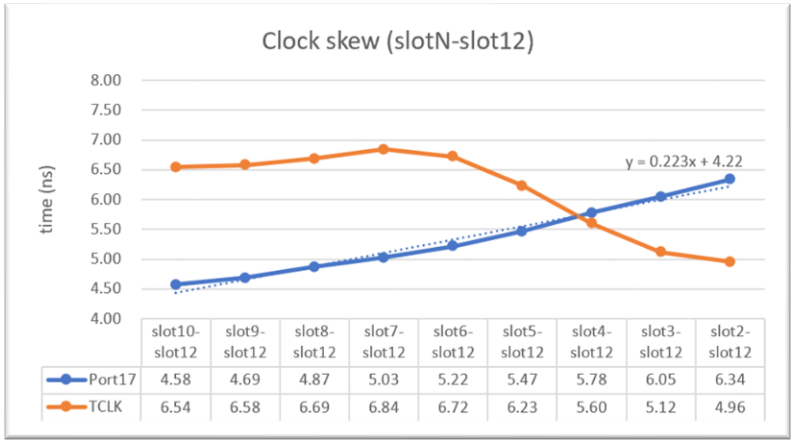
- MicroTCA architecture
  - Suitable for small and medium-sized experiments
- uFC series boards
  - FPGA-based MicroTCA compatible AMC board for generic system control and data acquisition in physics experiments
  - HPC FMC sockets
    - Provide additional clock signals, user-specific I/O and high-speed transceivers that can be used to extend the connectivity as well as the I/O bandwidth
- Support discrete device scheme and ASIC scheme for SiPM readout in one system

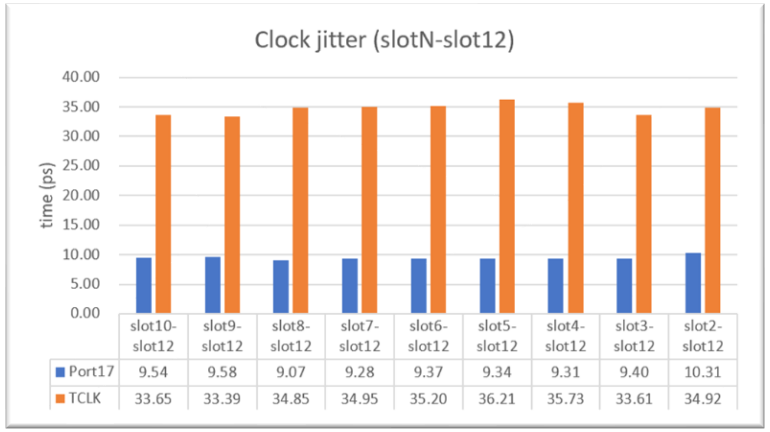
THANKS TO YOUR ATTENTION

CLOCK DISTRIBUTION IN MICROTCA

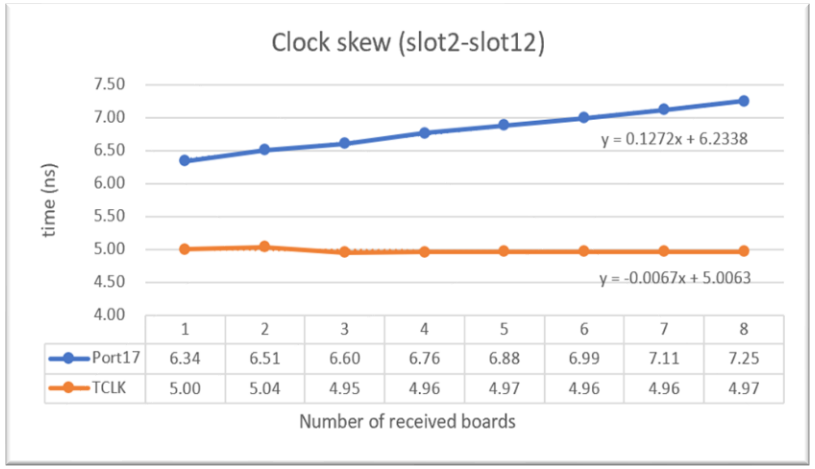


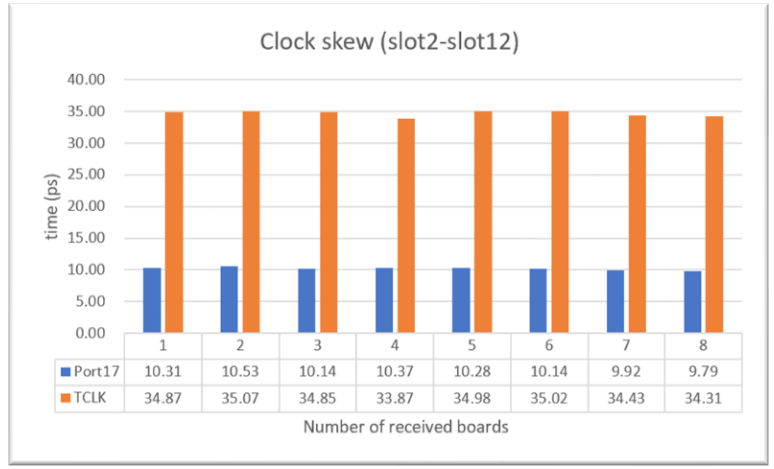
AMC with mini-WR fixed in slot 12, move AMC receiver





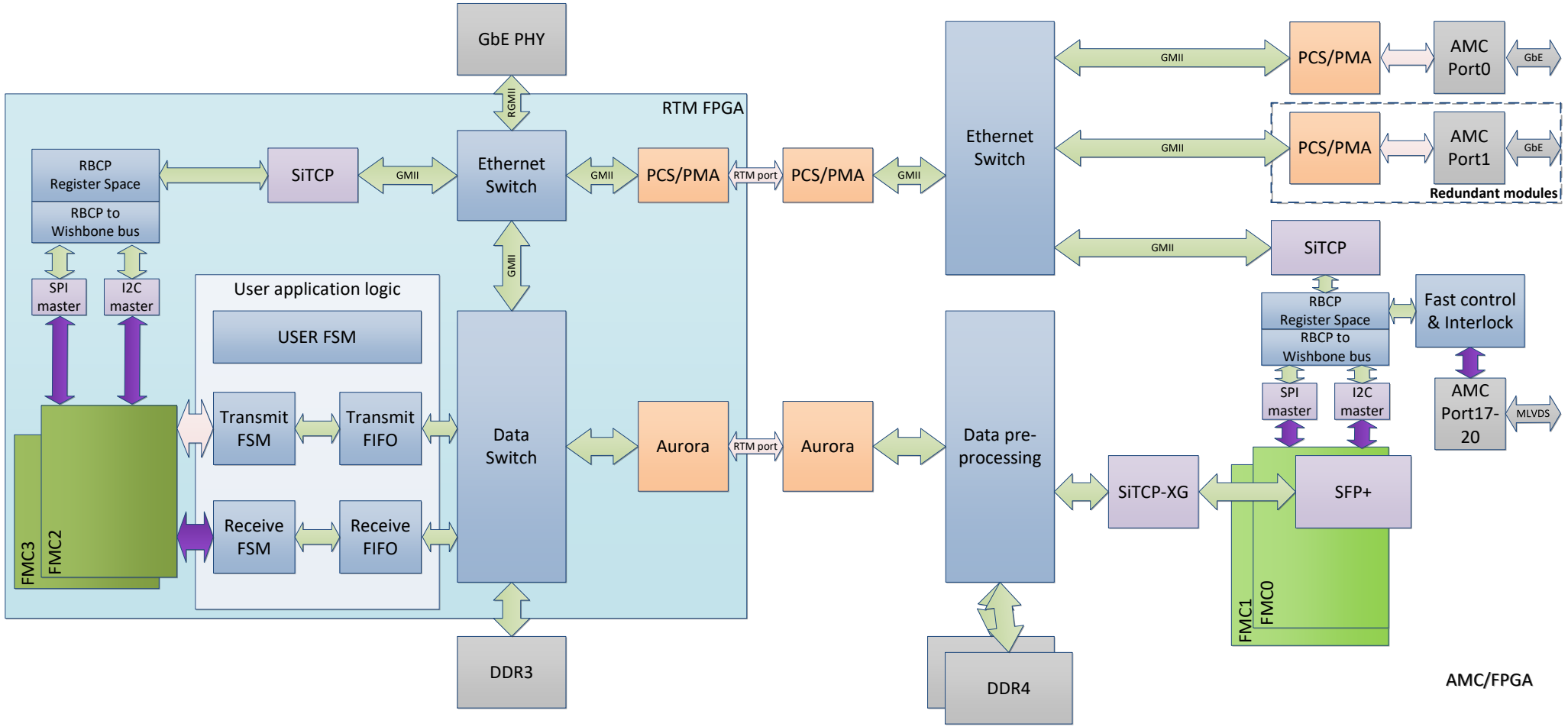
Receiver is fixed at slot 2, add more adjacent AMC boards





- TCLK scheme has deterministic skew, but more jitter
- Port17 scheme has smaller jitter, but the skew is related to the location and receiver quantity

FPGA Firmware



- **Config & monitor via UDP/IP**
- **Readout via TCP/IP**

FEASIBILITY

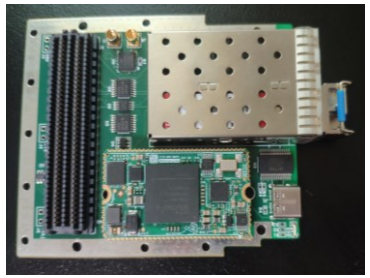
- AMC+RTM boards
  - With various FMC cards

FPGA node

FPGA node

FPGA node

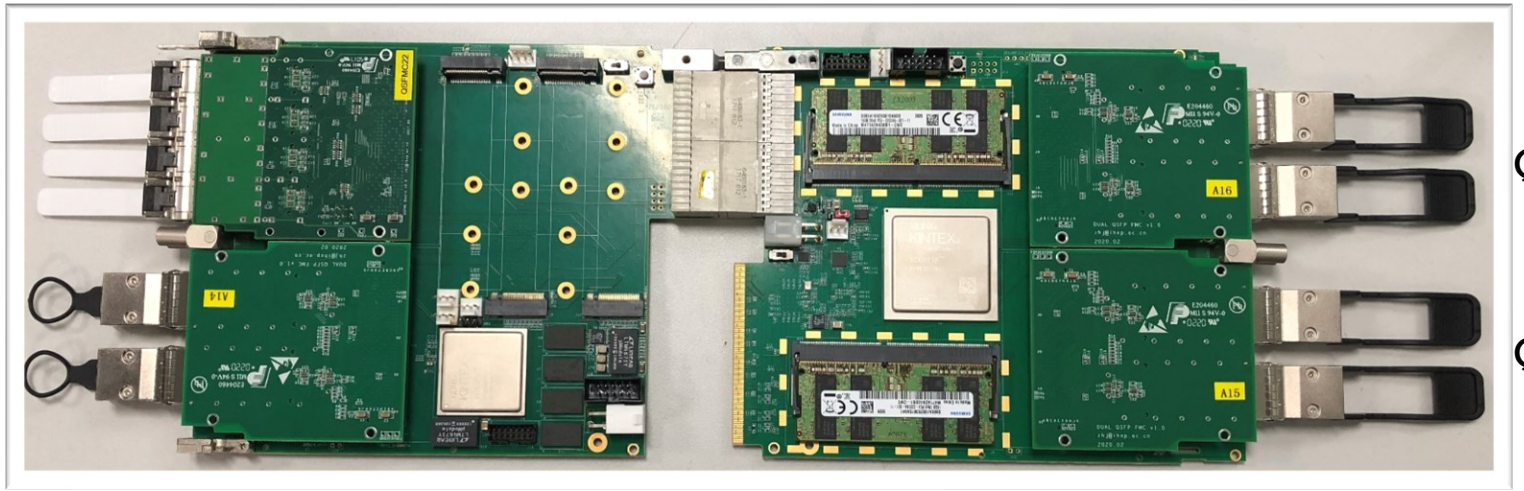
FPGA node



Mini-WR FMC

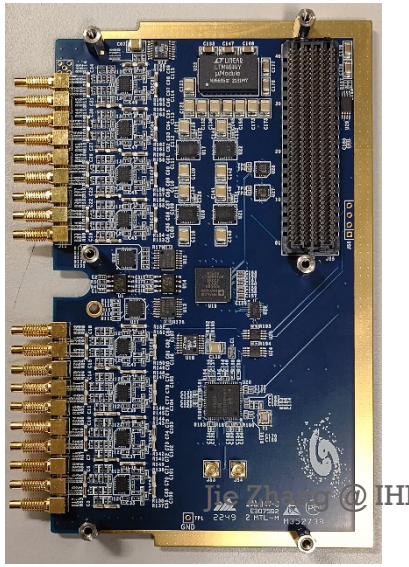
SFP+ x4

QSFP28 x2



QSFP28 x2

QSFP28 x2



ADC FMC board

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- DC coupled analog input
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- Raw sample rate up to 2 GSps