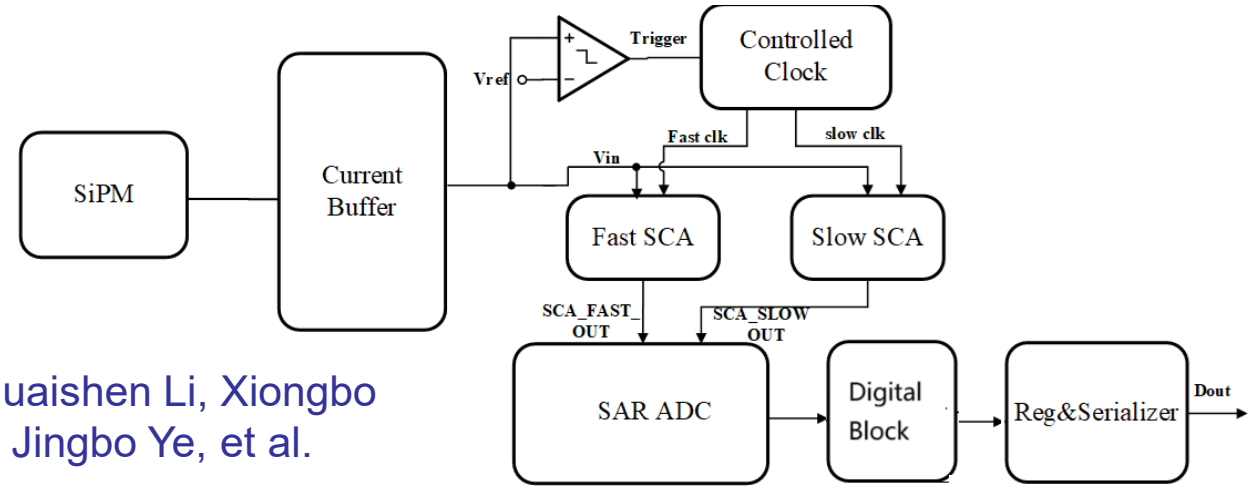
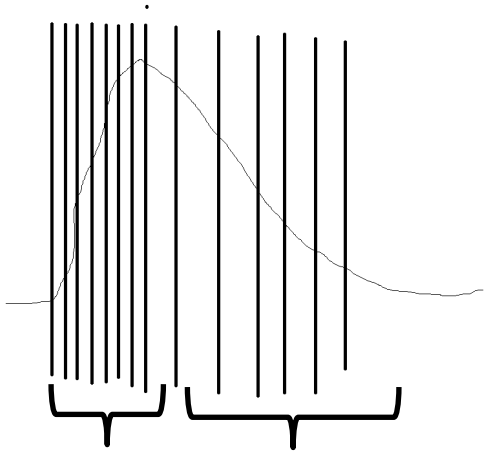
Discussion on possible solution for High-Z ECAL FEE



by Huaishen Li, Xiongbo Yan, Jingbo Ye, et al.

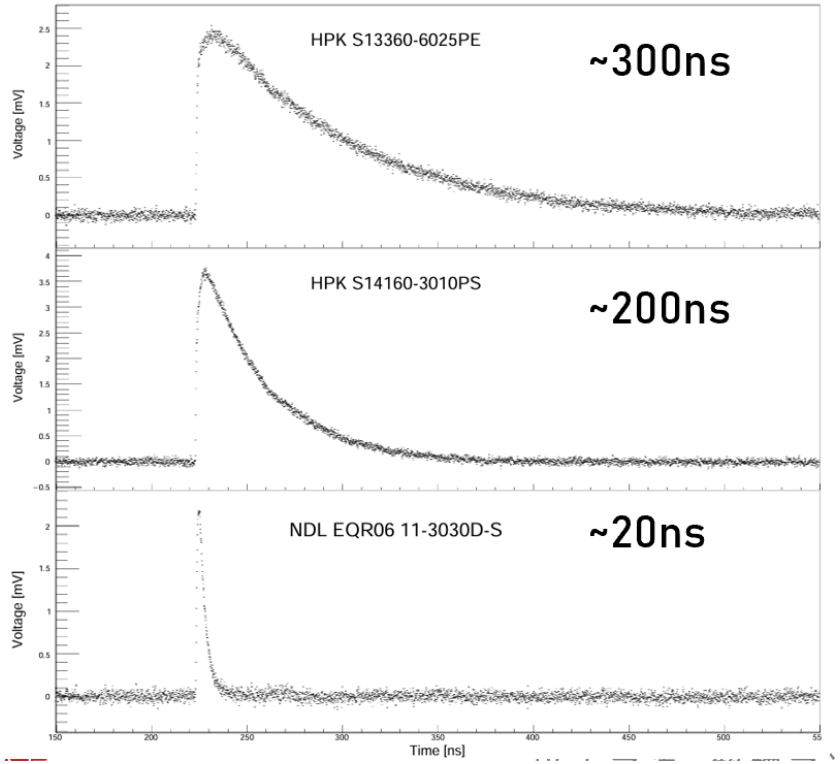


Fast sampling for timing, slow sampling for energy and low power

- **Possible solutions exist by using short length waveform samping + SARADC + digital processing**
  - **Combined with fast sampling for rising edge & slow sampling for falling edge, compromise with sampling depth & power**
- **Power consumption to be estimated, however, will be a significant rise than higgs mode**
- **Data rate also needs to be calculated, however, 2 fiber channels has already been used for a background rate of 100kHz avg.**
  - **If the bkgrd rate goes to 1MHz avg., even 4 fiber challenges (MTX) can not stand**
  - **More advanced algorithm for data compression must be used (potential issue for bugs & more iterations)**
- **Estimated power:25~30mW/chn (vs 15mW/chn for Low LumiZ)**
  - **15mW analog frontend + 10mW ADC + 5mW digital & periphery & driver**

More information needed for the detail scheme

- **Characteristics of the NDL SiPM, especially the waveform width & speed**
- **Corresponding PEs from the measurement waveform by laser**
- **Test setup of the NDL SiPM, component used related to the output waveform**

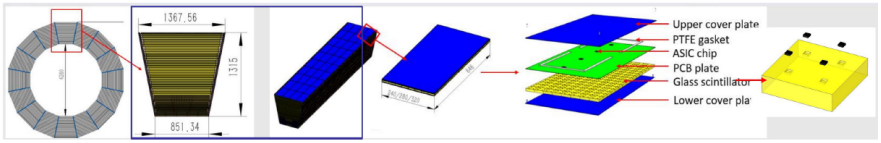


SiPM	Amplitude	Rise time	Decay time	
HPK S13360-6025PE	52mV	8.3ns	123.4ns	Laser enhance
	620mV	7.8ns	126.8ns	
	3100mV	5.7ns	126.2ns	
	4150mV	2.1ns	128.7ns	
HPK S14160-3010PS	47mV	1.8ns	55.4ns	Laser enhance
	900mV	1.9ns	55.2ns	
	3640mV	1.4ns	58.8ns	
	3830mV	1.5ns	58.9ns	
NDL EQR06 11-3030D-S	200mV	1ns	7.4ns	Laser enhance
	600mV	1ns	8ns	
	2300mV	1ns	11.1ns	
	3730mV	1ns	28.9ns	
	3090mV	1ns	47.5ns	
	2200mV	0.9ns	71.5ns	

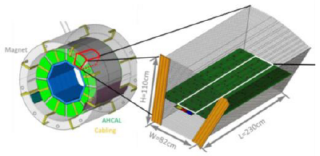
? pe

Discussion on HCAL electronics assembly

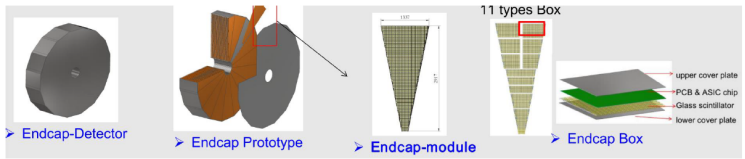
HCAL桶部电缆数量



- 探测器桶部内部电缆数量
  - 1/16分区每层电缆数量：5*3或者5*4（单向）
  - 1/16 分区电缆数量：19*3*5+29*4*5=865（单向）
  - 桶部内部总电缆数量：865*16=13840 （单向）
- 探测器桶部引出电缆
  - 1/16 分区引出电缆数量：19*3+29*4=173
  - 总电缆数量：一端173*16=2768，总5536



HCAL端盖电缆估算

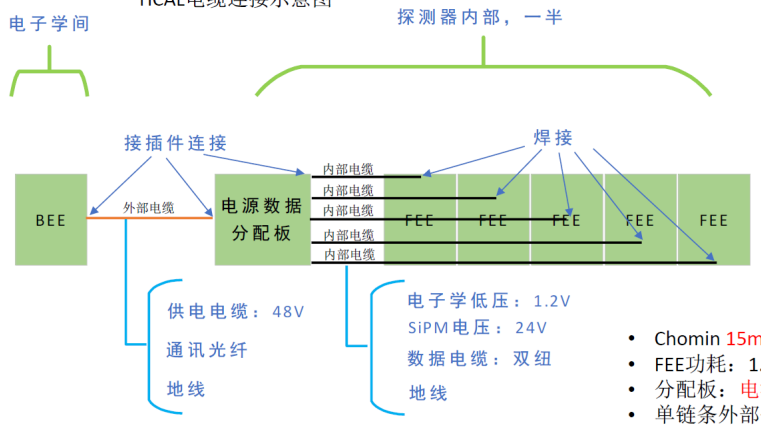


- HCAL端盖部排布
  - 总通道数：单端112万，总共224万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 端盖引出电缆数量
  - 电缆类型：供电，光纤
  - 每区每层功耗：1459*15mW=22W，
  - 每区每层汇总板功耗：(11+1)*1.18=14.2W （每层2块汇总板）
  - 1/16 分区电缆数量：48*2=96
  - 总电缆数量：一端48*2*16=1536，总3072
  - AWG12（线径2.05mm，电流：13.1A/14.9A）

- **Electronics related issue for HCAL assembly achieved an agreement during the electronics regular meeting first**
- **Joint discussion on HCAL module assembly scheme with detector, mechanical colleagues**

Discussion on HCAL&ECAL power dissipation on cable

HCAL电缆连接示意图

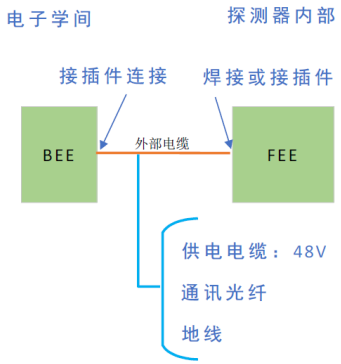


- Chomin 15mW/Ch, Chitu 0.75W, Kinwu 0.25W
- FEE功耗：1.92W （ 1.2V*1.6A）
- 分配板：电源效率85%，光纤模块功耗1W
- 单链条外部供电总功率：12.5W （48V*0.26A）

- 内部供电电缆最长3m，线损0.16W，占比1.3%（AWG18）
- 外部供电电缆按照100m计算
  - 线损0.145W，占比1% （AWG18）
  - 线损0.022W，占比0.18% （AWG12）

- AWG18（线径1.02mm，电流：3.2A/3.7A，铜芯电阻值21.4Ohm/km）
- AWG12（线径2.05mm，电流：13.1A/14.9A，铜芯电阻值3.3Ohm/km ）

ECAL电缆连接示意图



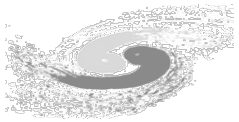
- Chomin 15mW/Ch, Chitu 0.75W, Kinwu 0.25W,
- 电源效率85%
- 单模块外部供电总功率：36.6W （48V*0.76A）

- 外部供电电缆按照100m计算
  - 线损1.24W，占比3.4% （AWG18）
  - 线损0.191W，占比0.5% （AWG12）

- AWG18（线径1.02mm，电流：3.2A/3.7A，铜芯电阻值21.4Ohm/km）
- AWG12（线径2.05mm，电流：13.1A/14.9A，铜芯电阻值3.3Ohm/km ）

- **HCAL**
  - **External cable to End-Board on the end of barrel for each layer**
  - **Inner cable with limited length max 3m**
    - ➢ **Thin cable (AWG18) can achieve a power dissipation ~1.3%**
- **ECAL**
  - **External cable to Back-Board on each module**
- **For external cable to elec-room (~100m for estimation)**
  - **Power supply@48V, current on cable can be small (less dissipation)**
  - **HCAL:AWG18 (thin) < 1% vs AWG12(thick) < 0.18%**
  - **ECAL:AWG18 (thin) < 3.4% vs AWG12(thick) < 0.5%**
  - **Power cost vs cable cost**

Discussion on electronics sockets



- For the possible maintainable scheme for sub-detectors, discussion on possible and the location for the sockets of electronics
- All electrical connection & fiber connection can find re-pluggable sockets, but sockets has big impact on system reliability, a compromise
- Issues mainly on barrel detectors, endcap tends to be reachable by default
  - To find the connection location between external cables (~100m) and inner cables
- Detectors with barrel-end structures, naturally reachable and be the location for the external cable
  - Muon, HCAL, ~~TPC~~, VTX
- ECAL:
  - To avoid 100m external cable all the way to the Back Board on module, propose to has a socket structure right at the end of the barrel (rather than the edge ring of all the cables)

Discussion on electronics sockets

- **OTK with TPC**
  - **If the TPC can be fully drawn out, then the full OTK can be reached**
  - **End connections for each layer & each ladder seem necessary**
- **ITK**
  - **Even fully drawn out, the inner 2 layers can not be reached**
  - **End connections for each layer & each ladder seem necessary**

Summary table for electronics room @Higgs

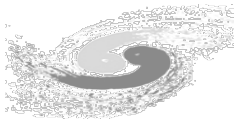
Detector	Max data rate per fiber (Gbps)	Fibers per module	Fiber sum	BEE sum	Data crate sum	Module Max Power (W)	Total Power (kW)	Power channels	Power crate sum	HV requirements	HV channels sum	HV crates sum	Comment
VTX	8	1~2	88	6	1	25	0.45	66	2	~-10V	66	1	
TPC	0.1	1	496	32	4	42	20	496	6	SHV	496	4	
ITK-Barrel	0.96	1	2204	139	14	11.2	31.59	2204	29	50~200V	2204	10	
ITK-EndCap	2.2	1	1696	106	12	7.4	11.1	192	2	50~200V	1696	8	
OTK-Barrel	1.4	1	540	34	4	56.3	251.1	3780	79	150~200V	3780	17	Det needs opt
OTK-EndCap	0.7	1	720	45	6	58.9	35.6	720	16	150~200V	720	4	Det needs opt
ECAL-Barrel	4.8	2	960	60	6	31	17.5	480	5	40~60V	480	2	
ECAL-EndCap	4.8	2	520	34	4	31	9.5	260	4	40~60V	260	2	
HCAL-Barrel	0.14	1	5536	346	36	9	66.1	5536	58	40~60V	5536	26	
HCAL-EndCap	1.75	1	3072	192	20	11	41.3	3072	32	40~60V	3072	14	
Muon-Barrel	0.004	1	288	18	2	2.6	0.76	288	3	40~60V	288	2	
Muon-EndCap	0.01	1	96	6	1	4.7	0.45	96	1	40~60V	96	1	
Sum			16216	1018	110		485.45	17190	237		18694	91	

Electronics room

- **Minimum crates from current MDI**
  - **110 data crates, 237 power crates, 91 Det-HV crates, 20 Trigger crates**
- **Minimum racks from current MDI**
  - **37 data racks, 24 power racks, 23 Det-HV racks, 10 trigger racks (94 in total)**
  - **More 2 racks for AC-DC power for all the above racks**
  - **96 racks in total**
- **Racks Size: 0.5m × 0.5m**
- **Side clearance 1.5m for heat, face clearance 2m for cabling & heat**

- **Total room: 500m^2×2floor = 25m × 20m × 2floor**
  - **10 × 10 × 2=200 racks capacity**
  - **Necessary redundancy for future upgrade**

Summary table for data



	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128			8~16 @common SiPM ASIC		
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID			TOT + TOA/ ADC + TDC		
Data Width /hit	32bit	42bit	32bit	40~48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg：2.9Mbps/chip Max：3.85Mbps/chip	Avg：38.8Mbps/chip Max：452.7Mbps/chip	~70Mbps/module Inmost	Avg. 0.96Gbps/module Max:9.6Gbps/module		Max. 144Mbps/module-layer	Max. 350Mbps/module-layer	Max： 10 Mbps/board
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)		< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	<=24:1 @ O (400 Mbps)
Detector Channel/module	1882 chips @Stch &Ladder 2204 modules	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.52M chn ~32500 chips 260 modules	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43.2k ch 72 Aggregation board
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	460Gbps	250Gbps	811.2Gbps	537.6Gbps	~ 2.07 Gbps

Progress on Ref-TDR

- **Approaching to the final draft0 (90%@71 pages), within one week**
- **Progress for each main chapter of electronics system**
  - **Introduction ……..100% (Wei Wei)**
  - **General architecture and Strategy ……100% (Wei Wei)**
  - **Sub-detector ASIC**
    - **OTK ASIC ……90% (Xiongbo Yan)**
    - **SiPM ASIC……TBU with new MDI bkgrd (Huaishen Li)**
  - **Data Link ……...100% (Di Guo, Xiaoting Li, Jingbo Ye)**
  - **Power System ……70% (Jun Hu, Jia Wang)**
  - **Wireless communication ……..100% (Jun Hu)**
  - **Clocking ……70% (Jun Hu)**
  - **Backend Electronics ……100% (Jun Hu)**
  - **Cabling, Crates & Elec Room ……100% (Wei Wei)**
  - **Previous R&D on electronics system ……..100% (Wei Wei)**