Discussion on ECAL FEE strategy

- **The SiPM ASIC – ChoMin is scheduled to tapeout in April**
  - **Aiming at the 3-year milestone for the platform, very tight schedule for a new chip**
  - **Otherwise will be too late due to the long iteration of ASIC**
- **To make it meaningful, the critical characteristics of SiPM+BGO is urgently to provide, otherwise the chip can not match with the real device**
  - **Proposed in the last Tuesday meeting**
    - **Characteristics of the NDL SiPM+BGO, especially the waveform width & leading edge**
    - **Corresponding PEs from the measurement waveform by laser**
    - **Test setup of the NDL SiPM, component used related to the output waveform**
- **Proposal: a specification of the ChoMin ASIC will be announced, then the scheme & functionality will be defined, then hard to change afterwards**
  - **Best case: real waveform can be understood, and main target can be defined**
  - **Worse case: short of time to get test results, then we should conclude for a spec list by detector & electronics**
  - **Worst case: electronics has to proposed a most possible target, and detector has to compromise afterwards if needed**

Discussion on ECAL FEE strategy

- **For the ECAL related electronics in Ref-TDR, concerning the High LumiZ**
- **Due to the time limit, seems hard to get a clear strategy on High LumiZ in 1~2 weeks**
  - **Only the previous scheme for Higgs & Low LumiZ was put into the document**
    - **Based on traditional Q&T measurement, 15mW/chn**
  - **Can be replaced with the new proposal on High Z anytime**
    - **Fast+slow short length waveform sampling based, 25~30mW/chn, scheme is ready**

计划及分工2024.11.27

- 11.20~12.01 确定前放及整体方案
- 11.20~12.08 各部分详细指标
- 12.09~1.25（7weeks） schematic完成
- 2.01~3.09 （5weeks） layout完成

- 3.10~3.31 （3weeks）IO、Post-sim
- 分工:
  - 前放、T-branch、Q-branch、外围电路

Discussion on Data Link tapeout schedule

- **Data Link also scheduled to tape out in April, 5 chips with a heavy task**
- **Main target: a "full" functional ChiTu chip, with all major blocks**
- **Secondary targets:**
  - **TaoTie chip: function relatively simple**
  - **KinWoo LDD/TIA: relatively mature before**
  - **PAM4 driver: future upgrade**
- **Aiming to have a system test by the end of this year**
- **Block functionality defined with detailed discussion**
- **Design task allocated to the charge person for each block**

2025年4月流片内容	说明	主要人员
TaoTie芯片	简化版本（不编码、不压缩），由肖乐负责。保障交付前提下，实现完整功能，保证芯片可与ChiTu芯片构成完整demo系统。	肖乐
ChiTu芯片	重点包含数字功能模块（魏老师）、时钟模块（筱婷）、Data Phase Control（DPC）、Clock Phase Control（CPC）、优化后的Serdes、I2C配置	郭迪、李筱婷、魏晓敏、王进红、柳琦
KinWooLDD芯片	完整四通道激光器驱动芯片 I2C配置、带缺省值、适配光模块组装 在原有基础上优化、改进	郭迪、赵子文
KinWooTIA芯片	完整四通道TIA跨阻放大芯片 带RSSI输出、适配光模块组装要求 有一定基础，待完全重新设计。	郭迪、代薇
PAM4激光器驱动芯片	2通道 10Gbps输入 输出1通道 10 GBaud （20 Gbps）PAM4信号驱动激光器	张黎、郭迪、王容格

- 4月8号流片
- 项目计划表格
  - 相应人员完成项目计划表格填写。
    - 肖乐： TaoTie芯片
    - 李筱婷：ChiTu芯片（时钟部分）
    - 魏晓敏：ChiTu芯片（数字部分）
    - 郭迪： ChiTu芯片（Serdes部分）
    - 张黎、王容格： PAM4激光器驱动芯片
    - 赵子文： KinWooLDD芯片
    - 代薇： KinWooTIA芯片
  - 根据时间节点，保障交付前提下，**认真评估工作量，确定工作内容**。
- 重要时间节点：
  - 3月15号 TaoTie芯片所有功能模块整体交付（肖乐），只剩PAD等顶层集成。
  - 3月15号 ChiTu芯片时钟部分交付（李筱婷）、数字部分交付（魏晓敏）、Serdes部分交付（郭迪），进入顶层集成。
  - 3月22号 KinWooLDD、KinWooTIA芯片完成，可递交GDS状态。

Progress on Ref-TDR

- **Approaching to the final draft0 (95%@81 pages), within one week**
- **Progress for each main chapter of electronics system**
  - **Introduction ……..100% (Wei Wei)**
  - **General architecture and Strategy ……100% (Wei Wei)**
  - **Sub-detector ASIC**
    - **OTK ASIC ……100% (Xiongbo Yan)**
    - **SiPM ASIC……80% (Huaishen Li)**
  - **Data Link ……...100% (Di Guo, Xiaoting Li, Jingbo Ye)**
  - **Power System ……80% (Jun Hu, Jia Wang)**
  - **Wireless communication ……..100% (Jun Hu)**
  - **Clocking ……70% (Jun Hu)**
  - **Backend Electronics ……100% (Jun Hu)**
  - **Cabling, Crates & Elec Room ……100% (Wei Wei)**
  - **Previous R&D on electronics system ……..100% (Wei Wei)**