



Progress of CEPC ref-TDR TDAQ

Fei Li, Jingzhou Zhao
On behalf of CEPC TDAQ Group



中國科學院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Progress of TDAQ

- TDR draft v0.4
 - Update Simulation/L1/HLT/DAQ/DCS
 - Add 5 to 32 pages now
- TDAQ meeting
 - Dec. 17th (Tue. afternoon)
- International cooperation
 - DRD 7.5a month meeting
 - Wolfgang Kuehn, Justus-Liebig-Universitaet Giessen, Germany
 - PIFI application

Chapter 12 Trigger and Data Acquisition	1
12.1 Introduction	1
12.2 Requirements	1
12.2.1 Experiment Requirements	1
12.2.2 Event rate & background rate estimation	2
12.3 Overall Design	3
12.3.1 Design consideration	3
12.3.2 TDAQ design structure	5
12.4 Trigger Simulation and Algorithms	6
12.4.1 Physics Signatures and primitives with sub-detectors	6
12.4.2 Sub-detectors trigger algorithms	11
12.4.3 Global trigger algorithms	12
12.5 Hardware Trigger	12
12.5.1 Introduction	12
12.5.2 System architecture	13
12.5.3 Common Trigger Board	14
12.5.4 Trigger Control and Distribution	16
12.6 Software and High Level Trigger	16
12.6.1 HLT software	18
12.6.2 Study of GPU usage in the HLT	18
12.6.3 Study of FPGA usage in the HLT	18
12.7 Data Acquisition System	19
12.7.1 Overview of System Functionality	19
12.7.2 Detector Readout	20
12.7.3 Dataflow Software	23
12.7.4 Online Software	24
12.8 Detector Control System	25
12.8.1 Requirements	25
12.8.2 Architecture design	26
12.8.3 Software architecture design	27
12.9 Experiment Control System	27
12.9.1 Requirements	27
12.9.2 Software framework design	28
12.9.2.1 Intelligent operations and maintenance platform	28
12.10 Summary	32

TDAQ meeting on Dec. 17th (Tue. afternoon)

■ Simulation progress

– Cross section of Bhabha

用 babayaga，去掉能量差的 cut，要求加探测器覆盖范围 8 度到 172 度

要求出射正负电子及光子都在 8 度到 172 度得到： Higgs: 652 pb; Z: 4031pb, ~ 2kHz

只要求出射正负电子在 8 度到 172 度得到： Higgs: 1000 pb, ~ 100Hz; Z: 6593pb, ~ 3kHz

– Hcal endcap background

- Energy cut 99% after software bug fixed

– Muon background

- Significant reduction after digitization
- Start tracking study

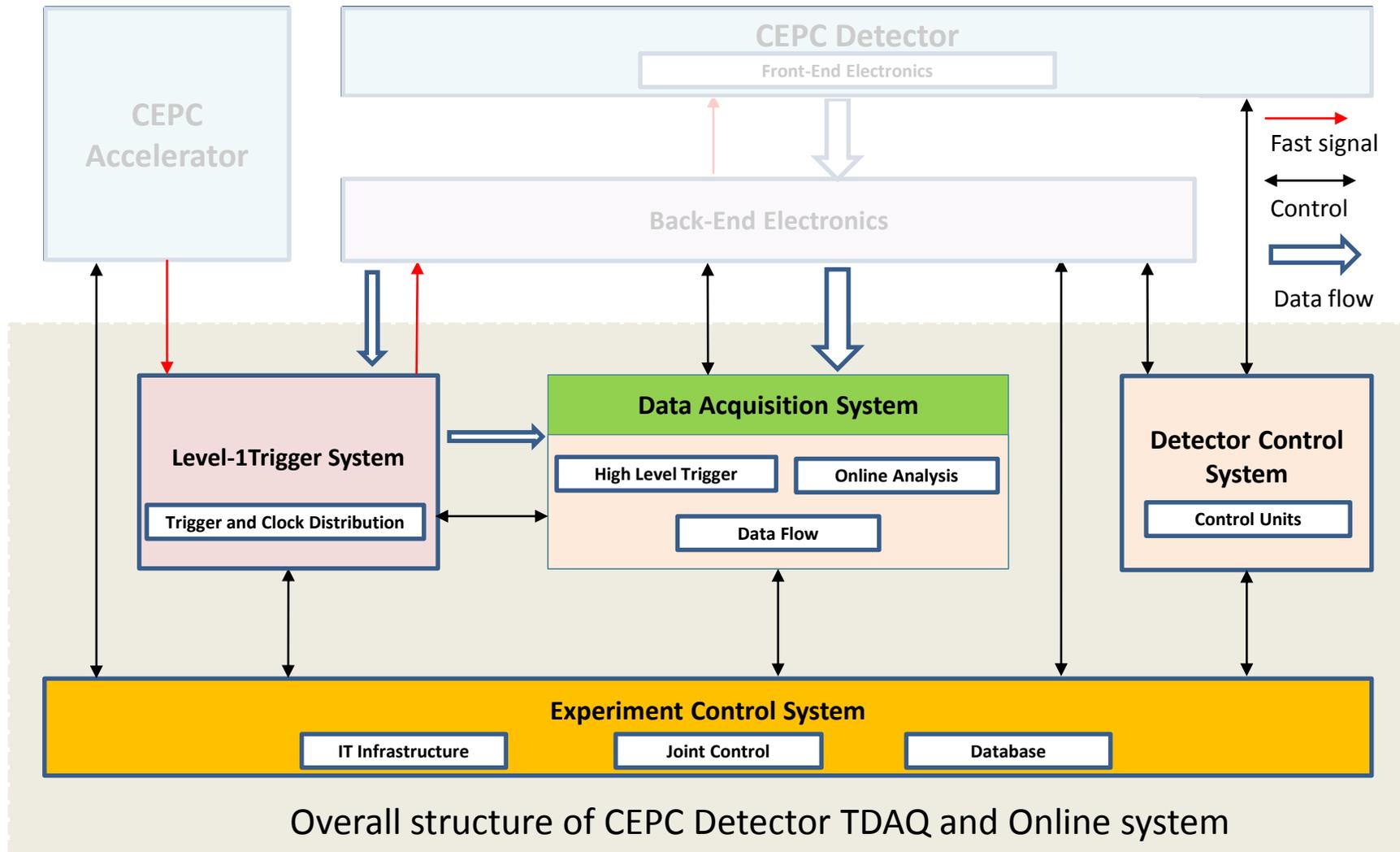
■ FPGA DNN development at Belle-II

■ TDR editing discussion

■ R&D discussion

CEPC TDAQ meeting		
Thursday Dec 12, 2024, 2:00 PM → 5:00 PM Asia/Shanghai		
2:00 PM → 2:10 PM	Introduction Speakers: Mr Fei Li (EPC, IHEP, Beijing, China), Jingzhou ZHAO (高能所), Xiaolu Ji (Institute of High Energy Physics, CAS)	10m
2:10 PM → 2:30 PM	Simulation & HLT Speakers: Boping Chen, Junhao YIN (南开大学), dong Liu (中国科学院高能物理研究所), 启东/Qidong 周/Zhou (山东大学/Shandong university) 	20m
2:30 PM → 3:20 PM	Detector Survey	
2:30 PM	Vertex Speakers: Hongyu ZHANG (EPC, IHEP, CAS, China), 畅徐 (高能所)	10m
2:40 PM	ITK&OTK Speakers: Sheng DONG (IHEP, CAS), Xiangyi Mu (高能物理研究所)	10m
2:50 PM	TPC&DC Speakers: Hongyu ZHANG (EPC, IHEP, CAS, China), 叙张 (高能所)	10m
3:00 PM	ECal&HCal Speakers: Boping Chen, dong Liu (中国科学院高能物理研究所)	10m
3:10 PM	Muon Speakers: Junhao YIN (南开大学), 剌明 李 (中科院高能物理研究所)	10m
3:20 PM → 3:30 PM	Trigger Hardware Speakers: Jingzhou ZHAO (高能所), Sheng DONG (IHEP, CAS), dong Liu (中国科学院高能物理研究所)	10m
3:30 PM → 3:40 PM	Readout Protocol Speakers: Hongyu ZHANG (EPC, IHEP, CAS, China), Sheng DONG (IHEP, CAS), 畅徐 (高能所)	10m
3:40 PM → 3:50 PM	DAQ software Speakers: Hongyu ZHANG (EPC, IHEP, CAS, China), Xiangyi Mu (高能物理研究所), Xiaolu Ji (Institute of High Energy Physics, CAS), Yi LIU (DESY), 叙张 (高能所)	10m
3:50 PM → 4:00 PM	DCS&ECS Speakers: Sheng DONG (IHEP, CAS), 斯马 (高能所)	10m

Overall Design



Backup

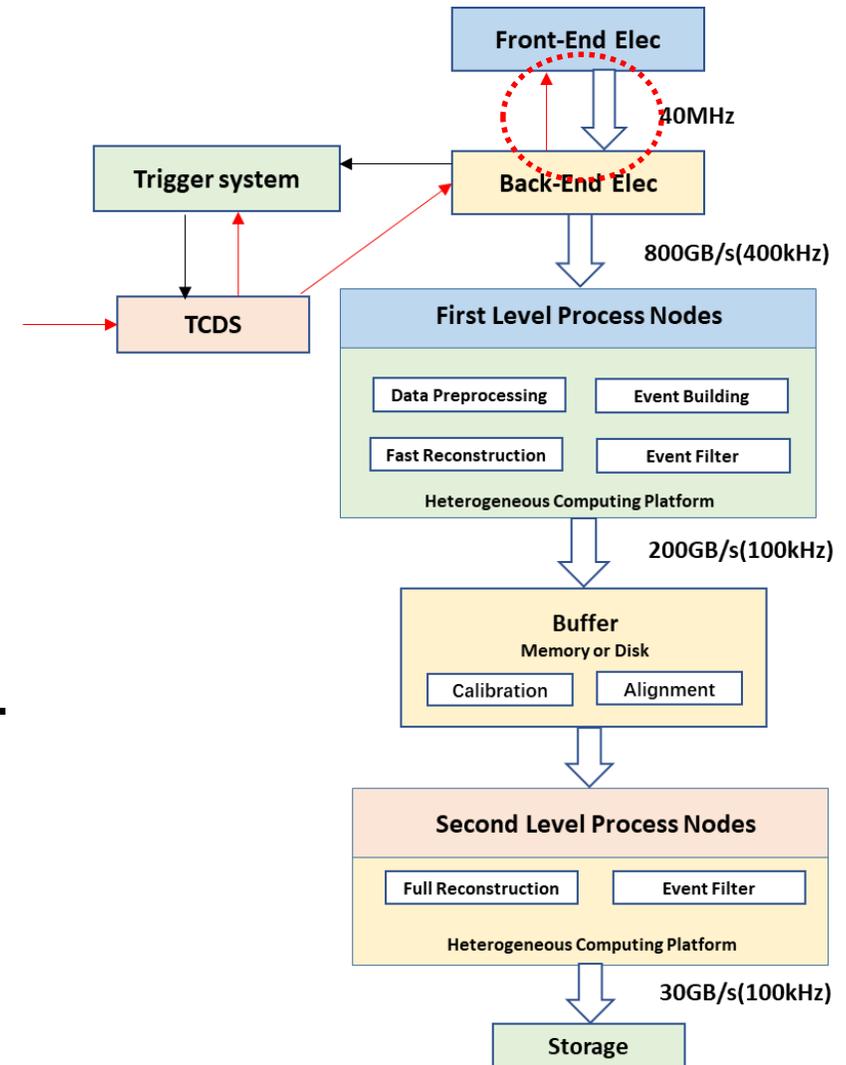
Trigger strategy on High Lumi-Z

■ Trigger on High Lumi-Z

- Same hardware trigger structure on High Lumi-Z and low Lumi-Z
- Hardware resource may increase-
common trigger boards

■ Electronic system

- Trigger send to FEE from BEE if needed.
- If trigger latency can not meet the requirements, private trigger link may needed from FEE to BEE.



Physical Event Rate

■ Higgs 240GeV(30MW/50MW)

- BX rate: 0.8(1.74)/1.34(2.9) MHz
- Physical event rate: **5Hz/8Hz** (Higgs: 0.02Hz)

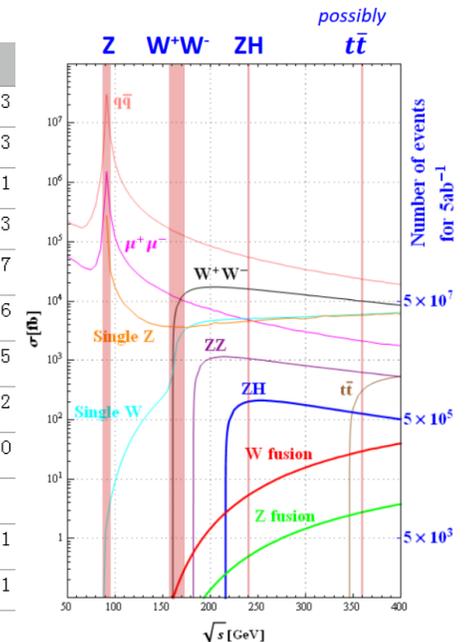
■ Z pole 91GeV(10MW/50MW)

- BX rate: 12(14.5)/39.4(43.3) MHz
- Physical event rate: **13.2kHz/66kHz**

	Higgs	Z		W	$t\bar{t}$
SR power per beam (MW)	30	30	10	30	30
Bunch number	268	11934	3978	1297	35
Bunch spacing (ns)	576.9 (×25)	23.1(×1)	69.2(×3)	253.8(×11)	4523.1(×196)
Train gap (%)	54	17	17	1	53
Luminosity per IP ($10^{34} \text{ cm}^{-2} \text{ s}^{-1}$)	5.0	115	38	16	0.5

	Higgs	Z	W	$t\bar{t}$
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 (×15)	23.1 (×1)	138.5 (×6)	2700.0 (×117)
Train gap (%)	54	9	10	53
Luminosity per IP ($10^{34} \text{ cm}^{-2} \text{ s}^{-1}$)	8.3	192	26.7	0.8

过程	xsection(nb)	百分比	事例率kHz
Bhabha	0.0586	0.001371951	0.068597543
muon	1.5361	0.035963374	1.798168703
tau	1.5249	0.035701158	1.78505791
qq	30.6522	0.717633315	35.88166573
电子中微子	2.9607	0.069316296	3.465814777
muon中微子	2.9896	0.069992906	3.499645306
tau中微子	2.9909	0.070023342	3.501167095
中微子总	8.9411	0.209330202	10.46651012
总共	42.7129	1	50
		亮度	
30MW		1.15E+36	4.91E+01
50MW		1.92E+36	8.20E+01



Z pole, ref: [MC /cefs/data/stdhep/CEPC91/2fermions/wi_ISR_20220618_50M/2fermions/](https://mc.cern.ch/cefs/data/stdhep/CEPC91/2fermions/wi_ISR_20220618_50M/2fermions/)

Beam Backgrounds

Ave. hit rate Higgs Vs Low Z

- Vertex: 0.49 -> 1.96, 5 times
- ITK: 0.0021 -> 0.08, 40 times
- ECal: 0.011 -> 0.35, 30 times

Higgs Vs Low Z

- BX rate 1.34 -> 12 MHz

Raw data rate @Higgs

- 400GB/s

Raw data size per BX @Higgs

- 300KBytes

	50MW Higgs, 346ns/BX
Pair Production	~1.82GHz in IR
Beam Thermal Photon	~0.30MHz/beam in IR
Beam Gas Bremsstrahlung	~0.04MHz/beam in IR
Beam Gas Coulomb	~0.23MHz/beam in IR
Touschek Scattering	~0.06MHz/beam in IR
Radiative Bhabha	
SR	~630 PHz/beam generated at last bending magnet

	50MW Higgs, 23ns/BX
Pair Production	~25.5GHz in IR
Beam Thermal Photon	~0.26GHz/beam in IR
Beam Gas Bremsstrahlung	~0.01GHz/beam in IR
Beam Gas Coulomb	~2.36GHz/beam in IR
Touschek Scattering	~6.24GHz/beam in IR

	10MW Z, 69ns/BX
Pair Production	~3.2GHz in IR
Beam Thermal Photon	~63MHz/beam in IR
Beam Gas Bremsstrahlung	~2.5MHz/beam in IR
Beam Gas Coulomb	~272MHz/beam in IR
Touschek Scattering	~62MHz/beam in IR

Sub-Detectors	Ave. Hit Rate(MHz/cm ²)	Max. Hit Rate(MHz/cm ²)	Max. Occupancy/BX(%)
Vertex	0.49	0.61	0.0022
ITK	0.0021	0.25	0.025(Strip)
TPC	2.7	6.0	0.0045
OTK – Endcap	0.0002	0.0006	0.35(Strip)
ECal – Endcap	0.011/bar	0.3/bar	0.0008
HCal – Endcap	0.002/GS	0.05/GS	0.0005
Muon – Endcap	0.00000001/cell	0.00002/cell	0.006
LumiCal – Crystal	3.37	7.82	9.1

Sub-Detectors	Ave. Hit Rate(MHz/cm ²)	Max. Hit Rate(MHz/cm ²)	Max. Occupancy/BX(%)
Vertex	15.64	18.34	3.73e-3
ITK	0.61	57.61	0.0543
TPC	2	3.5	0.0026
OTK – Endcap			
Ecal – Barrel	1.54/bar	22.3/bar	7.03
ECal – Endcap	2.84/bar	43.5/bar	9.29
HCal – Endcap			
Muon – Endcap			1.5

Sub-Detectors	Ave. Hit Rate(MHz/cm ²)	Max. Hit Rate(MHz/cm ²)	Max. Occupancy/BX(%)
Vertex	1.96	2.30	3.73e-3
ITK	0.08	7.20	0.0543
TPC	0.25	0.45	0.0026
OTK – Endcap			
ECal – Barrel	0.2	2.79/bar	7.03
ECal – Endcap	0.35	5.44/bar	9.29
HCal – Endcap			
Muon – Endcap			1.5
LumiCal – Crystal			

Raw Data Rate

Data rate before trigger

- <1 TB/s @ Higgs
- Several TB/s @ Z

L1 trigger rate

- O(1k) Hz @ Higgs
- O(100k) Hz @ Z

Event size < 2 MB

- Related to occupancy and read out window

Storage rate after HLT

- <100 Hz(200 MB/s) @ Higgs
- 100 kHz (200 GB/s) @ Z

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024	512*128	1024	128		128	8~16				
Data Width /hit	32bit	42bit	32bit	48bit		48bit	48bit				
Avg. data rate / chip	0.18Gbps/chip, 1Gbps/chip inner	3.53Mbps/chip	21.5Mbps/chip	2.9Mbps/chip	38.8Mbps/chip	~70Mbps/module Inmost	10kHz/ch	10kHz/ch	5kHz/channel	5kHz/channel	10kHz/channel
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.39 M chn	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43,176 chn, 288 modules
Avg Data Vol before trigger	474.2 Gbps	101.7 Gbps	298.8 Gbps	249.1 Gbps	27.9 Gbps	34.4 Gbps	460.8 Gbps	187 Gbps	811.2 Gbps	537.6 Gbps	24 Gbps
Occupancy(%)	0.022	0.025(Strip)		0.35(Strip)		0.0028	0.58		0.002		0.038
Sum	3.2 Tbps = 400GB/s										

Collected from each detectors @Higgs

Trigger & Data Rate

L1 trigger rate

- 13 kHz@Higgs, 120 kHz@low. Z

Read out window

- TPC 34 us
- CLIC rec. time window
 - ECAL & HCAL Endcaps & Silicon 10 ns
 - HCAL Barrel 100 ns

Readout event size

- 620KBytes @ Higgs
 - 100 BX/events and 3.2 KBytes/BX for TPC
- 2 MBytes @Low lum. Z
 - 500 BX/event for TPC(full readout)
 - 2 BX for Hcal (75 KBytes/BX)
- 5.3 MBytes @High lum. Z
 - 1472 BX/event for TPC(full readout)
 - 5 BX for HCal

DAQ data rate

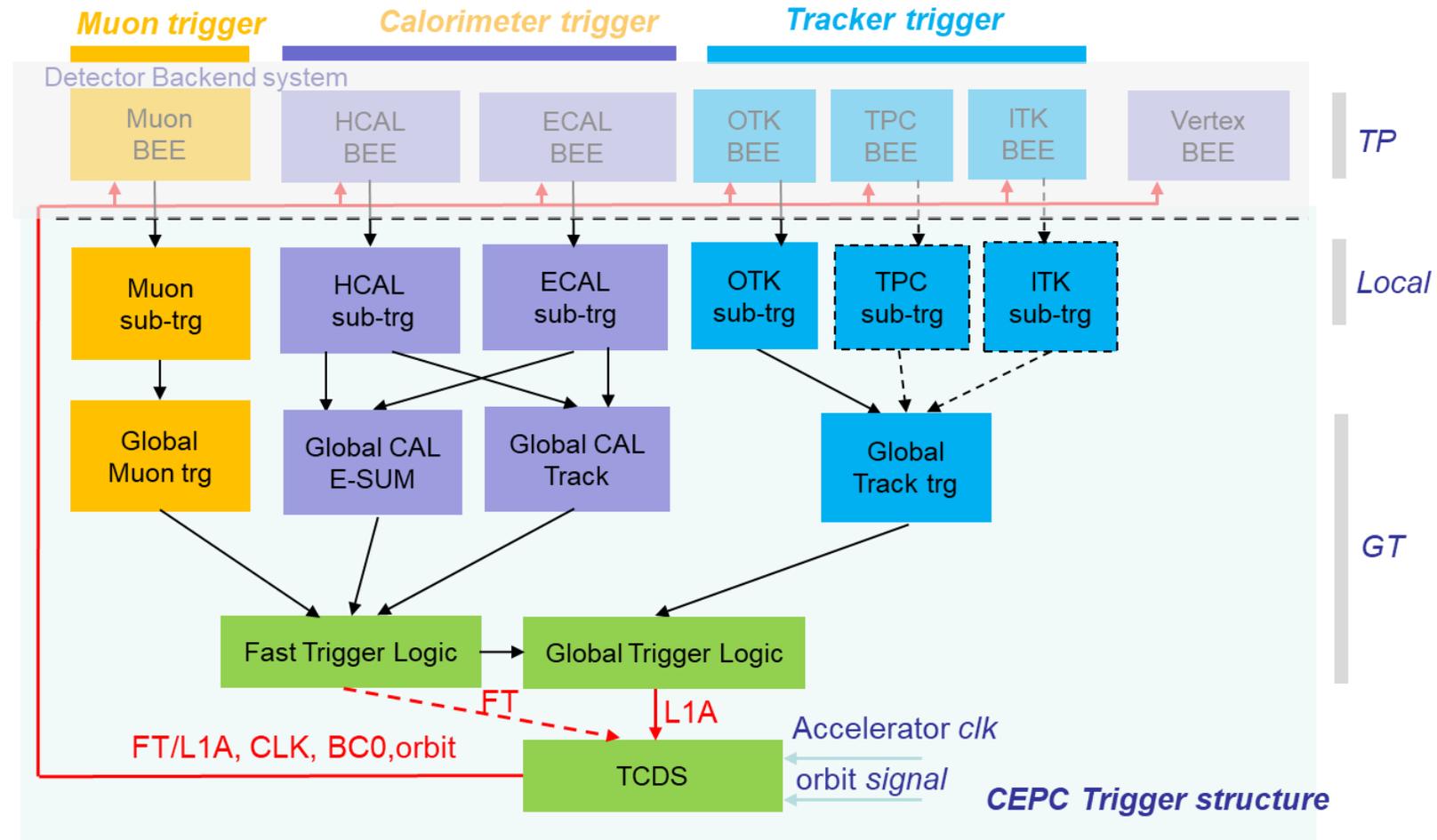
- Read out: 8 GB/s @Higgs, 83.4 GB/s @ Low lum. Z (120kHz*375KB + 12MHz*3.2KB)
 - 366 GB/s @ High lum. Z (400kHz*(300+75*4)KB + 39.4MHz*3.2KB)
- Storage: 0.6 GB/s @Higgs, 50 GB/s @Low lum. Z (7.5GB/s after event size compression)
- 1 year(3600h): 8 PB, 100 PB

	Higgs	Z(10MW)	Z(50MW)	W	tt
Luminosity(10E34/cm2/s)	8.3	38	192	26.7	0.8
Bunch space(ns)	346.2	69.3	23.1	253.8	4523.1
Bunch cross rate(MHz)	1.34	12	39.4	6.5	0.18
Raw data rate before trigger (TBytes/s)	0.4	3.6	11.82	1.95	0.048
Physical event rate(kHz)	0.008	13.2	66	0.1	0.002
L1 trigger rate(kHz)	13	120	400	65	2
DAQ readout rate(Gbyte/s)	26	240	800	130	4
High level trigger rate(kHz)	1	25	100	6	1
DAQ storage rate(Gbytes/s)	0.3	7.5	30	1.8	0.3

Event size: readout 2MB, storage 300KB

Design of Hardware Trigger Structure

- Trigger primitive(TP)
 - Extracted by BEE
- Local detector trigger
 - Sub energy and tracking...
- Global trigger
 - E-sum and tracking
 - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
 - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied

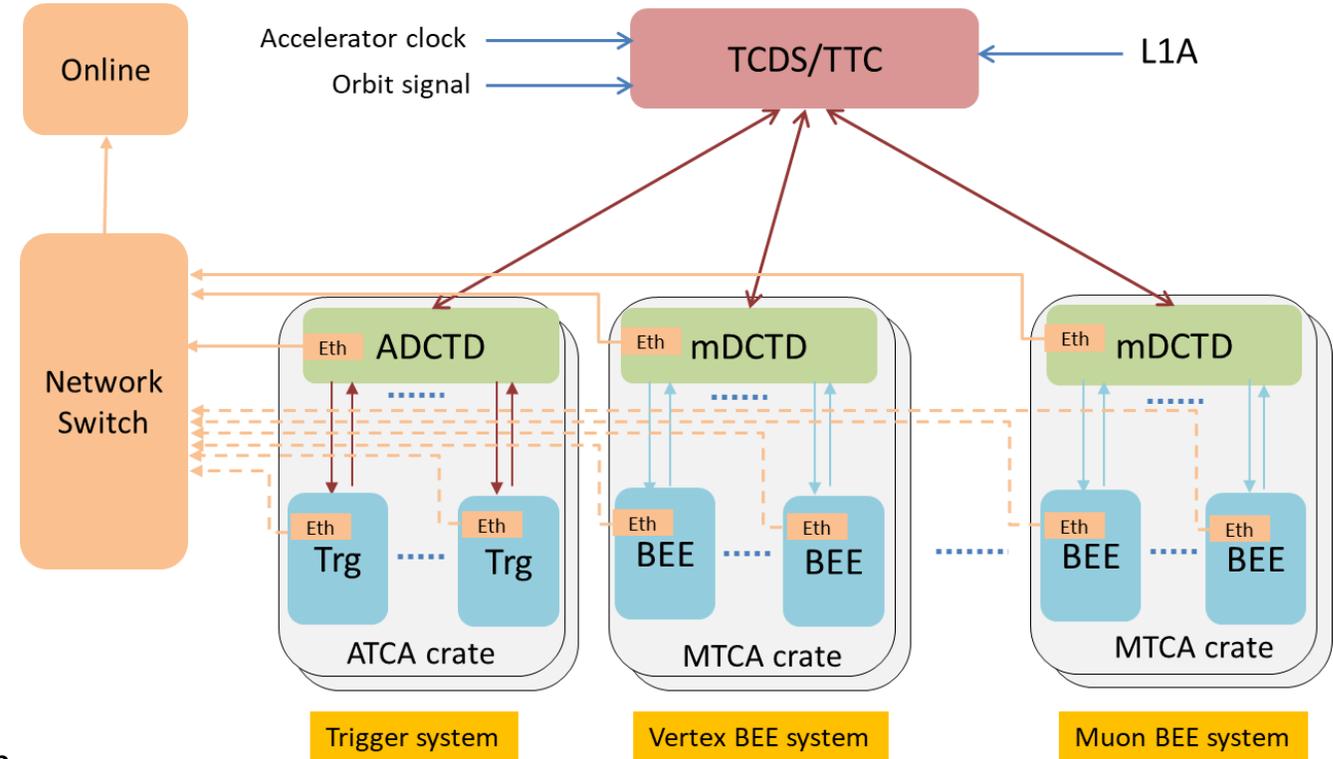


TCDS-Trigger Clock Distribution System

■ TCDS/TTC

- Clock, BC0, Trigger, orbit start signal distribution
- Full, ERR signal feed back to TCDS/TTC and mask or stop L1A

- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD-Data Concentrator and Timing Distribution
- BEE-Backend board Electronic



TDAQ are only responsible for system-level distribution, each system is then responsible for its own internal distribution.