CEPC CMOS Strip Tracker

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On behalf of CMOS Strip Tracker Team

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Ref TDR Progress

- ✓ Add more description of electronics

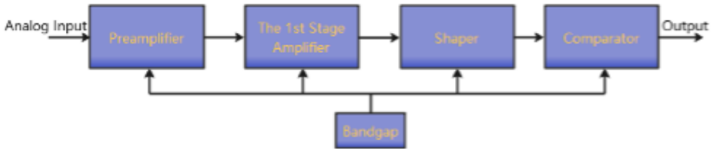


Figure 5.18: Structure of AFE.

The output port of the silicon microstrip sensor can be externally equivalent to a current source, and the pulse area of its output represents the charge quantity. The analog front-end (AFE) of the readout circuit converts this charge quantity into a voltage and processes this voltage signal through amplification, shaping, analog-to-digital (AD) conversion, and other operations. A single-channel readout circuit includes circuits such as a preamplifier, a first-stage amplifier, a shaping circuit, and a discriminator.

The preamplifier is used to initially amplify the output signal of the detector and complete the conversion of signal form. This design selects a charge-sensitive amplifier structure with excellent noise performance. The charge output by the sensor accumulates on the integrating capacitor, and the peak value of the output voltage signal is proportional to the input charge. The feedback resistor Rf and the feedback capacitor Cf constitute a charge-discharge circuit.

Although the output of the AFE is a binary signal, the entire AFE circuit still requires high linearity and a large dynamic range, as well as a certain level of noise suppression capability. This design incorporates a first-stage amplifier

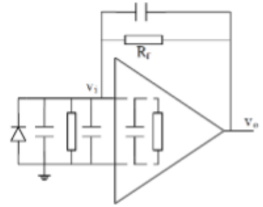


Figure 5.19: Structure of Preamplifier.

and adopts a folded cascode circuit structure to achieve a gain within the range of 80 to 100 mV/fC.

The shaping circuit performs shaping and filtering processing on the output signal of the preceding amplifier to reduce signal tailing, filter out noise and interference, and amplify the signal again. The shaping circuit adopts a differential structure circuit with single-ended input and double-ended output, providing a high power supply rejection ratio.

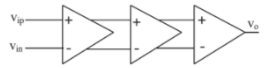


Figure 5.20: Structure of Discriminator.

The discriminator is a high-speed, high-resolution comparator that obtains a binary comparison result by comparing the output voltage signal of the shaping circuit with a reference voltage. In this design, the discriminator employs a structure of cascaded comparators with low open-loop gain but wide bandwidth, forming a high-speed, high-resolution comparator.

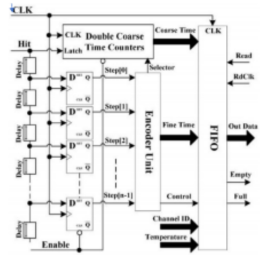
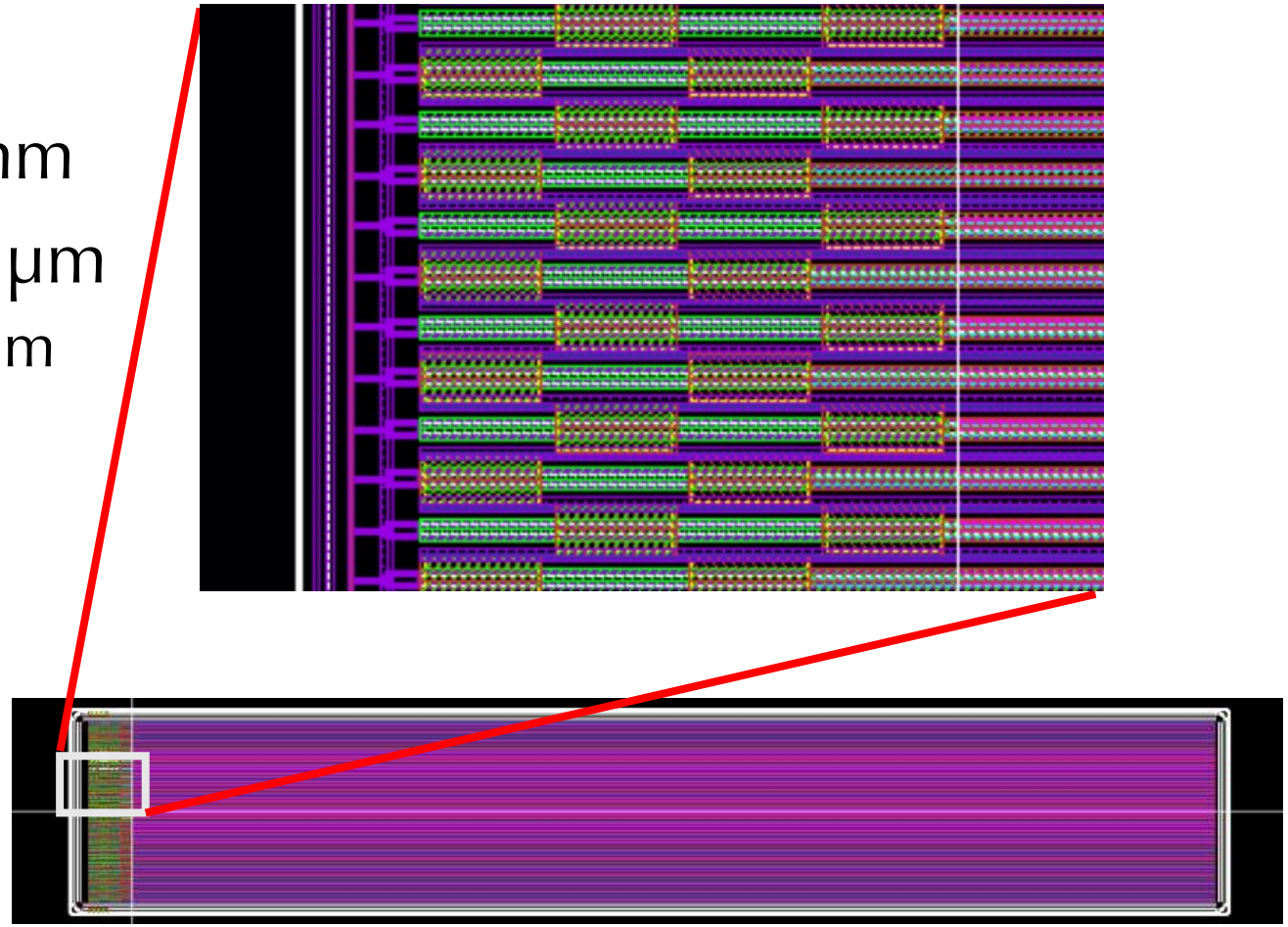


Figure 5.21: Structure of TDC.

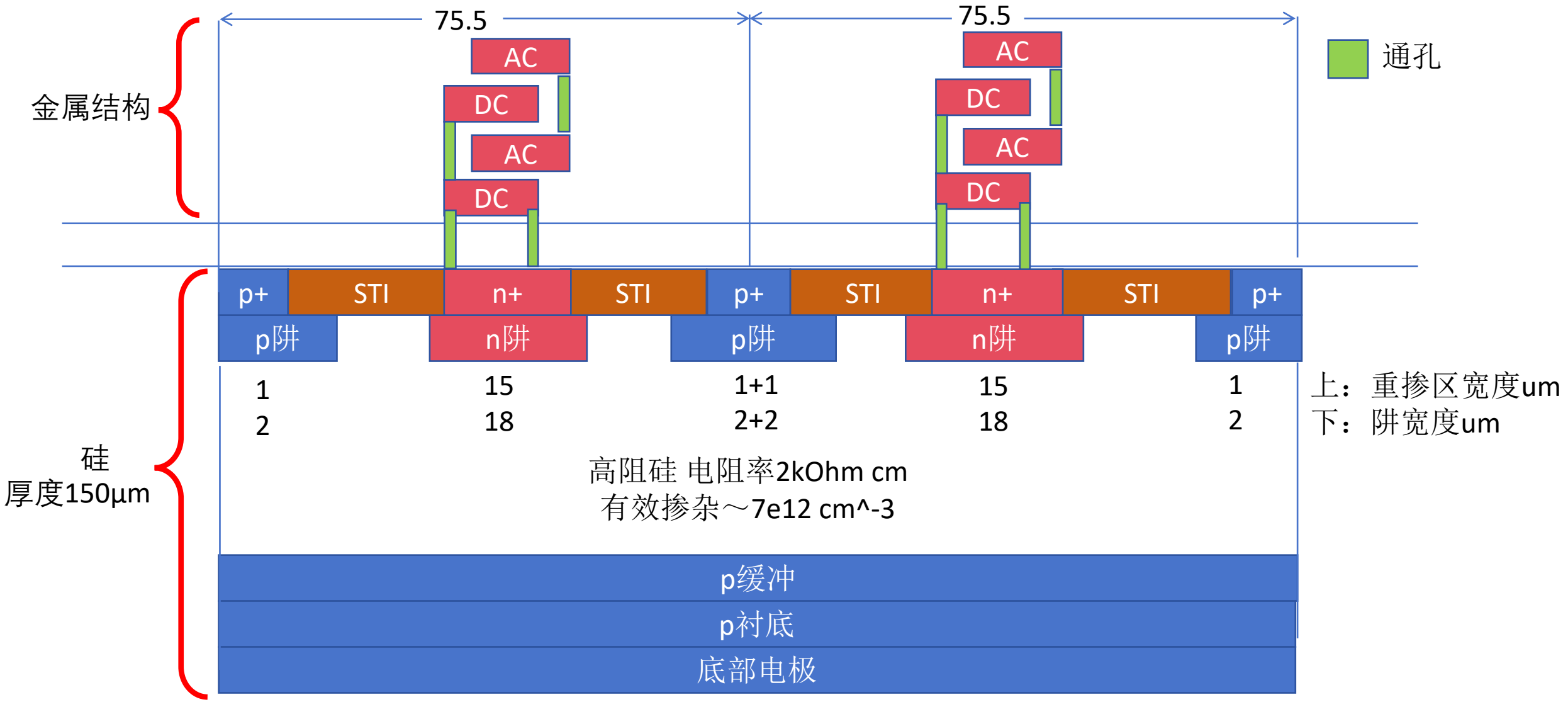
The main clock delivered to chip is synchronous with the beam. However, its phase, although constant, is difficult to predict in advance. Therefore, it is shifted in the dedicated low power DLL to obtain a precise alignment between the ADC sampling phase and the bunch crossing. The DLL produces a second replica of the 40 MHz clock, which is used to tune the delay of the internal test pulse for the analogue front-end.

传感器设计进展 – CSC1-A

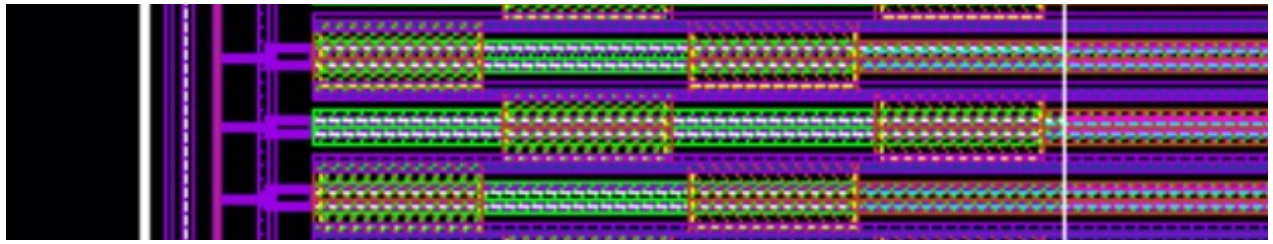
- 无锡上华CMOS 1P4M工艺
- 总尺寸 长20.000 mm 宽3.486 mm
- 电极条 长19.716 mm 间距 75.5 μm
  - 读出电极 n-well宽18μm, n+宽15μm
  - p-well宽4 μm, p+宽2 μm
- pad 面积 75μm * 180μm
- 总道数40道
- n-well通过阱电阻连接到偏压环
- 外侧两层n+ guard ring



CSC1-A：横截面


75.5
75.5
金属结构
AC
DC
AC
DC
AC
DC
AC
DC
通孔
p+
STI
n+
STI
p+
STI
n+
STI
p+
p阱
n阱
p阱
n阱
p阱
1
2
15
18
1+1
2+2
15
18
1
2
上：重掺区宽度um
下：阱宽度um
硅
厚度150μm
高阻硅 电阻率2kOhm cm
有效掺杂～7e12 cm^-3
p缓冲
p衬底
底部电极

CSC1-A：纵截面



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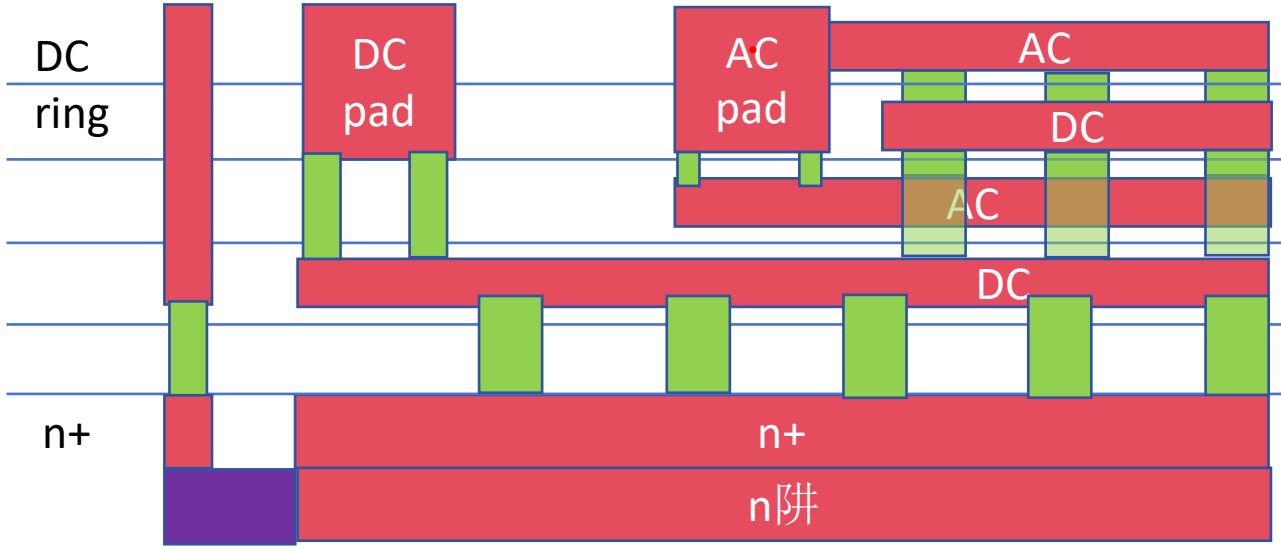
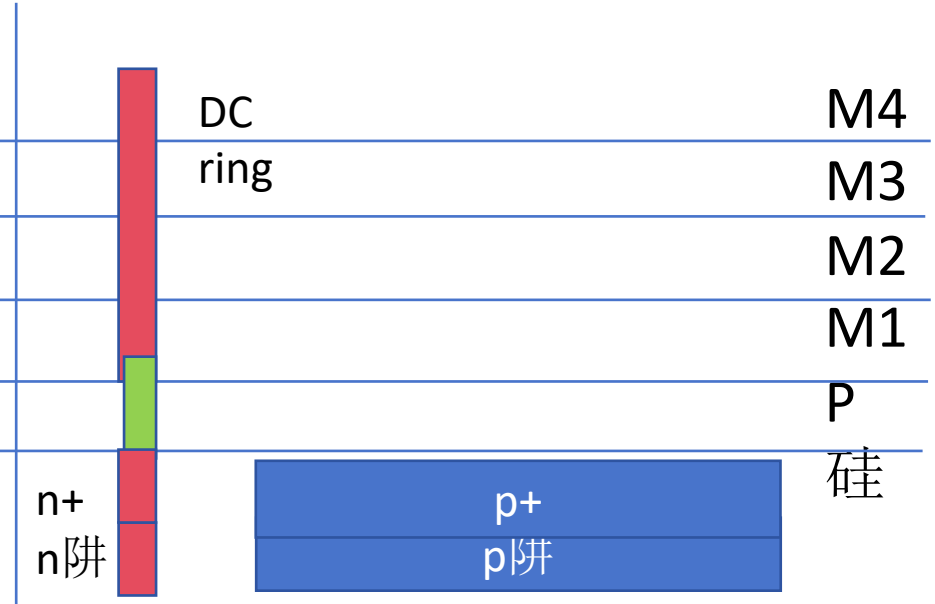


n阱电阻



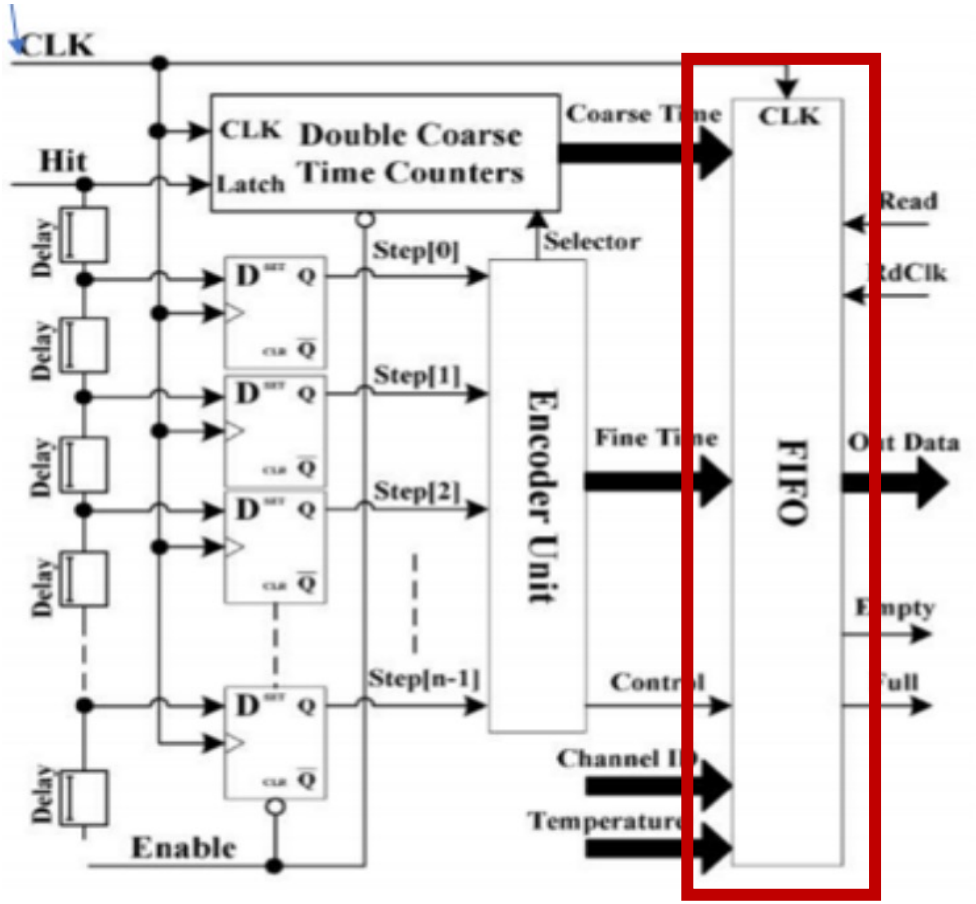
n-stop 处 | p-stop处

传感器部分小结

- 版图已经符合了全部设计规则，基本满足交付厂家生产的条件
  - 正在进行 gds 导入 TCAD 后仿真验证
- 下一步：
  - 设计更小 pitch 的 A-die
  - 选择合理排布测试 pad

TDC 数字建模

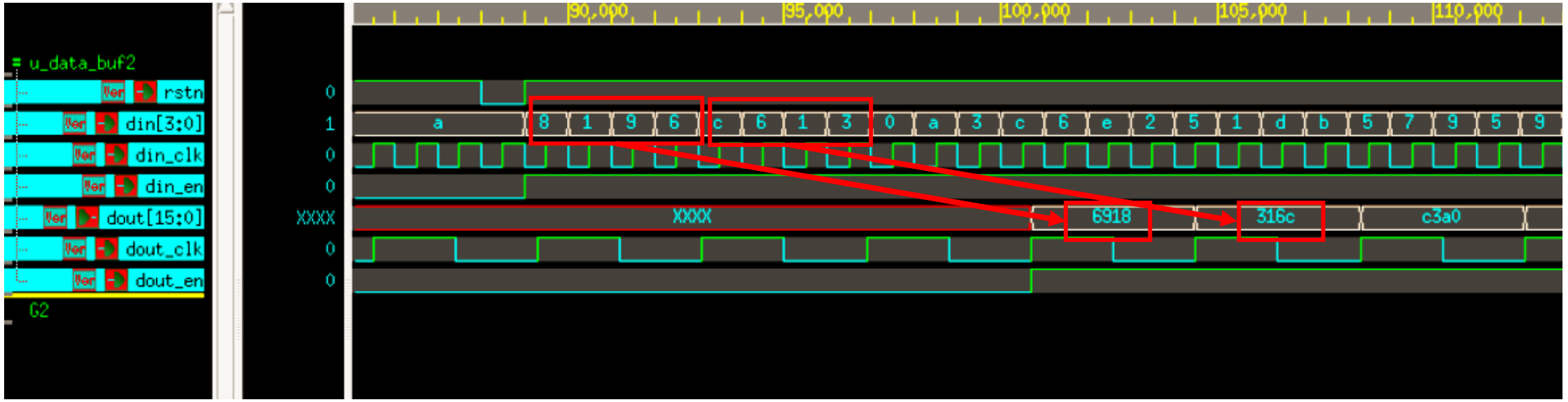
- 对TDC模块中FIFO进行建模



- FIFO宽度：细计数器8位+粗计数器8位
- FIFO深度：
  时钟周期1.28GHz 单个数据写入用时0.78ns
  若一次性突发写入100个数据：用时78ns
  读出时钟周期640Mhz 单个数据读出用时1.56ns
  Depth = 78ns/1.56ns = 50

模型仿真

读入时钟：1.28GHz
读出时钟暂时设定为读入的1/2：640MHz
数据输出时将输入的四个数据为一组并行输出，数据组合顺序输出



- 顺序写入个数据2b‘8、 2b’1、 2bd9、 2b’6、 2b‘c、 2b’6、 2bd1、 2b’3， FIFO先后并行输出四个数据的组合6918和316c
- 下一步工作：将TDC的输出与FIFO模块进行调试