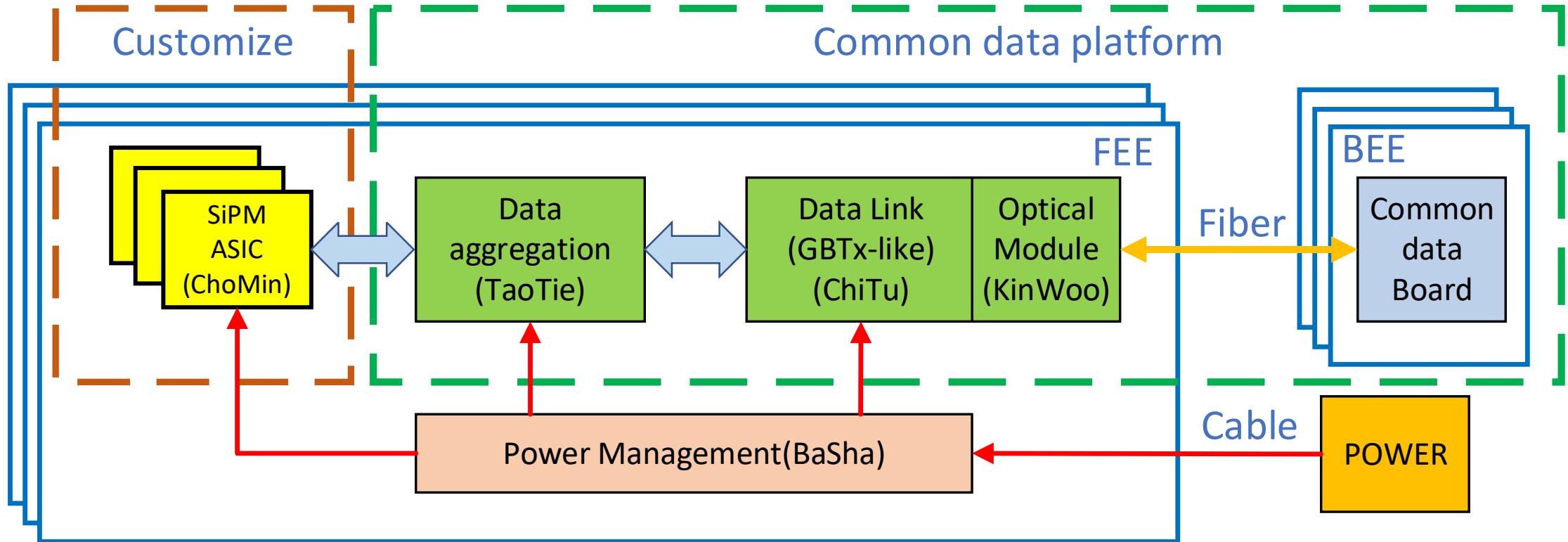
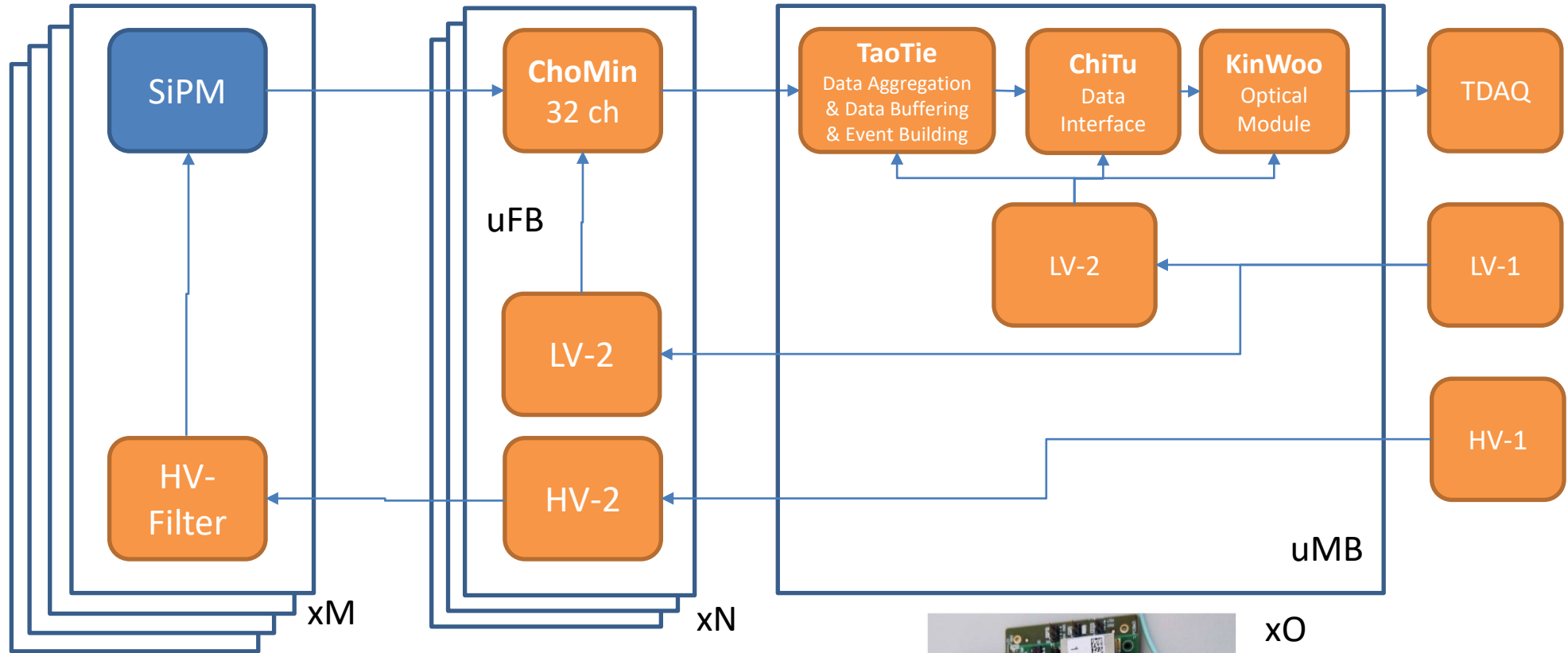


Baseline for SiPM readout

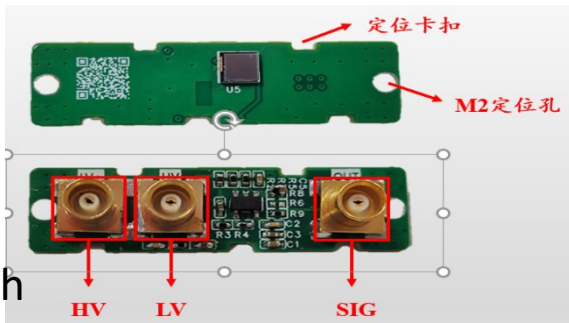


- Reuse the ASIC scheme (ChoMin) from ECAL or HCAL
- Revise according to the constraints from cooling and mechanical structure of the detector

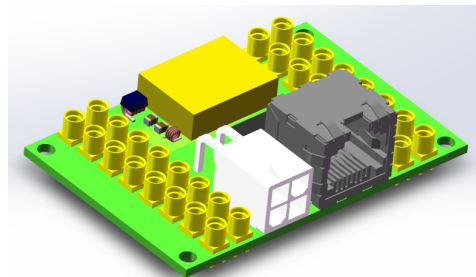
Stage scheme (M x N x O)



Example:



For each ch



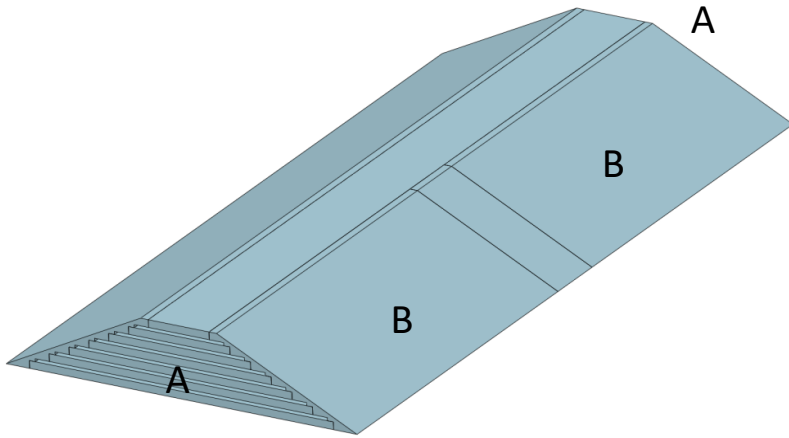
For each module



For each sector

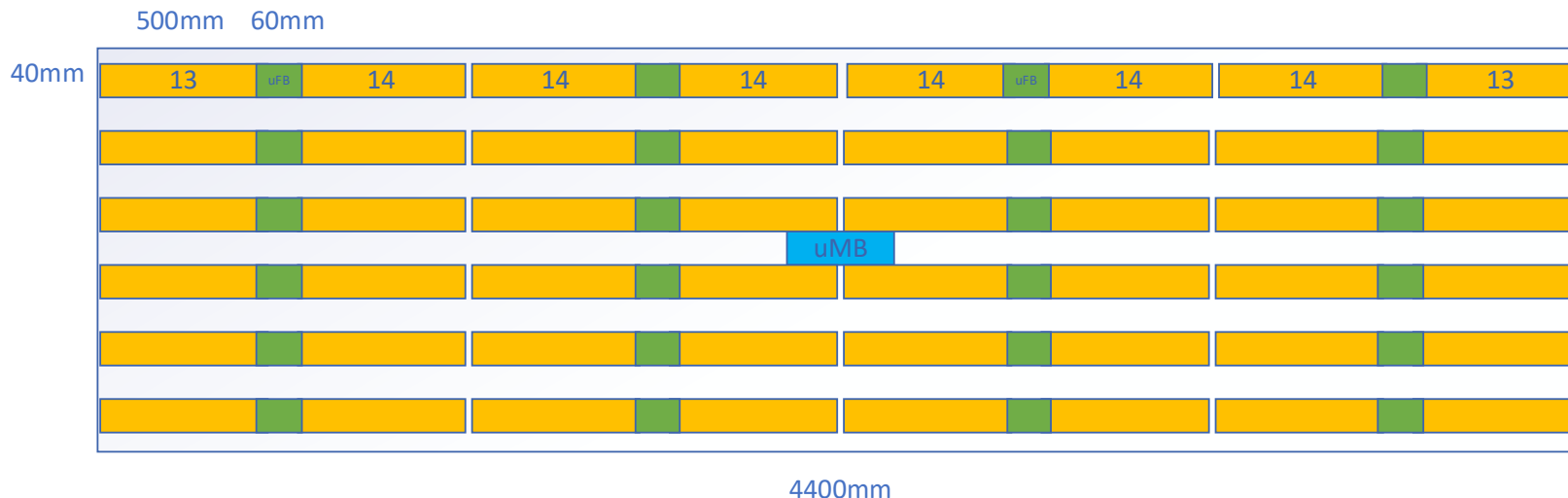
Electronics at B side

■ Row 6, Col 110



- uSiPM tile: Muon SiPM tile, 660 pcs
 - Small FR4 PCB
 - FPC connector1
- uFlex14: Muon flex cable, 48 pcs
 - Up to 14 ends to FPC connector1
 - 1 end to FPC connector2
- uFB: Muon front-end board, 24 pcs
 - 32 ch input, two FPC connector2
 - RJ45 and power connector

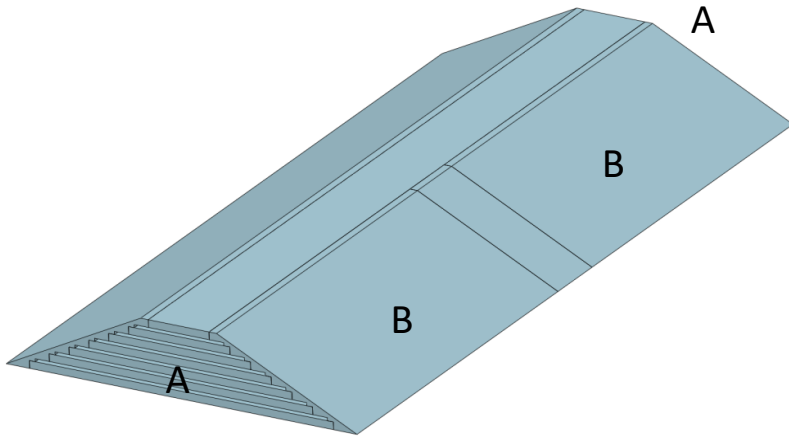
- uSiPM tile: Muon SiPM tile, 660 pcs
 - Small FR4 PCB
 - MMCX
- Coaxial cable
 - 2mm diameter
 - Could HV on shield, signal on core?
- uFB: Muon front-end board, 24 pcs
 - 32 ch input, MMCX
 - RJ45 and power connector



- uMB: Muon management board, 1 pc
 - Up to 24 RJ45 connectors, CAT6 shielded (5mm diameter, up to 3 meters) to uMB
 - Fiber to backend
 - Power input (AWG16 x4), 48V

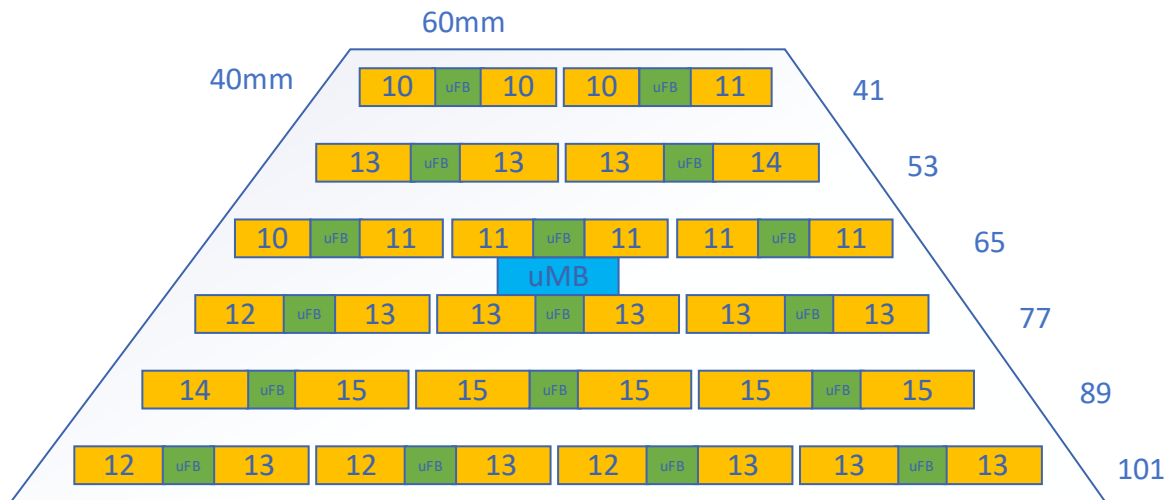
Electronics at A side

■ 6 Row



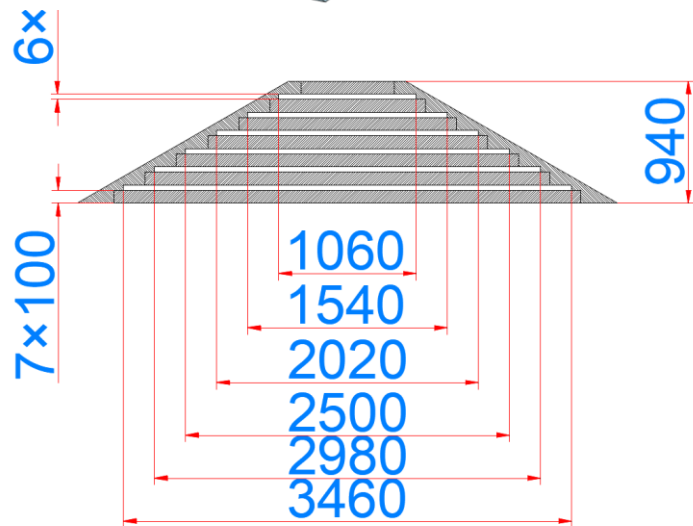
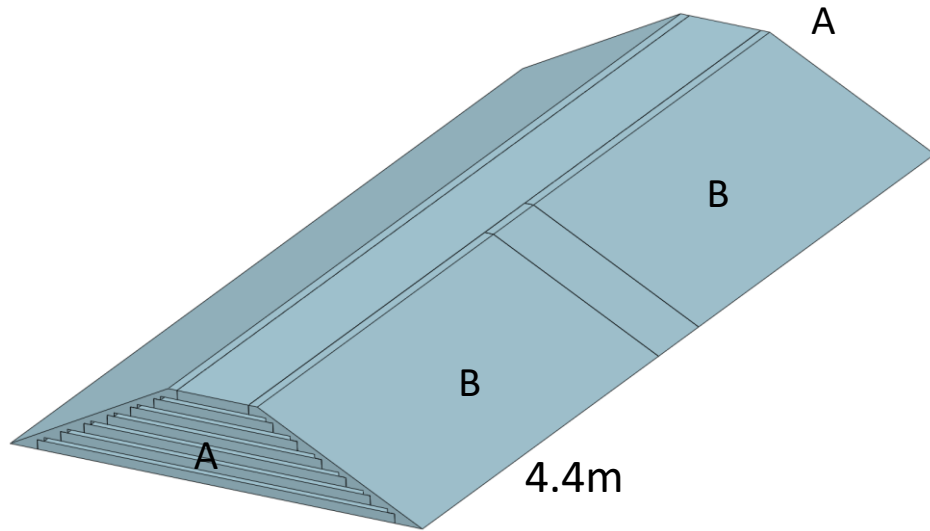
- uSiPM tile: Muon SiPM tile, 426 pcs
 - Small FR4 PCB
 - FPC connector1
- uFlex10~15: Muon flex cable, 48 pcs
 - Up to 14 ends to FPC connector1
 - 1 end to FPC connector2
- uFB: Muon front-end board, 17 pcs
 - 32 ch input, two FPC connector2
 - RJ45 and power connector

- uSiPM tile: Muon SiPM tile, 426 pcs
 - Small FR4 PCB
 - MMCX
- Coaxial cable
 - 2mm diameter
- uFB: Muon front-end board, 17 pcs
 - 32 ch input, MMCX
 - RJ45 and power connector



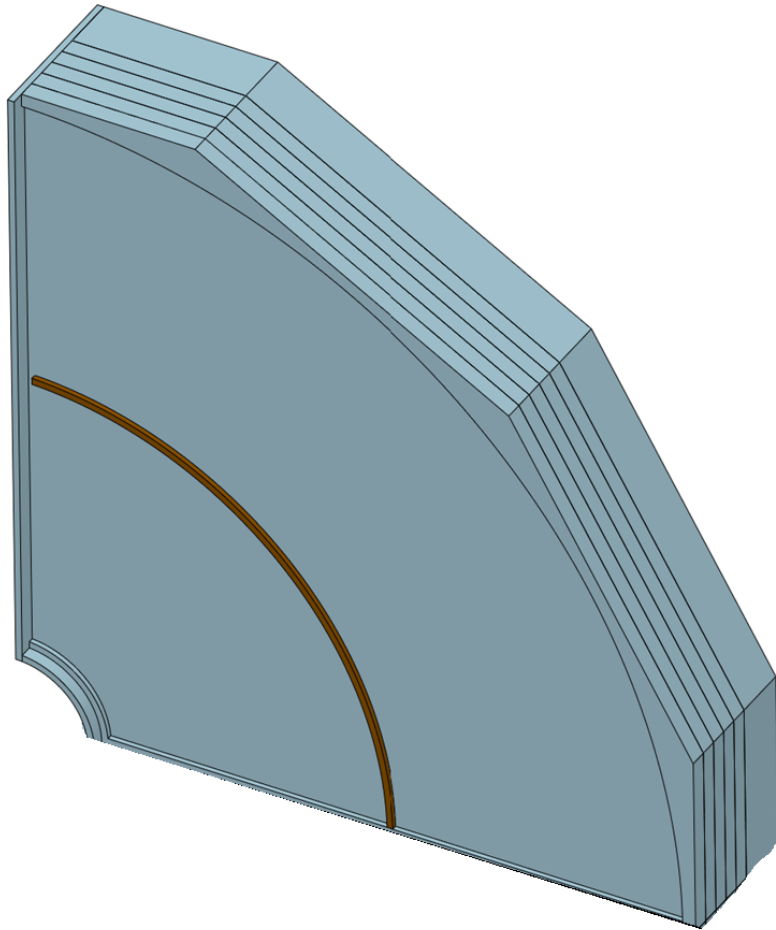
- uMB: Muon management board, 1 pc
 - Up to 24 RJ45 connectors, CAT6 shielded cable (5mm diameter, up to 2.5 meters) to uMB
 - Fiber to backend
 - Power input (AWG16 x4), 48V

Barrel sector

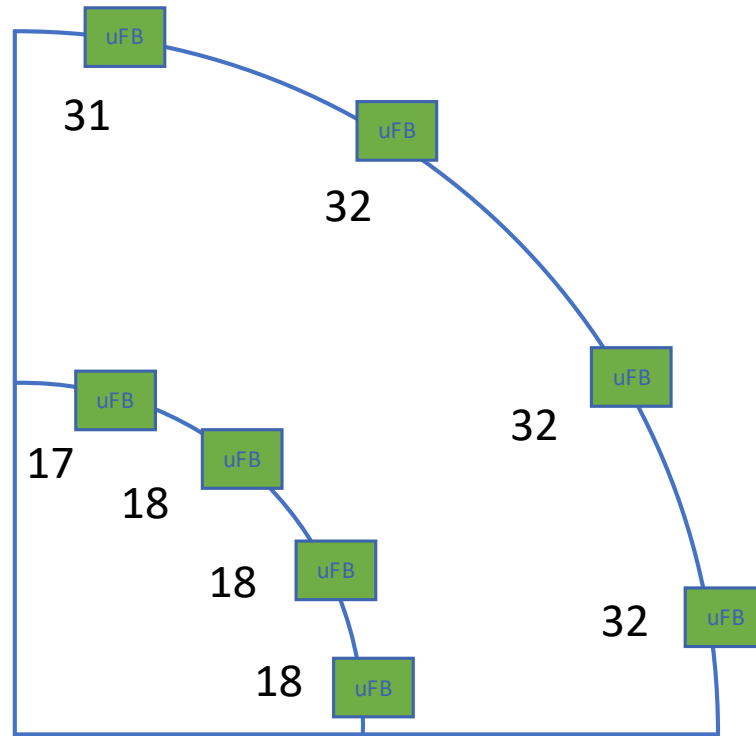


	M (uSiPM)	N (uFB)		O (uMB)
	ch	32-ch TDC board	Raw data rate / bps	Management board
A	426	17	161.28 M	1
B	660	24	318.24 M	1
Total per sector	2172	82	959.04 M	4
Total barrel (12 sectors)	26064	984	11.51 G	48

Electronics at Endcap



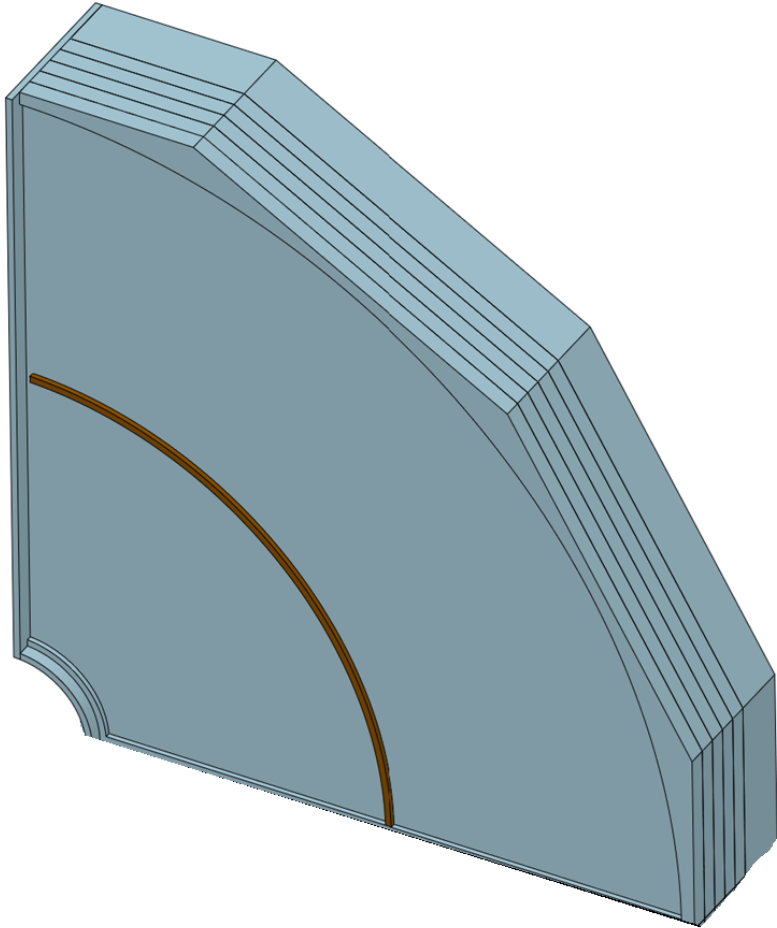
12 layers



One layer

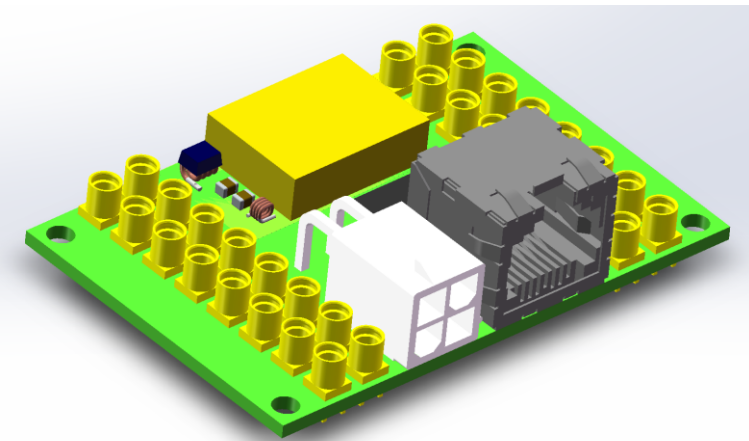
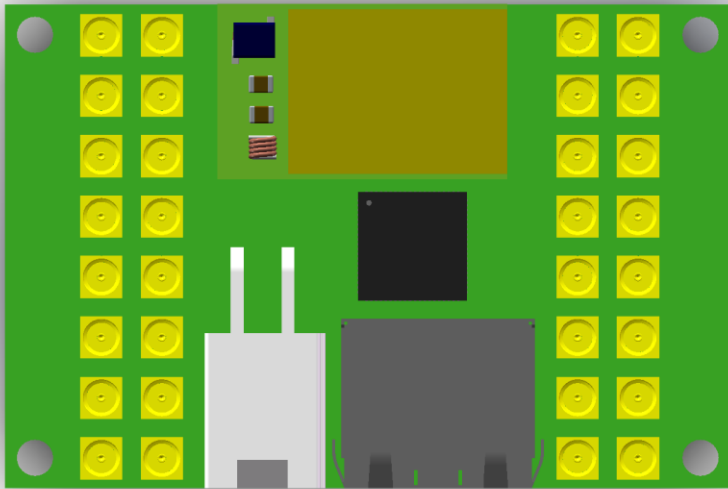
- uSiPM tile: Muon SiPM tile, 198 pcs
 - Small FR4 PCB
 - MMCX
- Coaxial cable
 - 2mm diameter
- uFB: Muon front-end board, 8 pcs
 - 50 mm x 40 mm FR4 PCB
 - 32 ch input, MMCX
 - RJ45 and power connector
- uMB: Muon management board, 1 pc for 24 uFBs
 - Up to 24 RJ45 connectors, CAT6 shielded cable (5mm diameter, up to 2.5 meters) to uMB
 - Fiber to backend
 - Power input (AWG16 x4), 48V

Endcap quadrant



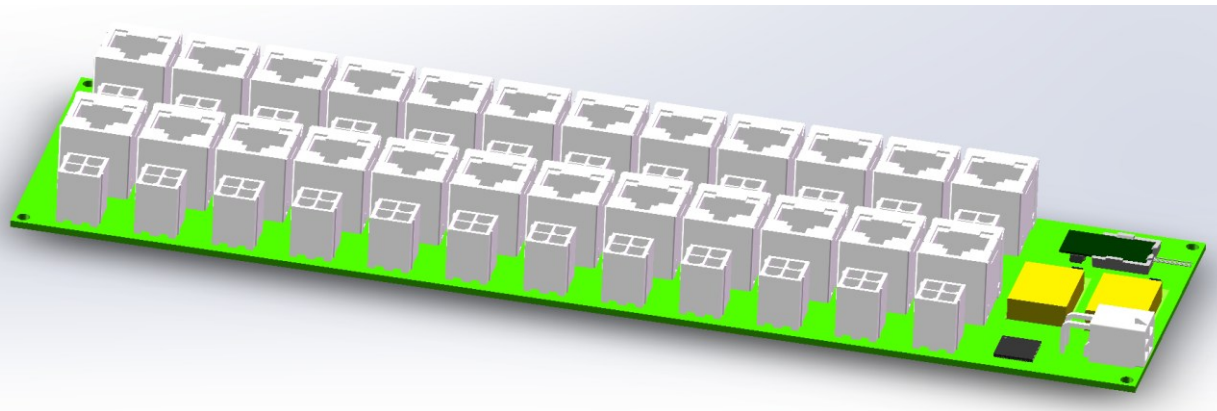
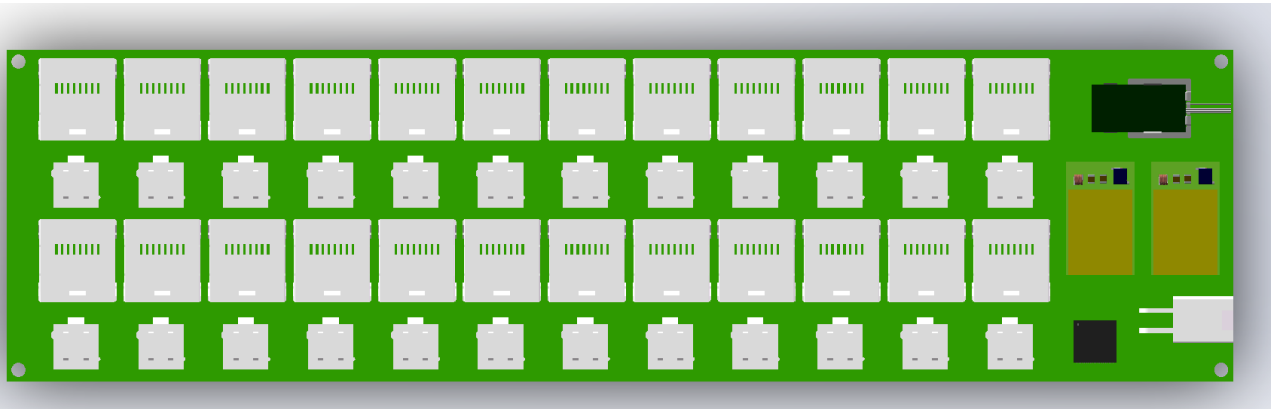
		M (uSiPM)	N (uFB)		O (uMB)
		ch	32-ch TDC board	Raw data rate / bps	Management board
Inner	layer	71	4	-	-
	quadrant	852	48	276.5 M	2
	endcap	3408	192	3.32 G	8
	Total	6816	384	6.64 G	16
Outer	layer	127	4	-	-
	quadrant	1524	48	737.3 M	2
	endcap	6096	192	2.95 G	8
	Total	12192	384	5.90 G	16

uFB (Muon front-end board)



- 60 mm x 40 mm FR4 PCB
- Front-end Interface
 - 32-ch input, MMCX to SiPM
 - 2 mm diameter coaxial cable
- Back-end Interface
 - RJ45 connector to uMB
 - 5 mm diameter CAT6 shielded cable
 - Mini-Fit Jr (Power) to back-end
 - AWG 18
- Chip
 - Chomin, ADC+TDC
- DC/DC with shielding and filters
 - 1.2V output
- 3D step file:
 - <https://ihepbox.ihep.ac.cn/ihepbox/index.php/s/g365tprrrMhNDxs3>

uMB (Muon management board)



- 260 mm x 70 mm FR4 PCB
- Front-end Interface
 - 24-ch RJ45 connector to uMB
 - 5 mm diameter CAT6 shielded cable
 - 24-ch Mini-Fit Jr (Power) to uMB
 - AWG 18
- Back-end Interface
 - Fiber
 - 1.1 mm diameter
 - Mini-Fit Jr (Power) to back-end
 - AWG 16 (2.35mm)
- Chips
 - TaoTie, ChiTu, KinWoo
- DC/DC with shielding and filters
 - 2.5V output
 - 1.2V output
- 3D step file:
 - <https://ihepbox.ihep.ac.cn/ihepbox/index.php/s/liyBhv4ApmZs8Bx>

Back-end cables

■ Fiber

- 1.1 mm diameter
- Quantity: 80

■ Power

- AWG 16 (2.35mm)
- Quantity: 80 x 4

Bandwidth requirement

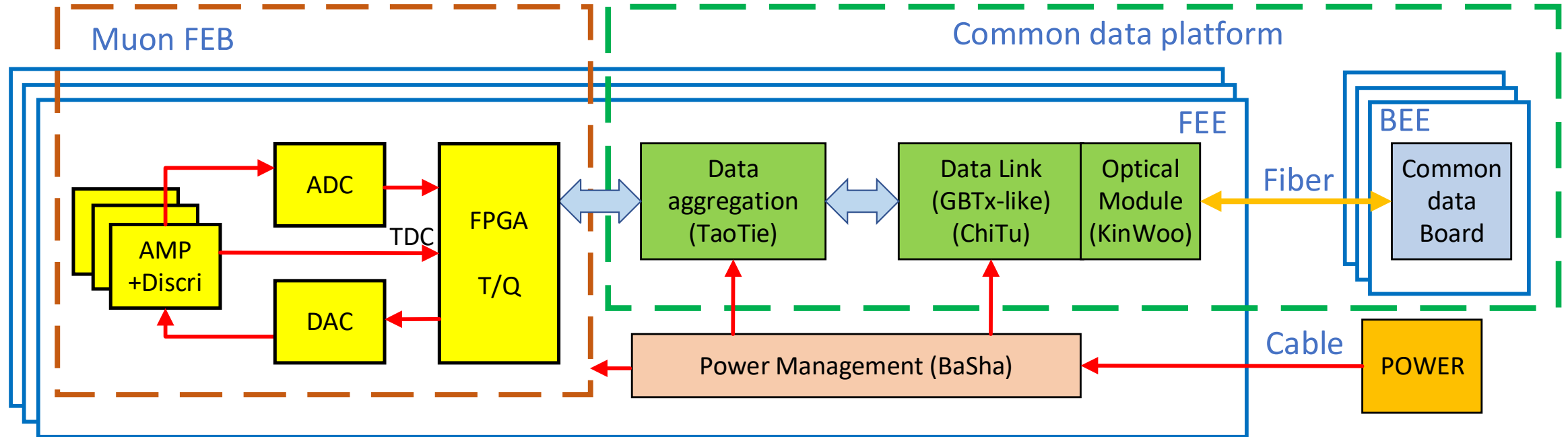
Muon	Readout Channel	Hit rate/Hz (preliminary worst case)	Data format	Raw data rate / Gbps
Barrel	26064	10 k	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	11.51
Inner endcaps	6816	10k~100 k, Average 20 k		6.64
Outer endcaps	12192	10 k		5.90
Total	~45 k			~24.04

bandwidth requirement

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	42bit (9b X+7b Y +14b BX + 6b TOT + 5TDC + 1b polarity)	32bit (10b chn ID + 10b BX + 6b TOT + 5b chip ID)	40~48bit (7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID)		48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg: 2.9Mbps/chip Max: 3.85Mbps/chip	Avg: 38.8Mbps/chip Max: 452.7Mbps/chip	~70Mbps/module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 Module 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)	Needs detector finalization	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	Needs detector finalization	Avg. 15.36 Mbps/chip Max. 153.6 Mbps/chip
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	<=24:1 @ O (368.7 Mbps)
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization	~ 24.04 Gbps

Backup

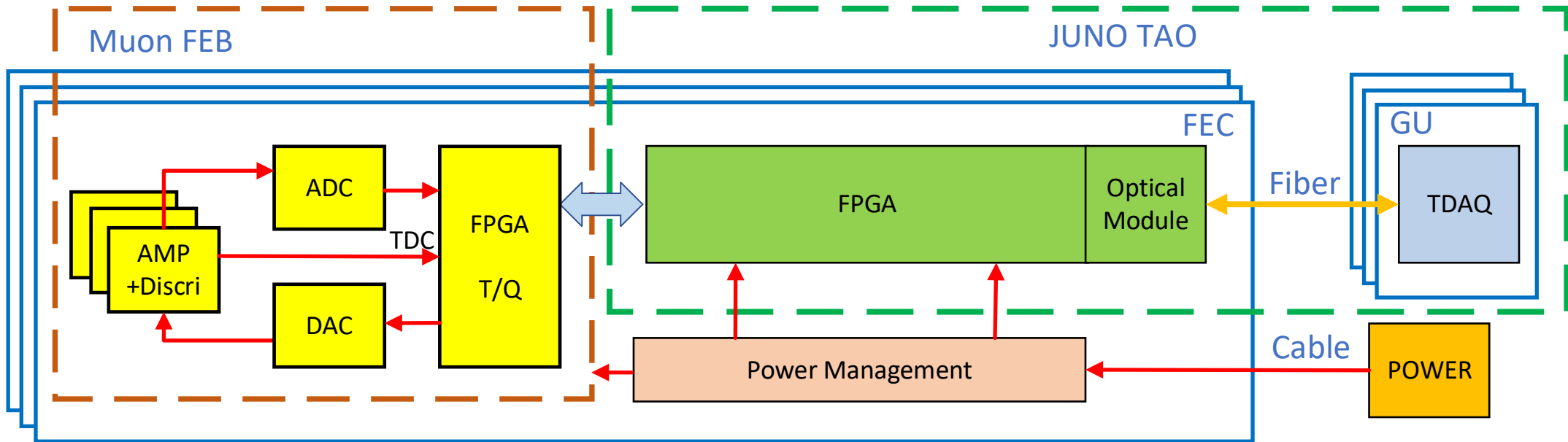
Alternative: discrete device scheme



■ FEB (Front-end Electronics Board)

- Commercial chips with radiation tolerance based on past studies for particle physics experiments
- FPGA based TDC for TOA and TOT measurement with ~ 1 ns time resolution
- ADC for charge measurement or TOT calibration
- DAC for threshold setting or SiPM bias voltage adjustment

Near-term test environment



- Reuse JUNO-TAO electronics for readout, clock synchronization and TDAQ
 - To accelerate the development schedule

Considerations of the backgrounds

- Very low level of the CR backgrounds, with the earth shield of > 50m.
- Reference to the beam backgrounds in Belle II.

Barrel Layer	Expected Hit Rate (Hz/cm ²)	Expected RPC Efficiency	Bad-case Hit Rate (Hz/cm ²)	Bad-case RPC Efficiency	Worst-case Hit Rate (Hz/cm ²)	Worst-case RPC Efficiency
0	—scintillators—		—scintillators—		—scintillators—	
1	—scintillators—		—scintillators—		—scintillators—	
2	2.6	0.86	26	0.00	260	0.00
3	1.7	0.91	17	0.14	170	0.00
4	0.9	0.95	9	0.54	90	0.00
5	0.5	0.97	5	0.54	50	0.00
6	0.5	0.97	5	0.54	50	0.00
7	0.3	0.98	3	0.84	30	0.00
8	0.5	0.97	5	0.54	50	0.00
9	0.2	0.98	2	0.89	20	0.00
10	0.2	0.98	2	0.89	20	0.00
11	0.1	0.99	1	0.94	10	0.49
12	0.1	0.99	1	0.94	10	0.49
13	0.1	0.99	1	0.94	10	0.49
14	0.2	0.98	1	0.94	10	0.49

Table 2: Neutron flux, hit rate per unit area, and instantaneous efficiency in each layer of the barrel KLM from the late-2020 simulations of beam-induced neutron backgrounds at the SuperKEKB design luminosity of $6 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$. Here, the Belle II hybrid configuration replaces the RPCs in the two innermost layers with scintillators and neutron-absorbing polyethylene sheets.

For a 4m long bar, the hit rate might be 160Hz. For the ‘bad-case’, it would be 1.6kHz!

