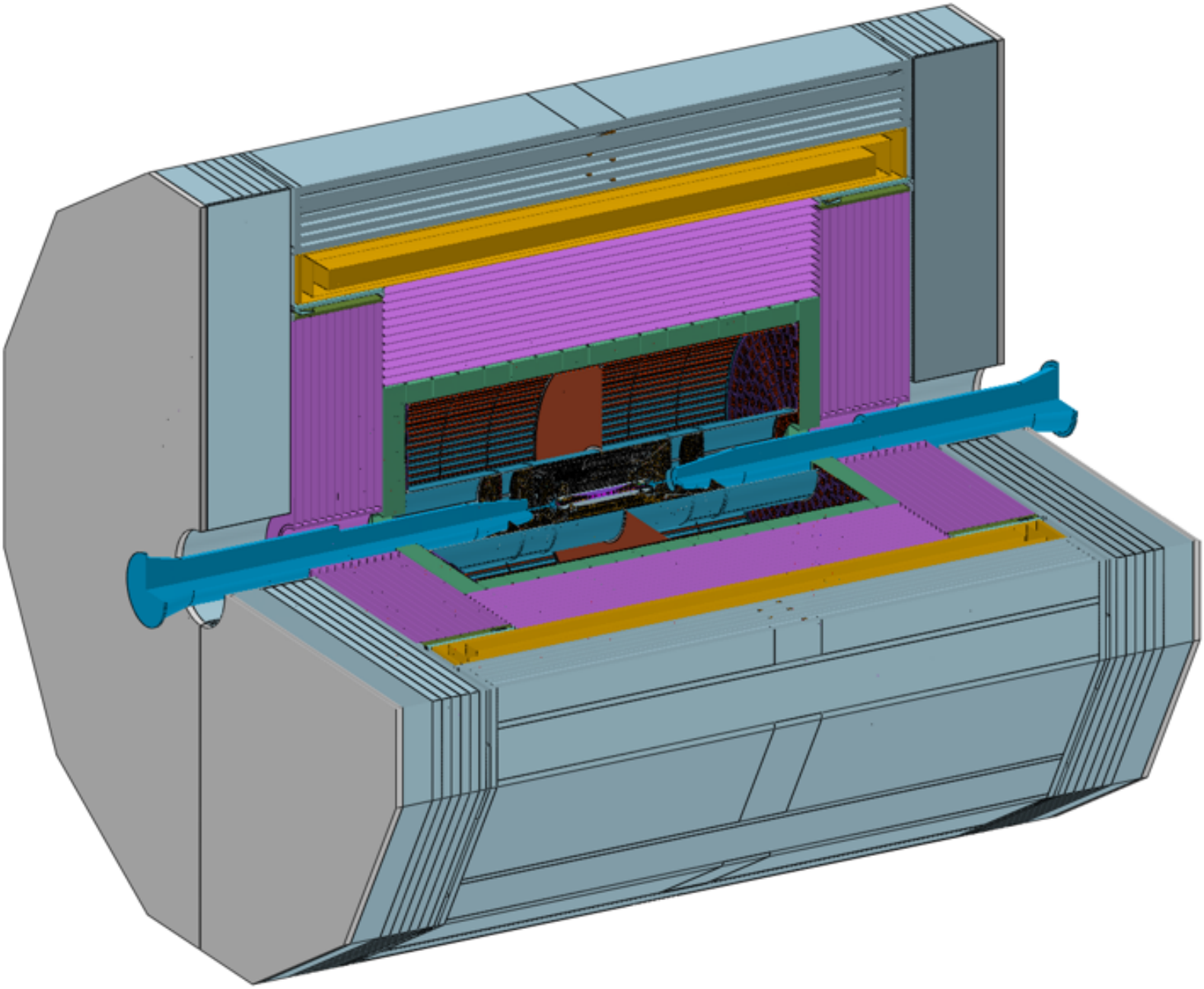

Technical Design Report of the CEPC Reference Detector

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Date: June 9, 2025

Version: 0.1

Bio: Information

Contents

Chapter 5 Silicon Trackers

Responsible person: Qi YAN, ...

The CEPC Silicon Tracker, positioned outside the Vertex detector, consists of the Inner Silicon Tracker (ITK) and the Outer Silicon Tracker (OTK). The ITK and OTK are separated by the Time Projection Chamber (TPC). The ITK utilizes advanced CMOS sensor technology to achieve precise position measurements for accurate particle trajectory determination. In addition to position measurement, the OTK integrates AC-LGAD semiconductor detectors for precise time measurement of charged particles, significantly enhancing particle identification capabilities ...

5.1 Requirements

Responsible person: Qi YAN, Gang LI, ...

The CEPC is designed to operate across a wide energy region, including Z-pole (91 GeV), W^+W^- threshold (160 GeV), the energy maximizing ZH production (240 GeV), and $t\bar{t}$ threshold after upgrade (360 GeV). In High Lumi Z mode, the luminosity reaches $\mathcal{L} = 115 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 30 MW ($192 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 50 MW), with a 23 ns interval between bunch crossings. The stringent requirements of both physics and operational conditions impose high demands on the CEPC tracking system.

5.1.1 Physics requirements

The CEPC tracking system must provides broad precision momemtum measurements up to 100 GeV and beyond, enabling the detection of high-momentum isolated tracks such as leptons for Higgs and electroweak physics, as well as moderate- and low-momentum tracks within jets.

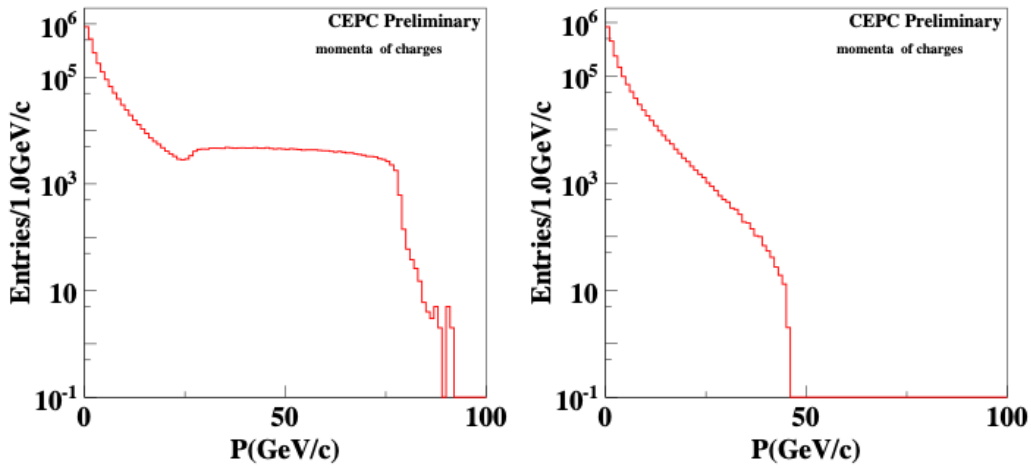


Figure 5.1: Momentum distributions of $e^+e^- \to ZH \to \mu^+\mu^- H$, $H \to$ anything (the left panel) and $e^+e^- \to Z \to$ hadrons (the right panel).

For instance, in Higgs and electroweak physics studies, the golden channels $e^+e^- \to ZH \to \mu^+\mu^- H$ (with $H \to$ anything) and $e^+e^- \to Z \to$ hadrons serve as prime examples. The momentum distributions of these tracks are illustrated in Fig. 5.1. For the process $e^+e^- \to ZH \to \mu^+\mu^- H$ (with $H \to$ anything), the muons' momenta must fall within the range of 20 to 80 GeV at a beam center-of-mass energy of 240 GeV. A straightforward calculation reveals that to achieve a precision of a few MeVs in Higgs mass measurement, based on an integrated luminosity of 20 ab^{-1}, the muons' momenta must be determined with an accuracy at the permille level.

For flavor physics, the precise reconstruction of B and D hadrons, with masses on the order of GeV, requires achieving a high signal-to-noise ratio and excellent mass resolution, typically a few MeV. This level of precision demands

a momentum resolution better than 1 permille, along with accurate trajectory determination for vertex reconstruction and effective particle identification (PID) of their decay products (e.g., K/π/p). These capabilities are critical for distinguishing between different decay channels and reducing backgrounds in measurements. To meet these stringent requirements, advanced detector technologies must be employed, including high-resolution tracking system to measure the trajectories of decay products with exceptional spatial and curvature precision, as well as precise Time-of-Flight (TOF) or dN/dx (ionization cluster counting) detectors to effectively separate decay products. Accurate measurement of the properties of these hadrons is essential for testing the predictions of the Standard Model and exploring new physics beyond it.

In flavor physics studies and jet substructure analysis, beside the determination of primary and secondary vertices using high spatial resolution tracking system, particle identification of decay products is vital in suppressing combinatorial backgrounds, distinguishing between particles with similar topologies, and providing additional information for flavor tagging of hadrons and jets (b or c). For PID, both dN/dx and TOF are indispensable techniques for achieving the necessary precision. The dN/dx method determines the number of ionization clusters produced by a charged particle as it traverses a gaseous detector. This technique will be elaborated upon in the chapter on the Gaseous Tracker. Time-of-Flight, another fundamental technique in PID, measures the time for a particle to travel a specific distance. TOF, which will be discussed in this chapter, requires both high time resolution and a sufficiently long path length. Combining with the dN/dx technique, it significantly enhances particle identification capabilities.

To summarized the physics requirements discussed:

- **Excellent momentum resolution** at permille level or better, which ensure achieving mass resolutions of few MeV for Higgs mass measurement via $e^+e^- \to l^+l^-$H, and for beauty and charm hadrons with masses of a few GeV in flavor physics studies.
- **Excellent impact parameter measurement** to a few microns for charged tracks, enabling precise primary and secondary vertex reconstruction. This is essential for effective jet flavor tagging and high reconstruction efficiency of long-lived beauty and charm hadrons, which are critical for flavor physics studies.
- **Excellent particle identification** for flavor physics and jet substructure related physics.
- The tracker, along with the entire detector, provides nearly 100% solid angle coverage of the interaction point. This not only provides high detection efficiency for collision events, but also enhances sensitivity to many new physics searches, such as invisible decay searches in Higgs decays via $e^+e^- \to f\bar{f}$H.

5.1.2 Specific requirements on Silicon Tracker

To enable precise measurements of Higgs properties and other key physics objectives, CEPC requires an overall track momentum resolution at the permille level or better for momenta below 100 GeV/c. The primary goal of the Silicon Tracker is to precisely meausre momentum of the particles. Together with the Vertex detector, the Silicon Tracker also identifies primary and secondary vertices for tagging long-lived objects like b or c quarks, and τ-leptons.

Among all the tracker system in CEPC (Vertex, Silicon Tracker, and TPC), the Silicon Tracker spans the largest lever arm with high intrinsic spatial resolution for accurate trajecotry determination of charge particles. The basline design of the CEPC Inner Silicon Tracker (ITK) includes 3 barrel layers and 4 endcap layers, while the basline design of the Outer Silicon Tracker (OTK) consists of 1 barrel layer and 1 endcap layer. From the innermost barrel layer of the ITK to the OTK, the bending lever arm is $\sim$1.6 meters. Each detector layer is required to achieve a spatial resolution of 10 microns or better in the particle bending direction, while the material thickness needs to be minimized to reduce multiple scattering, which is essential for low momentum resolution. The material budget should be below $1\%\mathrm{X}_0$ per tracker layer.

In Z-pole mode, the high luminosity with a 23-nanosecond gap between successive bunch crossings necessitates that the detector can distinguish between adjacent bunch crossings, requiring a timing resolution better than a few nanoseconds. Additionally, effective particle identification (PID) is crucial for distinguishing between various particle types, supporting the CEPC's flavor physics studies and the measurement of jet substructure. This can be achieved through time-of-flight (TOF) measurements with a time precision of $\sim$50 ps in the OTK, enabling robust PID for K/π/p seperation below a few GeV/c momentum range.

5.2 Overview of ITK and OTK

Responsible person: Qi YAN, Gang LI, ...

In the realm of high-energy physics, the design of track detectors plays a crucial role in the accurate measurement and identification of particle trajectories. This section delves into the intricacies of the inner and outer trackers, which are integral components of such detectors, particularly focusing on silicon trackers.

The inner tracker (ITK)is located outside the vertex detector and inside the Time Projection Chamber (TPC) and consists 3 barrel layers and 4 end-cap layers, as shown in Fig. 5.2 and Tab. 5.1, covering a relatively large area $\sim$20 m^2, while the Outer Tracker (OTK) lies in the outermost of the whole tracker system, providing precision both spatial and time measurements. The total area of the OTK is up to 70 m^2.

Detector		**Radius R [mm]**		**$\pm z$ [mm]**	**Material budget [X_0]**
ITK Barrel	Layer 1	153		371.3	0.65%
	Layer 2	300		664.9	0.65%
	Layer 3	564		664.9	0.65%
OTK Barrel	Layer 4	1811		2900	0.65%
		R_{in}	R_{out}		
	Disk 1	81.5	242.5	506.5	0.50%
	Disk 2	110.5	352.3	719.7	0.50%
ITK End-cap	Disk 3	163	564	1,001.5	0.65%
	Disk 4	2223	564	1,500	0.65%
OTK End-cap	Disk 5	419.3	1,810	2,930	0.65%

Table 5.1: Parameters and layout of the CEPC silicon tracker. Silicon pixel sensors (HV-CMOS) and LGAD technologies are planned for the inner tracker and outer tracker baseline, respectively, while silicon microstrip sensors are envisioned as backup for both. The column labelled $\pm z$ shows the length of the barrel layers, and the z position of the end-cap disks.

The silicon tracker detectors provide high-precision position measurements and a large lever arm, which are essential for determining the trajectory of particles with high accuracy. On the other hand, the Time Projection Chamber (TPC) gas detectors offer continuous multi-point measurements and particle identification capabilities, which are vital for distinguishing between different types of particles.

The discussion begins with the barrel end-cap ratio considerations. After careful deliberation, a design with an R_{max} of 1.8 meters and a half-z of 2.9 meters are chosen for the barrel. This choice ensures a larger coverage in polar angle for the barrel, enhancing the detector's ability to capture a broader range of particle trajectories.

Moving on to the end-cap region, also known as the forward region, the design incorporates four layers of ITK and one layer of OTK. This configuration is chosen to maximize the precision of momentum measurements in the forward region, where the lever arm is relatively small. Consequently, all measurement points in this region are high-precision silicon tracker detectors, ensuring the most accurate data capture.

Finally, it is important to note that all designs have undergone optimization processes to ensure the most efficient and effective performance. This optimization is critical in achieving the desired balance between precision, coverage, and the overall functionality of the detectors.

In summary, the inner and outer trackers are meticulously designed to work in tandem, leveraging the strengths of both silicon and gas detectors to provide comprehensive and accurate measurements in high-energy physics experiments.

5.2.1 Technology Options and Boundary Conditions

The optimization of the inner and outer trackers is predicated on a set of technology options and boundary conditions that define the operational parameters and constraints of the detectors.

- Spatial measurement precision: The detectors must achieve high precision in position measurements to ensure the accurate tracking of particle trajectories, which is fundamental for data analysis in high-energy physics experiments.

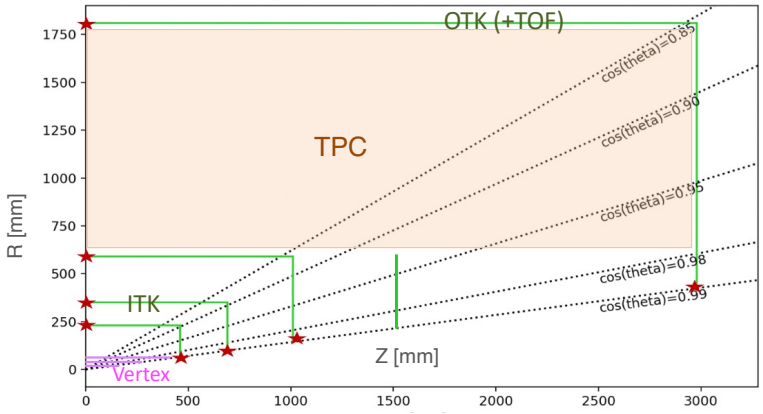


Figure 5.2: The layout of the CEPC tracker system.

- Total material budget: The optimization considers the material budget of the detectors and their auxiliary components to minimize interactions that could affect the measurements, thus preserving the detectors' sensitivity and radiation tolerance.
- Material distribution: The distribution of material at measurement points is optimized to balance structural integrity with minimal interference in the particle detection process.
- TPC and Vertex Detector: The TPC and vertex detector are optimized separately but serve as boundary conditions for the inner and outer tracker optimization, influencing the overall design and performance.
- Backgrounds asscociated the accelerator.
- Overall cost of the detector system.

5.2.2 Optimization Tools

The Lic Toy (LDT) optimization tool is employed to facilitate the complex process of balancing various design parameters and constraints. The LDT is a software tool designed to model and optimize the layout of detectors, taking into account physical constraints, performance metrics, and material budget. This tool is used to simulate different configurations of the inner and outer trackers, allowing for the assessment of their impact on position measurement precision and overall detector performance.

5.2.3 Layout Optimization

The layout optimization phase involves the strategic placement and configuration of detector layers to achieve the best possible performance within the given constraints.

5.2.3.1 The tracker length

5.2.3.2 Barrel Region

The optimization of the TPC's inner radius and the layering and positioning of the inner tracker within the barrel region are crucial for achieving the desired coverage and performance without exceeding the material budget.

The TPC inner radius

The positions of ITK layers

The spatial resolution requirement on the OTK

5.2.3.3 End-cap Region

In the forward region, where the lever arm is smaller, the optimization focuses on enhancing position measurement precision, the number of detector layers, and the distribution structure to ensure high accuracy.

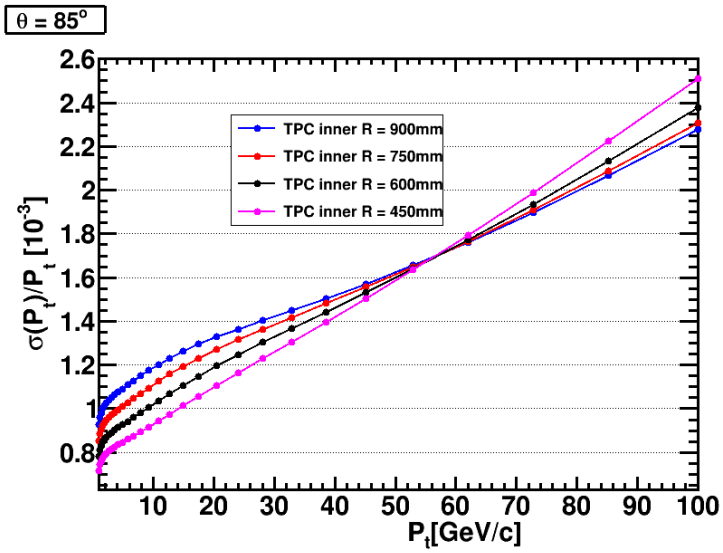


Figure 5.3: The volume of time projection chamber: position of the inner wall.

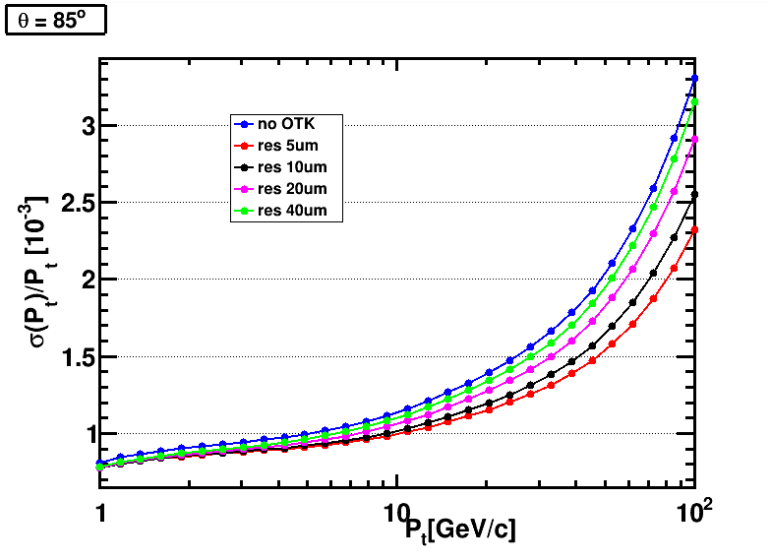


Figure 5.4: Options of OTK: different spatial resolution

The number of layers and their positions of ITK layers

5.2.4 Summary and discussion on tracker system layout

The integrated optimization of the inner and outer trackers is a critical component of the high-energy physics detector system. By systematically addressing technology options, employing optimization tools like Lic Toy, and focusing on layout optimization, the design team can achieve a layout that meets the performance metrics and ensures the robustness of the detectors. This framework will be further detailed with diagrams and tables to provide a comprehensive view of the optimization process and its outcomes.

5.3 Inner silicon tracker (ITK)

Responsible person: Qi YAN

The Inner Silicon Tracker (ITK) is located outside the vertex detector and consists 3 barrel layers and 4 endcap layers, as shown in Fig. 5.2, covering a relatively large area $\sim$20 m^2. The spatial resolution of ITK should be comparable to

that of the vertex detector. To accurately match tracks with their corresponding bunches and minimize pipe-up events, the CEPC ITK requires a high time resolution on the order of a few nanoseconds, which is significantly better than the vertex detector.

This section provides a detailed description of the CEPC ITK. Subsection 5.3.1 outlines the CMOS chip R&D efforts, including the development of HV-CMOS pixel sensor and CMOS strip sensor. The baseline and alternative designs for the CEPC ITK are presented in Subsection 5.3.2. Subsection 5.3.3 introduces the ITK readout electronics, while Subsection 5.3.4 discusses the ITK mechanical and cooling design. Finally, Subsection 5.3.5 covers the prospects and plans for the ITK.

5.3.1 CMOS chip R&D

5.3.1.1 HV-CMOS pixel R&D

Responsible person: Yiming LI, Yang ZHOU

5.3.1.1.1 Technology survery for silicon pixel detectors Hybrid pixels vs MAPS

Pixel detectors are essential for high-energy physics experiments, and two prominent technologies dominate this field: Hybrid Pixel Detectors and Monolithic Active Pixel Sensors (MAPS). Both approaches have distinct design principles, strengths, and challenges, making them suitable for different applications.

Hybrid pixel detectors consist of separate silicon sensor layers and readout electronics chips, interconnected via bump bonding. This separation allows independent optimization of the sensor and electronics, enabling exceptional radiation tolerance and high-speed timing performance. These detectors have been widely deployed in high-radiation environments, such as the ATLAS and CMS experiments at the LHC. However, the reliance on bump bonding increases the material budget and production complexity, making hybrid pixel detectors expensive and less scalable for large areas. Additionally, their higher power consumption requires advanced heat management systems.

In contrast, MAPS integrate the sensor and readout electronics on a single silicon substrate, simplifying fabrication and drastically reducing material usage. Fabricated using standard CMOS technology, MAPS are cost-effective and highly scalable. Their compact design and low material budget make them ideal for precision tracking at the CEPC inner tracker.

HVCMOS and its advantages

Historically, MAPS faced limitations in radiation tolerance and timing resolution due to shallow depletion regions and slower charge collection. However, modern innovations such as high-voltage CMOS (HV-CMOS) have significantly improved their performance, bridging the gap with hybrid pixel detectors in radiation hardness and charge collection efficiency.

Table 5.2: Summary of Key Differences

Aspect	Hybrid pixel detectors	Monolithic Active Pixel Sensors
Material Budget	High	Low
Radiation Tolerance	Excellent	Improving with HV-CMOS
Fabrication Complexity	High	Low
Timing Performance	Excellent	Moderate
Cost	Expensive	Cost-effective

Hybrid pixel detectors excel in high-radiation, high-rate environments but come with higher material budgets and production complexity. MAPS, on the other hand, offer a lightweight and cost-effective solution, especially for applications requiring large-scale deployment. Emerging technologies such as HV-CMOS have made MAPS increasingly competitive, presenting a promising choice for CEPC.

5.3.1.1.2 Development of HVCMOS pixel sensor for CEPC

The evolution of High-Voltage CMOS (HVCMOS) pixel detectors began with their application in high-energy physics experiments to address the need for precise tracking, high radiation tolerance, and reduced material budgets. Early developments in the 2000s explored the use of CMOS

technologies to integrate sensing and readout electronics on a single substrate. The incorporation of deep n-well structures in HV-CMOS sensors marked a significant advancement, enabling larger depletion volumes for efficient charge collection and enhanced radiation hardness.

Most HVCMOS sensors in high energy physics utilize 180 nm and 150 nm CMOS processes, providing a strong foundation for integrating sensor and signal-processing capabilities. These designs were successfully deployed in experiments like Mu3e and served as prototypes for further optimization. For early development of the CEPC tracker, module design and prototyping are based on ATLASPix3 sensor chip [**atlaspix3**], which is a full-size full-functioning chip with pixel size or $50\,\mu\text{m} \times 150\,\mu\text{m}$ and reticle size of $2\,\text{cm} \times 2\,\text{cm}$. For the ultimate requirement of CEPC inner tracker, better spatial resolution in the bending plane and better timing resolution is required.

To achieve the CEPC requirements, development of HVCMOS sensors in smaller feature size of 55 nm was launched [**coffee1**], mainly driven by two reasons. First of all smaller feature size has the potential for better performance as in the same area more functionalities can be accommodated with reduced power especially for the digital circuit. Equally important is the reliability of the process. As the most advanced processes in industry always leads the high energy physics application by one or two decades, the processes used at R&D phase might not be available during mass production. Therefore it is more secure to start with more advanced processes. This is a general trend also for MAPS development using CIS process migrating from 180 nm to 65 nm process, and front-end electronics even further to 28 nm processes. Two prototype COFFEE1 and COFFEE2 were designed and submitted in MPWs in 55 nm processes, with COFFEE2 the first sensor prototype in 55 nm HVCMOS process.

5.3.1.1.3 COFFEE1 The COFFEE1 chip is fabricated in 55nm Low-Leakage process in an MPW in 2022. This is not a High-Voltage process but has a similar deep n-well structure underneath the electronics which could serve as a large electrode, as illustrated in the right part of Fig. 5.5. The default wafers with low resistivity of a few $\Omega \cdot cm$ are used.

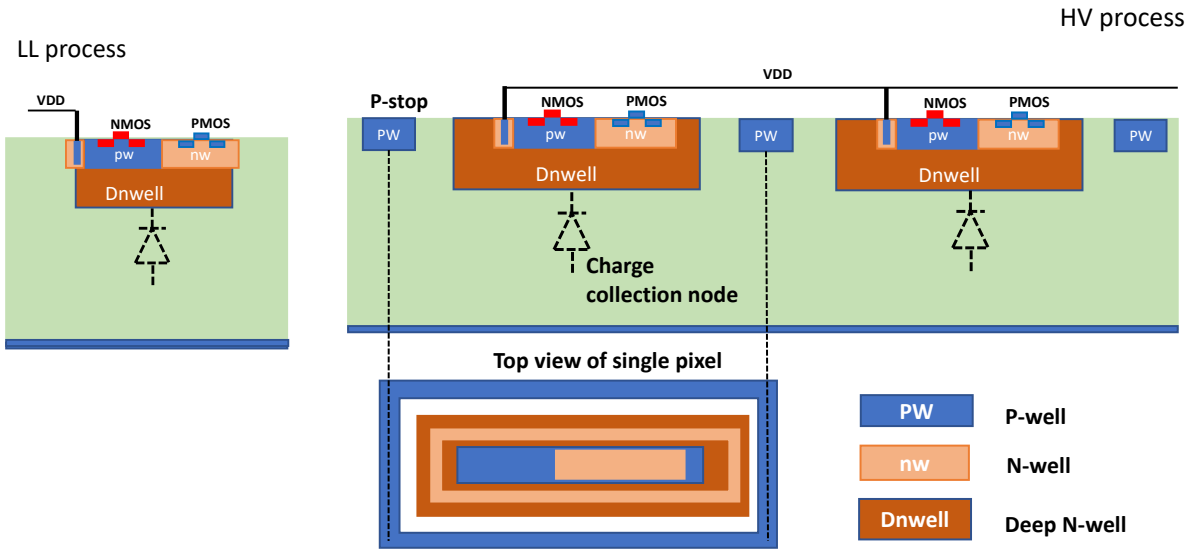


Figure 5.5: Cross-section of the 55nm Low-Leakage (left) and High-Voltage CMOS (right) processes.

The COFFEE1 floorplan is shown in Fig. 5.6. It has an area of $3\,\text{mm} \times 2\,\text{mm}$, with twelve different variations of passive diode sensor arrays. Each array has 4×3 pixels. The design variations are:

- Pixel area $25 \times 150\,\mu\text{m}^2$ or $50 \times 150\,\mu\text{m}^2$;
- With or without p-stop between pixels;
- Gap of $5\,\mu\text{m}$, $10\,\mu\text{m}$ or $15\,\mu\text{m}$ between neighbouring deep n-well.

Note that all dimensions quoted are designed value, while the actual size is scaled down by a factor of 0.85 for the 55nm processes used. A pixel size of $50 \times 150\,\mu\mathrm{m}^2$ is chosen to be similar as existing chips for LHC upgrade purpose. For the tracking detector at CEPC better spatial resolution is required in order to achieve desired momentum resolution, so smaller pixels of $25 \times 150\,\mu\mathrm{m}^2$ are designed.

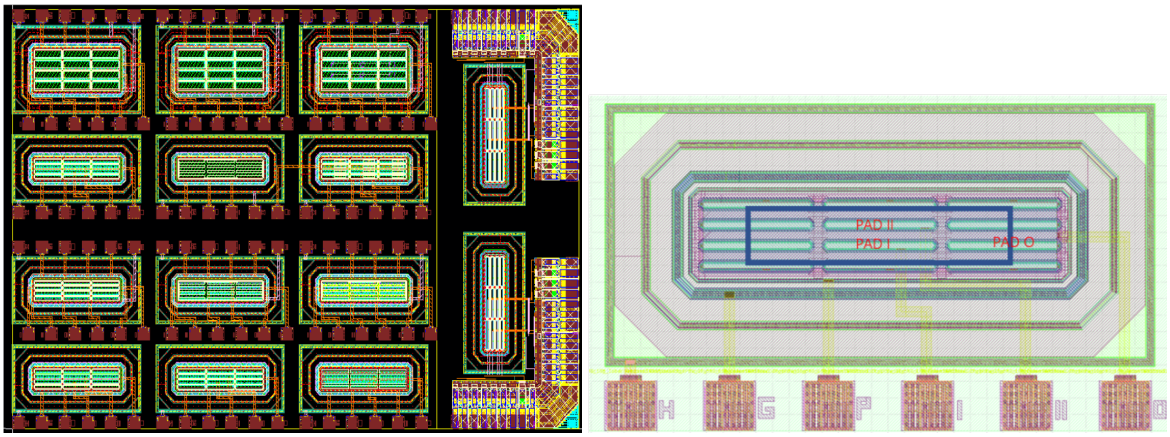


Figure 5.6: (Left) COFFEE1 floorplan and (right) the structure of a 12-pixel diode array. The blue line indicates ten interconnected pixels in the array.

A typical array is shown in Fig. 5.6 (right). The middle two pixels can be read out individually, while the 10 pixels surrounding them are connected. The current-voltage curves for a single pixel or the 10 connected pixels are shown in Fig. 5.7. The breakdown voltage is around $-9\,\mathrm{V}$. The leakage current is as low as pA level before breakdown is reached.

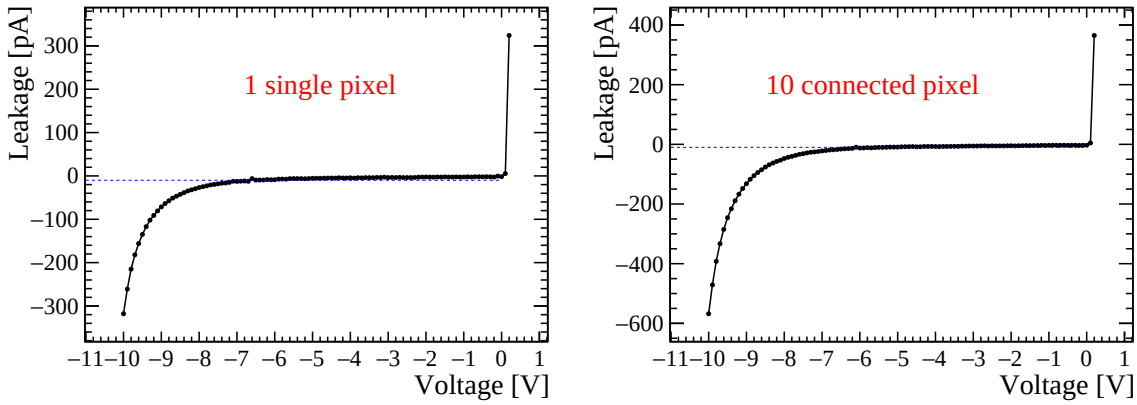


Figure 5.7: The IV curves of (left) a single pixel and (right) 10 connected pixels on COFFEE1.

The capacitance-voltage curves of a single pixel or 10 pixels are shown in Fig. 5.8. With offset subtracted, the capacitance of a single pixel of $25 \times 150\,\mu\mathrm{m}^2$ is in the range of $150 \sim 200\,\mathrm{fF}$ at the bias of $-9\,\mathrm{V}$, depending on the gaps between adjacent pixels.

As windows are left open in the metal layer for all diode arrays, we can use laser to study the signal response in the sensor when biased. The setup is illustrated in Fig. 5.9. A red laser with spot size around 0.5 mm is used. Ten connected pixels as shown in Fig. 5.6 are read out using an external charge sensitive preamplifier-shaper chip, IDE1140mounted on a custom-made readout board. The signal generated by the red laser is clearly visible comparing to the pedestal as shown in Fig. 5.9. The gain of the readout system is calibrated using other dedicated sensors and input sources, yielding one count of ADC corresponding to input charge of $\sim 87\,e^-$. Therefore the signal of 28 ADC counts in COFFEE1 indicates a total amount of $\sim 2400\,e^-$ charge collected. The noise level of the readout system increases from 2.1 ADC to 3.8 ADC after connecting to the testing diode on COFFEE1, including contribution from noise in the sensor diode, the capacitance introduced by the connection and the instability of the laser. The frame rate capability of the readout system is estimated

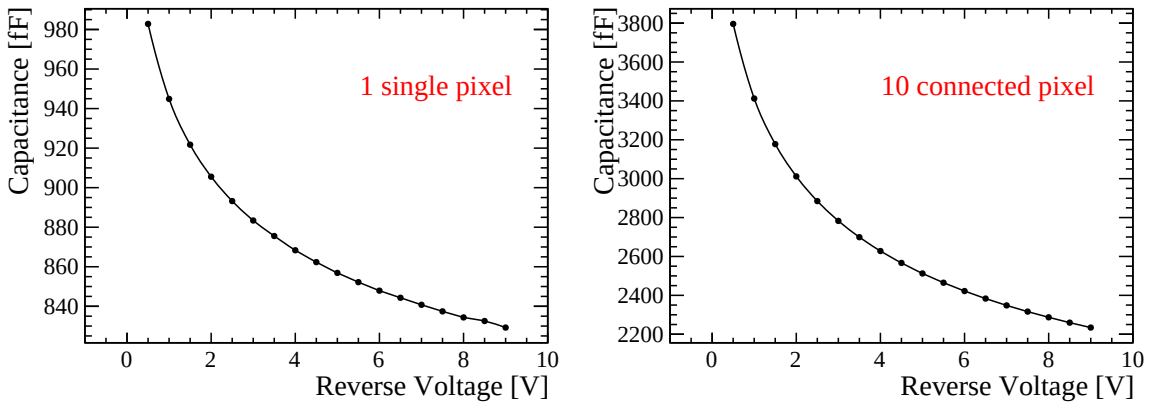


Figure 5.8: The CV curves of (left) a single pixel and (right) 10 connected pixels on COFFEE1.

to be above 10 kHz, and the trigger rate was set to 500 Hz when performing the laser test to ensure there is no spill-over.

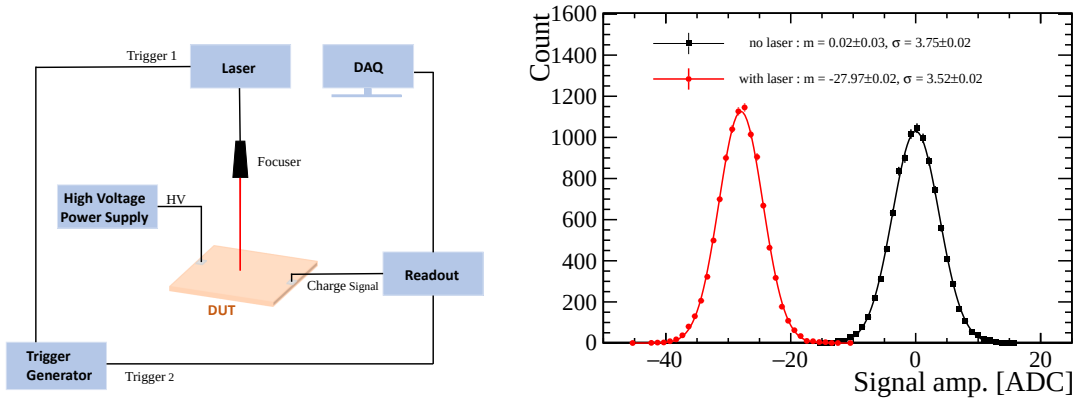


Figure 5.9: Setup for laser test and signal generated in COFFEE1.

5.3.1.1.4 COFFEE2 With the experience accumulated with COFFEE1, a first proof-of-principle sensor chip in 55nm HVCMOS process, COFFEE2, was submitted designed and tested. The cross-section of the HVCMOS process is illustrated in Fig. 5.5. The process is a triple-well process, namely n-, p- and deep n-wells are available. Up to ten metal layers can be used for fine pitch routing, including two thick metal layers for power. In this MPW six metal layers are used including a thick metal layer for power lines.

The floorplan and a photo of the COFFEE2 chip are shown in Fig. 5.10. The chip has an area of $4\,\mathrm{mm} \times 3\,\mathrm{mm}$.[1] There are three sections of different design purpose.

Section labelled "1" has a 32×20 pixel matrix with in-pixel circuit. Section "2" consists of passive diode arrays similar to COFFEE1. Pixels in both sections 1 and 2 have the same pixel sizes. Section "3" is designed for imaging application with small pixels not directly relevant to the CEPC use case. The initial plan was to have pixels of $25 \times 150\ \mu\mathrm{m}^2$ as the smaller pixels in COFFEE1; However this would be extremely challenging in the narrower side as a few micrometer of clearance has to be kept from the edge of the deep n-well, leaving no more than $10\ \mu\mathrm{m}$ in one side for the circuit. Therefore we adopted a less elongated pixel shape while keeping a similar pixel area, yielding a pixel size of $40 \times 80\ \mu\mathrm{m}^2$. The schematic design of in-pixel electronics in Section "1" is shown in Fig. 5.11. A pixel consists of a charge-sensitive preamplifier (CSA) connected to the front-end collection electrode through AC coupling, a comparator via another AC coupling stage is connected to the output stage of the CSA. This arrangement ensures the transmission of the analog signal while isolating the different stages electrically. Only one pixel in the array can be read out at a time when the `column_select` and `row_select` are both selected. The variations in diode or in-pixel electronics in Section "1" include:

[1] All designed values are scaled down by a factor of 0.9.

- Gaps between neighbouring deep n-well are 10, 15 or 20 μm;
- With or without p-stop between pixels;
- Pixels with only amplifiers or with both amplifiers and comparators;
- By default the comparators are implemented using both PMOS and NMOS, and in the left 4 columns comparators using only NMOS are designed. The NMOS-only design is aimed at mitigating possible crosstalk between deep n-well and n-well.

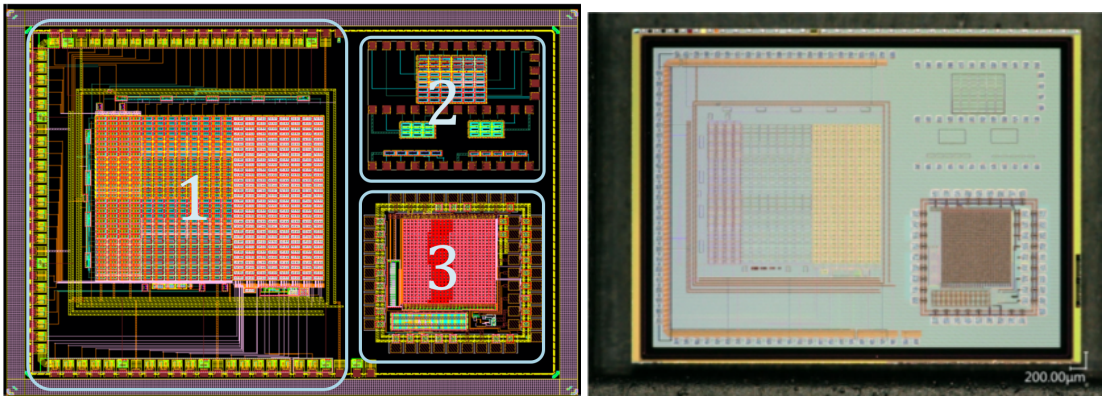


Figure 5.10: COFFEE2 floorplan and photo.

The IV curve of a typical diode in section 2 is shown in Fig. 5.12. The breakdown voltage can be as large as $-70\,\mathrm{V}$. The increase of breakdown voltage of COFFEE2 with respect to COFFEE1 is due to the different CMOS process. The sudden increase of current beyond breakdown voltage may imply that the breakdown happens at the edge of the deep n-well. This is consistent with the TCAD simulation also shown in Fig. 5.12. Simulation also demonstrates that the breakdown voltage can be significantly increased by using high-resistivity wafers. The leakage current is at a few pA level at low bias.

The capacitance as a function of bias voltage is shown in Fig. 5.13 for a single pixel and for 8 connected pixels. Full depletion is not reached when breakdown happens. The capacitance should be proportional to pixel area; however offset exists due to various reasons, for instance the parasitic capacitance of metal routing. We take the derivative of the CV curves and extract the ratio of 8-pixel versus a single pixel to eliminate the offset, and the ratio agrees well with eight, the ratio of their area, as shown in Fig. 5.13. The raw capacitance of a single pixel at $-70\,V$ is $\sim 200\,\mathrm{fFm}$, which becomes $30 \sim 40\,\mathrm{fFm}$ after subtracting the offset.

The test setup for region "1", namely sensors with in-pixel circuit, is shown in Fig. 5.14. A dedicated carrier board is design and fabricated, which is connected to the general-purpose Control and Readout (CaR) board [**CaRsystem**], a Xilinx KC705 FPGA and a PC. The amplifier response to charge injection is shown in the left of Fig. 5.15, consistent with expectation.

From the amplifier output we also observed clear response to laser signal and radioactive sources such as ^{55}Fe as shown in Fig. 5.16. More thorough characterization of the COFFEE2 chip is ongoing, which will address key performance related to the new process such as uniformity between pixels, and possible cross-talk between the deep N-well and N-wells.

Future development using the 55 nm process is planned towards a full-size full-functioning sensor chip for CEPC ITK. More details are covered in later section of prospects and plans (Sec. 5.3.5).

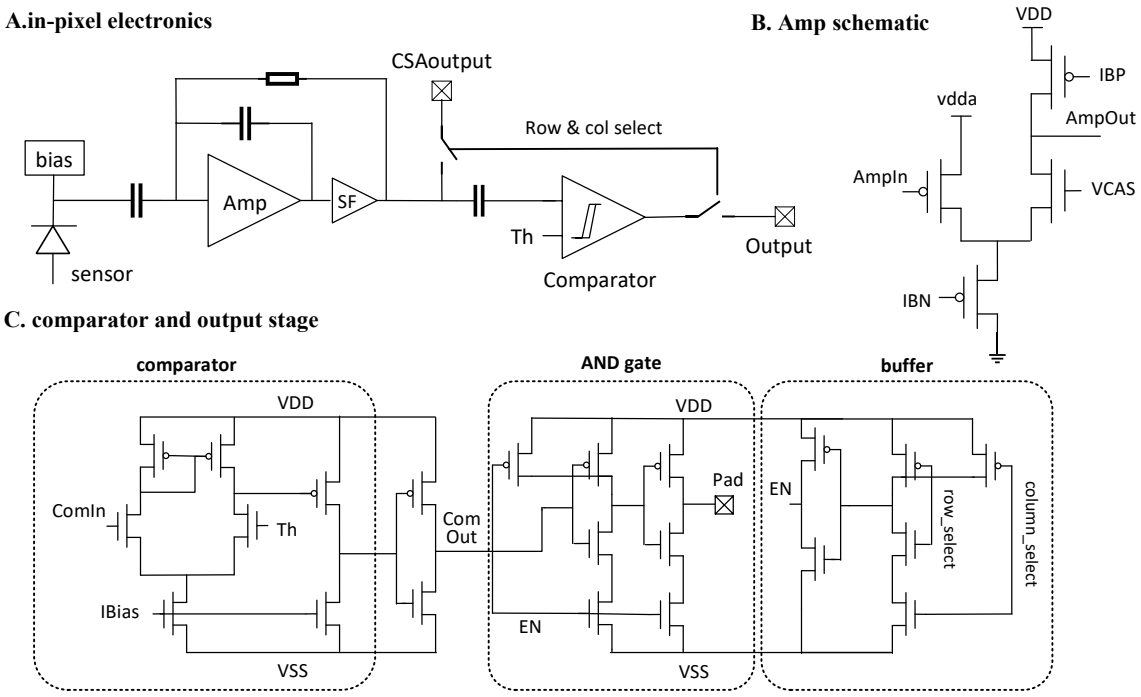


Figure 5.11: The schematic diagram of in-pixel electronics in Section 1 of COFFEE2. In section A, the sensor generates a signal that is amplified by a charge-sensitive amplifier based on a gain stage (Amp) and a source follower (SF). The amplified signal, labeled as "CSAoutput", is fed into a comparator after AC coupling. The comparator, as depicted, converts the analog signal into a digital output, which is routed to the pixel's exterior. The digital signal output utilizes a shared output bus per column of pixels, with row and column select signals managing the address of the pixel to be read on the bus. Section B illustrates the amplifier (Amp) schematic. The amplifier uses "IBN" as current bias necessary for its operation. "VCAS" is a voltage bias signal. Section C shows detailed circuit elements in the comparator and output stage. The comparator processes the input signals "ComIn" and compares it with threshold reference "Th". The current bias is "IBias". The output of the comparator "ComOut" then passes through an AND gate and a buffer before reaching the external output pad. This configuration ensures robust digital signal readout controlled by enable signals "EN", and further facilitates the selection of rows and columns (row_select and column_select). ALL these bias signals are controlled externally from the array, allowing the amplifier to be tuned to its optimal operating point during testing.

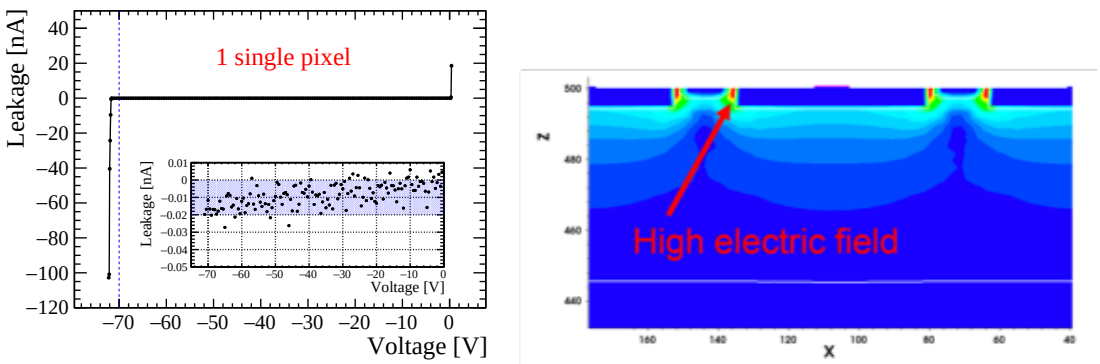


Figure 5.12: (Left) IV curve of a pixel in COFFEE2 chip; (Right) TCAD simulation of the passive diode under reverse-bias of -70V.

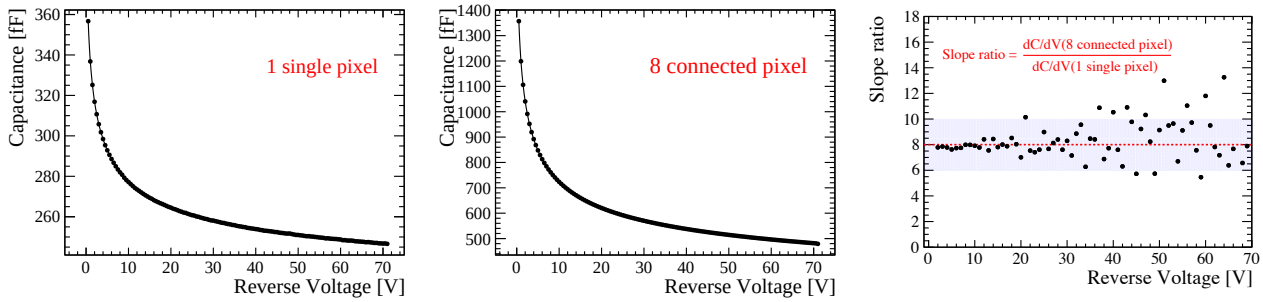


Figure 5.13: CV curves of (left) a pixel or (middle) 8 connected pixels in COFFEE2 chip. (Right) The ratio of capacitance of 8-pixel with respect to 1 pixel as a function of reversed bias.

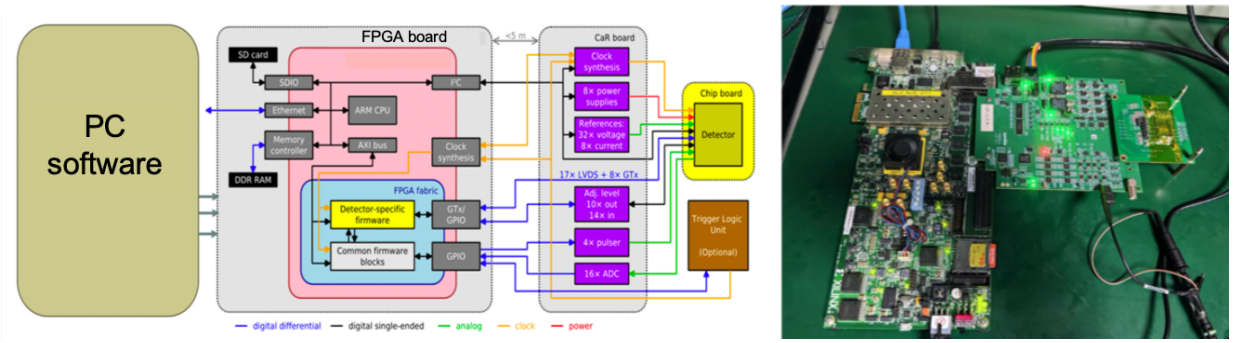


Figure 5.14: Test setup for COFFEE2 chip.

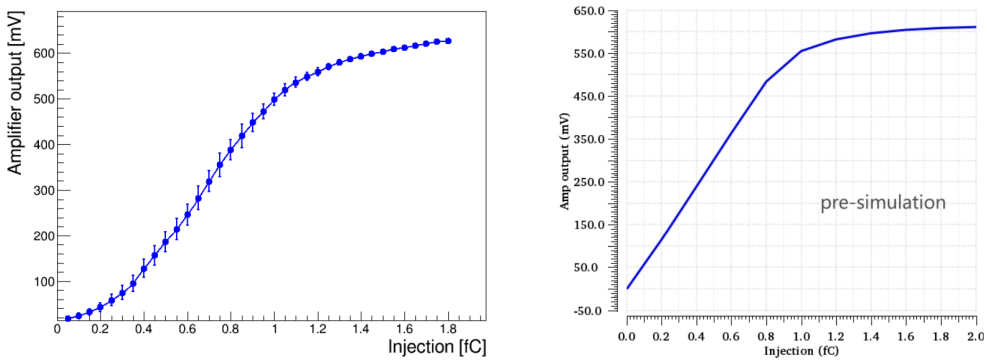


Figure 5.15: (Left) Amplifier output in COFFEE2 pixels as a function of injected charge and (right) its simulation.

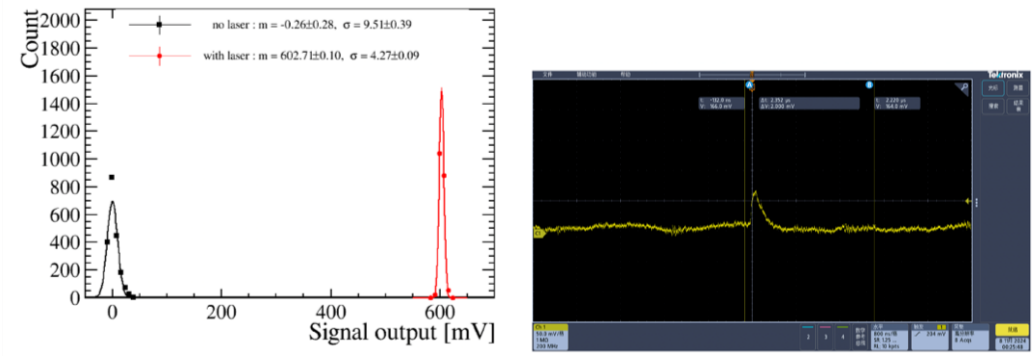


Figure 5.16: Response to (left) red laser signal and (right) X-ray from ^{55}Fe in a pixel of COFFEE2.

5.3.1.2 CMOS strip R&D

Responsible person: Xin SHI

Because of its good position resolution, high charge response sensitivity and low material budget, silicon strip detectors are widely used in high-energy physics (HEP) and nuclear physics experiments. Both the past HEP experiments such as Argus, Aleph, CDF and current running experiments at CERN such as ATLAS, CMS, LHCb and ALICE have used silicon strip detectors. In addition, the ATLAS phase 2 upgrade will also utilize the silicon strip as it's main component of the all-silicon tracker, which can be as large as $160\ \mathrm{m}^2$. The sizes of these silicon strip detectors are illustrated in Fig. 5.17. As one can see, with the size of the tracker on the collider increases, the coverage area of the corresponding silicon strip detector enlarged as well. Consequently, silicon strip detectors will be a reliable candidate for future large tracking detectors.

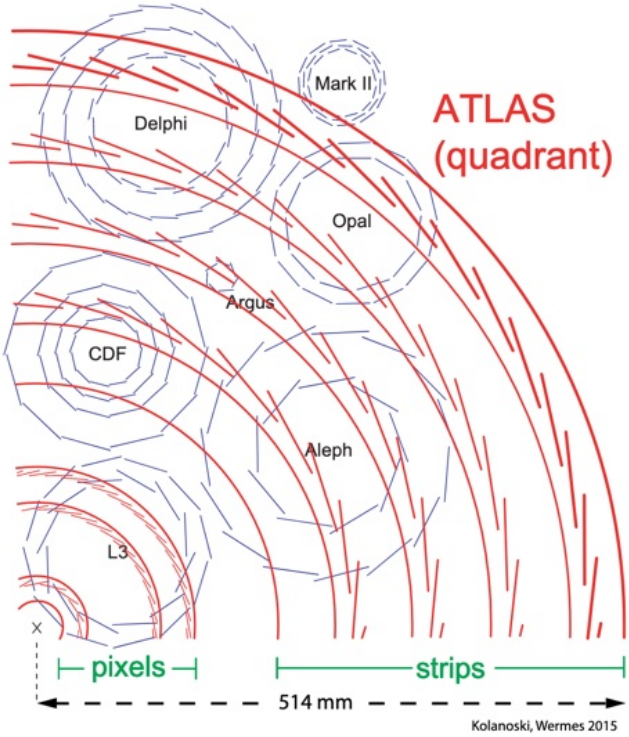


Figure 5.17: The history of strips in HEP experiments and ATLAS ITk strips.

To meet the physics requirement of CEPC Inner Tracker, the high spatial resolution impose challenging pitch size for strip detector design and fabrication. To reach less than $10\ \mu\mathrm{m}$ spatial resolution, a pitch size less than $30\ \mu\mathrm{m}$ has to be achieved, which will be a nightmare for conventional wire bonding process. For example, ATLAS ITk strip wire bonding is already reached 4 layers for wires per chip even with just $75.5\ \mu\mathrm{m}$ pitch size, and more than 5000 wires to be used on just one strip module, as illustrated in Fig. 5.18. Further more, highly customized silicon sensor fabrication process relying on a few foundries (in ATLAS and CMS case, only one company is used) to provide large quantities of sensors last for more than three years imposes big risk for the project. Apparently, new method to construct the silicon strip detector has to be explored.

As the mainstream in the semiconductor industry, CMOS process has been widely used in variety of fields. It provides a natural combination of the active detection sector and readout electronics sector to make them into a monolithic unit. Compared with the CMOS pixel detector, the CMOS strip detector has the advantage of relative simple readout since the readout ASIC only located at the end of strip and there is negligible interference between sensors and ASIC. The main difference between CMOS strip and CMOS pixel is shown in Fig. 5.19.

The first large sized CMOS passive sensor with 4.1 cm strip length and $75.5\ \mu\mathrm{m}$ pitch has been fabricated using 3-5 $\mathrm{k}\Omega$ wafer with LFoundry 150 nm stitching process. The electrical tests with Sr-90 source of the CMOS strip sensor indicates the full depletion can be reached around 30 V for $150\ \mu\mathrm{m}$ thickness and the charge collection efficiency reached

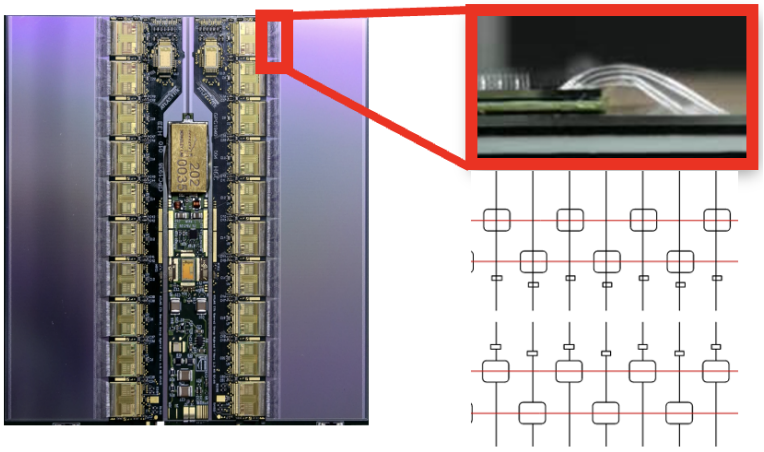


Figure 5.18: The ATLAS Inner Tracker (ITk) strip module assembled at IHEP. The right-hand side shows the four layer bonding wires and the bonding pad schematics.

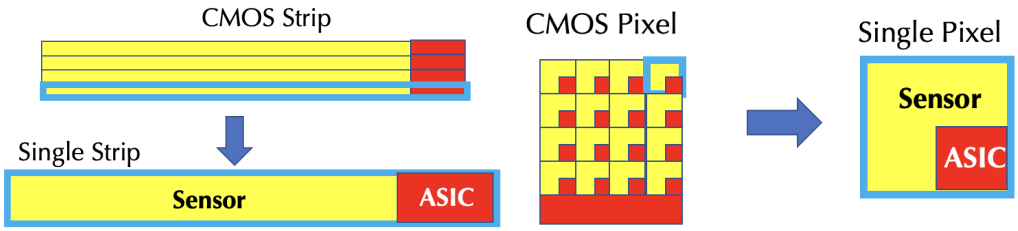


Figure 5.19: The difference between CMOS strip and CMOS pixel.

close to 100%. This confirms the feasibility of CMOS strip sensor as a valid research path. So far, there is no integrated CMOS strip with both sensor and readout ASIC yet.

The ultimate goal for the team is to fabricate a CMOS strip chip (CSC) targeting 20 μm pitch, so that a high spatial resolution (less than 5 μm), good time resolution (within 5 ns), and high charge resolution (better than 20%) can be reached. The schematic of the CSC chip as well as the CMOS circuit in the periphery is shown in Fig. 5.24 with the chip parameters shown in Table 5.3. The electronics is composed of Amplifier, Shaper, Discriminator, TDC, FIFO, and Serializer, as shown in the CSC1 Design Diagram 5.25.

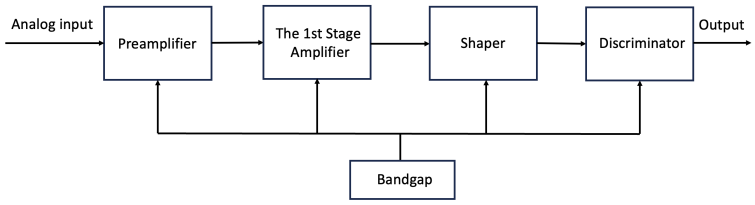


Figure 5.20: Structure of AFE.

The output port of the silicon microstrip sensor can be externally equivalent to a current source, and the pulse area of its output represents the charge quantity. The analog front-end (AFE) of the readout circuit converts this charge quantity into a voltage and processes this voltage signal through amplification, shaping, analog-to-digital (AD) conversion, and other operations. A single-channel readout circuit includes circuits such as a preamplifier, a first-stage amplifier, a shaping circuit, and a discriminator.

The preamplifier is used to initially amplify the output signal of the detector and complete the conversion of signal form. This design selects a charge-sensitive amplifier structure with excellent noise performance. The charge output by the sensor accumulates on the integrating capacitor, and the peak value of the output voltage signal is proportional to the input charge. The feedback resistor Rf and the feedback capacitor Cf constitute a charge-discharge circuit.

Although the output of the AFE is a binary signal, the entire AFE circuit still requires high linearity and a large

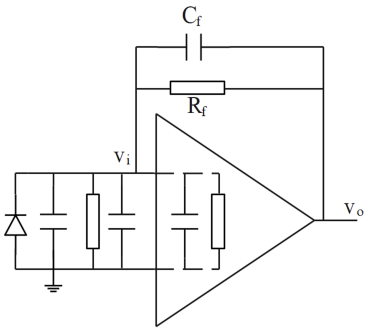


Figure 5.21: Structure of Preamplifier.

dynamic range, as well as a certain level of noise suppression capability. This design incorporates a first-stage amplifier and adopts a folded cascode circuit structure to achieve a gain within the range of 80 to 100 mV/fC.

The preamplifier is based on a classical cascode configuration. The nominal bias current of the input transistor is tuned to for the device operating close to weak inversion and ensures low value of excess noise factor. Dimensions of the input transistor will be optimized by taking into account of the channel thermal noise, the gate induced current noise , their correlation and the flicker noise. The active feedback circuit will be used since they offers much lower parasitic capacitance of the feedback loop compared to a resistive feedback. Low input impedance ensures small cross talk between channels via the interstrip capacitance and relatively small loss of input charge on the detector capacitance.

The shaping circuit performs shaping and filtering processing on the output signal of the preceding amplifier to reduce signal tailing, filter out noise and interference, and amplify the signal again. The shaping circuit adopts a differential structure circuit with single-ended input and double-ended output, providing a high power supply rejection ratio.

The first integrator stage is built of voltage amplifier consisting of two cascaded common source amplifiers. The following differential pair provides adjusting of the gain and of the peaking time of the entire signal chain. The differential pair translates the external differential threshold voltage for the internal threshold of the comparator. A fully differential structure of the comparator provides very good rejection of common mode noise from the digital power supply and good threshold uniformity.

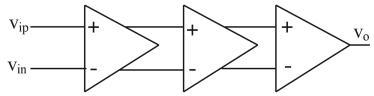


Figure 5.22: Structure of Discriminator.

The discriminator is a high-speed, high-resolution comparator that obtains a binary comparison result by comparing the output voltage signal of the shaping circuit with a reference voltage. In this design, the discriminator employs a structure of cascaded comparators with low open-loop gain but wide bandwidth, forming a high-speed, high-resolution comparator.

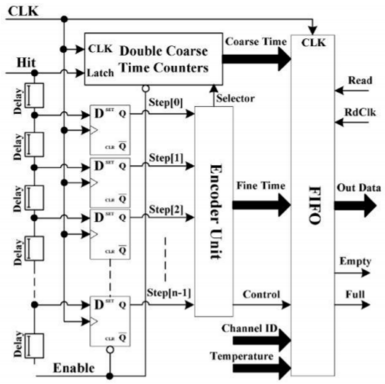


Figure 5.23: Structure of TDC.

Table 5.3: CSC Parameters (v1.3)

Strip width	10 µm
Strip pitch	20 µm
Strip number/ chip	1,024
Chip size	2.1×2.3 cm^2 (active area: 2.05×2.05 cm^2)
Spatial resolution	$\sigma \sim 5$ µm
Time resolution	~ 3 ns
Power consumption	~ 80 mW/cm^2
Data size per hit	32 bits (10b BXID, 10b address, 6b TOT + other 6 bits)
LV / HV	1.8V/ 200V
Wafer resistivity	2k Ω cm
Technology node	180 nm

The main clock delivered to chip is synchronous with the beam. However, its phase, although constant, is difficult to predict in advance. Therefore, it is shifted in the dedicated low power DLL to obtain a precise alignment between the ADC sampling phase and the bunch crossing. The DLL produces a second replica of the 40 MHz clock, which is used to tune the delay of the internal test pulse for the analogue front-end.

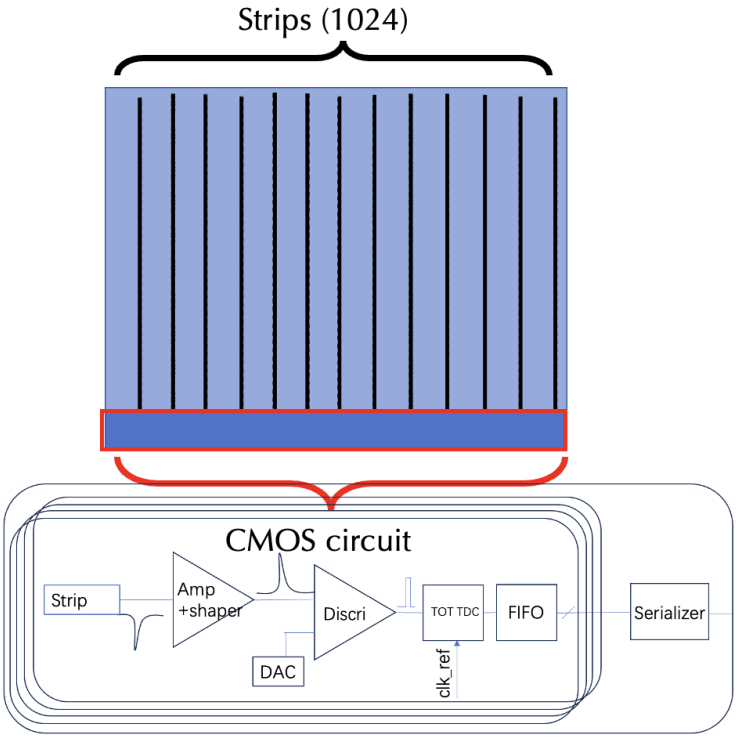


Figure 5.24: Schematic of the CSC chip with 1024 strips on top and the CMOS circuit in the bottom periphery.

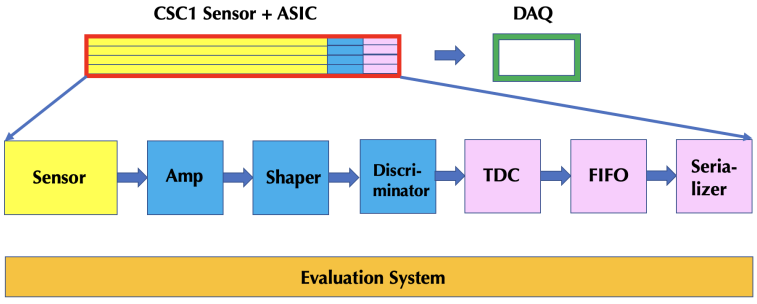


Figure 5.25: Design diagram of CSC1.

To start with, the team has conducted a comprehensive fast simulation of the minimum ionizing particle (MIP)

and laser response signals for the CMOS Strip Chip utilizing the team developed open-source code RASER. The main simulation workflow inside RASER is sketched in Fig. 5.26. Firstly, a detector geometry is created with a suitable mesh based on DevSim, in which the electric field and carrier distribution can be calculated. Secondly, an incoming particle is generated by Geant4, and the deposited energy is converted into carrier excitation. After the charge carriers drift and diffuse, an induced current is generated on the readout electrode, followed by amplification and waveform shaping simulated by NGSpice front-end electronics. Finally, With noise simulation, statistical results for arrival time, hit position, and dE/dx can be evaluated, allowing for the determination of the detector's time, spatial, and energy resolution.

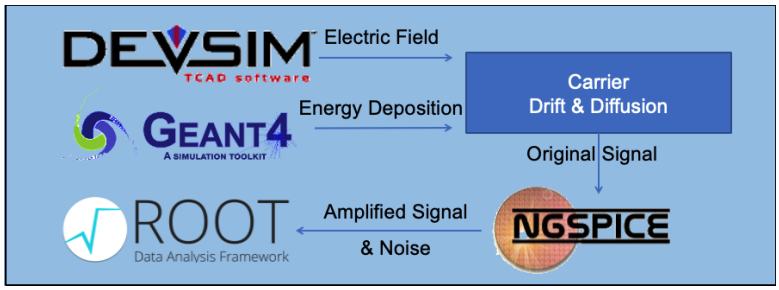


Figure 5.26: Simulation work flow by RASER

We have developed a strip detector model based on XXX, integrated with a CMOS processing design, as illustrated in Fig. 5.27, each strip readout is equipped with an n-plus well connected to the cathode, along with two p-stops shared by neighboring readouts to reduce the charge sharing effect.

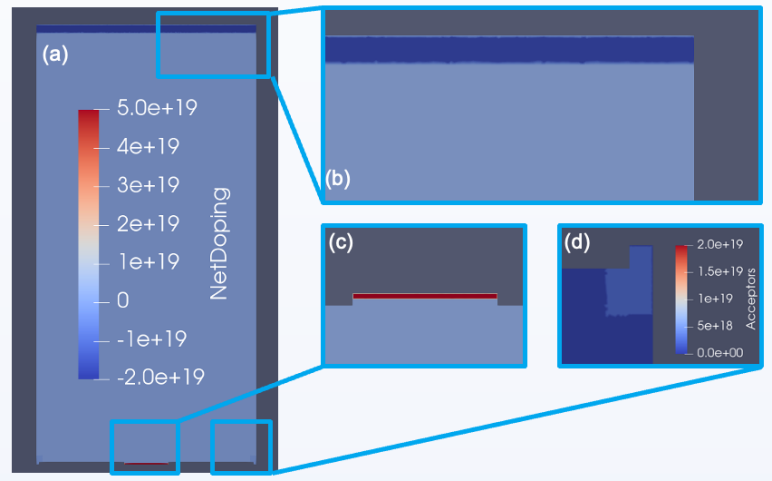


Figure 5.27: Doping profile of (a) the sensor, (b) p-contact (c) n-well, (d) p-stop.

We have evaluated the in-circuit properties of the detector, including the current-voltage (I-V) and capacitance-voltage (C-V) relations. The C-V relationship indicates that the detector reaches full depletion at 30 V. Meanwhile, the I-V relationship shows a relatively mild leakage current of 1uA at operating voltages. These results are shown in Fig. 5.28.

To validate the electronics simulation procedure. we simulated the ATLAS ABCStar amplifier, which consists of three stages: a preamplifier, a first boost amplifier, and a second amplifier with a shaper. This design is with good noise tolerance. The circuit achieves a gain of 87.7 mV/fC, a rise time of 21.7 ns, and a waveform full width at half maximum (FWHM) of approximately 32 ns. These results are consistent with the ABCStar data, which reports a gain of 85 mV/fC, a rise time of 22 ns, and an FWHM of 34 ns, as shown in Fig. 5.29.

Finally, we use both ^{90}Sr as MIP and 660 nm wavelength laser in Geant4 to simulate the response of the detector. The drift paths of the carrier after ^{90}Sr and laser are shown in Fig. 5.30. The current and voltage response of the sensor are shown in Fig. 5.31 and Fig. 5.32 respectively.

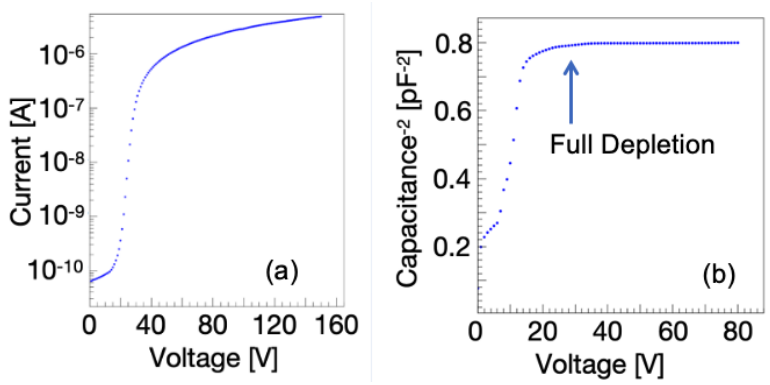


Figure 5.28: Electrical properties of CSC sensor simulation (a) I-V and (b) C-V.

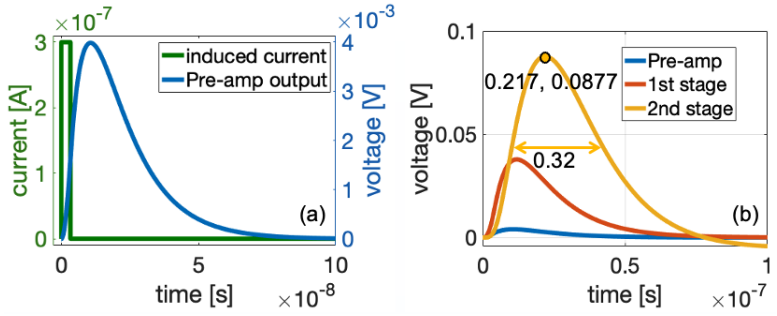


Figure 5.29: Electronics for CSC using the ABCStar as a reference. After injecting 1 fC charge, the signals (a) before and after the Pre-amp, (b) after every stage.

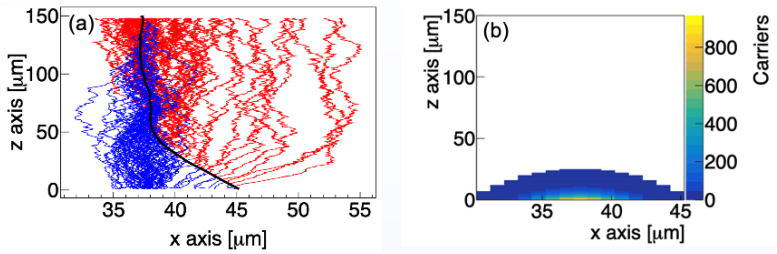


Figure 5.30: Visualization of (a) carrier drift paths after ^{90}Sr injection and (b) carrier distribution after laser injection.

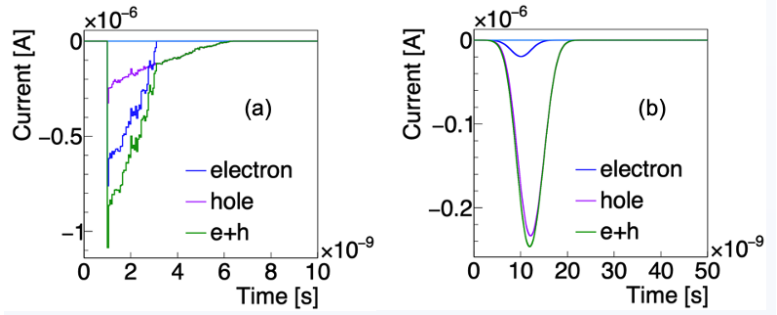


Figure 5.31: Sensor response current of (a) beta ray and (b) laser injection.

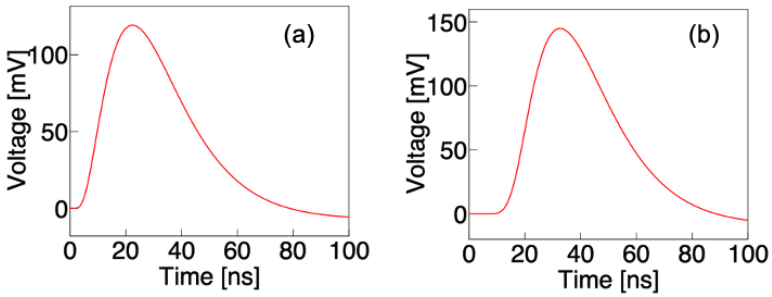


Figure 5.32: Amplified waveform of (a) beta ray and (b) laser injection.

5.3.2 ITK design

Responsible person: Qi YAN, Yiming LI, Xin SHI

The baseline design of the ITK consists of 3 barrel layers with detector radii of 240 mm, 350 mm, and 564 mm, and lengths of 987.0 mm, 1,410.4 mm, and 1,974.0 mm, respectively. The ITK endcap baseline design includes 4 pairs of detector layers with radii of 78.8 mm $< r <$ 241.4 mm, 121 mm $< r <$ 352.3 mm, 150 mm $< r <$ 564 mm, and 219 mm $< r <$ 564 mm, positioned at $|z|$ =506.5 mm, 719.7 mm, 1,001.5 mm, and 1,500 mm, respectively.

The ITK baseline design employs monolithic HV-CMOS pixel sensors, which is detailed in Subsections 5.3.2.1 and 5.3.2.2. These sensors have a pixel size of 34 μm$\times$150 μm, providing a spatial resolution of 8 μm in the bending direction and 40 μm in the non-bending direction, as well as a time resolution of 3–5 ns for each individual layer. An alternative ITK design, utilizing monolithic CMOS strip sensors, is introduced in Subsection 5.3.2.3.

5.3.2.1 ITK barrel design

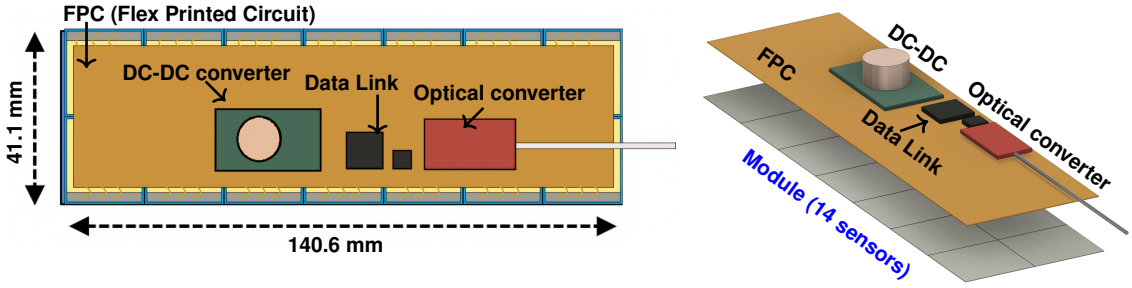


Figure 5.33: ITK Module

The ITK barrel design begins with the barrel module, which consists of 14 monolithic HV-CMOS pixel sensors arranged in 2 rows and 7 columns, with their backside glued to a flexible PCB (FPC) that holds electronic components, including radiation-tolerant DC-DC converters, a data aggregation chip, a data link chip (GBTx-like), an optical module, and power cables. A schematic of a barrel pixel module is shown in Fig. 5.33. Each sensor used in the module has dimensions of 20 mm$\times$20 mm, with an active area of 17.4 mm$\times$19.2 mm (512$\times$128 pixels) and a thickness of 150 μm. The pixels size of the sensor is 34 μm$\times$150 μm, providing a spatial resolution better than 8 μm$\times$40 μm. The time resolution for a crossing particle is 3–5 ns. The inactive area of a sensor is mainly due the region reserved for the peripheral electronics, located along one edge of the sensor. For the sensor layout in a module, the sensors are orientated so that these inactive regions are along the two long edges of the module, as shown in the grey areas in Fig. 5.33. These inactive regions also provide metal pads for electric connection to the FPC.

In each module, the sensors are connected to the FPC via wire bonds, which transmit clock and command inputs, data output, low voltage, and sensor high voltage. The sensors are powered in parallel from a common low voltage input on the FPC, supplied by DC-DC converters. A single downlink data line is connected to the ITK module, from which clock and command signals are extracted and routed in parallel to each sensor. The uplink data streams from all sensors in a module are aggregated by a data aggregation chip and sent to a data link chip, which then routes the data to the optical converter. The data is transmitted between a module and backend electronics (BEE) through an optical fiber, which serves as both the downlink and uplink data line. The detailed discussion about ITK electronics can be found in Section 5.3.3.

Every 7, 10, or 14 modules are assembled onto long supporting and cooling structures, forming 3 types of staves with a width of 41.1 mm and lengths of 987.0 mm, 1,410.4 mm, and 1,974.0 mm, respectively, as illustrated by a stave in Fig. 5.34. These staves are used to construct the three ITK barrels (ITKB1, ITKB2, and ITKB3).

Modules for each stave are positioned onto a carbon fiber supporting plate using a specialized assembly system with precision optical metrology and vacuum pick-up tools. The pick-up tools include adjustment mechanisms that allow fine-tuning of the module's position, achieving a placement accuracy better than 10 μm in the local coordinate system.

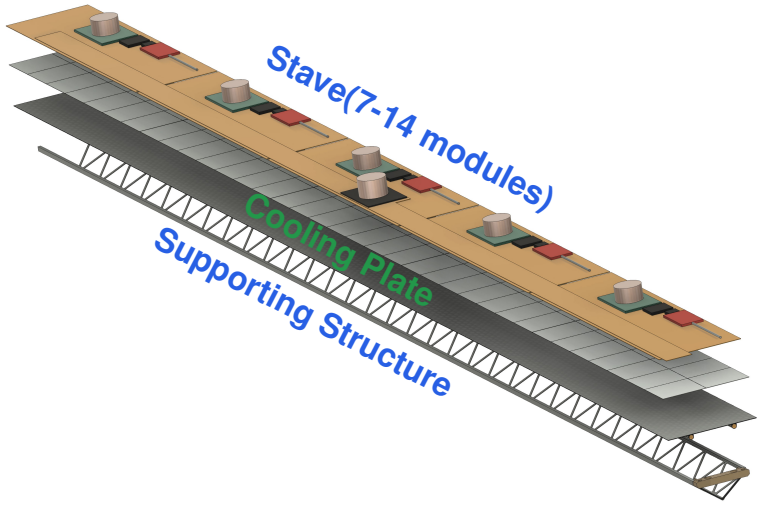


Figure 5.34: ITK Stave

Specific glue, characterized by its radiation resistance and high thermal conductivity, is used to establish robust mechanical and thermal contact between the modules' backside and the surface of the supporting structure.

After gluing all the modules onto a carbon fiber plate of a stave, 1 or 2 long power bus FPCs are connected on top of the modules for power transmission. A stave of the innermost ITK barrel (ITKB1) uses a single power bus FPC to connect all 7 modules, as shown in Fig. 5.34. A stave of ITKB2 or ITKB3 uses two power bus FPCs, each serving 5 (ITKB2) or 7 modules (ITKB3) from one end. Each power bus FPC integrates a DC-DC converter positioned in the middle. The high voltage (HV, 150 V) is directly transmitted to individual modules for sensor biasing via the power bus FPC. The original low voltage (LV, 48 V) is transmitted through the power bus FPC to its DC-DC converter, which steps down the 48 V LV input to 12 V. The 12 V LV is then distributed to individual modules via the same power bus FPC. The DC-DC converters in each module further converts the LV from 12 V to 1.2 V to supply power to the sensor circuits.

The overall stave, employing a truss structure with embedded cooling tubes, is designed for low mass (with a radiation length of 0.673% X_0) while providing high stiffness and effective heat dissipation, efficiently removing the heat generated by the modules. The details about the ITK mechanical and cooling design, as well as the performance, will be presented in Section 5.3.4.

The 3 ITK barrels have radii of 240 mm, 350 mm, and 564 mm. Since the inactive regions of the modules (see Fig. 5.33) are concentrated along the two long edges of a stave, the staves in a barrel are mounted in a staggered structure. With this arrangement, each stave is aligned parallel to the z-axis and tilted by 73.3 mrad around it to allow sufficient overlap between neighboring staves, as illustrated in Fig. 5.35. To minimize dead space, there are 44, 64, and 103 staves required for the 3 individual barrels. Table 5.4 summarizes the detailed information about the staves, modules, and sensors used for the construction of the 3 ITK barrels.

5.3.2.2 ITK endcap design

The ITK endcaps can also be designed using monolithic HV-CMOS pixel sensors. Four pairs of ITK endcaps are positioned at $|z|$ =506.5 mm, 719.7 mm, 1,001.5 mm, and 1,500 mm. To achieve full acceptance for incoming particles with a polar angle of $\cos(\theta) < 0.99$, the active area radii of the four pairs of endcaps are set as 81.5 mm $< r <$ 242.5 mm, 110.5 mm $< r <$ 352.3 mm, 163 mm $< r <$ 564 mm, and 223 mm $< r <$ 564 mm, respectively.

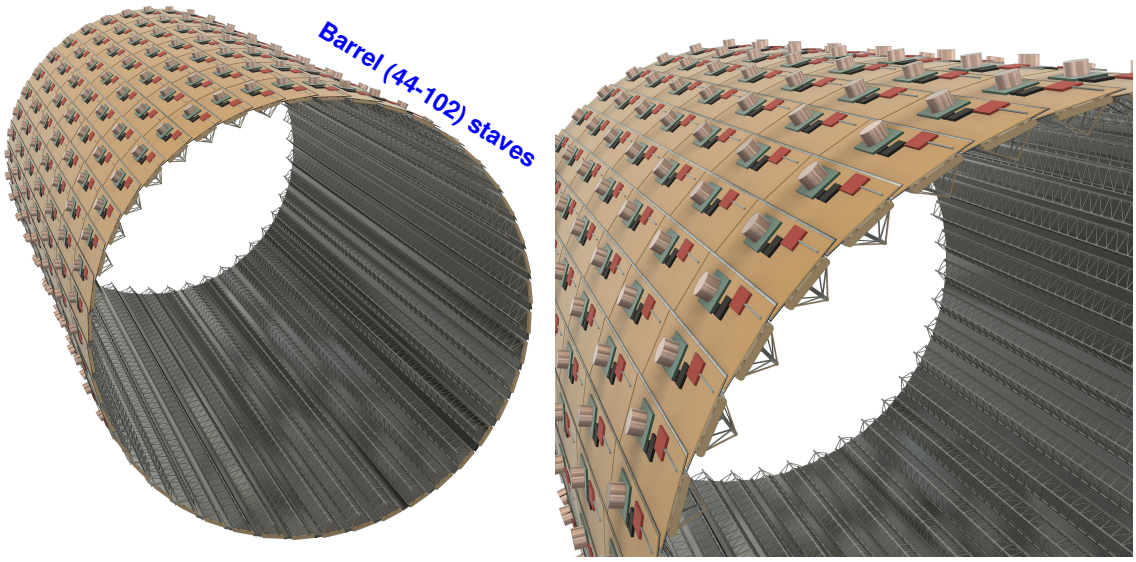


Figure 5.35: ITK Barrel

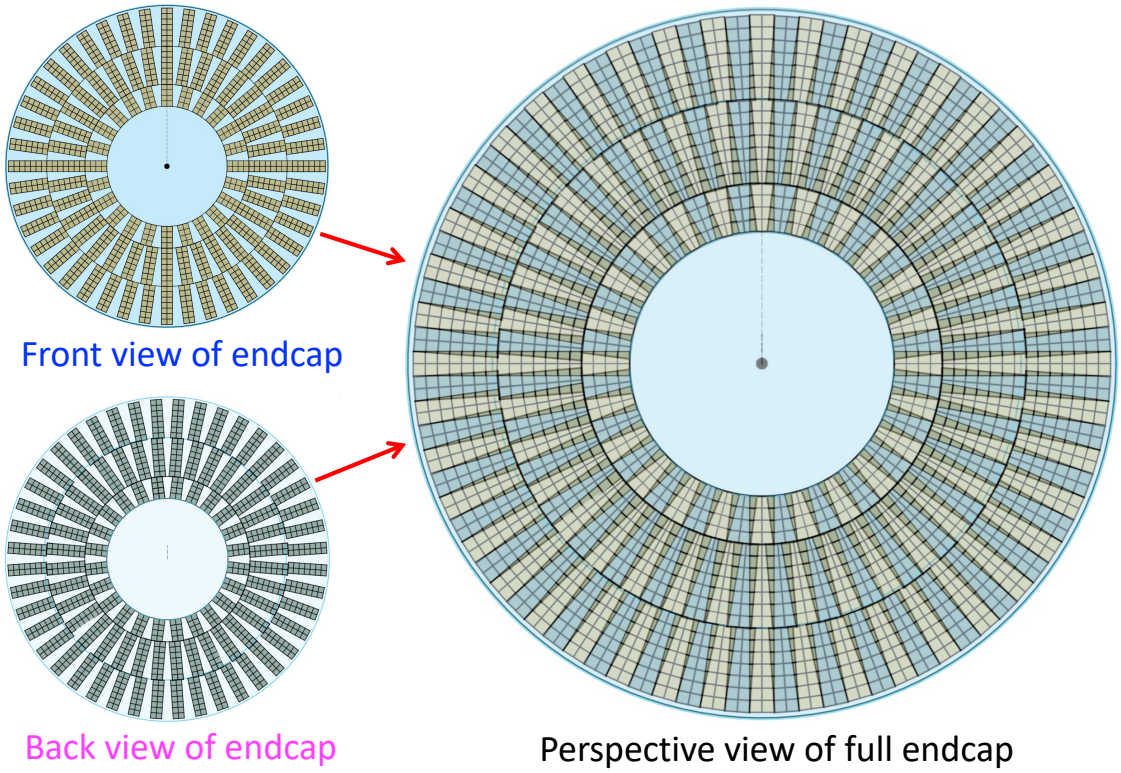


Figure 5.36: Each ITK endcap has 2 faces, containing 2 types of modules with different number of sensors. All ITK endcaps use 3 types of modules, one of which is shared with the barrel.

Information about staves, modules, and sensors used for 3 ITK barrels construction					
Barrel	Number of staves	Modules per stave	Sensors per module	Total number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4312	1.72
ITKB2	64	10	14	8960	3.58
ITKB3	102	14	14	19992	8.00
Total	210			33264	13.31

Table 5.4: Information about staves, modules, and sensors used for 3 ITK barrels construction.

Similar to the barrels, the assembly process for the ITK endcaps begins with the HV-CMOS pixel modules. After assembling a few types of modules with different numbers of sensors (3 types of modules containing 8, 12, and 14 sensors for all ITK endcaps), the modules are precisely positioned and glued onto the two faces of a carbon fiber honeycomb support plane disk. Figure 5.36 (left panel) shows the front and back views (module layout) of the 4^{th} ITK endcap. As shown, there are 3 rings of modules on both the front and back faces of the endcap. Modules in the outermost ring contain 14 sensors each, modules in the middle ring contain 12 sensors each, while modules in the innermost ring contain 8 sensors each. Optimal spatial resolution in the bending direction (ϕ) is achieved by arranging the longitudinal direction of the rectangular modules in each ring along r (see Fig. 5.36).

To minimize dead detection area for the endcap, the layout of the modules on the back face of the endcap is offset relative to those on the front face, creating overlaping regions between the two faces. Figure 5.37 (right panel) provides a perspective view of the complete 4^{th} ITK endcap, where the overlap regions between the modules from the two faces are highlighted in dark green triangles.

The layouts of the modules, along with their electronic components, for all 4 ITK endcaps (ITKE1, ITKE2, ITKE3, and ITKE4) are displayed in Fig. 5.37. Detailed information about the modules and sensors for a single face of each ITK endcap is summarized in Table 5.5. In total, 13,920 sensors (3480×2 faces×2) are used in constructing the ITK endcaps, with the total number of modules amounting to 1,128.

The Module and Sensor Layout of a Single Face of Each ITK Endcap				
Endcap	Number of module rings	Number of modules per module ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	248
ITKE2	2	16,24,28	8,8,8	528
ITKE3	3	24,36,44	12,14,14	1382
ITKE4	3	24,36,44	8,12,14	1290
Total				3448

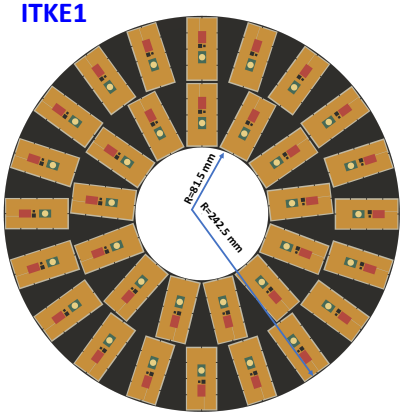
Table 5.5: The Module and Sensor Layout of a Single Face of Each ITK Endcap

Yiming: Please update the endcap layout corresponding to Fig. 5.38 and Table 5.6. The layout is designed so that the number of modules in each ring can be divided by eight or four, to facilitate modular assembly and production.

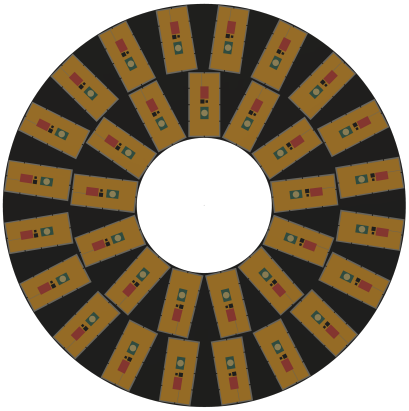
The Module and Sensor Layout of Each ITK Endcap disk.				
Endcap	Number of module rings	Number of modules per module ring	Number of sensors per module	Total sensors
ITKE1	2	24,36	8,8	480
ITKE2	2	32,56	8,14	1040
ITKE3	3	48,72,88	12,14,14	2816
ITKE4	3	48,72,88	8,12,14	2624
Total				6960

Table 5.6: The Module and Sensor Layout of Each ITK Endcap disk. The total number of sensors are supposed to be doubled for the whole ITK endcap.

a) ITKE1

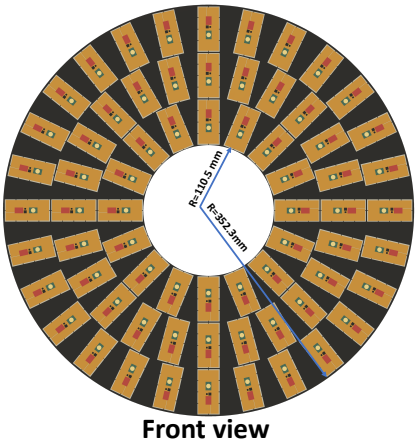


Front view

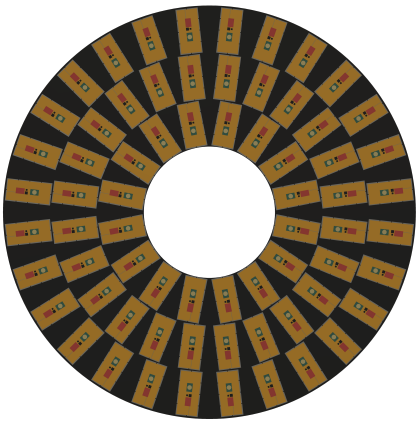


Back view

b) ITKE2

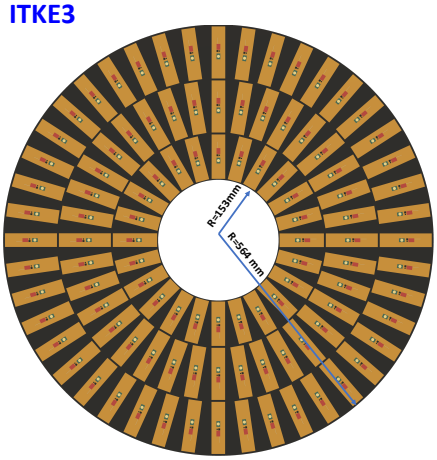


Front view

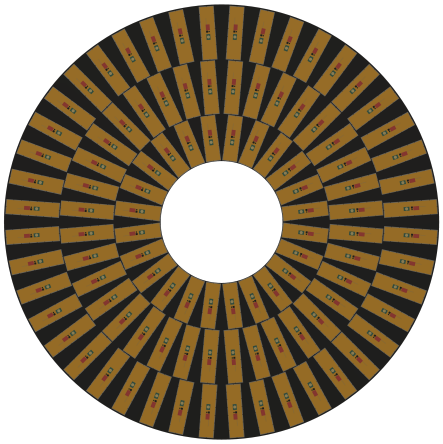


Back view

c) ITKE3

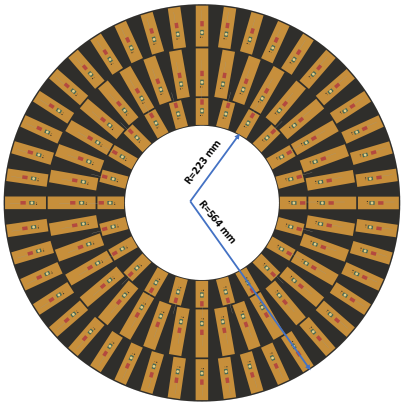


Front view

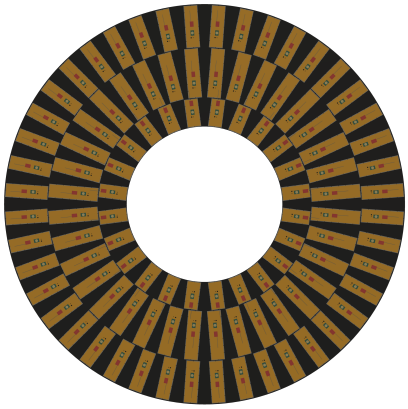


Back view

d) ITKE4



Front view



Back view

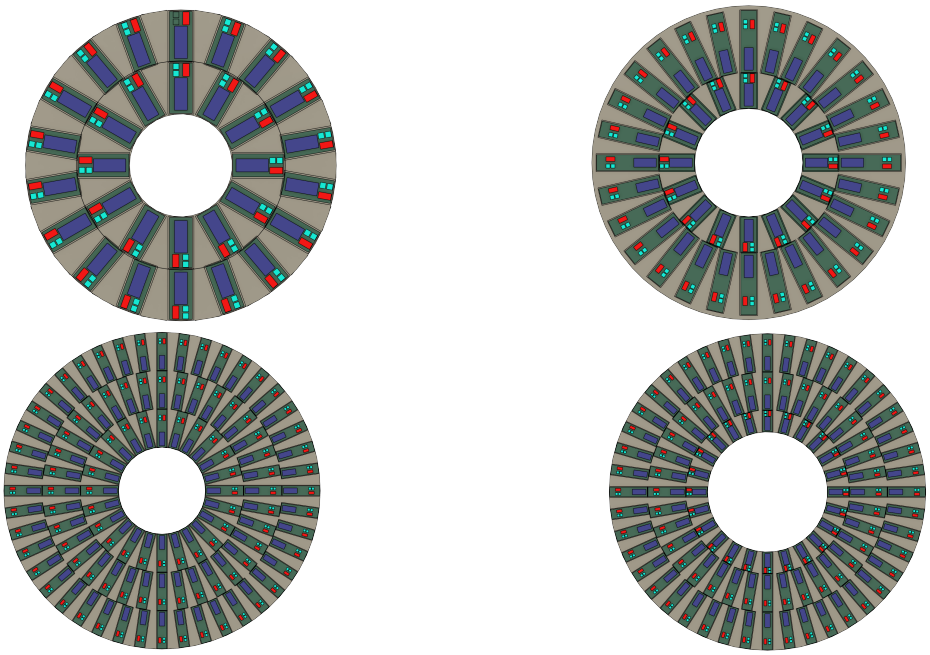


Figure 5.38: Four endcap disks (front side).

5.3.2.3 Alternative design for the ITK

The alternative design of the ITK is based on monolithic CMOS stirp sensors. Each sensor has dimensions of 21 mm×23 mm×0.3 mm implanted with 1,024 strips. With a strip pitch size of 20 μm, the spatial resolution is 5 μm, and the time resolution is 3-5 ns.

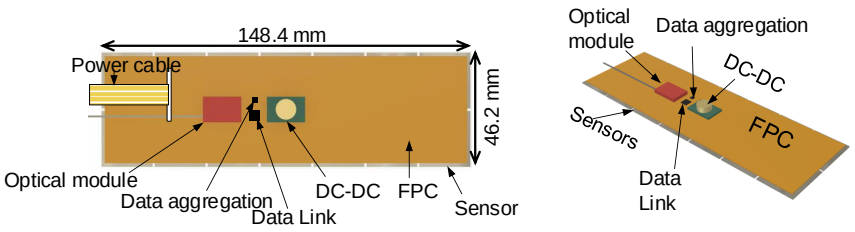


Figure 5.39: ITK Half Endcap with CMOS Strips

Similar to the ITK pixel module, a CMOS strip module consists of multiple strip sensors (4-15) glued to a FPC equipped with electronic components, including radiation-tolerant DC-DC converters, a data aggregation chip, a data link chip, an optical module, and power cables. A schematic of one module is shown in Fig. 5.39. Sensors in a module are oriented so that their strips run along the shorter direction of the module, and the bonding pads of the sensors are located along the long edge of the module. The sensors are connected to the FPC via wire bonds, which transmit clock and command inputs, data output, low voltage, and sensor high voltage.

One full ITK endcap comprises two detector disks, with each disk filled with modules referred to as a half-endcap. Each ITK half-endcap is divided into 8 sectors, with each sector consisting of several CMOS strip modules closely assembled, as illustrated by a sector of the 4^{th} endcap in Fig. 5.40. Figure 5.41 provides a perspective view of the sensors distribution within the half-endcap. As shown, the overlapping areas between neighboring sectors are designed to be minimal.

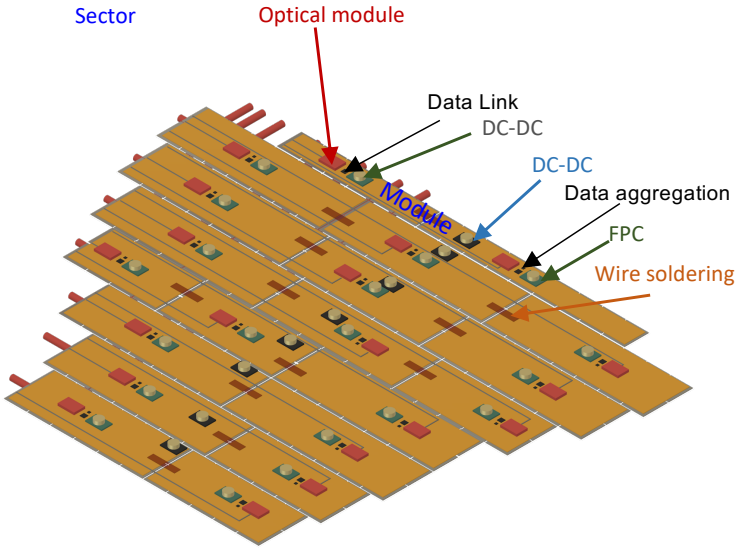


Figure 5.40: ITK Half Endcap Sector with CMOS Strips

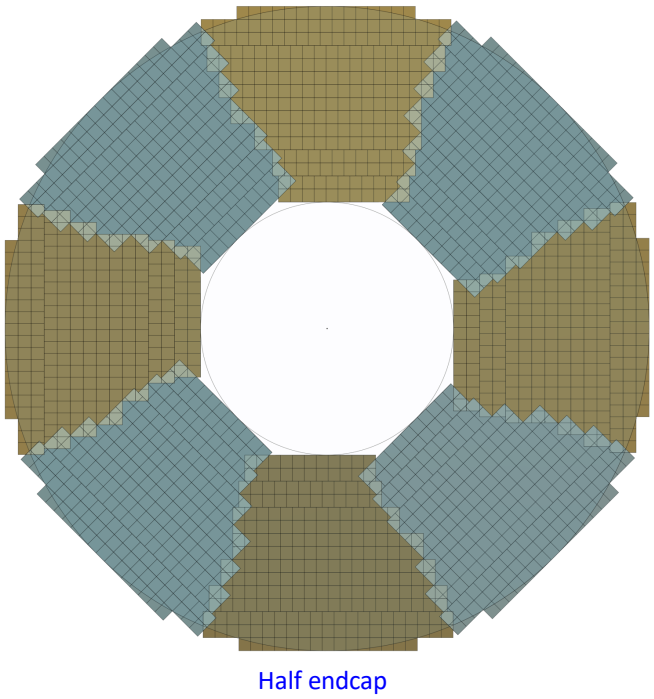


Figure 5.41: Each ITK half endcap is divided into 8 sectors, with each sector consisting of CMOS strip modules. The overlapping areas between the neighboring sectors are designed to be minimal.

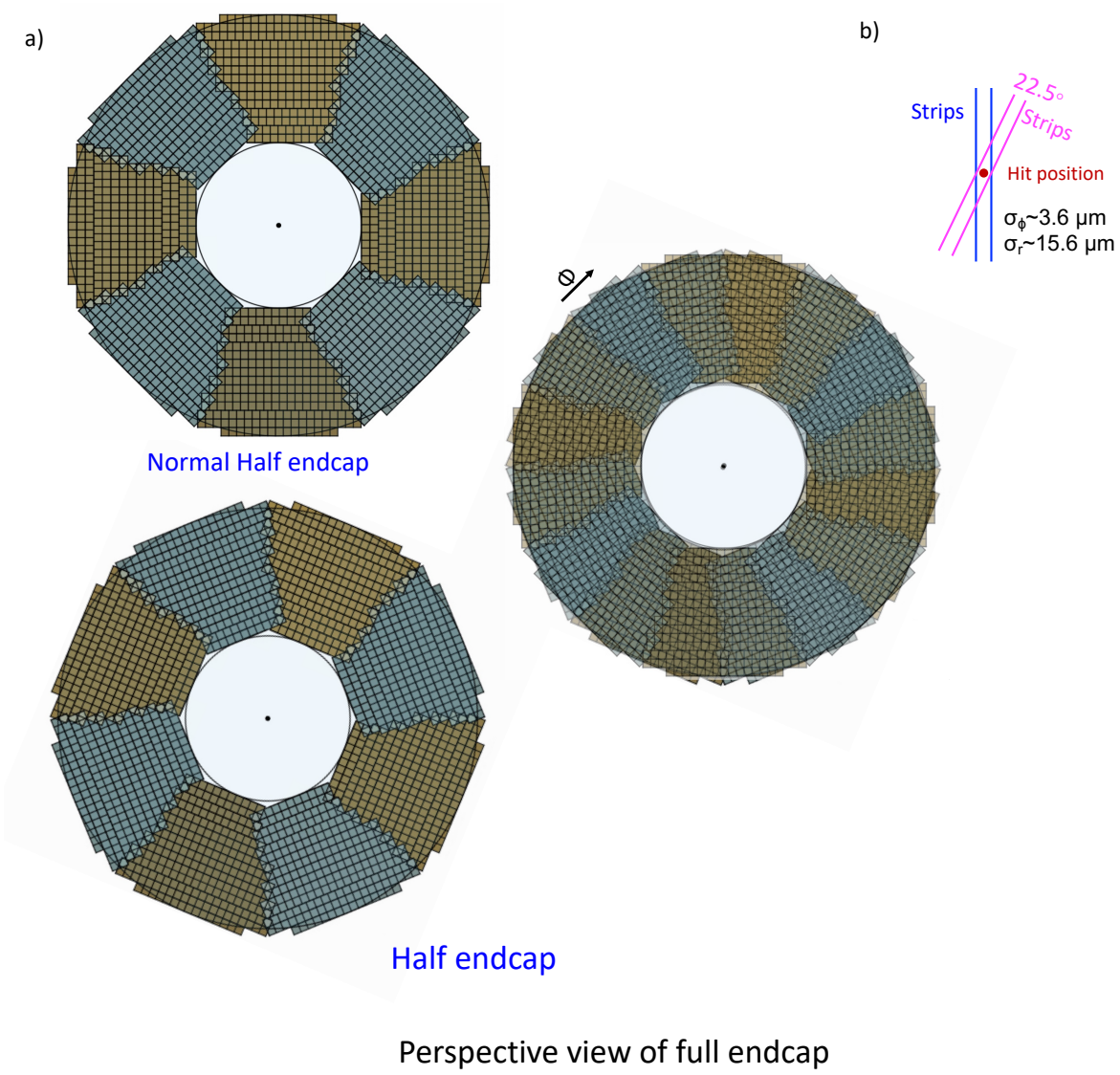
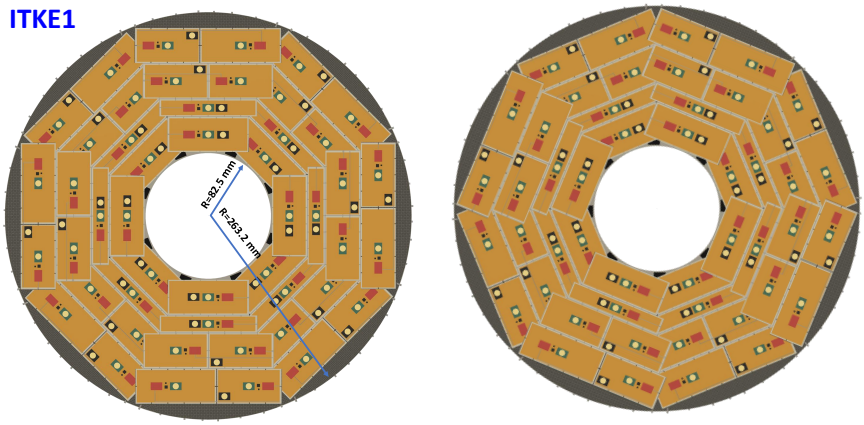


Figure 5.42: ITK Endcap with CMOS Strips

To form one complete ITK endcap, the two half endcaps are rotated 22.5° relative to each other, as shown in Fig. 5.42 (a). With this design, the track resolution in the bending direction (ϕ) is maximized. Figure 5.42 (b) shows a particle hit detected by two parallels of strips from the two half-endcaps. The spatial resolution in the bending direction is $\sigma_\phi = 3.6$ μm, and in the non-bending direction, it is $\sigma_r = 15.6$ μm.

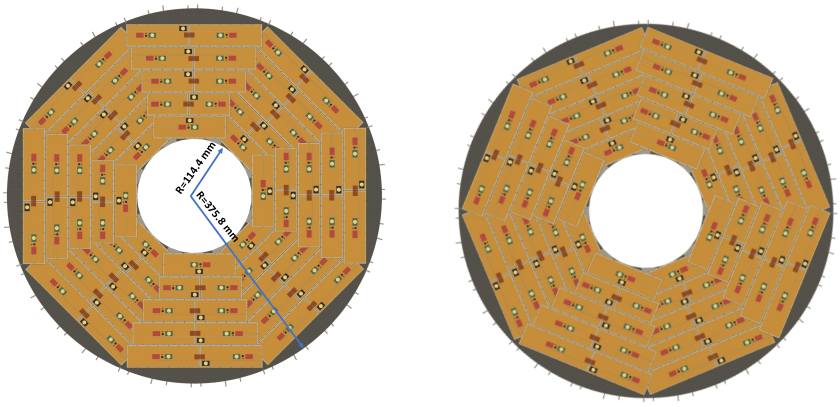
For completeness, Figure 5.43 shows the module layouts for all 4 ITK half-endcaps. Table 5.7 summarizes the detailed information about the modules and sensors for all ITK half-endcaps. A total of 20,288 sensors are required to construct the ITK endcaps, and the total number of module types is 6 , and the total number of modules is 232 . The design of the ITK endcap mechanical structures will be addressed in Section 5.3.4.

a) ITKE1



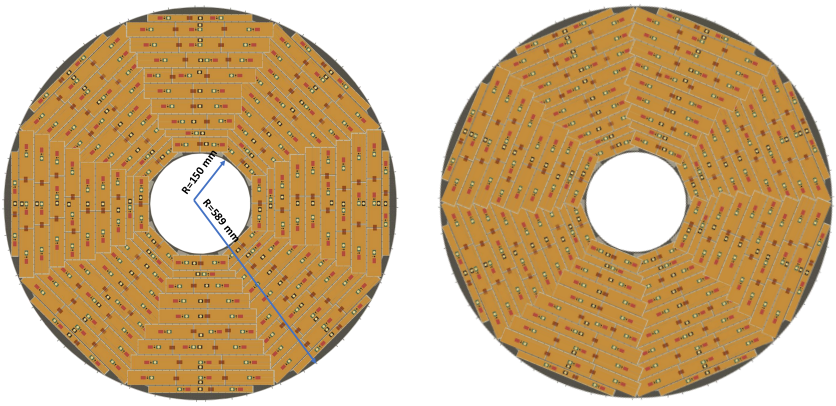
Front view Back view

b) ITKE2



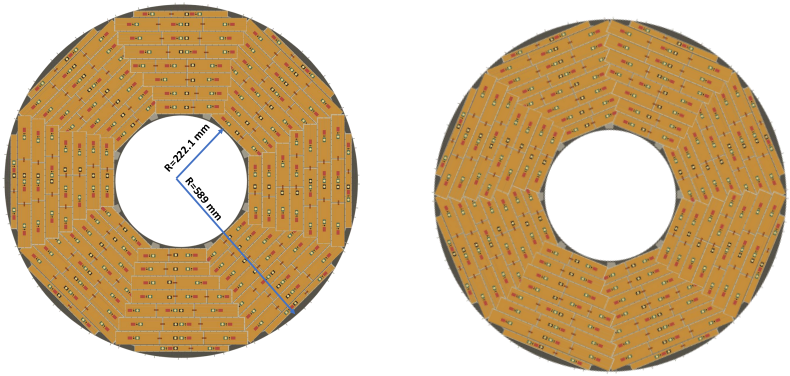
Front view Back view

c) ITKE3



Front view Back view

d) ITKE4



Front view Back view

The Module and Sensor Layout of a ITK Half-Endcap with CMOS Strip Sensors				
Endcap	Number of modules	Number of Module types	Number of sensors per module	Total sensors per Half-Endcap
ITKE1	6	3	6,8,10	400
ITKE2	9	4	8,10,12,14	800
ITKE3	23	6	6,8,9,10,12,14	2072
ITKE4	19	6	6,8,9,10,12,14	1800
Total				20288

Table 5.7: The Module and Sensor Layout of a ITK Half-Endcap with CMOS Strip Sensors

5.3.3 Readout electronics

Responsible person: Xiongbo YAN, Qi YAN

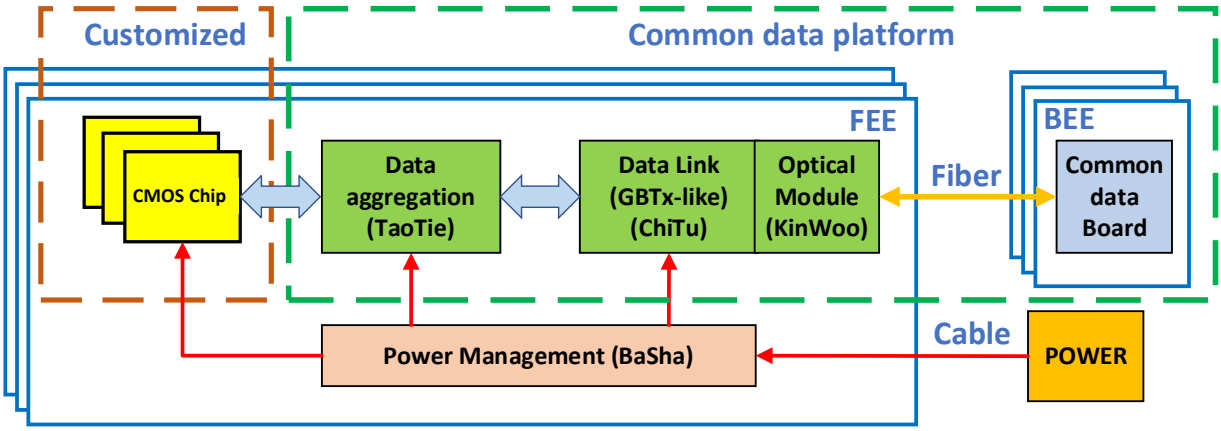


Figure 5.44: ITK Readout Electronics

In each ITK module, 14 monolithic HV-CMOS pixel sensors are bonded to a common flexible PCB (FPC), as shown in Fig. 5.33. The FPC transmits digital signals from the sensors to the data aggregation chips and subsequently to the optical fiber. To ensure error-free data transmission, the FPC integrates two ASICs for data aggregation: the TaoTie chip and the ChiTu chip.

As illustrated in Fig. 5.44, the TaoTie chip collects data from multiple sensors and transfers it serially, while the ChiTu chip (GBTx-like) gathers data from several TaoTie chips and routes it to the optical module (KinWoo) for fiber readout. The hit rate varies across different radial regions. To address this variation, a dedicated buffer is incorporated into each aggregation ASIC to average the rate fluctuations and optimize the speed of the e-link driver's transceiver inputs. Optical fiber transmist the aggregated data out of the detectors to the backend electronics DAQ system (BEE).

The ChiTu chip operates at a maximum data rate of 9.71 Gbps. For HV-CMOS pixel sensor, each fired pixel generates 42 bits of data, with an average of $\sim$1.5 pixels firing per hit. In the current ITK design, the supported data rate per sensor is up to 693.33 Mbps. The required bandwidth of the readout e-link of each sensor strongly depends on the beam background, specifically the accelerator operation mode and the radial region it covers. As detailed in Section 5.5 on beam background estimation, the current ITK design is robust to handle data transmission under various operating conditions.

To synchronize different detectors, the reference clock signal is downlinked from the BEE through optical fiber to the ChiTu chip. Clock recovery is handled by the ChiTu's Clock and Data Recovery (CDR) circuit. The ChiTu provides six clock output options: 43.33 MHz, 86.67 MHz, 173.33 MHz, 346.67 MHz, 693.33 MHz and 1.39 GHz, which are used in the front-end electronics of different detectors.

Considering a total power consumption of 200 mW/cm^2 and a sensor area of 2 cm$\times$2 cm, each module with 14 sensors will have 1 or 2 DC-DC converters (BaSha12V) on the module FPC to meet the current demand, with a total current of $\sim$10 A at 1.2 V. The 48 V low voltage (LV) supplied from the power crate is stepped down to 12 V with a DC-DC (BaSha48V) at the first stage and further to 1.2 V at the second stage.

As illustrated in Fig. 5.34 for an ITK barrel stave, the long power bus FPC in transmits the original 48 V LV to a DC-DC converter positioned in the middle of the stave. This converter steps down the 48 V LV input to 12 V. The 12 V LV is then distributed to individual modules via the same power bus FPC. In each module, dedicated DC-DC converters further drop the 12 V LV to 1.2 V to supply power to the sensor circuits and 3.3 V or 2.5 V for the VCSEL driver. FPCs are used to transmit both LV and high voltage HV from the end of the barrel or endcap to the modules. These FPCs are connected to composite cables, along with optical fibers from outside, to deliver power and signals.

For monolithic CMOS strip sensor, the readout scheme is very similar.

5.3.4 Mechanical and cooling design

Responsible person: Qi YAN

5.3.4.1 Barrel local support

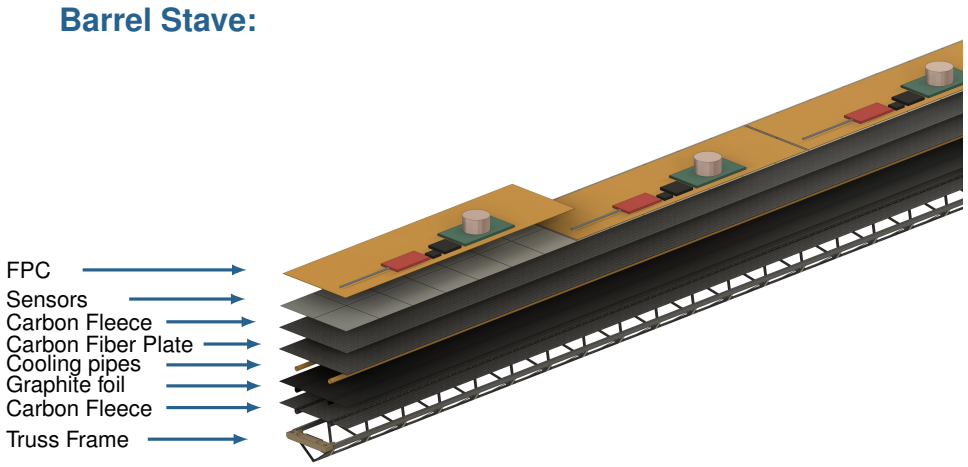


Figure 5.45: ITK barrel mechanics and cooling

The segmented element of the ITK barrel in the azimuthal direction is called a stave – a long structure that spans the entire length of the ITK layer. It acts as the fundamental building block, integrating both structural and functional components, as illustrated in Fig. 5.34 and 5.35. The design of the ITK stave is similar to that of the ITS2 used in ALICE. Key requirements for the stave structure include a low material budget, high rigidity and stability, and efficient cooling capability.

The stave structure can be divided into three functional units, as shown in Fig. 5.45:

- Sensor Modules: These consist of sensors glued onto flexible printed circuits (FPCs) integrated with associated electronics.
- Cooling Plate: A carbon fiber plate embedded with cooling pipes that are in direct thermal contact with the chips to efficiently dissipate heat. The cooling pipes are glued to the carbon plate, and the thermal contact is enhanced by a layer of graphite foil. To increase the structural rigidity, an additional thin layer of carbon fleece is added to both the top and bottom sides of the cooling plate.
- Truss Frame: A carbon fiber support structure that provides mechanical support and enhances the stiffness of the stave.

5.3.4.1.1 Materials The design of the ITK stave imposes strict requirements to achieve a minimum material budget. The Cooling Plate is stiffened by the Truss Frame, which has a triangular cross section made from carbon fiber with a high Young's modulus, such as K13C2U, which can achieve up to 900 GPa. For the Cold Plate, the carbon fiber used for the plate has high thermal conductivity, such as K13D2U, with a thermal conductivity of up to 800 W/(m·K). Additionally, the thermal performance is enhanced by a layer of graphite foil, which has high thermal conductivity in the horizontal direction, reaching over 1500 W/(m·K). This helps to maintain a more uniform temperature field across the plane.

Water with polyimide cooling pipes has been selected as the baseline cooling medium for the ITK. Polyimide possesses excellent properties such as high temperature resistance, corrosion resistance, radiation resistance, and high strength. Additionally, it has a low coefficient of friction and good sliding performance, which reduces frictional losses when transporting fluids or gases, thereby effectively improving the efficiency of the water-cooling system. A detailed thermal analysis of the water-based cooling strategy will be discussed later.

Table 5.8 lists the estimated contributions of the ITK stave to the material budget. The overall estimated material budget for a stave is 0.673% X_0. Neighbouring staves are partially superimposed to ensure the detector hermeticity, as illustrated in Fig. 5.35. The overlap area accounts for 8% of the stave area, corresponding to 6% of the stave materials.

Estimation of ITK stave material contributions					
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64	28.41	0.013
	Carbon fluid	Water		35.76	0.105
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Total					0.673

Table 5.8: Estimation of ITK stave material contributions

5.3.4.1.2 Structural characterisation The structural characterization is performed using finite element simulations. The two key structural parameters that define the achievable accuracy and stability in the position of the sensors are the stave sag under its own weight and the first natural frequency of the stave. The sag provides information on the deviation of the sensors' final position relative to the nominal one, while the first natural frequency indicates the frequency at which an external impulse can induce resonance phenomena in the structure, resulting in oscillations of the sensor positions.

Both the sag and the natural frequency for a given stave mass depend on the stave stiffness, which is mainly provided by the Truss Frame. As a conservative assumption, the contribution of the FPC and cooling pipes to the overall stiffness has been neglected in the analysis.

A finite element model of an ITK stave was created with the following assumptions:

- The contribution of structures other than the carbon fiber frame and carbon fiber plates is neglected, and a uniformly distributed load is applied to the first layer of the carbon fiber plate.
- Both stave ends are assumed to be fixed supports (i.e., all translational and rotational degrees of freedom at both ends are constrained).

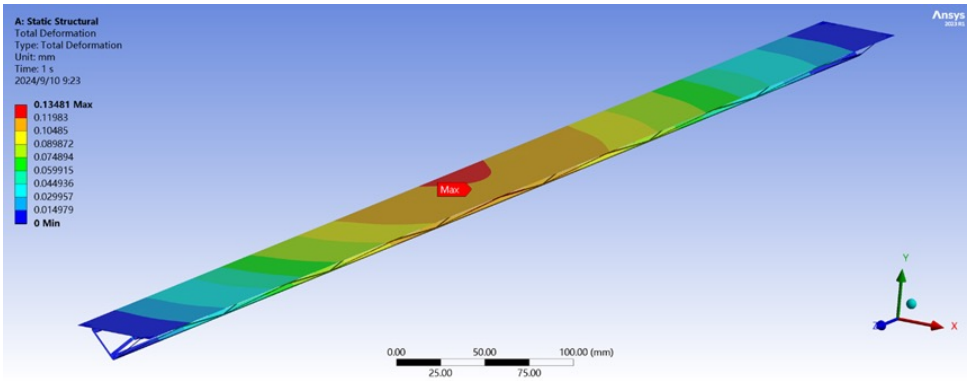


Figure 5.46: ITK Stave Deformation

Based on this, preliminary static and modal analyses were performed to evaluate the maximum deflection and the first natural frequency, as shown in Fig. 5.46 and Fig. XXX. The results indicate sags of aaa μm, bbb μm, and ccc μm are derived for staves of the 3 barrels, with corresponding first natural frequencies of aaa Hz, bbb Hz, and ccc Hz.

5.3.4.1.3 Thermal characterisation The heat transfer simulation analysis is conducted to optimize the cooling design. The primary goal is to meet the physical and performance requirements of the detector. According to the sensor specifications for ITK, the cooling design should achieve the following:

- The overall sensor operating temperature should not exceed 30°C.
- The temperature uniformity across a single sensor should be maintained within 5°C.

A water cooling fluid structure coupled finite element model was established to study the temperature distribution along the entire longitudinal length of the stave, considering a specific water cooling flow rate. The following configurations were made for this model:

- The heat generated by sensors is uniformly distributed on the carbon fiber plate, with a magnitude of 200 mW/cm^2 (sensor heat flux).
- The cooling water enters the stave with a flow velocity of 1 m/s and a temperature of 15°C.
- Natural convection and radioactive heat transfer are not considered.

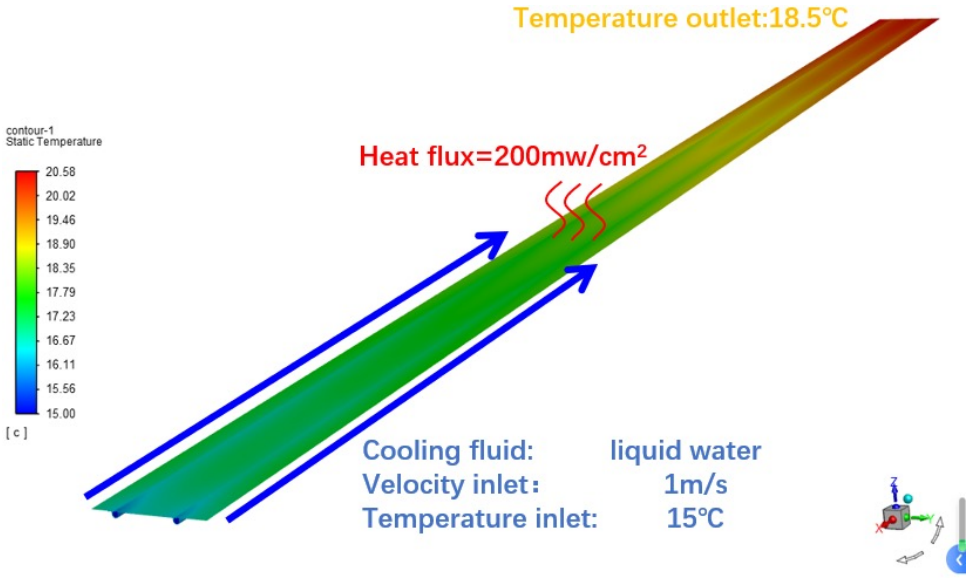


Figure 5.47: Simulation results of water cooling with a flow velocity of 1 m/s and a temperature of 15°C, with inlets on the same side

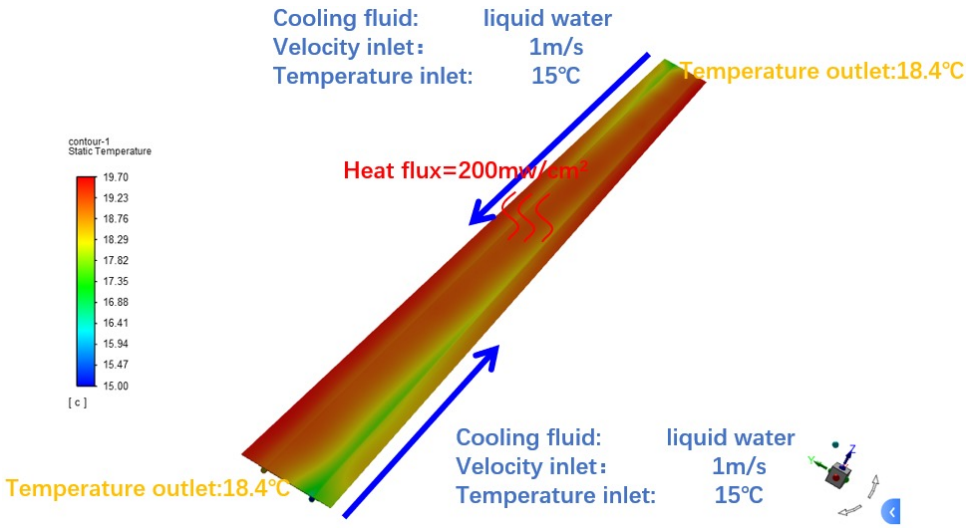


Figure 5.48: Simulation results of water cooling with a flow velocity of 1 m/s and a temperature of 15°C, with inlets on both sides.

The simulation results, shown in the Fig. 5.47 and Fig. 5.48, illustrate that with a cooling water flow velocity of 1

m/s and the inlets of the two pipes on the same side, the temperature gradient along the 987 mm length of the stave can be controlled within 5°C. When the inlets are set on both sides, the maximum temperature on the stave is reduced, but the temperature difference between adjacent two sensors in the transverse direction increases. In both cases, providing a cooling flow velocity of 1 m/s with pipe inner diameter of XXX, the water cooling meets the detector's requirements.

In additional to the water cooling, two phase CO_2 flow cooling is an alternative solution, where the CO_2 undergoes a phase change from liquid to gas. This phase transition allows for more heat to be carried away, enabling the use of thinner cooling pipes and a smaller quantity of refrigerant, especially in terms of mass. However, since water cooling has already met the requirements and considering the overall system simplicity, water cooling was chosen as the baseline for the current design.

5.3.4.2 Endcap local support for CMOS strip detector

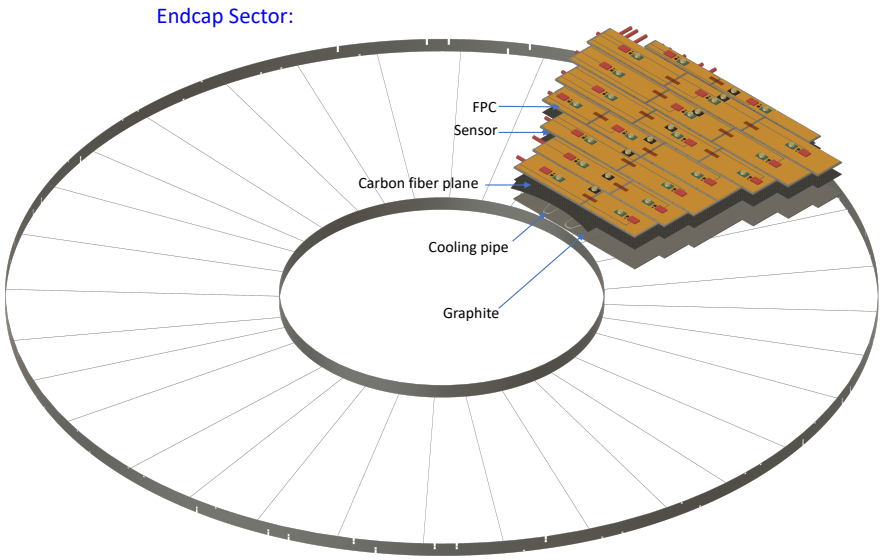


Figure 5.49: ITK endcap mechanics and cooling

The ITK endcap support frame for the CMOS strip detector is designed with minimal material to support 16 sectors (1/8 disk detector structures) across two half-endcaps, as shown in Fig. 5.49. The frame, made of aluminum, comprises an inner structural ring and an outer structural ring connected by thin metal bars.

Each sector covers ∼1/8 of the endcap disk area, including both the detection units and the cooling plate:

- Sensor Modules: These consist of sensors glued onto flexible printed circuits (FPCs) integrated with associated electronics.
- Cooling Plate: A carbon fiber plate embedded with cooling pipes that are in direct thermal contact with the chips to efficiently dissipate heat. Two closed-loop cooling circuits are used for sector cooling, with the inlets and outlets of the circuitry located at the same end of the sector. Thermal contact is enhanced by a layer of graphite foil. to

improve structural rigidity, an additional thin layer of carbon fleece is applied to both faces of the cooling plate.

5.3.4.2.1 Materials The materials used for the ITK endcap sector is similar to those used in the ITK barrel stave. The Cooling Plate is constructed from a carbon fiber plate with high thermal conductivity, and its thermal performance is further enhanced by a layer of graphite foil, which provides excellent thermal conductivity in the transverse direction. Water circulated through polyimide cooling pipes has been selected as the baseline cooling medium. Table 5.9 lists the estimated contributions of the ITK endcap sector to the material budget. The overall estimated material budget for a sector is 0.537% X_0.

Estimation of ITK endcap sector material contributions					
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64	28.41	0.013
	Cooling fluid	Water		35.76	0.105
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Total					0.537

Table 5.9: Estimation of ITK endcap sector material contributions

5.3.4.2.2 Structural characterisation

5.3.4.2.3 Thermal characterisation

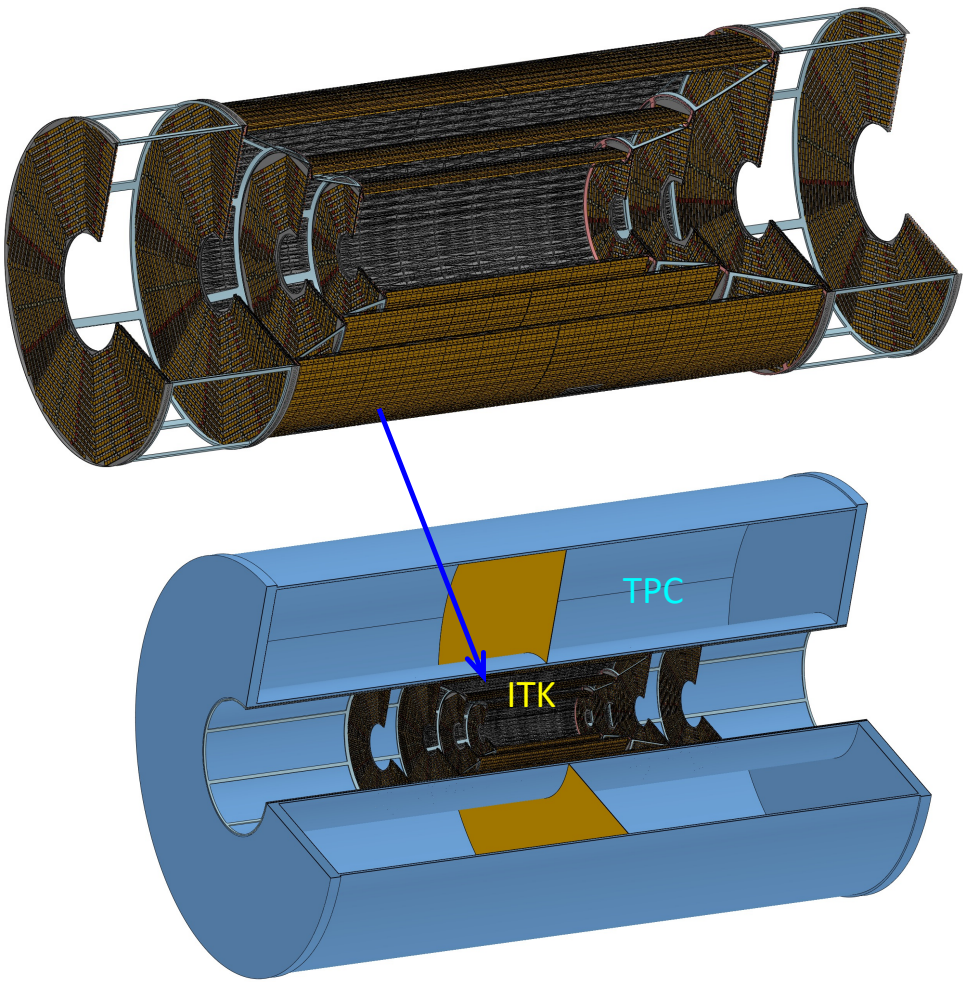


Figure 5.50: ITK installation

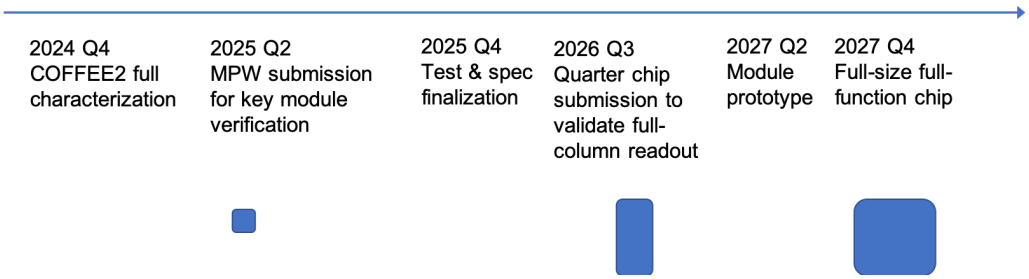


Figure 5.51: Timeline of HVCMOS development.

5.3.5 Prospects and plan

Responsible person: Qi YAN, Yiming LI, and Xin SHI

5.3.5.1 Development of the CMOS pixel sensor

For the sensor technology regarding the HVCMOS process, the priority in the coming few year is to develop a full-functional full-size sensor chip that meets the requirements imposed by the CEPC inner tracker. The development will be performed through a few iterations of chip submissions, including:

- A small pixel array which implement the targeted readout architecture (early 2025);
- One of more small prototypes for performance optimisation (2026);
- A large chip that meets or very close to the production version (2027).

With the small-scale sensor chip key performance will be studied and input will be provided for detector final design and prototyping. A timeline of HVCMOS development is illustrated in Fig. 5.51. The priority is to produce a full-functioning full-scale pixel sensor chip in approximately 3 years time, which will satisfy the key parameters as listed in Table 5.10.

Parameter	Value
Pixel size	$34\,\mu\text{m} \times 150\,\mu\text{m}$
Reticle size	$2\,\text{cm} \times 2\,\text{cm}$
Array size	512×128
Time resolution	3-5 ns
Power consumption	200 mW/cm^2

Table 5.10: Key specification of the HVCMOS sensor chip for CEPC inner tracker.

In the specifications the timing resolution of a few nanoseconds, motivated by the need of tagging the 23 ns bunch crossings, is particularly challenging especially in combination of the moderate power consumption. Novel readout architecture will be implemented, which is data-driven with in-pixel fine TDC. This will fully exploit the potential of small feature size of 55nm that allows more functionality in the limited pixel area. A diagram of the readout architecture design is illustrated in Ref 5.52.

For the current HVCMOS process of the COFFEE series (as illustrated in Fig. 5.5), the N-well of the PMOS transistor is directly in contact with the charge-collecting deep N-well. The flipping of the PMOS transistor could result in a voltage change in the deep N-well which is in turn enhanced by the front-end amplifier. The cross-talk effect could be largely mitigated by adding a deep p-type layer separating the N-well and charge collection electrode. Opportunity of process modification to allow such separation (”four-well process”) will be pursued with possible foundries. In the most pessimistic case that no modification is possible for the project’s timescale, dedicated design will be prepared to address the cross-talk issue. A possible solution is to keep only NMOS transistors in pixels. Next prototype with NMOS-only pixel array is being designed for the next MPW. Process modification with reduced cross-talk is preferred as it will allow more flexibility and funcionality for circuitry within each individual pixel.

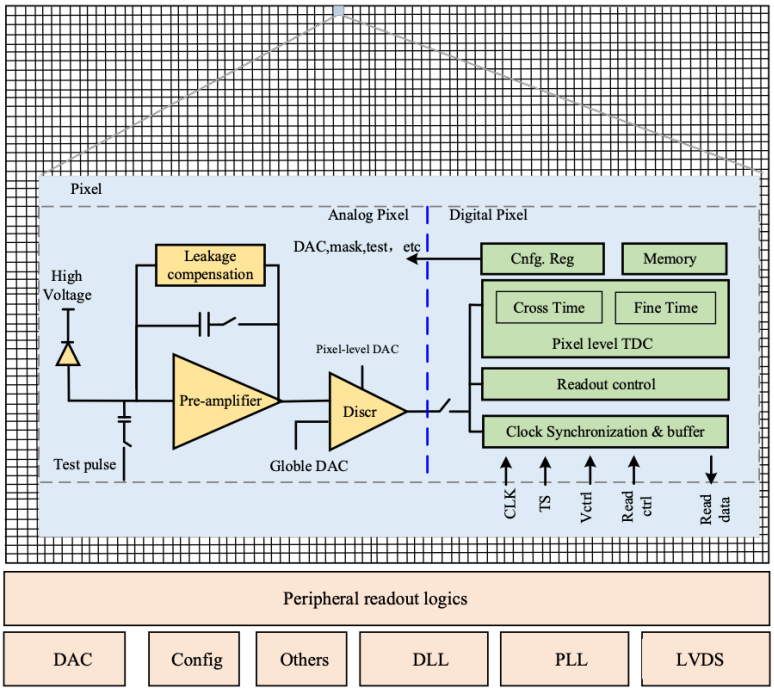


Figure 5.52: Block diagram of HVCMOS sensor readout architecture.

5.3.5.2 Development of the CMOS strip sensor

The research and development timeline of CMOS Strip Chip for the next three years is listed in Fig. 5.53 where three versions of the CSC are scheduled to be fabricated. The CSC1 will be mainly focus on the independent CMOS strip sensor and front-end electronics separately. A preliminary reticle design for the CSC1 is sketched in Fig. 5.54. Once the devices are fabricated, a detailed evaluation of the macroscopic characteristics such as leakage current and capacitance as the function of bias voltage for the CMOS strip sensor (CSC1-A) will be carried out. In addition, the collected charge of the CSC1-A will be determined for both before and after irradiation. For the readout ASIC (CSC1-B), the initial noise and gain will be investigated utilizing customized testing board.

The CSC2 will explore the integration of CMOS strip sensors and circuits together on small area and large pitch, where the special attention need to be taken in terms of exploring the best strategy to separate the sensor with the active circuits when the sensor is applied high bias voltage. Finally, the target of the CSC3 will be the integration of large-area (2cm $\times$ 2cm) and narrow-pitch (20μm) monolithic chip in which a working solution to prevent the cross-talk between each strip need to be consolidated.

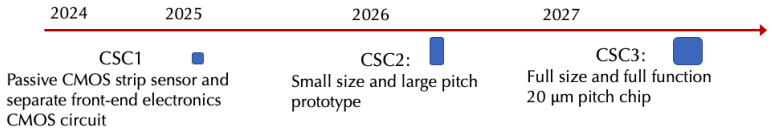


Figure 5.53: CSC Research Timeline.

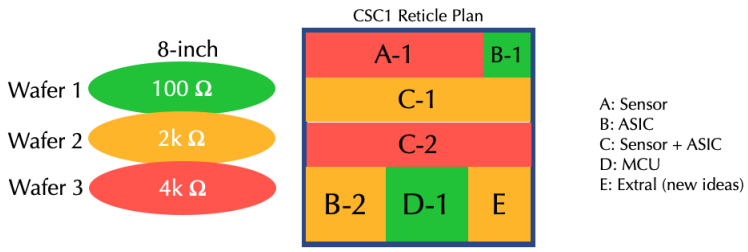


Figure 5.54: CSC1 Reticle Design.

5.3.5.3 Module and system level development

The prototyping of the detector modules, including the integration process, the supporting and cooling structure will be carried out in parallel to the development of the sensor chips. Small scale sensor chip can already be used to assemble prototypes with sensor, readout and supporting structures as key intermediate steps.

As the full-sized sensor prototype will be only available after a few submissions, most prototyping studies can be carried out with dummy silicon sensors with the similar size and thickness. Certain traces can be added on the dummy sensors to allow definition of assembly steps, especially with automatic gantry system. Such systems already exist in the participating institutes for silicon detector assembly such as the L0 upgrade of the AMS experiment, and can be easily converted to other uses. The dummy sensors, together with extra components dissipating heat, will be useful for thermal and mechanical studies.

5.4 Outer silicon tracker (OTK) with TOF

Responsible person: Qi YAN

The OTK is the outermost tracking detector, consisting 1 barrel layer and 1 endcap layer, as shown in Fig. 5.2, covering an area of $\sim$85 m^2. Positioned close to the calorimeter, the OTK maximizes the lever arm, enhancing the momentum resolution, and reduces the extrapolation distance between the last tracking measurement and the calorimeter shower. OTK also serves as a time of flight detector in the CEPC detector system. Accurate particle velocity measurements benefit from a long flight path. In dense collision environments, achieving precise time measurements for each charged particle requires a high granularity time detector, especially for dense jets. The outermost layer of the CEPC tracking detector employs microstrip detectors based on AC-coupled Low Gain Avalanche Detector (AC-LGAD) technology to precisely measure both the timing and position of charged particles.

This section provides a detailed description of the CEPC OTK. Subsection 5.4.1 highlights the R&D efforts related to AC-LGAD, including the development of both AC-LGAD sensor and its readout ASIC. The baseline design of the CEPC OTK is detailed in Subsection 5.4.2. Subsection 5.4.3 focuses on the OTK readout electronics, followed by Subsection 5.4.4, which addresses the mechanical and cooling design of the OTK. Lastly, Subsection 5.4.5 outlines the future prospects and plans for the OTK.

5.4.1 AC-LGAD sensor and ASIC R&D

5.4.1.1 AC-LGAD Sensor R&D

Responsible person: Mei ZHAO

Low Gain Avalanche Detectors (LGADs) have demonstrated excellent timing performance, making them essential for precise timing measurements in particle physics experiments. LGAD detectors have been selected for use in the ATLAS HGTD and CMS ETL timing layers to address pile-up issues in the HL-LHC experiment. The timing resolution and collected charge of LGADs from various vendors, both before and after irradiation, are shown in Fig. 5.55. The IHEP LGAD achieves a collected charge greater than 15 fC (4 fC) and a timing resolution of less than 35 ps (50 ps) before (after) irradiation at a fluence of $2.5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, which will contribute to 90% of the sensor production in the ATLAS HGTD project.

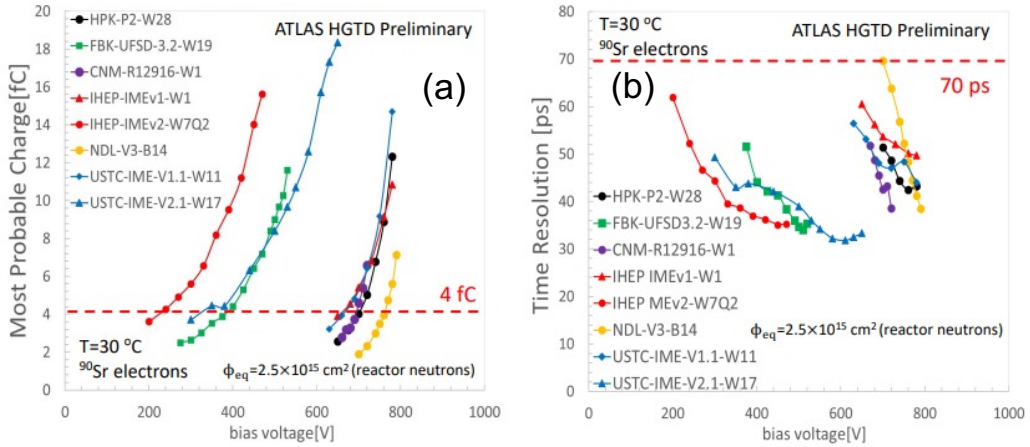


Figure 5.55: Timing resolution and collected charge before and after irradiation (test results from HGTD group)

Beam test results conducted by the HGTD group at the CERN SPS beamline, shown in Fig. 5.56, also demonstrate that LGADs can deliver a timing resolution better than 35 ps before irradiation and maintain a timing resolution better than 50 ps after irradiation.

Despite good timing capability, LGADs face limitations in achieving high-precision spatial resolution due to pixel size constraints. Moreover, the Junction Termination Extension (JTE) and P-stop structures between pixels result in dead

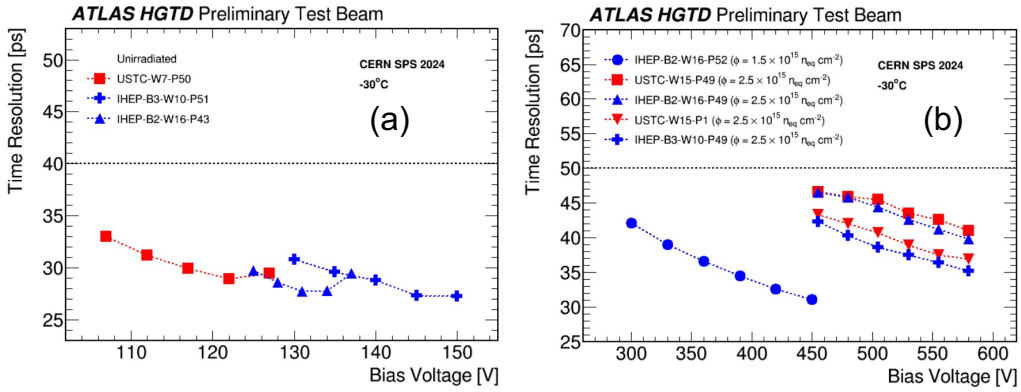


Figure 5.56: Timing resolution before and after irradiation (test beam results from ATLAS HGTD group)

zones within the detectors. To address these challenges and minimize the dead area, AC-Coupled LGADs (AC-LGADs) have been developed as an advancement of LGAD technology.

In AC-LGADs, AC coupling electrodes and a dielectric layer are placed above the n+ layer of the LGAD, as illustrated in Fig. 5.57. When a particle pass through the detector, the induced charge is distributed among electrodes near the impact point. By using signals from collected by electrodes, the particle's impact position can be accurately reconstructed. This enables AC-LGADs to provide high-precision timing and spatial measurements while achieving a nearly 100% fill factor.

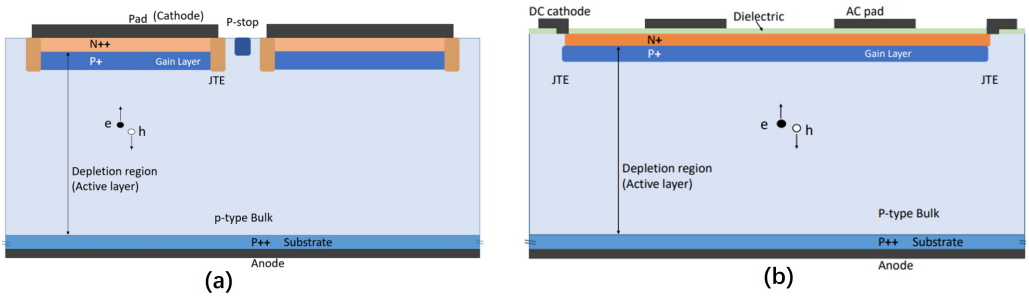


Figure 5.57: structures of (a) standard LGAD and (b) AC-LGAD

AC-LGADs have been studied by many research institutes and companies including FBK, CNM, BNL, INFN,IHEP, USTC, etc[]. They offer the ability for 4D tracking and can function as time-of-flight detectors[]. Additionally, the AC-LGAD with strip-shaped readout electrodes reduce the number of readout channels while delivering excellent spatial resolution in the bending direction. With the combination of high spatial resolution and granularity as time-of-flight detector, AC-LGAD strip detector has been chosen as the outer tracker and time-of-flight detector for the CEPC.

Extensive R&D efforts have been undertaken at IHEP to advance the development of AC-LGADs. The process and structural parameters of AC-LGAD devices have been extensively simulated using TCAD software. These simulations explore the impact of various process parameters and structures on AC-LGAD performance. The details of these simulations are described in Subsection 5.4.1.1.1. Two types of prototypes have been fabricated and studied: pixelated AC-LGADs with varying process parameters and strip AC-LGADs with different pad-pitch sizes. Testing setups using TCT laser scans and Beta tests have been established, as outlined in Subsection 5.4.1.1.2. The pixelated AC-LGAD prototypes are used to evaluate fabrication process parameters and their effects on sensor performance, including charge collection and timing. This is discussed in Subsection 5.4.1.1.3. The strip AC-LGAD prototypes are designed to study the influence of pad-pitch size on spatial and timing resolution, detailed in Subsection 5.4.1.1.4.

5.4.1.1.1 AC-LGAD simulation Simulations of AC-LGAD devices were performed using a TCAD software incorporating all key structural components, such as the n+ layer, gain layer, AC coupling dielectric, and metal pad. The simulated model structure is shown in Fig. 5.58. These simulations focus on AC-LGAD-specific structures that differ from standard LGADs and significantly impact timing and spatial resolution.

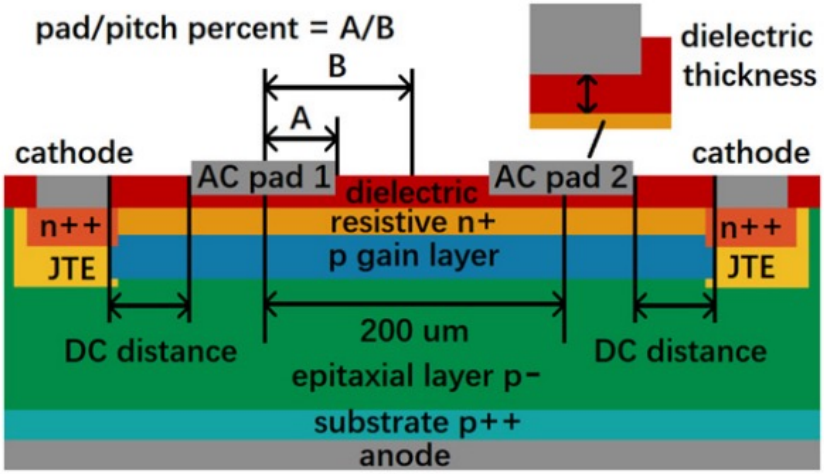


Figure 5.58: Sketch of AC-LGAD with 2 AC pads

Key findings include:

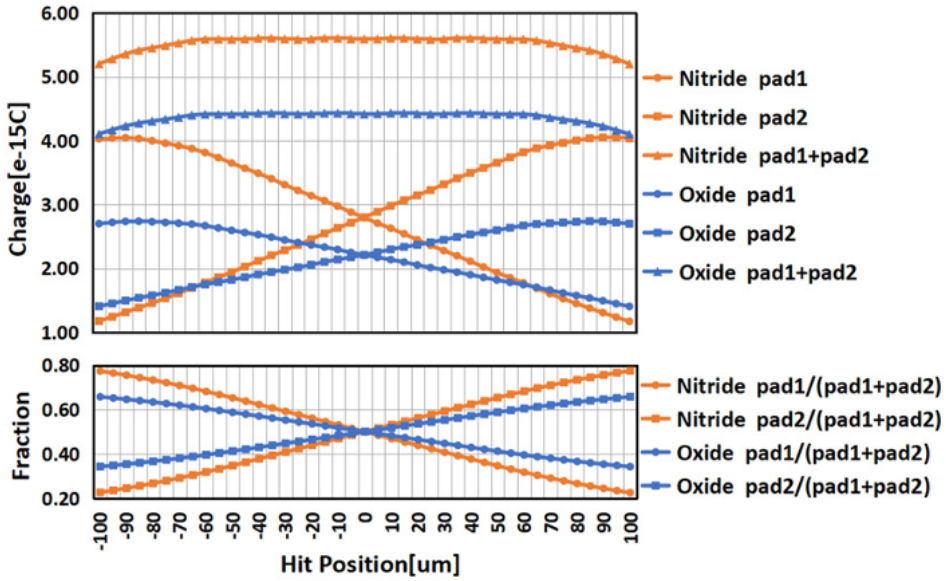


Figure 5.59: Charge collection of two pads for 2 different dielectric materials: oxide and nitride

- The n+ layer dose affects signal shape, spatial resolution, and charge sharing between electrodes. Lowering the n+ dose improves spatial resolution (Fig. 5.59.).
- Variations in dielectric material and thickness also influence spatial performance (Fig. 5.60).
- Other structure parameters, such as metal pad-pitch size, were simulated for its effects on performance. More details are available in the referenced publication [].

Based on the simulation results, R&D prototypes were produced for further study. Testing systems were established to verify the timing and spatial resolutions of AC-LGAD devices.

5.4.1.1.2 Testing setup The testing platforms, utilizing TCT laser scans and Beta tests, are illustrated in Figs. 5.61 and 5.62. These setups include readout boards, amplifiers, oscilloscopes (Teledyne LeCroy HDO9204 with 2 GHz bandwidth and 20 G/s sampling rate), laser sources, and Beta sources. Signals from AC-LGAD electrodes are processed through preamplifiers and recorded by the oscilloscope.

For the TCT laser scan, a picosecond laser pulse with a wavelength of 1064 nm strikes the AC-LGAD strip at a

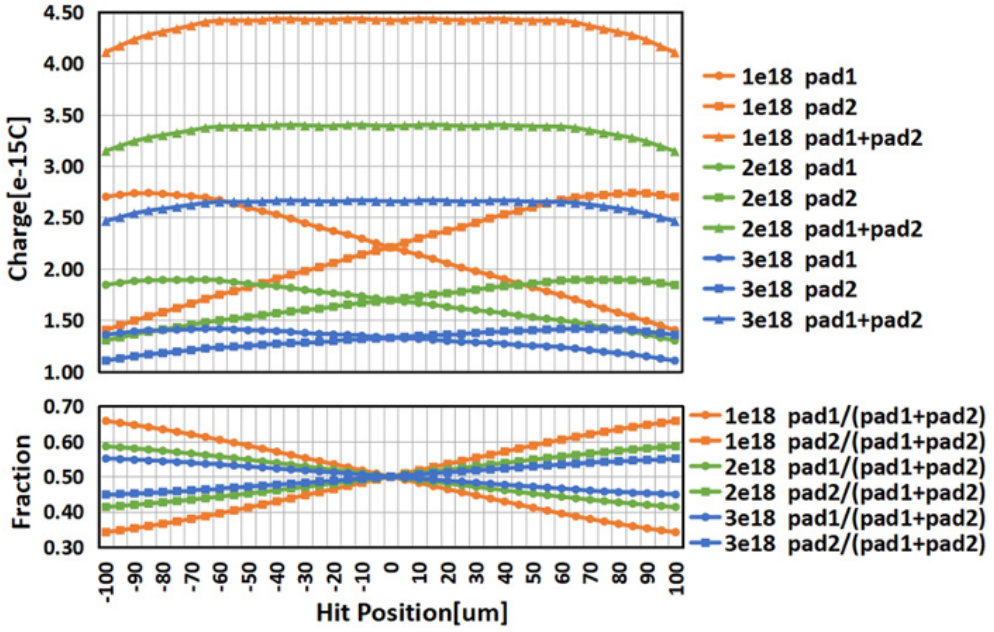


Figure 5.60: Charge collection of two pads for 5 different values of n+ dose: $1 \times 1018cm - 2$,$2 \times 1018cm - 2$ and $3 \times 1018cm - 2$

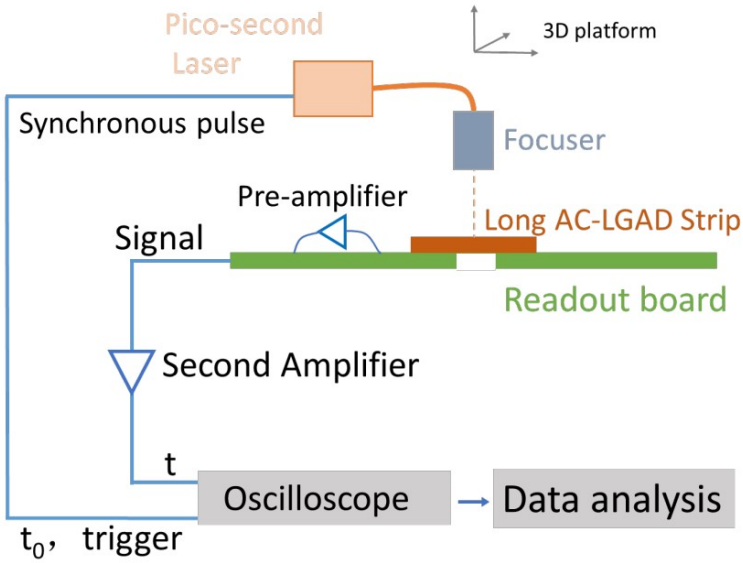


Figure 5.61: The schematic of the TCT testing platform

frequency of 20 MHz via a focuser. The focuser, mounted on a precision pinning table, achieves movement accuracy better than 1 μm. The laser scan begins at the upper edge of stripe electrode 1 and concludes at the lower edge of stripe electrode 4, advancing in μm steps. At each point, 1,000 waveforms are recorded before proceeding to the next position. The laser spot size is maintained within 1.5 μm throughout the scan.

The timing resolution of the AC-LGAD strip sensor (σ_t) consists of the following components:

$$\sigma_t^2 = \sigma_{\text{TimeWalk}}^2 + \sigma_{\text{Landau}}^2 + \sigma_{\text{Jitter}}^2 \tag{5.1}$$

- Time walk effect (σ_{TimeWalk}): Variations in signal amplitudes from different hits cause time walk, which can be mitigated using the Constant Fraction Discriminator (CFD) method.
- Energy deposition fluctuation (σ_{Landau}): Non-uniformities in energy deposition due to Landau fluctuations contribute to timing uncertainty as particles traverse the detector.
- Noise jitter (σ_{Jitter}): Noise in the electronic components during signal propagation and collection contributes to

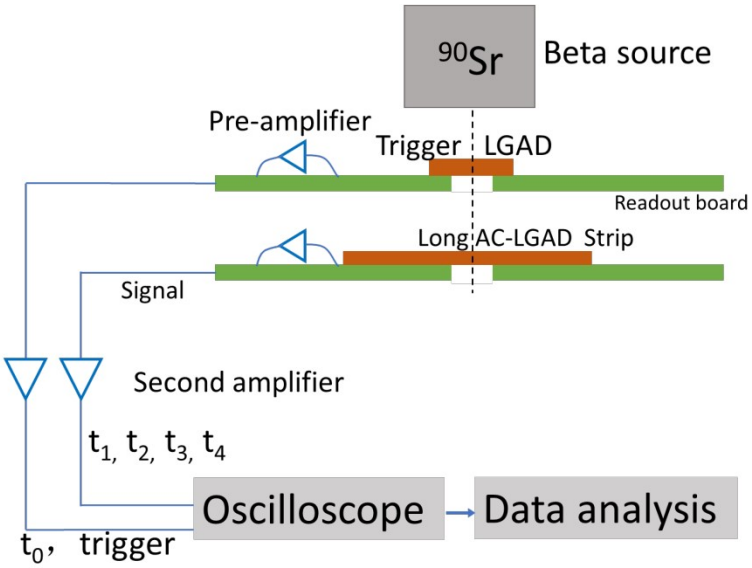


Figure 5.62: The schematic of the Beta testing platform

this term.

Since the laser hit does not involve ionization energy deposition, the TCT scan can only investigate the Jitter term. The contribution of the Landau term is analyzed separately using Beta tests.

To measure the timing resolution of the device under test (DUT), a trigger LGAD with a timing performance of 28.5 ps is used as the reference device. Once signals from both the trigger LGAD and the AC-LGAD strip are recorded, the variation in the flight time of a minimum ionizing particle (MIP) between the trigger LGAD and the AC-LGAD is calculated and defined as ΔT.

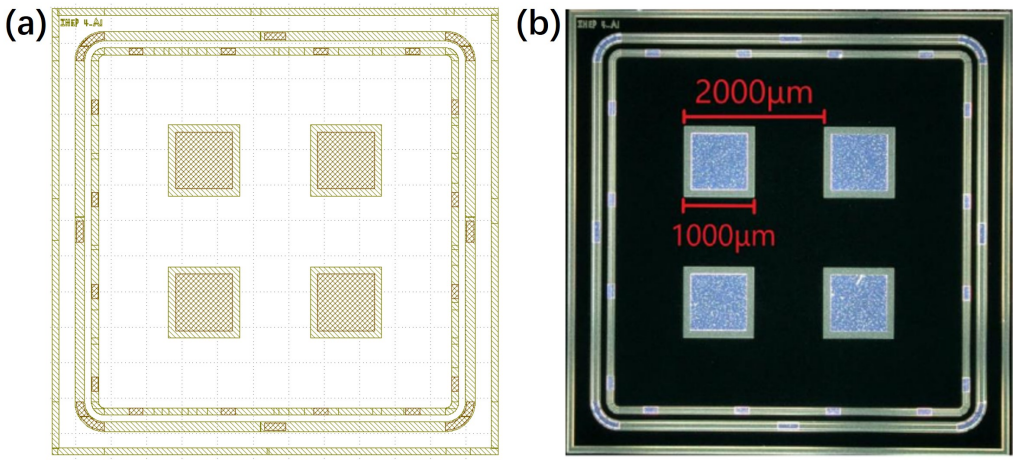


Figure 5.63: Pixelated AC-LGAD prototype

5.4.1.1.3 Pixelated AC-LGAD prototypes The pixelated AC-LGADs are fabricated on 8-inch wafers with a 50 μm P-type epitaxial layer and a 725 μm substrate. These AC-LGADs include four square AC pads for AC-coupled signal readout, as illustrated in Fig. 5.63. The innermost ring serves as the DC ring (DC-cathode), while the second ring is a guard ring. The DC-cathode can be utilized for DC-coupled signal readout or grounded during testing. The AC pads have a size of 1000 μm, with a pitch size of 2000 μm.

To investigate the effects of N+ dose on spatial and timing resolution, five types of sensors were designed with varying doses: 10.0 P, 5.0 P, 1.0 P, 0.5 P, and 0.2 P. Here, "P" represents the phosphorus dose unit specific to the IHEP AC-LGAD.

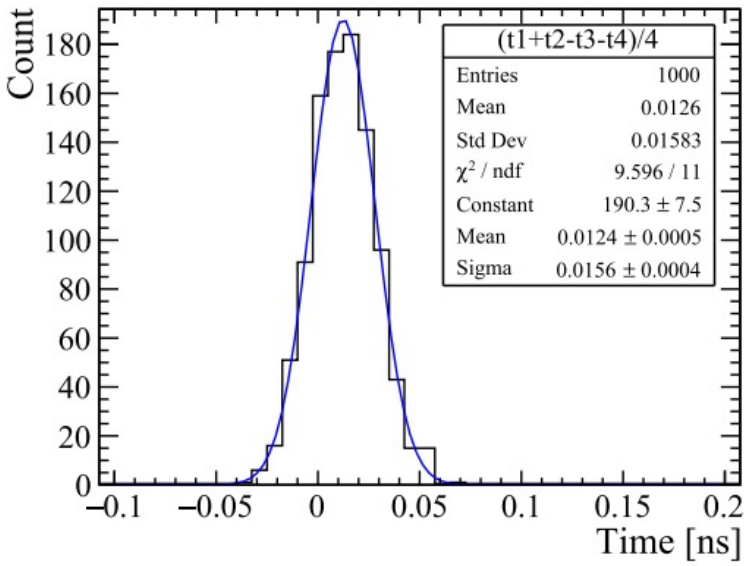


Figure 5.64: Distribution of $(t_1 + t_2 - t_3 - t_4)/4$ at one position in 6×6 laser test array

Timing performance To minimize the impact of trigger jitter, $(t_1 + t_2 - t_3 - t_4)/4$ is used to calculate the time resolution of AC-LGAD sensors. Figure 5.64 shows the distribution of $(t_1 + t_2 - t_3 - t_4)/4$, yielding a time resolution of 15.6 ps. This measurement, derived from laser tests, only accounts for the jitter component. Figure 5.65 displays the jitter component of the timing resolution across different N+ doses, which shows a slight variation between 15 ps and 17 ps.

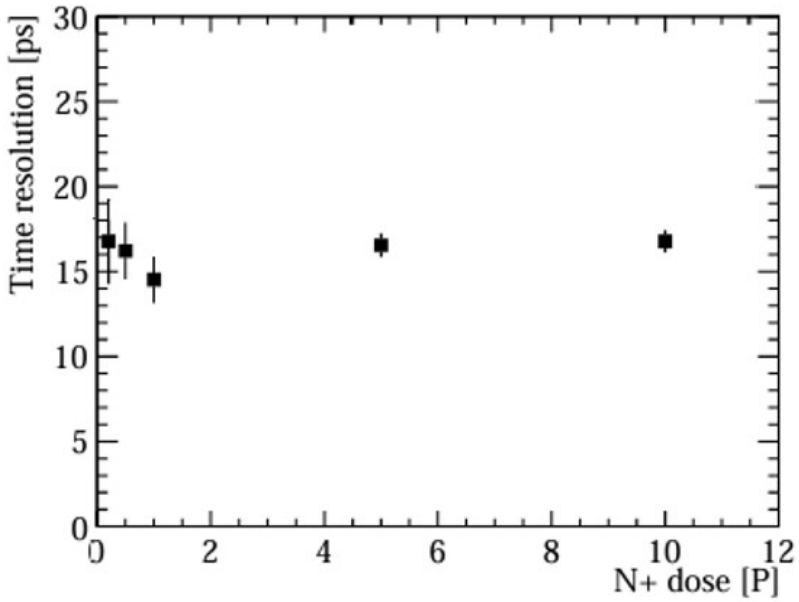


Figure 5.65: The jitter component of the time resolution with different N+ doses

Spatial resolution The hit position (X,Y) of a laser or particle is determined by the charge or amplitude imbalance between the AC pads along the X and Y directions. During the laser induced signal process, the sensor can be considered as a Discretized Positioning Circuit (DPC).

The reconstructed positions of a 6×6 laser test array for a sensor with a dose of 0.2 P are shown in Fig. 5.66, along with the laser spot positions measured by the TCT stage. By comparing the reconstructed laser injection positions with the actual injection positions, the differences are calculated. The standard deviation (sigma) of these differences defines the spatial resolution. The measured spatial resolution of pixelated AC-LGAD sensors is presented in Fig. 5.67.

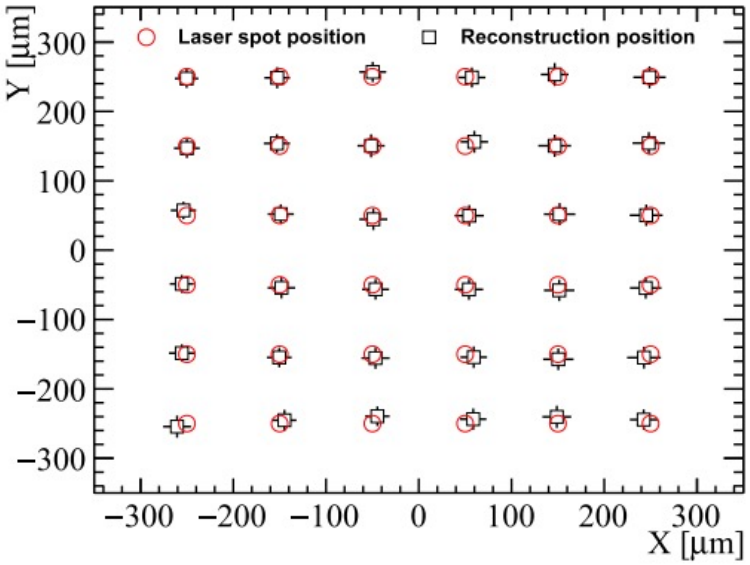


Figure 5.66: Reconstruction position of 6×6 laser test array of sensor with dose 0.2 P (black squares) and the laser spot position as measured by the TCT stage (red circles)

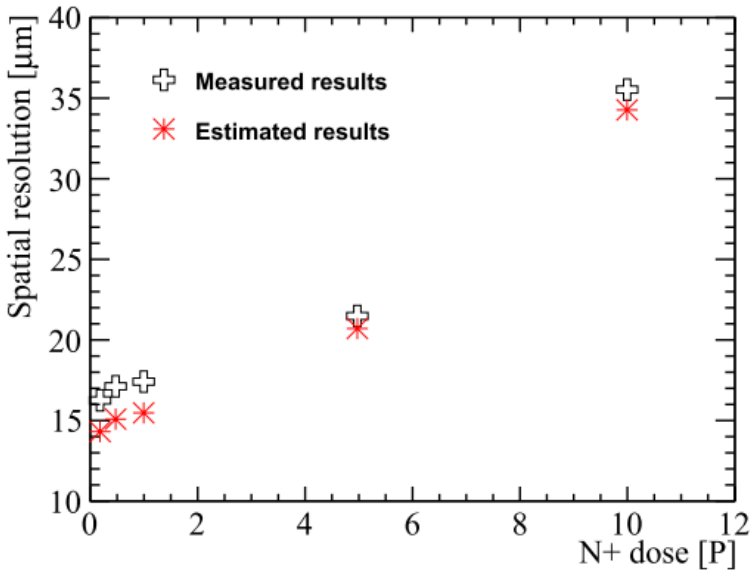


Figure 5.67: The measured spatial resolution (black marks) and estiamted spatial resolution (red marks) at different N+ doses.

5.4.1.1.4 Strip AC-LGAD prototype and properties A strip AC-LGAD prototype has been designed and fabricated by IHEP, featuring strip electrodes with a length of 5.65 mm. The timing and spatial resolutions of the long strip AC-LGADs have been investigated through laser and beta tests.

The strip AC-LGAD device consists of strip electrodes, a dielectric layer, DC electrodes, an N+ layer, a P+ layer, a P-type bulk, a P++ layer, and an aluminum anode, as illustrated in Fig. 5.68. The AC-LGAD strip sensor with a total thickness of 775 μm, includes a 50 μm P-type epitaxial layer (active layer). The length of the strip electrodes is 5.65 mm. The schematic of the long strip AC-LGAD is illustrated in Fig. 5.69. Three pitch sizes of 250 μm, 200 μm, and 150μm are designed, with the width of the strip metal electrodes being 100 μm.

The breakdown voltage of the device is 385 V, with a leakage current on the order of 10 nA. The capacitance value is 28.9 pF when fully depleted. The Vgl of the AC-LGAD strip is 21.5 V, and Vfd is 34.8 V. The capacitance between

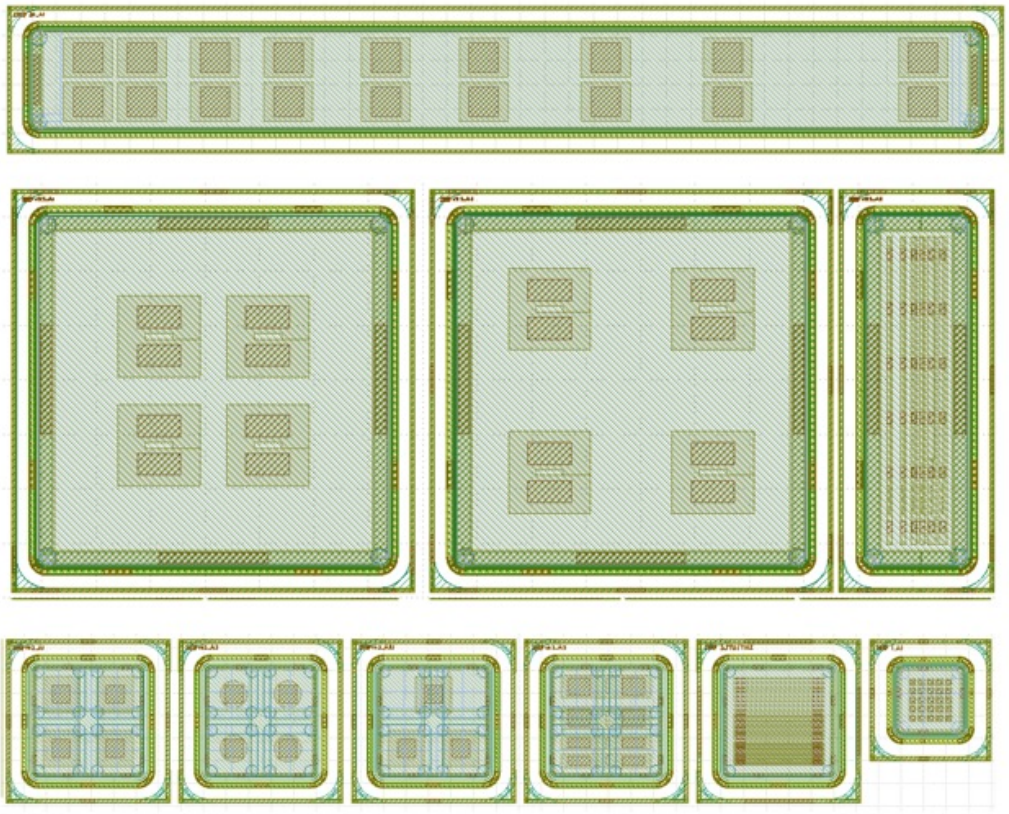


Figure 5.68: Strip AC-LGAD prototype

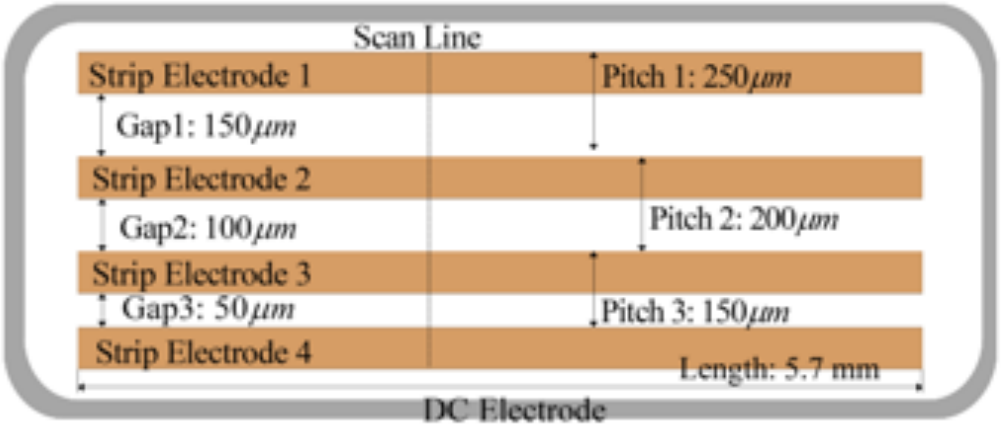


Figure 5.69

the strip electrodes and the DC electrode/N+ layer is measured to be 170±0.2 pF. The timing resolution of the sensor has been tested using both laser and Sr-90 beta sources.

Timing performance from Laser testing The timing resolution of the AC-LGAD strip can be calculated from the histogram of $(t_1 - t_2)/2$ of 1000 waveforms. Here t_1 and t_2 are the cross-threshold times of strip electrodes 1 and 2, obtained using the constant fraction discriminator (CFD) method. The timing resolution is defined as the sigma of the distribution of $(t_1 - t_2)/2$. The distribution of $(t_1 - t_2)/2$ is shown in Fig. 5.70. Timing resolutions of the AC-LGAD sensors with pitch as 250 μm, 200 μm, and 150 μm are 14.8 ps, 14.7 ps, and 14.8 ps, respectively.

Timing performance from Beta testing For the beta test, a calibrated LGAD (trigger LGAD) is placed above the AC-LGAD strip as the trigger, and a 90Sr beta source is placed above the trigger LGAD as the particle source. From

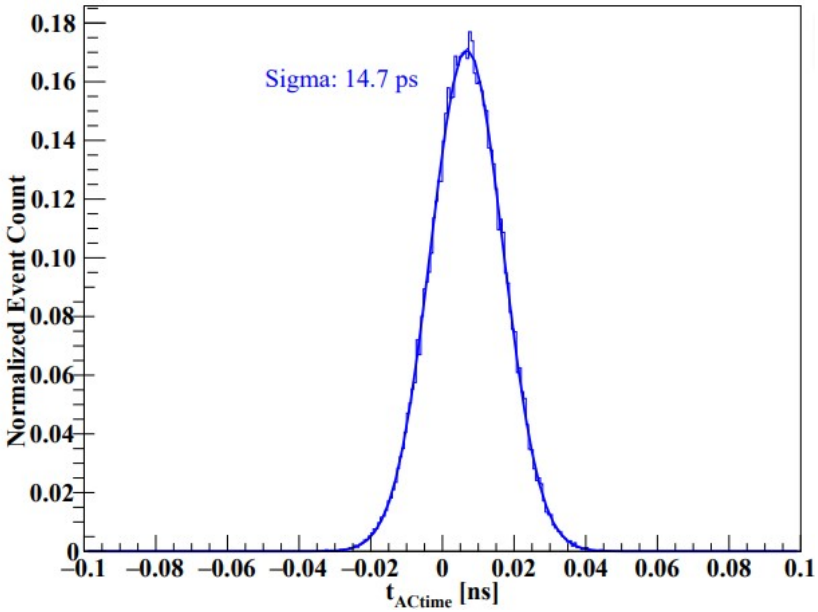


Figure 5.70: Distribution of $t_{ACtime} = (t_1 - t_2)/2$. The sigma of the distribution is 14.7 ps.

the testing, ΔT is calculated as the time difference between the arrival times of signals from the trigger LGAD and the AC-LGAD strip device, as

$$\Delta T = T_{trigger} - \frac{\sum_i a_i^2 T_i}{\sum_i a_i^2} \tag{5.2}$$

where T_i and $T_{trigger}$ are the arrival times of signals measured on strip electrodes 1, 2, 3, and the trigger LGAD, and a_i is the signal amplitude of strip electrode 1, 2, or 3. This amplitude weighting emphasizes the contribution of the strip electrode closest to the hit point, improving the timing resolution by reducing the effects of noise.

The timing resolution of the AC-LGAD strip is calculated using the equation:

$$\sigma_{AC-LGAD} = \sqrt{\sigma_{\Delta T}^2 - \sigma_{trigger}^2} \tag{5.3}$$

The distribution of ΔT is shown in Fig. 5.71, with a sigma of 47.1 ps. Considering the timing resolution of the trigger LGAD is 28.5 ps, the AC-LGAD strip has a timing resolution of 37.6 ps.

Spatial resolution The TCT method is used for studying the spatial resolution of the AC-LGAD strip device. The amplitude of the signal induced by the laser decays with distance from the electrode, which leads to variations in the signal amplitudes (collected charge) across the four electrodes. The position reconstruction method relies on the variation in signal amplitudes between the two strip electrodes closest to the hit position. When the laser or particles hit gap 1, the signal amplitudes of electrodes 1 and 2 change with the hit position. The hit positions are characterized by the ratio R:

$$R = \frac{a_2}{a_1 + a_2} \tag{5.4}$$

To obtain the spatial resolution, 1000 waveforms per laser hit position are recorded, resulting in 1000 reconstructed positions per laser hit position. The difference between the reconstructed and laser hit positions for all hits in the gap is plotted as a histogram. The sigma of the fit corresponds to the spatial resolution of the gap. Figure 5.72 shows the histogram of the differences between the reconstructed and true positions. The spatial resolutions of the AC-LGAD with pitch sizes of 250 μm, 200 μm, 150 μm are 12.8 μm, 10.9 μm, and 8.3 μm, respectively.

Summary The AC-LGAD strip detectors, characterized by their lower readout electronic density, exhibit significant potential for application in future colliders. IHEP has designed a long AC-LGAD strip prototype with a length of 5.7 mm with three pitch sizes. Laser TCT scanning tests and beta tests were conducted to investigate the variations in spatial and timing resolutions for different pitch sizes. Experimental results show that the timing resolution is around 37.6 ps, and the

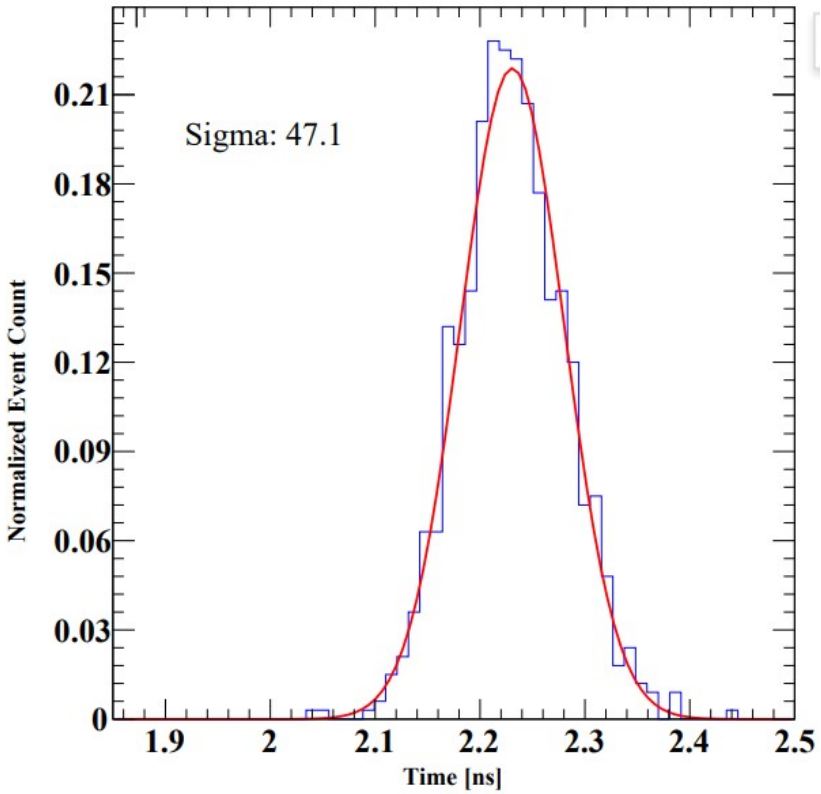


Figure 5.71: Distribution of ΔT of strip electrode 2 (strip with pitch as 200 μm). The sigma of the distribution is 47.1 ps.

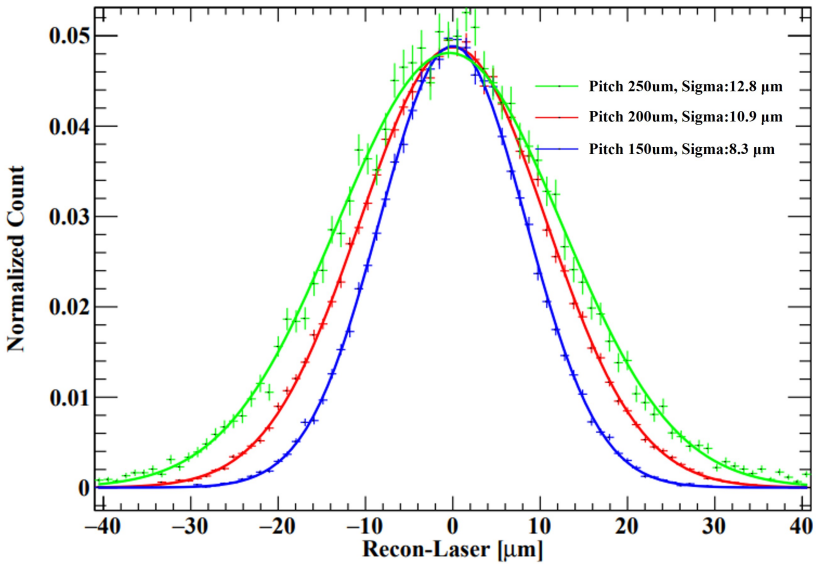


Figure 5.72: Spatial resolution of strip LGAD with different pad-pitch size,the resolutions of gap 1, gap 2, and gap 3 are 12.8 μm, 10.9 μm, and 8.3 μm, respectively.

pitch size has no significant effect on the jitter component of the timing resolution, which remains around 14.7 ps. The spatial resolutions of the long AC-LGAD strip with pitch sizes of 50 μm, 200 μm, and 250 μm are 8.3 μm, 10.9 μm, and 12.8 μm, respectively. The spatial resolution can be improved by reducing the pitch size. The performance of the long AC-LGAD strip makes it a promising choice for 4D trackers in future particle physics experiments.

5.4.1.2 AC-LGAD ASIC R&D

Responsible person: Xiongbo YAN

This section describes the required performance, design, and latest prototype testing of the ASIC chip, which will have 128 readout channels in future. The main challenge in the design of this ASIC is a high time resolution for time measurement and charge resolution for position, in order to match the excellent performance of the LGAD. The time contribution comes mainly from the jitter and the time walk. The most critical aspect concerning the jitter is the design of the analog front-end electronics, which are composed of a transimpedance amplifier followed by a shaper and a fast discriminator. The measured time-of-arrival (TOA) and time-over-threshold (TOT) are digitized using two time-to-digital converters (TDCs), and stored in a local memory at the channel level. The TOT can be recognized as charge because the charge is related to the time over a certain threshold. The charge resolution is determined by time resolution and TOT width. The contribution of time walk will be addressed by applying a correction based on the fact that the variations in the TOA of the pulse are related to the TOT. The ASIC common digital part is composed of clock generator and alignment, slow control configuration and data transimission. A prototype chip has been produced and will be tested so far: OTKROC, integrated 8 channels, with the preamplifier and the discriminator, TDC and digital components. The chip will be test in the end of 2024.

The requirements imposed by the data taking conditions, the sensor and the targeted performance are presented first in Section 5.4.1.2.1. The ASIC architecture is described in Section 5.4.1.2.3, first going through the single-channel architecture and then the entire ASIC. Section 3.3 describes in detail the design of the single-channel readout electronics, followed by the description of the ASIC common digital part in Section 3.4. The radiation tolerance is described in Section 3.5 and the power distribution in Section 3.6 The performance results obtained so far in test bench and test beam are described in Section 3.7. The description of the monitoring can be found in Section 3.8. Lastly, a brief account is given of the future steps towards the completion of the design and testing of the ASIC in Section 3.9.

5.4.1.2.1 General requirements The requirements of the ASIC can be divided into two types. On one side the considerations regarding the operational environment of the ASIC, its powering and electrical connections. These requirements are summarized in Table 5.11. The second group concerns the ASIC performance, driven by the targeted time resolution. A summary of these requirements is presented in Table 5.12.

- The target for the electronics is to be able to read out signals from 16 fC up to 50 fC throughout the lifetime.
- Each readout channel needs to match the sensor strip, with a pitch of 100um. It will be capable of handling up to 5 μA leakage current from the sensor.
- The electronics jitter is required to be smaller than 30 ps for an input charge of about 16 fC, that is smaller than intrinsic dispersion of LGAD. A detector capacitance of about 4 pF is considered. The TDC bin size for TOA measurement should be less than 30 ps, thus the contribution from TDC will be negligible. The time walk should be smaller than 10 ps over the dynamic range after correction.
- The charge measurement is applied by TOT measurement. A resolution of 1.6 fC is necessary for a special resolution of 10 um. The bin size for TOT will be the same as TOA, thanks to the reusing of delay chain.
- The TOA and TOT information are transferred to the data acquisition system, therefore integrating the protocol of data aggregation is necessary.
- The charge generated by MIP will be shared by adjacent strips, it should be possible to set the discriminator threshold for small enough values of input charge. The minimum threshold (4 fC) should provide an efficiency above 95
- The ASIC will have to withstand high radiation levels. The expected radiation levels have been presented before, considering a safety factor for the electronics leading to a maximal TID of ? MGy

5.4.1.2.2 Data transmission bandwidth requirements The required bandwidth of the readout e-link of each ASIC strongly depends on the radial region it covers at barrel or endcap, as shown by the distribution of the average number of hits per ASIC in Figure ?. The number of bit per hit is 48 as described in Section ?. Each module consisting of 2 slides of sensors, and each sensor needs 8 ASICs to readout. 16 ASICs are on one FE board, and are connected to a aggregation chip TaoTie. 4 FE boards connect to a Concentrator Card (CC) via flex cables and connectors. The CC transfers digital

Voltage	1.2 V
Channel	128
Channel pitch	< 100 µm
Power dissipation per area (per ASIC)	300mW/cm2
e-link driver bandwidth	320 Mbps, 640 Mbps, or 1.28 Gbps
Temperature range	-40 °C to 40 °C
TID tolerance	1.0 MGy

Table 5.11: Geometrical, environmental, electrical and power requirements for the OTK ASIC

Maximum leakage current	5 µA
Single channel noise (ENC)	$<$ 10000 e = 1.6 fC
Cross-talk	$< 10\%$
Threshold dispersion after tuning	$< 10\%$
Maximum jitter	30 ps at 16 fC
TDC contribution	$<$ 30 ps
Time walk contribution	$<$ 10 ps
Minimum threshold	4 fC
Dynamic range	16 fC–50 fC
TDC conversion time	$<$ 23 ns

Table 5.12: Performance requirements for the OTK ASIC. The values given for the noise, minimum threshold and jitter have been specified considering a detector capacitance Cd = 4 pF.

signals from the flex cables to optical fibers connected to the back-end DAQ. A dedicated buffer is needed in each ASIC to average the rate variation and match the best speed of the ChiTu transceiver inputs:

- The largest average hit rate at small radius does not exceed 20 hits per ASIC and per event, equivalent to a rate of 500 Mbps (not including header). In the current design a bandwidth of up to 1.28 Gbps was considered for the innermost radius ASICs.
- For the barrel, taking into account a considerable safety margin, a 160 Mbps bandwidth can be used. For the innermost radius ASICs at endcap, a 640 Mbps e-link driver is needed.

5.4.1.2.3 ASIC architecture Building on the preliminary results of LGAD, an ASIC, the Out Tracker Read-Out Chip (OTKROC), is proposed to be developed in a CMOS technology. OTKROC includes 128 channels. The height of each channel should be less than 100um, which matches the pitch of the LGAD strip. Each channel in OTKROC has a preamplifier, a discriminator, and a time-to-digital converter (TDC) for the Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements. The preamplifier and discriminator are most critical parts for the contribution of jitter. The TOT is used to calculate the charge as well as to correct the time walk due to the charge Landau distribution in LGAD. The power consumption of OTKROC must stay below 2.5 W per chip, which means 20 mW per channel, constrained by the system cooling capacity. This value translates to a power budget of 15 mW for the front-end analog readout circuits in each channel. The time resolution of the Out Tracker is determined by the LGAD sensor and OTKROC together. The LGAD sensor has a jitter of about 40 ps due to non-uniform charge deposition. The OTKROC contribution should be below 30 ps to achieve 50 ps overall time resolution per hit. The Most Probable Value (MPV) of the charge from the LGAD sensor is around 16 fC. Considering the charge sharing with adjacent strips, the expected operating range of the charges is 8–50 fC. Due to such a small signal from the LGAD sensor, the analog readout circuits, including the preamplifier and the discriminator, dominate electronics' jitter contribution and are critical for the Outer tracker precision timing performance.

5.4.1.2.4 Single-channel readout electronics

Preamplifier The preamplifier consists of two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower (M3) as the second stage. The bias current of the input transistor (M1) has two components: the constant current The preamplifier consists of two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower

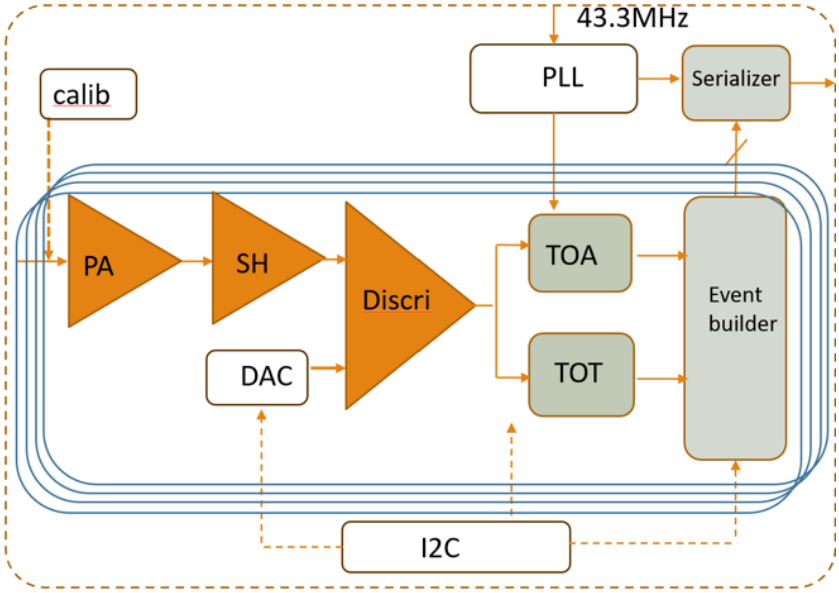


Figure 5.73: OTK ASIC

(M3) as the second stage. The bias current of the input transistor (M1) has two components: the constant current *IB1* is small due to that the VGS of M2 should not be too large. The transistor M2 and its gate voltage Vb set the DC operating point of M1. Vb is the replica bias voltage from *IB1*. The gain and bandwidth depend on the Gm of transistor M1. Most of the current of M1 is provided by a tunable *IB2*. The feedback resistor *Rf* is programmable to adjust the gain of the preamplifier. The load capacitance *CL* of the first stage is also programmable to optimize the bandwidth. The drain current *IB3* of M3 is generated by a resistor. The gain of the first stage and the second stage are negative and positive, respectively. Since the preamplifier's input signal is a negative pulse, the output signal is a positive pulse, whose rise edge is the leading edge and falling edge the trailing edge. Both the leading and trailing edges of the preamplifier should be considered. A faster leading edge can be achieved with a higher bias current of M1 and a smaller load capacitance of *CL*. When the *IB2* is biased to its highest value, the preamplifier output's leading edge time can be set to several 1ns with a bandwidth of 400MHz. Small load capacitance leads to a fast leading edge but introduces more noise because of the large bandwidth. Therefore, the load capacitance can be selected to fine-tune the jitter. The default setting is to use the smallest load capacitance. The time constant, the product of the total capacitance *Cs* and the input impedance *Rin*, determines the trailing edge time of the preamplifier output. The input impedance should be considered because the 4 cm strip is a transmission line to a signal with a leading edge of 1 ns. The input impedance *Rin* is given by the feedback resistance *Rf* divided by the open-loop gain. The open-loop gain depends on the bias current. Thus, *Rf* is programmable with four settings to adjust the gain, the trailing edge time of the preamplifier output and input impedance. Based on the simulation with LGAD signals, a default feedback resistor will be selected. The bias current *IB2* allows different trade-offs between the power consumption and the timing performance. A larger signal slew rate (*dV/dt*) and a faster rise time of the preamplifier output *tr* can be achieved at a higher bias current, and thus the better performance is expected.

Discriminator The discriminator consists of three stages of fully differential amplifiers, a comparator, and an internal buffer. The three stages of amplifiers receive the small input pulses, and generate the larger pulses comfortable for the comparator. The overall gain for three stages of amplifiers will be 20-40 dB with a bandwidth of around 400 MHz. The comparator discriminates the differential input at the crossing point with programmable hysteresis. The internal buffer delivers the digital output to the following circuits. The internal buffer is composed of two CMOS inverters and relieves the loading pressure. As shown in figure 5.74, the comparator has two stages: The first stage is a common-source differential amplifier of high gain with the transistors M1 and M2. The loads is comprised of a transistor pair M3 and M4, which are diode-connected PMOS. M11 and M12 provide the bias current with a source current *I* bias, shared with the three-stage amplifiers. The first stage digitizes the differential input at the crossing point with a tunable hysteresis. The hysteresis is used to alleviate ringing due to noise and generated by the transistors M9 and M10. The second stage

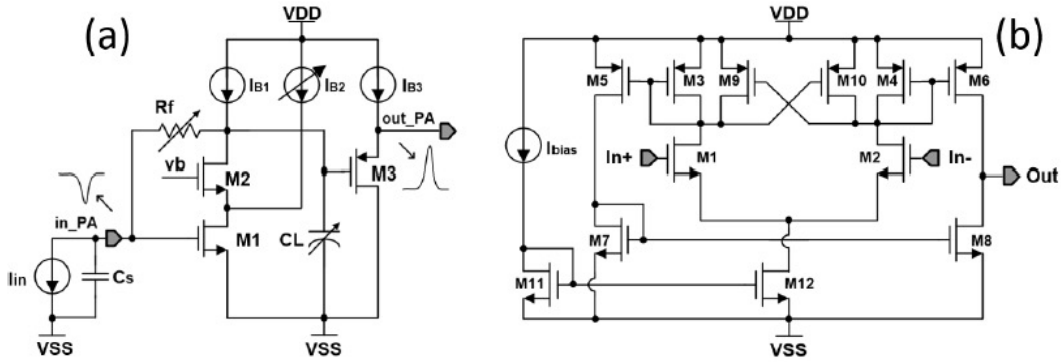


Figure 5.74: OTK ASIC2

converts the differential output of the first stage into single-ended. The leading edge of the discriminator output provides the TOA, while the trailing edge, combined with TOA, provides the TOT. The discriminator threshold is connected to the inverting input and set by an internal 10-bit DAC. The DAC is comprised of a global 6bit DAC and a local 4-bit DAC in each channel. Since the preamplifier's baseline varies for different channels with temperature, bias setting, and irradiation. The DAC output range is from 0.6 to 1 V with an LSB (Least significant bit) of 0.4 mV. A reference voltage generator provides a 1 V reference voltage to the DAC. To minimize the DAC noise contribution to threshold, a RC filter is added to the DAC output.

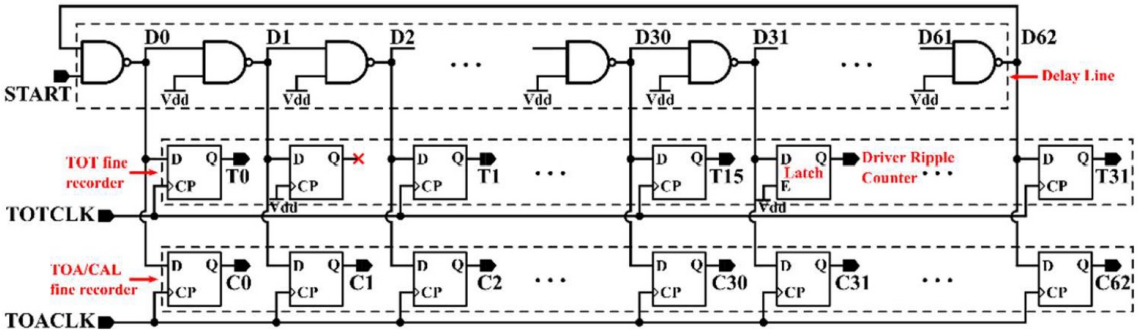


Figure 5.75: OTK ASIC3

TDC The schematic of the TDC core is shown in the figure 5.75. The OTKROC design faces two main challenges: the large area required for the OTK and the necessity of achieving both time and charge measurements while maintaining low power consumption. Additionally, the pitch of the LGAD strips is only 100 μm, which means that the height of the single-channel circuitry must also be less than 100 μm. To realize this on a smaller area, a single delay line is employed to simultaneously measure the time of arrival (TOA) and the time over threshold (TOT), with each delay cell providing a delay of 30 ps. The flip-flops record the times of the signal's rising edge, falling edge, and the reference clock's rising edge, storing these values sequentially in registers. The chip utilizes a single delay line without a delay-locked loop (DLL), and to reduce the number of delay cells, a cyclic structure is implemented. The delay of the delay line is influenced by process variations, power supply voltage, and temperature (PVT); thus, a pulse self-calibration scheme is necessary to compensate for the effects of PVT variations. This calibration is performed periodically using the system clock to measure and calibrate the delay chain. The data width of the TDC output includes 8 bits for TOT, 9 bits for TOA, 1 bit for hit flag, 8 bits for calibration, 7 bits for channel identification (128 channels), 8 bits for bunch ID, and 7 bits for chip ID, resulting in a total of up to 48 bits.

Calibration and Internal pulser The calibration circuit is designed to mimic the injection of input charge and can be used during the production phase to verify the proper functioning of the chip's TOA and TOT measurement capabilities.

This calibration circuit acts as a pulse generator, charging a 200 fF capacitor to a certain voltage using a DAC. By directly shorting the DAC output to ground through a switch, it generates a current signal that is similar to that of a sensor. The DAC consists of a 6-bit adjustable current mirror and a 50 kΩ resistor. The dynamic range of the DAC can reach up to 250 mV, which means the injected calibration charge can be as high as 50 fC (with LSB = 0.8 fC). The output of the DAC can be connected to a pad or supplied externally. The rising edge of the calibration signal is contingent upon the speed of the switch signal. Variations in the fabrication process can also lead to inaccuracies in the capacitor and resistor values. The final calibration will be conducted using physical events that provide a reference for the time of arrival, as the leading edge of the pulse generated by the calibration signal differs from that of the signal produced by the actual LGAD. The differing rise and fall times of the pulse result in distinct jitter characteristics in the measured timing between the calibration signal and the LGAD signal.

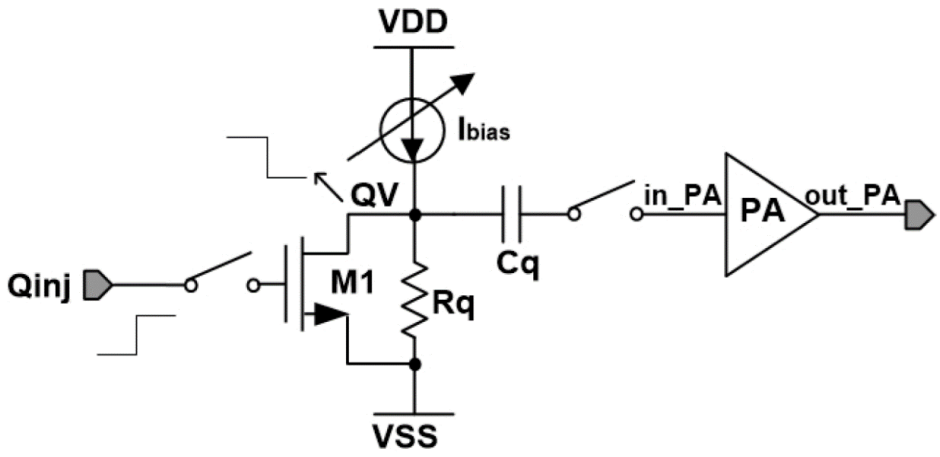


Figure 5.76: OTK ASIC4

Data process and digital blocks

Clock generation unit The clock generator unit provides clock signals to all functional blocks in the OTKROC chip. The oscillator in the PLL works at 1.28 GHz which is the highest frequency, as an input of 43.3 MHz clock. Effective clock distribution of skew and jitter is a critical challenge in the design. A binary tree, as the most common and conservative clock distribution scheme is planned to use. In this scheme, the clock is branched from a central point (root) to all its destination nodes (leaves). The 7-stage tree structure ensures that the clock distribution network is balanced and that all the path lengths from the clock source to each channel are equal. The Buffers are added along the transmission path to ensure the quality of the clock signal.

Data readout process The TDC data of each channel is buffered in a circular buffer. A scrambler is utilized and a pseudo random binary sequence (PRBS) block is adopted for test purposes. The OTKROC provides three serial output data rates streams, depending on the anticipated occupancy of the chip. The slowest data rate is 320 Mbps, where a single byte is transmitted during a 40 MHz main clock cycle. The next highest data rate is 640 Mbps, or one 16-bit word is transmitted during each 40 MHz clock cycle. Finally, the highest supported data rate is 1.28 Gbps where a 32 bit double word is transmitted during a single 40 MHz clock cycle. Forward error correction bits like 8b/10 or 64b/66b encoding schemes are used on the serial output.

Slow control Slow control mechanisms are implemented to configure the registers within the chip. The chip contains different registers that manage various functions and operating modes, such as different gains for the amplifiers, test modes, or data acquisition modes, as well as calibration controls. An I2C link is utilized in the ASIC, configured through the I2C master in ChiTu chip.

5.4.1.2.5 Prototype A prototype chip named FPMROC is designed, including 8 complete readout chains, with each chain comprising the following components: a low-noise preamplifier, a discriminator, and a time-to-digital converter (TDC) for both time of arrival (TOA) and time over threshold (TOT) measurements. An data event builder is integrated to manage data flow, along with fast data serialization and data driver for output. The TOT is employed to correct the time walk effect in the TOA measurements [5]. Peripheral circuits include digital-to-analog converters (DACs) for calibration and threshold adjustment, a phase-locked loop (PLL) to generate high-qualify clocks, and a serial peripheral interface (SPI) module for slow control. Additionally, the prototype incorporates a charge injection circuit for testing and calibration.

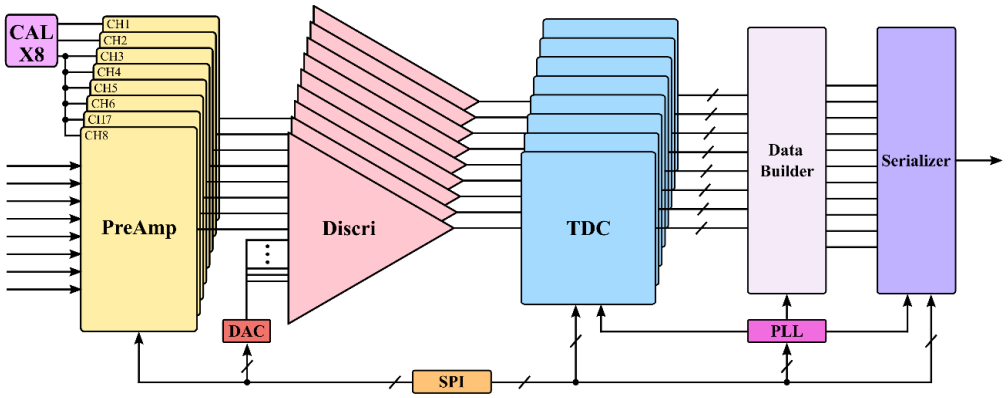


Figure 5.77: Block diagram of the FPMROC

Design Figure 5.77 presents the block diagram of the FPMROC ASIC (application-specific integrated-circuits). Eight channels collectively utilize a data event builder for buffering, framing, scrambling and encoding parallel data from various channels. The ASIC includes a serializer for off-chip data transmission at a rate of 10.24 Gbps, and a low-jitter LC-based PLL for the generation of 5.12 GHz and 40 MHz clocks for the serializer and TDCs, respectively. Additionally, an SPI is integrated to provide configurations up to 200 bits.

Front-end circuit

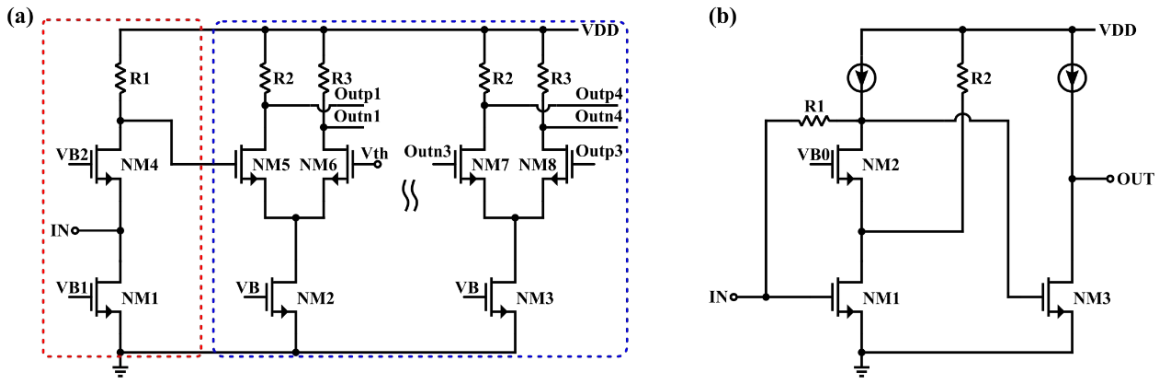


Figure 5.78: (a) Schematic of the saturated amplifier, (b) Schematic of the trans-impedance amplifier

Design Two types of preamplifiers are implemented in the FPMROC. The first design employs a 4-stage amplifier to saturate the signal, where each stage offers high bandwidth but low gain, as illustrated in Fig. 5.78 (a). The second design incorporates a classic trans-impedance amplifier (TIA) that provides higher gain but operates at a slower speed, as shown in Fig. 5.78 (b). Both designs maintain an input impedance of approximately 50 Ω to ensure proper impedance matching [6].

The discriminator converts analog pulses from the preamplifier into digital signals. It comprises a four-stage preamplifier and a comparator with programmable hysteresis. The preamplifier stages amplify small input pulses to a level

suitable for reliable processing by the comparator. The comparator digitizes the differential input at the crossing point, with the hysteresis providing adjustable noise immunity. The hysteresis helps prevent false triggering near the threshold ensuring robust signal detection.

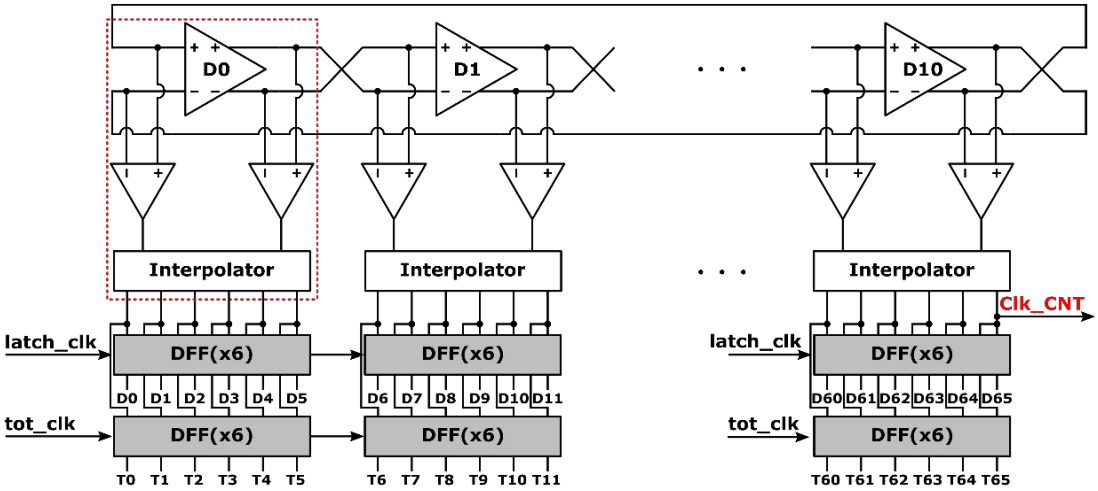


Figure 5.79: The architecture of the TDC delay line

Time-to-digital converter The TDC block utilizes 11 voltage-controlled differential delay cells, which construct a ring oscillator using an interpolator approach, as shown in Fig. 5.79. Each delay cell is designed to facilitate precise time measurements by integrating interpolated differential delay cells for fine time resolution, combined with two sets of ripple counters for coarse time measurement. To address propagation variations, a self-calibration mechanism is implemented that records timestamps twice. This approach utilizes two recorders, constructed as chains of D-flip-flops (DFFs), to capture snapshots of both fine and coarse time for TOA and TOT measurements, as well as for calibration purposes. The delay cell xxx .

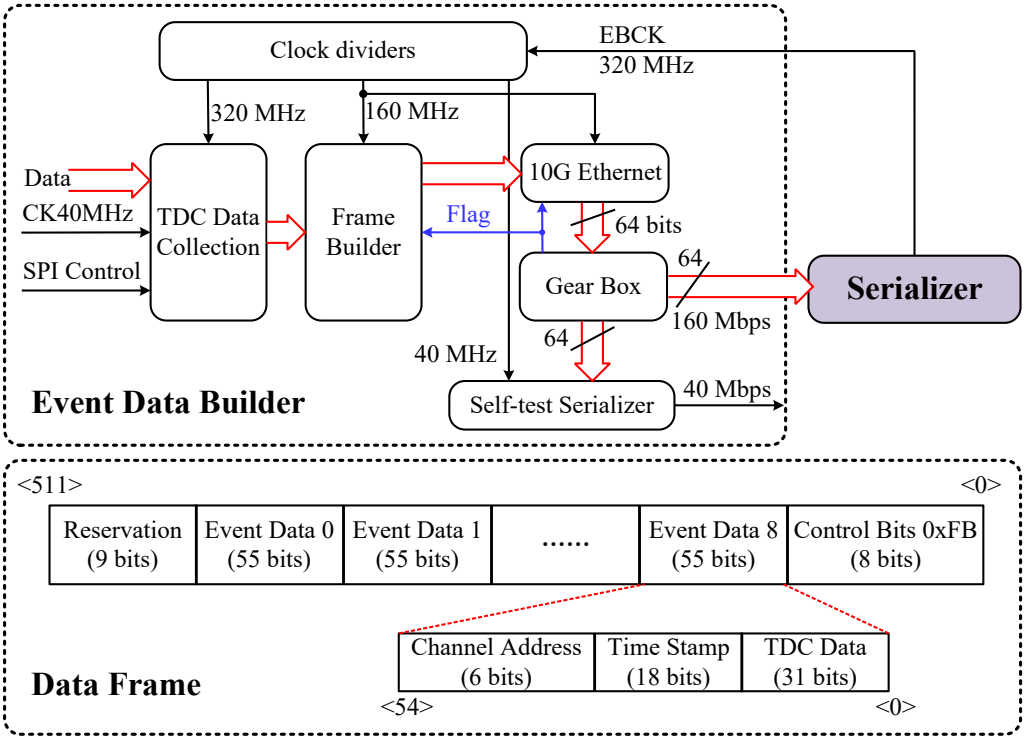


Figure 5.80: The scheme and data frame of the event data builder

Event data builder The event data builder receives data from eight TDC channels, along with a 320 MHz synchronous clock from the serializer, to generate 64-bit parallel data at a rate of 160 Mbps. Figure 5.80 gives the scheme and data frame architecture. Two-level FIFOs are employed for data storage and aggregation. A frame builder retrieves and combines the data, which is subsequently forwarded to a 64B66B encoder incorporating scrambling algorithms from 10 Gigabit Ethernet to maintain DC balance within the data stream. Ultimately, a gearbox ensures alignment with the data rate and width requirements of the high-speed serializer.

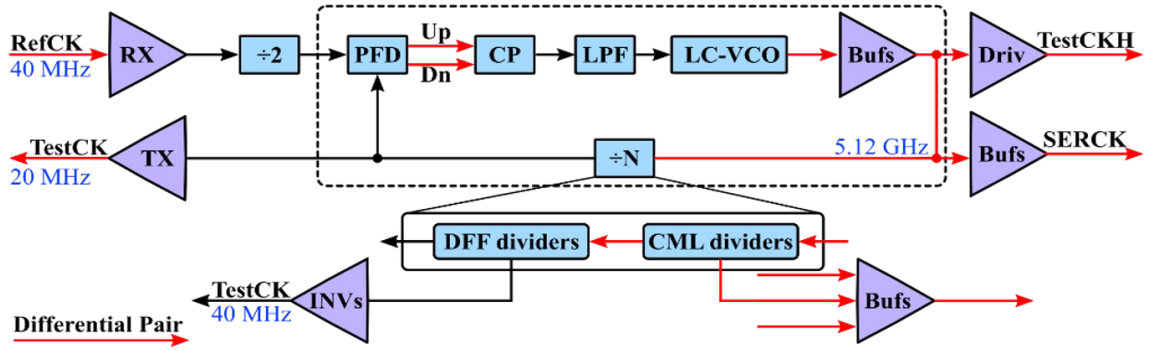
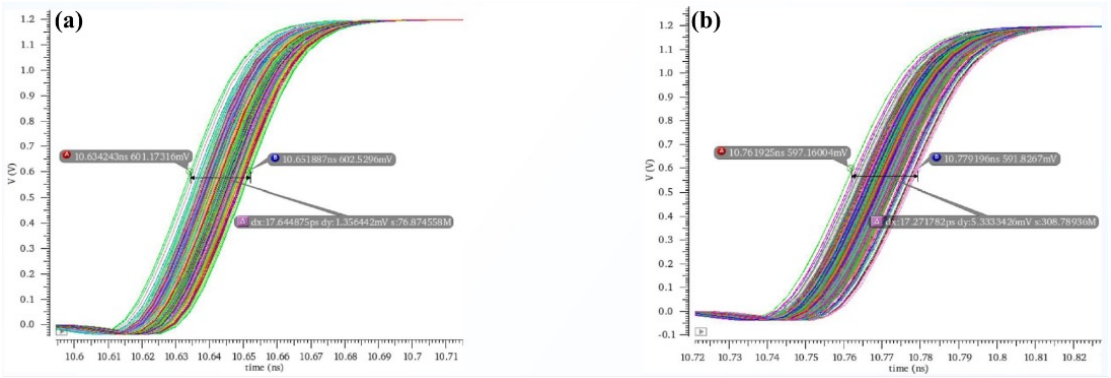


Figure 5.81: The block diagram of the PLL and serializer

PLL and serializer Figure 5.81 shows the architecture of the PLL and serializer. Both designs have been silicon-proven and modified for this specific application. The PLL mainly comprises a phase-frequency detector (PFD), a charge pump (CP), an LC-based voltage-controlled oscillator (LC-VCO), a low-pass filter (LPF), and dividers and buffers [7]. The serializer facilitates the conversion of 64 bits into a pair of differential serial outputs by employing four low-speed CMOS-logic 16:4 subunits, four CMOS-logic 4:1 subunits, and a high-speed current-mode logic (CML) multiplexer paired with a driver. A PRBS15 (pseudorandom binary sequence) generator is also integrated in the serializer for fast self-tests. Figure 6 shows the overall layout, which occupies an area of 2.2×3.4 mm^2.

Simulation Results The capacitance Cs for the MCP-PMT is estimated to be approximately 4 pF. A stimulus input charge of 16 fC is injected during the simulation, characterized by rise and falls times of 100 ps and a pulse width of 100 ps. A total of 400 transient noise simulations were conducted for both front-end schemes. The total jitter of the discriminator for both schemes is less than 18 ps, as shown in Figure 5. For the preamplifier in the first scheme, the root mean square (RMS) noise is 158 µV, with a slop of 67 V/µs. In contrast, the RMS noise for the second scheme is 508 µV, with a slop of 145. V/µs.



(a) saturated amplifer (b) trans-impedance amplifier

Figure 5.82: Transient noise simulation for output of preamplifier

The transfer function of the TDC is illustrated in Fig. 5.82 (a). In the TOA measurement, the arrival time of the input

pulse increases in fixed steps of 1 ps with each clock cycle. A minimum-square linear fitting of the measured data is also shown in Figure 6(a) (dashed blue line). The fitting curve indicates that the TDC achieves a time resolution of 9.18 ps. The integral nonlinearity (INL) quantifies the deviation of each stair center in the transfer function from the expected time. Figure 6(b) shows the INL and differential nonlinearity (DNL) of the TDC. According to the simulations, the INL of the delay line is less than ±0.6 least significant bit (LSB), and the DNL is less than ±0.7 LSB.

Since the PLL has been silicon-proven, detailed performance metrics can be found in the reference [7], which indicates a total jitter less than 7.5 ps. Furthermore, a spectrum analyzer was used to characterize the phase noise performance of the frequency-halved output clock (2.56 GHz), with a corresponding measurement shown in Figure 8 (a). Figure 8(b) presents a clear eye diagram, simulated at 10.24 Gbps, of the modified serializer, while the earlier design has been verified with a measured total jitter of less than 43 ps.

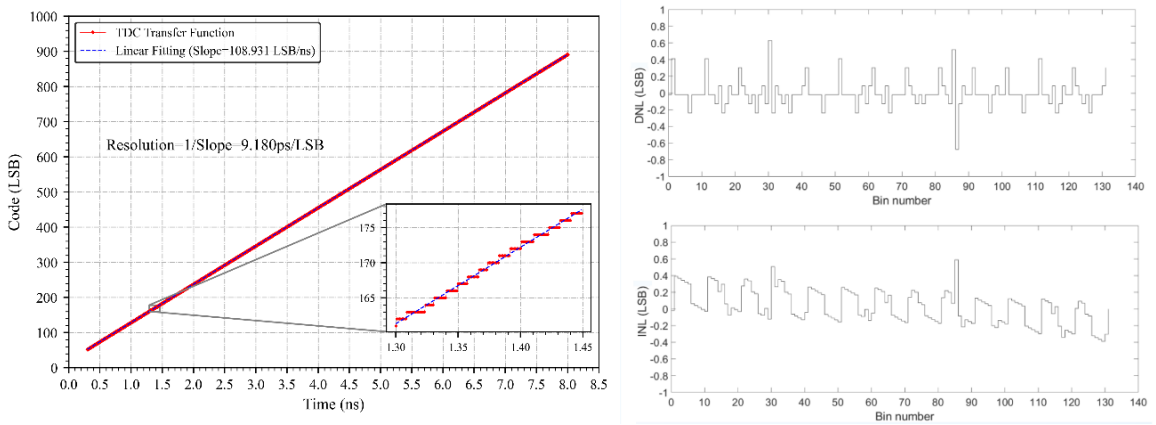


Figure 5.83: (a) TDC transfer function curve, (b) DNL and INL of the delay line

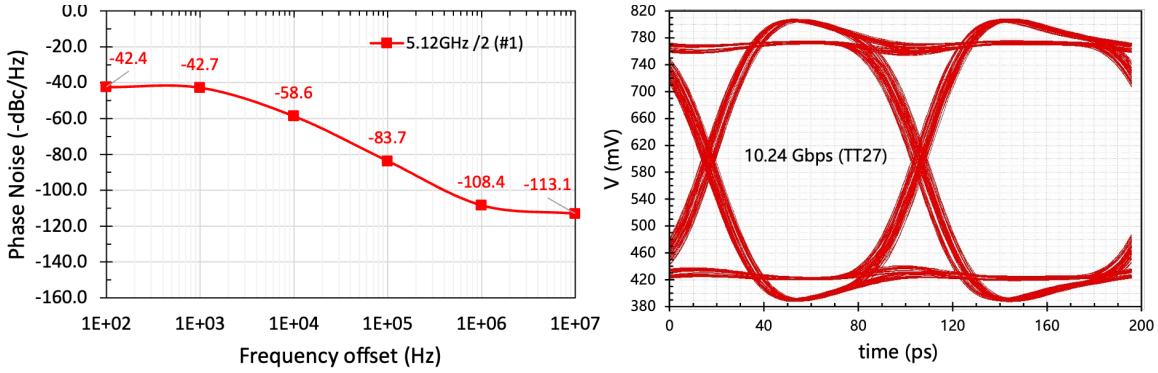


Figure 5.84: (a) Phase noise measurement of the divide-by-2 output clock (b) 10.24-Gbps eye diagram

5.4.1.2.6 Power distribution and grounding To ensure the accuracy of signal timing measurements, the allocation of current sources within the chip must be carefully considered. The power and ground for the analog and digital sections are kept independent, with key devices in the analog section located within a deep N-well. Given the large number of channels in the chip and the significant area required for power distribution, it is essential to minimize the impedance of the power lines to reduce IR drop.

5.4.1.2.7 Radiation tolerance In terms of radiation hardness design, the primary considerations are Total Ionizing Dose (TID) effects and Single Event Effects (SEE). TID can lead to an increase in the threshold voltage of MOSFETs, thereby degrading the timing performance of the circuit. To mitigate TID effects, relatively high bias currents are employed in the circuit, and the use of minimum-sized transistors is avoided. Additionally, substrate contacts are increased to prevent latch-up phenomena. The critical components of the digital logic in the chip are designed using Triple Modular Redundancy (TMR) to enhance Single Event Upset (SEU) tolerance.

5.4.1.2.8 Monitoring The monitoring of the ASIC primarily focuses on operational temperature, voltage, and the leakage current of the sensors. While the chip itself is not sensitive to temperature, the LGAD is sensitive to temperature variations, allowing temperature detection through the channels to ascertain whether cooling has failed. Voltage monitoring within the chip can be used to determine if the chip is functioning properly and to control the shutdown of any malfunctioning modules.

5.4.1.2.9 Development plan and schedule In the second half of 2024, the design of the LGAD readout scheme and the verification of the corresponding ASIC will be conducted. In the Q1 of 2025, the ASIC will be submitted for wafer production to validate the performance of the preamplifier, discriminator, and TDC modules, along with the design of the ASIC test system. Performance testing of the ASIC will be carried out by the end of the year, and each module will undergo radiation hardness testing. In the Q4 of 2025, the ASIC design will be improved, incorporating a digital logic control section, and the first version of the multi-channel integrated design will be submitted for wafer production. In the first half of 2026, the design of the multi-channel ASIC test system will be completed, alongside performance testing of the ASIC and radiation hardness testing, culminating in the completion of the connection and debugging with the LGAD. In the end of 2026, the multi-channel ASIC design will be further refined, and the V1 version of the ASIC will be submitted for wafer production. Simultaneously, the prototype design of the LGAD readout frontend electronic system will be initiated. In the first half of 2027, performance testing of the V2 version of the ASIC will be conducted, along with testing of the LGAD readout electronic system prototype, ensuring coordination with the LGAD. In the second half of 2027, the prototype system will be finalized in preparation for the mass production of the chips.

5.4.2 OTK design

Responsible person: Qi YAN

The baseline design of the OTK consists of 1 barrel detector layer with a radius of ∼1,800 mm and a length of 5,680 mm, along with 1 pair of endcaps with a detector radius of 406 mm $< r <$ 1,816 mm positioned at $|z|$ =2,910 mm.

The baseline OTK barrel and endcap are constructed from AC-LGAD microstrip sensors diced from 8-inch silicon wafers. The sensors designed for the OTK construction have a rectangular shape for the barrel and a trapezoidal shape for the endcap. Together with a high-resolution hybrid ASIC, the OTK features sensors with a strip pitch size of ∼100 μm, providing a spatial resolution of ∼10 μm and a time resolution of ∼50 ps.

5.4.2.1 OTK barrel design

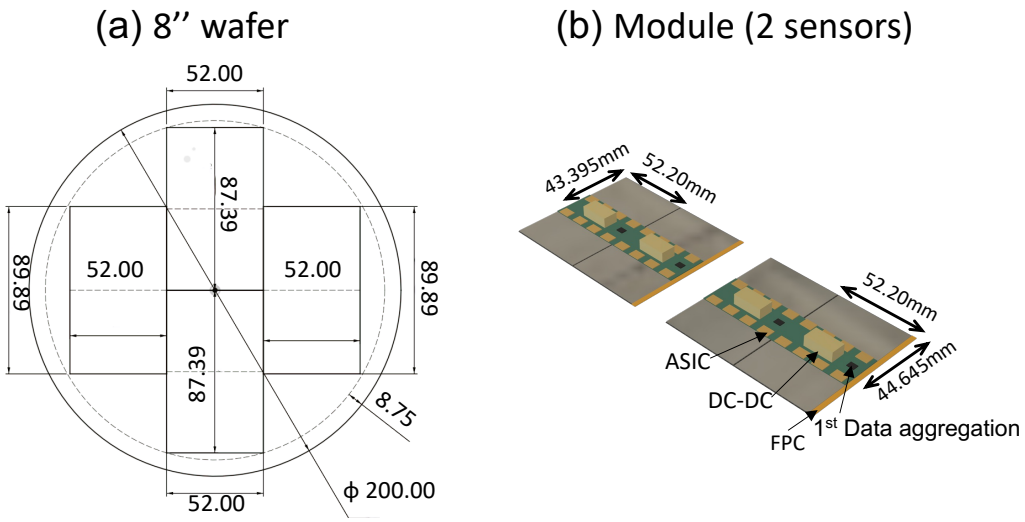


Figure 5.85: OTK Module

The OTK barrel sensors are designed to have 2 types, with a surface dimensions of 87.39 mm×52.20 mm and 89.89 mm×52.20 mm, and active area of 86.79 mm×51.60 mm and 89.29 mm×51.60 mm, respectively. These 2 sensor types, which differ in length, are diced from a common 8" silicon wafer, as shown in Fig. 5.85 (a). The thickness of the sensors is 300 μm. In the longitudinal direction, each sensor contains 2 sets of short parallel strips, with strip lengths of 43.395 mm and 44.645 mm for the 2 types of sensors, respectively, as illustrated in Fig. 5.85 (b). In the transverse direction, each set has 512 strips, resulting in a strip pitch of 100 μm.

A barrel strip module consists of 2 sensors placed side by side and a low-mass PCB equipped with radiation-tolerant DC-DC converters, readout ASICs, and data aggregation chips, as illustrated in Fig. 5.85 (b). The 2 lengths of sensors correpond to 2 types of modules. A module is assembled by gluing the PCB to the silicon sensors using conductive epoxy. Thermal vias are included in the PCB design to improve vertical heat transfer from the ASICs to the sensor through the PCB. Each readout ASIC has 128 channels, connected to the silicon strips via wire bonding. The DC-DC converters provide low voltage (1.2 V) to 2 rows of readout ASICs (see Fig. 5.85 (b)), with each row of ASICs wire-bonded to a set of strips on one half of a module. Each module contains 16 ASICs to read out 2,048 strips.

Every 8 modules (16 sensors) are glued to a common carbon fiber support plane with a thickness of 0.3 mm, forming a mechanical and electronic unit called a ladder, as shown in Fig. 5.85. There are 2 types of ladders, with lengths of 699.6 mm for short ladder and 719.6 mm for long ladder, assembled using the 2 types of sensors, respectively. A 2$^{\text{nd}}$ data aggregation PCB integrating an aggregation chip, a data link chip, and an optical converter, is glued near the middle of the ladder. At the edge of the ladder, a long kapton flexible printed circuit (FPC) cable is connected (see Fig. 5.87 (b)) to

transmit high voltage (200 V) for sensor bias, low voltage for DC-DC, data, clock signals, and chip commands. Signals collected from the strips are digitized in the ASICs, aggregated within each module, transmitted through the FPC, and then reach the second data aggregation board. Data from all the modules in a ladder undergoes second aggregation, passes through a data link chip (GBTx-like), and is subsequently converted to optical signals via the optical module for readout.

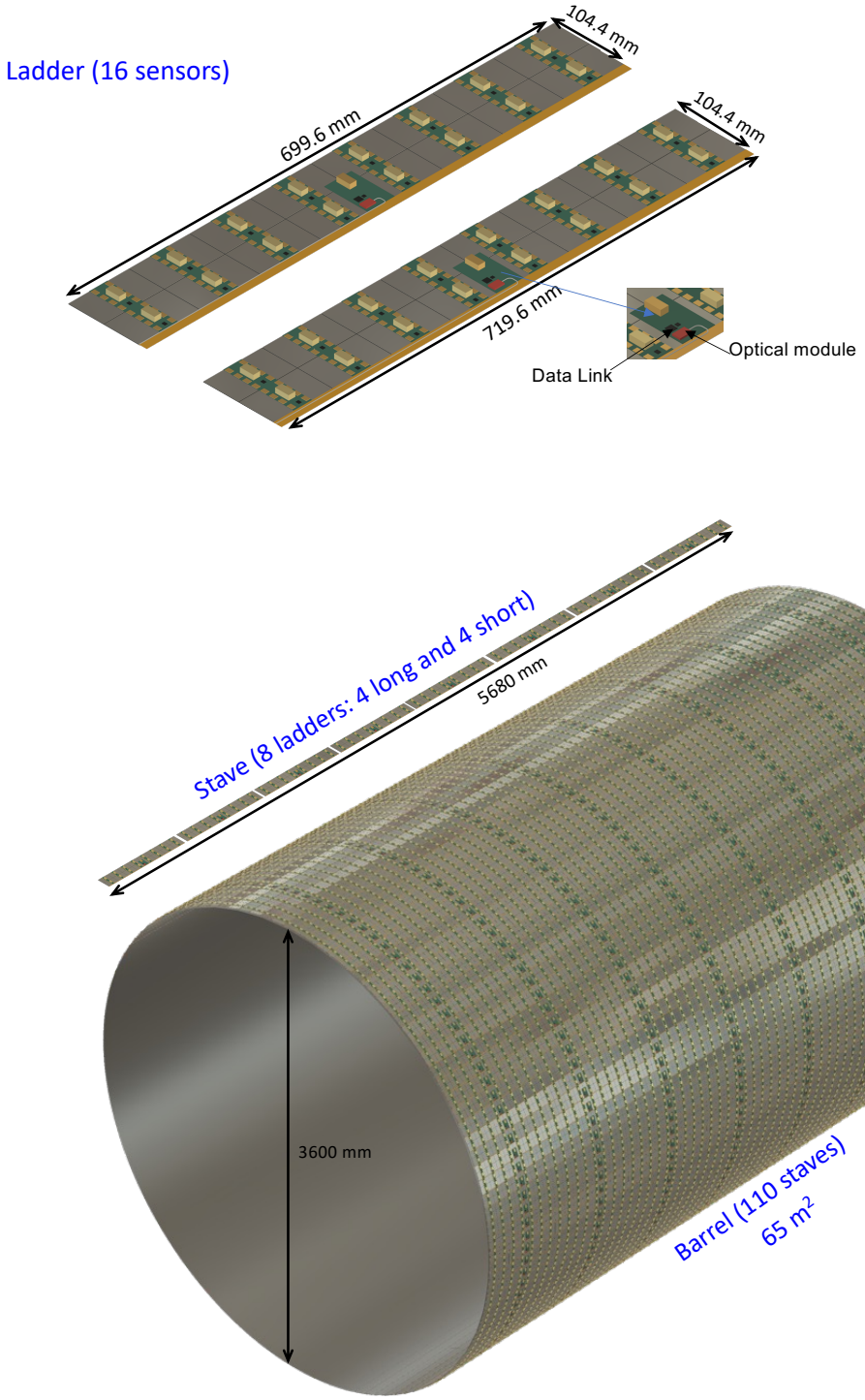


Figure 5.86: OTK Barrel

To match the length of the OTK barrel, 4 long ladders and 4 short ladders are placed on the TPC outer barrel in a row, forming a long structure called a stave, with a total length of 5,680 mm. In each stave, the central 4 ladders are short, with 2 long ladders positioned at each end. The diameter of the OTK barrel is 3,600 mm, requiring 110 staves to cover the full detector area of 65 m^2, as shown in Fig. 5.87 (b). Neighboring staves are designed to overlap in the transverse direction

Figure 5.87: OTK Half Stave

to reduce the dead area. The detailed mechanical supporting designed for the OTK will be elaborated in section 5.4.4.

For the CEPC OTK barrel construction, the design of the OTK sensor mask and subseqent sensor dicing strategy from 8" silicon wafers, shown in Fig. 5.85, have been optimized to maximize the usage efficiency of silicon wafers for the OTK barrel and reduce the costs. For the entire OTK barrel, a total of 3,520 wafers are needed, with a 15% higher efficiency compared to a conventional single-piece sensor dicing from a wafer.

5.4.2.2 OTK endcap design

A pair of OTK endcaps is positioned at $|z|$ =2,910 mm. Each endcap has substantial dimensions, with a radius of 406 mm $< r <$ 1,816 mm and a surface area of $\sim$10 m^2. Together with the barrel layer, these endcaps cover full acceptance of incoming particles with a polar angle of $\cos(\theta) < 0.99$. To facilitate sensor production and assembly, and to maximize the usage efficiency of silicon wafers, the CEPC OTK endcap was specifically designed with trapezoid sensors.

The OTK sensors are fabricated from 8" silicon wafers. Figure 5.88 (a) shows a 1/16 sector of the OTK endcap, which consists of 14 rings arranged into 4 groups: Group A, Group B, Group C, and Group D, each indicated by a different color. Each group contains 2-4 types of trapezoidal sensors that can fit to a common 8" silicon wafer. Figure 5.89 displays the wafer layouts for sensors from individual groups.

The long sensors—specifically A1 and A2 in Group A, B1 in Group B, C1 and C2 in Group C, and D3 and D4 in Group D—each contain 4 segments, with boundaries indicated by dotted lines on the sensor, as shown in Fig. 5.89. Other short sensors, namely B2 and B3 in Group B, C3 and C4 in Group C, and D1 and D2 in Group D, contain 2 segments. Each segment of a sensor has a set of implanted strips. Trapezoidal sensors with a middle width below 43 mm are classified as narrow sensors, while those above 43 mm are classified as wide sensors, with each segment containing 384 and 512 strips, respectively. The sensor geometric parameters are illustrated in Fig. 5.89, and sensor strip parameters are tabulated in Table 5.13. For example, the surface dimensions of the top segment for trapezoidal sensor A1 in Fig. 5.89 (b) are 41.92 mm in top width, 39.40 mm in bottom width, and 32.075 mm in height. With a total of 384 strips, the radial strip pitch in the top segment of sensor A1 varies from a maximum of 107.6 μm at the top to a minimum of 101 μm at the bottom, while the strip length is 31.755 mm.

In the OTK endcap design (see Fig. 5.88), each group of sensors is aligned to a 1/16 sector, with 16 sectors constituting the full endcap. This unique design requires only 4 masks for sensor fabrication and maximizes wafer usage efficiency, both of which contribute to reducing overall costs. Table 5.14 summarizes the sensors and silicon wafer usage per OTK

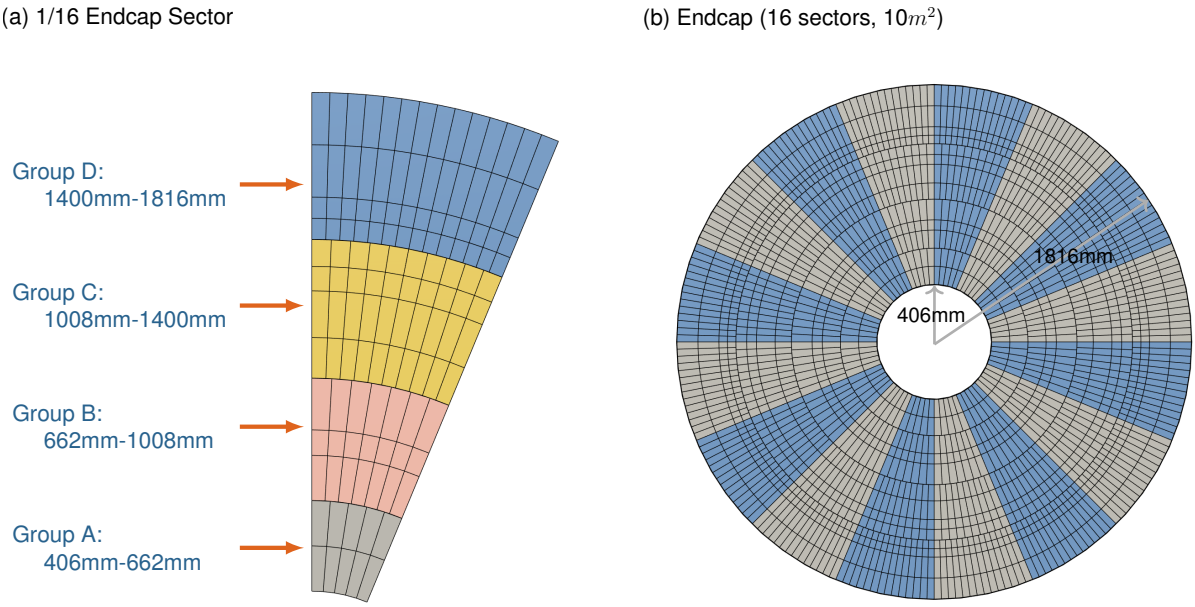


Figure 5.88: OTK endcap sensors arrangement

OTK Endcap Trapezoidal Sensor Strip Parameters				
Sensor type	Number of strip sets	Number of strips per set	Strip pitch [μm]	Strip length [mm]
A1	4	384	81.5-107.6	31.755
A2	4	512	80.7-100.3	31.755
B1	4	384	95.1-113.8	31.630
B2	2	512	85.3-93.2	35.610
B3	4	512	93.2-109.2	36.255
C1	4	384	101.5-113.2	28.380
C2	4	512	84.9-95.0	32.755
C3	2	512	95.0-100.3	34.110
C4	2	512	100.3-106.1	37.610
D1	2	384	100.6-105.0	29.360
D2	2	384	105.0-109.4	29.610
D3	4	512	82.0-90.1	36.755
D4	4	512	90.1-98.2	36.755

Table 5.13: Trapezoidal Sensor Strip Parameters

endcap. For each endcap, 2,032 silicon sensors will be fabricated from a total of 576 silicon wafers.

Sensors and Silicon Wafers Usage per OTK Endcap													
Mask	A		B			C				D			
Sensor type	A1	A2	B1	B2	B3	C1	C2	C3	C4	D1	D2	D3	D4
Number of sensors	80	80	112	112	112	160	160	160	160	224	224	224	224
Number of wafers	80		112			160				224			

Table 5.14: Sensors and Silicon Wafers Usage per OTK Endcap

The basic assembly unit for the OTK endcap is the module. As shown in Fig. 5.90 (a), each endcap module, similar to the barrel module, consists of a sensor and low-mass PCBs equipped with DC-DC converters, readout ASICs, and data aggregation chips. Each PCB, glued to the sensor, serves as the primary data aggregation board, reading out 2 sets of strips. For modules with a long sensor, 2 PCBs handle 4 sets of strips, while modules with a short sensor use 1 PCB to manage 2 sets of strips. Each PCB has 6 ASICs for wide sensor modules and 8 for narrow sensor modules, with the ASICs wire-bonded to the strips.

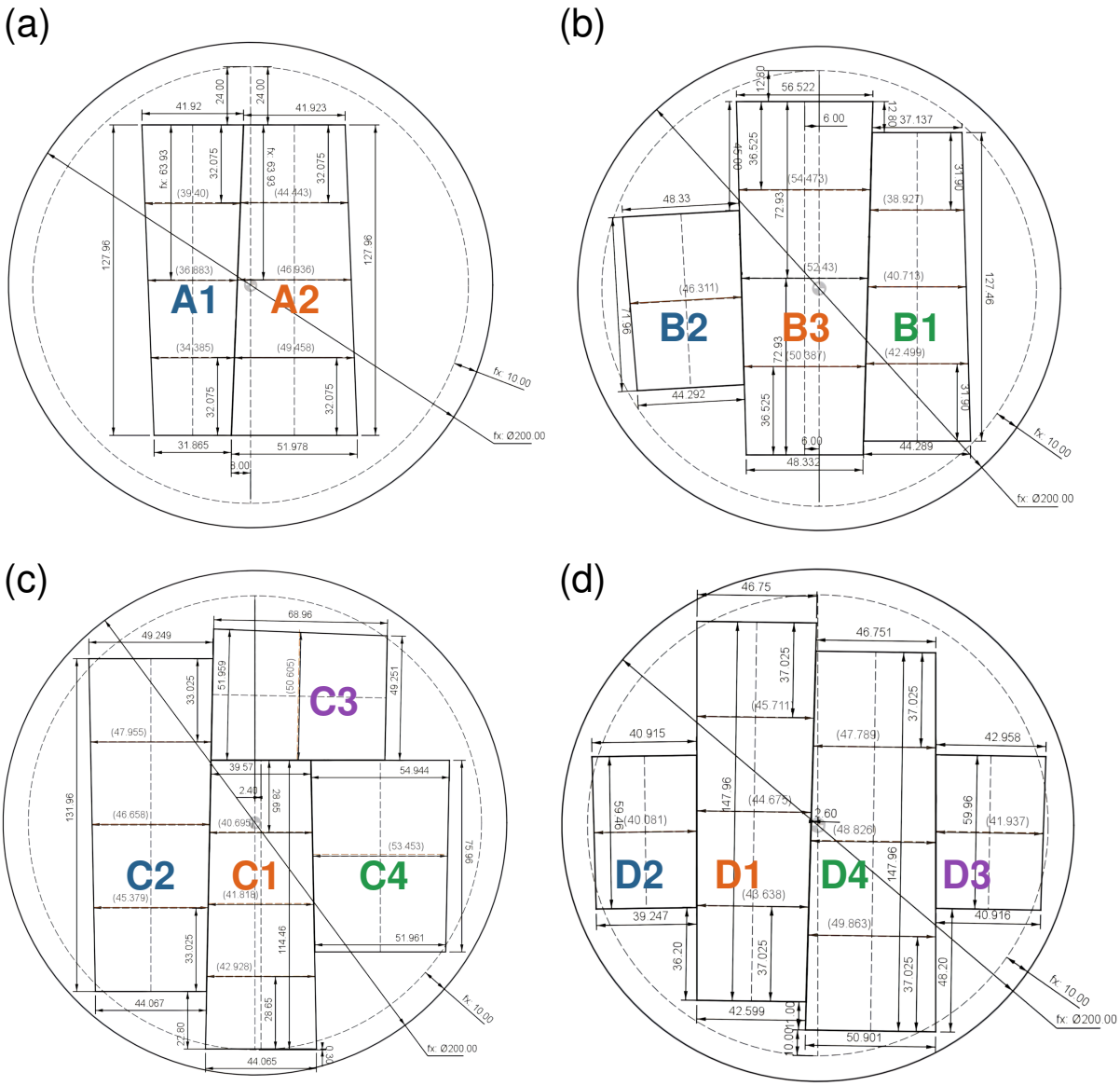


Figure 5.89: Endcap sensors from 8" silicon wafer

For OTK endcap, 1/16 sector is designed as a complete mechanical and functional unit. To construct it, as shown in Fig. 5.90 (b), 2,032 modules are glued on a 1/16 sector carbon fiber plane. Next, 17 2nd data aggregation boards are glued to the sensor surfaces of 1/16 sector, with each 2nd data aggregation board connected to the 2 lateral rows of primary data aggregation boards. As illustrated in Fig. 5.90 (a), each 2nd data aggregation board includes a data aggregation chip, a data link chip, an optical module, power cables, and a DC-DC converter. The primary aggregation board connects to the 2nd aggregation board via a shielded flexible printed circuit (FPC) connector. The lateral row of PCBs, or primary aggregation boards, in 1/16 sector are interconnected using compact connectors or wire soldering (the final method has yet to be decided). These connections enable the transmission of power, data, clock signals, and chip commands between the 2nd aggregation board and any primary aggregation board.

As shown in Fig. 5.90 (b) of a 1/16 OTK sector, 17 long power bus FPCs are arranged into 3 groups and fixed on 3 supporting frames. These FPCs extend from the outermost rim of the OTK sector to connect with the 17 2nd data aggregation boards. The high voltage (HV, 200 V) and original low voltage (LV, 48 V) are trasmitted to the 2nd data aggregation boards through these power bus FPCs. The DC-DC converter in the 2nd data aggregation board steps down the 48 V LV input to 12 V, along with 200 V HV supply, distributes power to the primary aggregation boards. The 200 V is used for sensor biasing, while the DC-DC converter in the primary aggregation board of each module further drops the

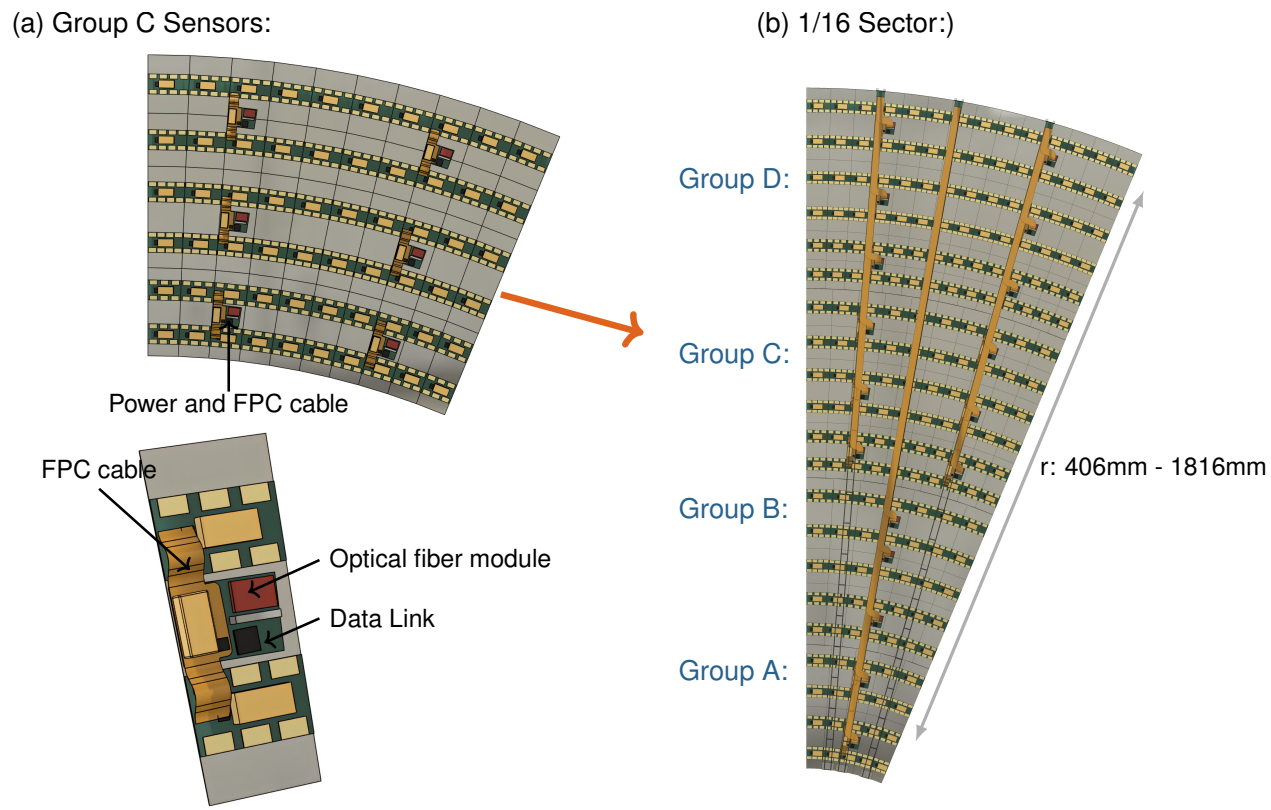


Figure 5.90: OTK endcap Sector

LV from 12 V to 1.2 V to supply power to the sensor readout ASICs. Data readout from the sensor ASICs is aggregated on the primary aggregation board and transmitted to the 2^{nd} data aggregation board. The 2^{nd} data aggregation board processes the data, converts it to an optical signal, and transmits it through an optical fiber. The 17 optical fibers from the 17 2^{nd} data aggregation boards in a sector are attached to the same mechanical frames as the power bus FPCs.

The complete OTK endcap consists of 16 sectors. Figure 5.91 shows the OTK endcap with sensors and electronic components. A detailed description of the OTK electronic design is provided in Section 5.4.3. The mechanical and cooling design for the OTK endcap will be presented in section 5.4.4.

Endcap (16 sectors, 10m^2):

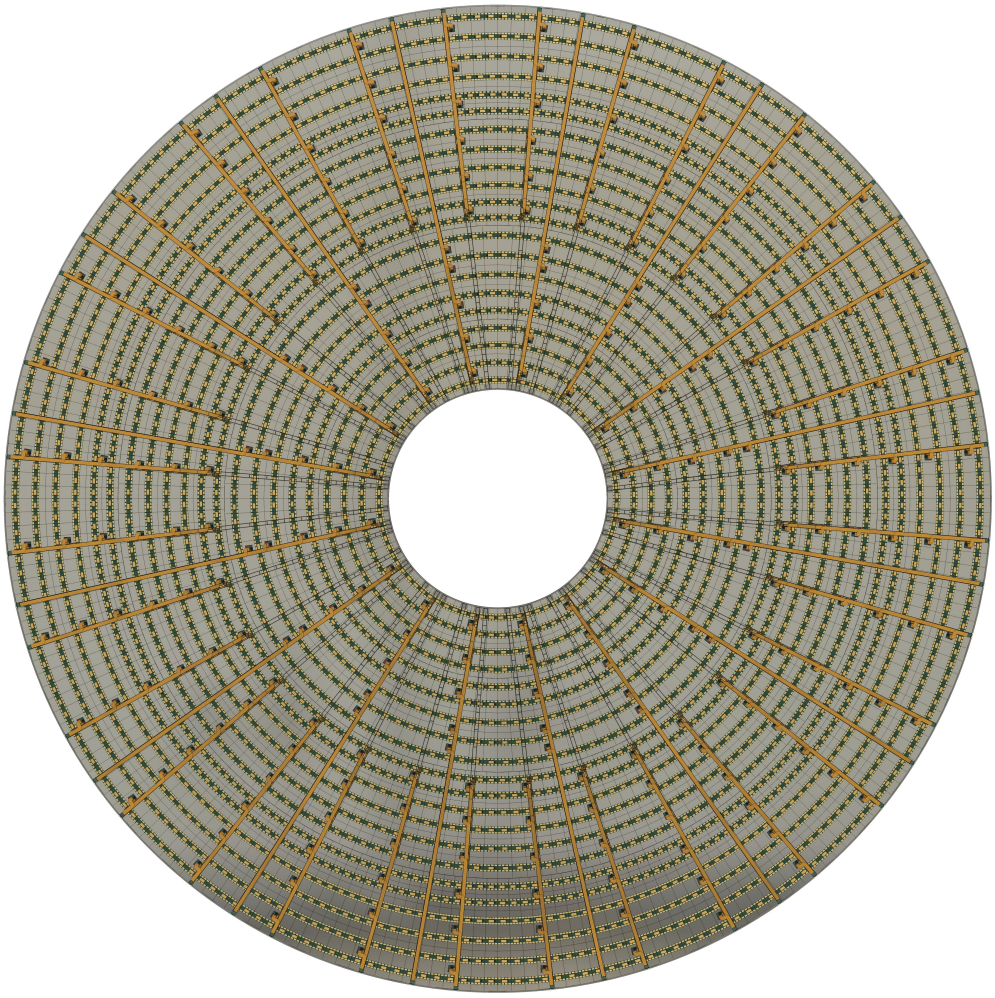


Figure 5.91: OTK endcap

5.4.3 Readout electronics

Responsible person: Xiongbo YAN

5.4.3.1 Front-end board

The FE board receives signals from LGAD strips that are processed by six OTKROC ASICs. No need of AC coupled thanks to the internal coupling design. The coupling isolates the circuit from the large leakage current and protect the ASIC from being damaged by the bias voltage in case of LGAD failure.

The OTKROC ASIC is powered by a single 1.2 V supply. This voltage is regulated and filtered by the DC-DC BaSha ASIC. The BaSha delivers up to 10A current, which is sufficient for the operation of 8 OTK ASICs. The 2 slides of sensor (4cm$\times$104cm) share one FE board, on which has 2 BaSha ASICs and 16 OTKROC ASICs.

In the baseline design, the distribution of the LGAD bias voltage is provided by external bias channels, each channel serving a LGAD module. Each bias channel has two HV wires transmitted over the services cables. The HV wires for each module are independent. The LV wires are connected by shunt cables between two neighbor FE boards. The FE board interfaces to the Concentrator Card through board side-to-side connectors transferring the following signals:

- Clock: sixteen ChiTu e-clocks (43.3 MHz), one per OTKROC ASIC ;
- Data readout: 1 up E-links (320 Mb/s) per TaoTie connecting to ChiTu on the CC;
- Configuration: one down E-link (43.3 Mb/s) for OTKROC configuration shared by sixteen OTKROCs;
- Sync/reset: one down E-link (43.3 Mb/s) for OTKROC resync/reset shared by sixteen OTKROCs;
- Monitoring: provision for sixteen temperature sensors per FE board (sensor and electronics temperatures).
- Power and ground.

Each FE board is served by 2 DC-DC converters providing 1.2 V. In order to have a more stable and precise regulation of the analog power supplies and to reduce the switching noise introduced by DC-DC, filter with passive components will be used. The aggregation chip TaoTie provides up to 16 upstream links (1.28 Gbit/s) and up to 16 clocks (43.3 MHz), and 16 downstream links (43.3 Mbit/s). This allows each FE board to receive a dedicated clock from the ChiTu and to transmit data over one dedicated uplink to one ChiTu. The sixteen OTKROCs in the FE board share two downstream links used to provide the OTKROCs with configuration, synchronization. In order for various OTKROCs to share the configuration downlinks, the configuration protocol includes a 4-bit address. Each OTKROC chip is given its 4-bit address though dedicated ID pins in the chip, which can be connected to a jumper or hardwired in the PCB. To implement reliable reception of the downstream links from the TaoTie, the OTKROC chip can use either the falling edge or the rising edge of CLK to latch the input signals.

5.4.3.2 Concentrator card and power distribution

The Concentrator Card is designed to interface the system readout with four FE boards. Its location with respect to the sensor modules, cooling bar, and FE boards on the barrel or endcap tray. The CC uses the ChiTu to provide an interface between E-links and an opto module. Each opto module has a single channel receive and a single channel transmit. The command downlink (receive) will be at 2.771 Gb/s and the data uplink will be at 11.093 Gb/s. The average rate of each data link from the FE board is 500 Mb/s. This translates to an aggregate rate of about 2 Gb/s, which can be transmitted by one ChiTu at its lower output bandwidth of 5.542 Gb/s. Another important feature of the ChiTu is to ensure the precise clock distribution, received from the downlink, to the front-end system, achieved by the high frequency clock noise filter in the PLL. The power is distributed from the DC-DC converter module BaSha, which is a step-down converter module with a radiation tolerant ASIC. To power the CC components as well as the FE cards, two other kinds of converters are needed. The BaSha1 converts 48 V to 12V on CC. The BaSha2 converts 12V to 1.2V for frontend ASIC on FE board, or 3.3V for VCSEL driver on CC. For the full channel capacity, we will use two BaSha's for reliability on FE.

5.4.3.3 Slow control and monitoring

The ChiTu provides a set of slow control and monitoring features, I2C master controllers, JTAG master controller, programmable and bidirectional IO ports, memory-like bus master controller with data and address. The preliminary of slow control and monitoring functions are following:

- Slow Control bits
- powering control bits
- configuration bits of frontend ASIC
- Monitor
- DC-DC status
- ASIC status
- temperature on FE
- temperature on CC
- leakage current of LGAD

5.4.3.4 Clock distribution

The distribution of a precise clock to the front-end is a major requirement for OTK. The clocks in the backend system are recovered from the ChiTu down links. The clock is synchronized to the 43.3MHz frequency bunch crossings rate. In order to achieve the target timing performance, the clock distribution system should have less than 15 ps rms link-to-link jitter over all clock distribution links. For instance, a 50 ps timing performance obtained from the sensors and readout electronics would be degraded by 2.2 ps by a clock distribution system with 15 ps rms jitter. The high frequency clock noise is expected to be filtered by the PLL in the ChiTu. Low frequency clock jitter and possible phase instability, in particular arising from temperature variations or low frequency response of the clock chain, will require special attention.

5.4.4 Mechanical and cooling design

Responsible person: Qi YAN

5.4.4.1 Barrel support

Similar to the ITK, the OTK barrel is also composed of segmented elements in the azimuthal direction, known as staves. Each stave is a long structure spanning the entire length of the OTK barrel, with a length of 5,680 mm — significantly longer than those in the ITK, which range from about 1,000 mm to 2,000 mm. While the three layers of ITK staves are fixed to individual barrel flanges, the OTK staves are directly mounted on the TPC outer barrel — a carbon fiber cylinder integrally molded with a specifically designed support structure — to optimize support for the longer staves while minimizing material usage.

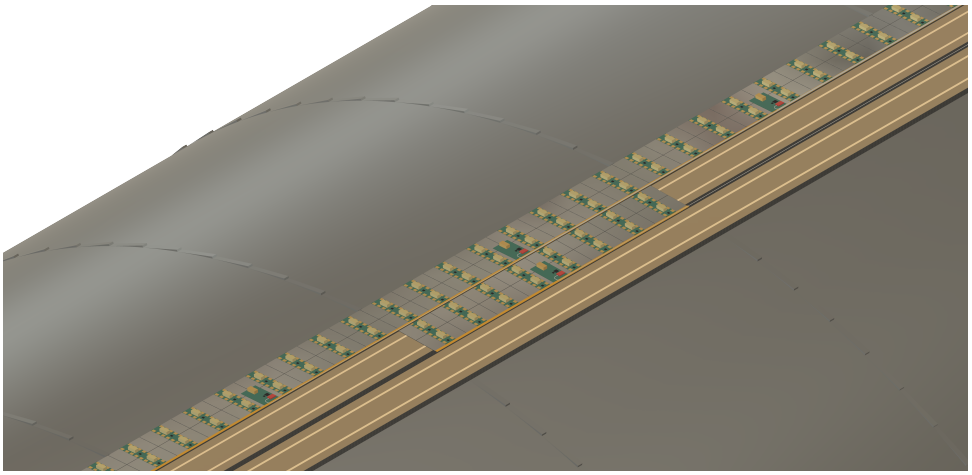


Figure 5.92: OTK barrel support

The installation procedure of an OTK stave are briefly illustrated as follows and shown in Fig. 5.93:

1. The TPC outer barrel is made of a carbon fiber cylinder with stepped ramp rings used for OTK barrel support.
2. As part of a stave, the lower support carbon fiber facesheet, with a carbon fiber honeycomb glued on top, was mounted onto the stepped ramp rings.
3. Two cooling pipes, ∼6 meters in length, were then inserted into the gaps of the carbon fiber honeycomb, sealed with high conductivity foam surrounding them.
4. Subsequently, 8 ladders were glued on top one by one to enclose stave honeycomb and complete the construction of one stave. Each OTK ladder (∼0.7 meters) has its own support, consisting of 16 sensors, electronic components, and a carbon fiber facesheet, all cured together.

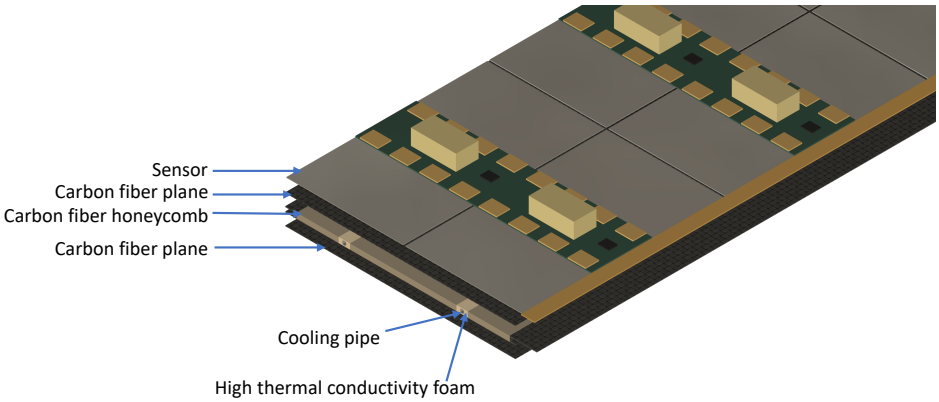


Figure 5.93: OTK barrel mechanics and cooling

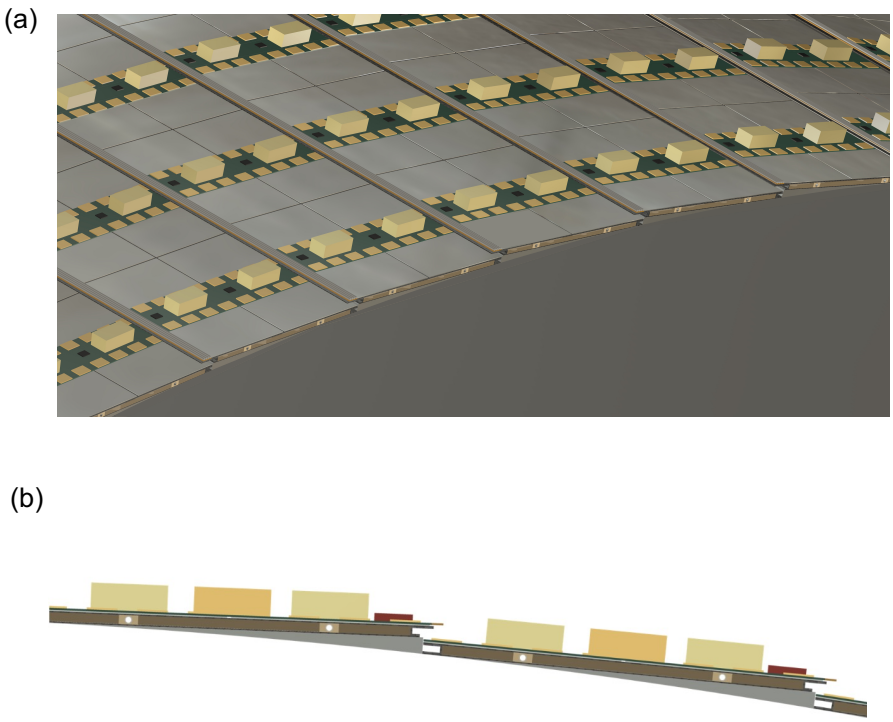


Figure 5.94: OTK stave cross section

The cross section of internal structure of a stave is shown Fig. 5.93. The OTK stave structure can also be divided into three functional units:

- Sensor Modules: The sensors glued with low-mass PCBs equipped with radiation-tolerant DC-DC converters, readout ASICs, and other components.
- Support Structure: The support structure consists of two layers of 0.3 mm carbon fiber facesheets sandwiching a carbon fiber honeycomb core. The transverse edges of the stave are enclosed by side closeouts, which are C-shaped channels made of carbon fiber. These side closeouts are important mechanical interfaces to the global support structures, increasing the stave's stiffness and reducing deformation.
- Cooling Structure: The sensors in the modules are attached to the carbon fiber facesheet using thermal adhesive. The area around the cooling pipes and the honeycomb core is filled with low-mass, high thermal conductivity foam. The carbon fiber facesheet and honeycomb are bonded using an adhesive infused with thermally conductive carbon particulates.

With the stepped ramp rings support structure for stave mounting, neighbouring staves are partially superimposed to ensure the detector's hermeticity, as illustrated in Fig. 5.94, which shows the cross section of the OTK barrel.

5.4.4.1.1 Materials The facesheets are constructed from layers of high-modulus unidirectional carbon fiber material combined with cyanate ester resins, designed to meet the overall stiffness requirements for local support and the thermal demands of conducting heat generated in the modules to the cooling structures embedded in the core.

The central portion of the local support core is filled with a low-density, high-performance carbon fiber-based honeycomb core material. The honeycomb core maintains the separation of the facesheets to ensure good bending stiffness and provides a sufficiently flat and robust surface for adhesive attachment of the modules without requiring excessively thick glue layers.

The interface between the cooling tubes and the facesheets is formed using thermally conductive carbon foam, such as Allcomp K9. Water with titanium cooling pipes (tube wall thickness of 0.2 mm and and a diameter of 5 mm) has been selected as the baseline cooling medium for the OTK. Titanium offers high corrosion resistance, lightweight properties, excellent radiation hardness, and high pressure resistance.

Table 5.15 lists the estimated contributions of the OTK stave to the material budget. The overall estimated material budget for a stave is 1.584% X_0. The overlap area between neighbouring staves accounts for 8% of the stave area,correponding to 6% of the stave materials.

Estimation of OTK stave material contributions					
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	PCB metal layers	Cu		1.436	0.200
	PCB Insulating layers	Polyimide		28.41	0.070
	Sensor	Silicon	300	9.369	0.320
	Glue		100	44.37	0.023
	Other electronics				0.100
Structure	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Cooling tube wall	Titanium		3.560	0.169
	Cooling fluid	Water		35.76	0.105
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	6000	186	0.322
	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Glue	Cyanate ester resin	200	44.37	0.045
Total					1.584

Table 5.15: Estimation of OTK stave material contributions

5.4.4.1.2 Structural characterisation The maximum sag of the OTK stave under its own weight and the first natural frequency are two key parameters that define the displacement and stability of the sensors' positions. The stiffness of the stave is provided by the carbon fiber facesheet, carbon fiber honeycomb, and the carbon fiber C-shaped channels. An OTK stave is divided into 8 ladders, each ∼0.7 m long, with both ends of each ladder mounted to the ramp structures of the TPC outer barrel, as shown in Fig. 5.94.

A finite element model of an OTK ladder for structural analysis was created with the following assumptions:

- Contributions of structures other than the carbon fiber frame and honeycomb structure were neglected. A uniformly distributed load was applied to the upper carbon fiber facesheet.
- Both ends of ladder were assumed to be fixed supports (i.e., all translational and rotational degrees of freedom at both ends were constrained).

Based on model, preliminary structural analyses were performed to evaluate the maximum deformation and the first natural frequency, as shown in Fig. 5.95 and Fig. 5.96. The results indicate a sag of 135 μm for the OTK ladder, with a corresponding first natural frequencies of 76 Hz.

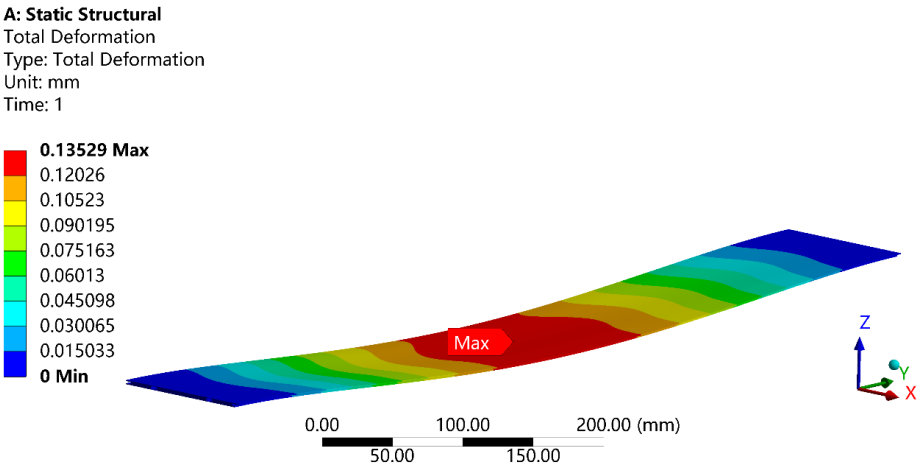


Figure 5.95: The deformation of OTK ladder

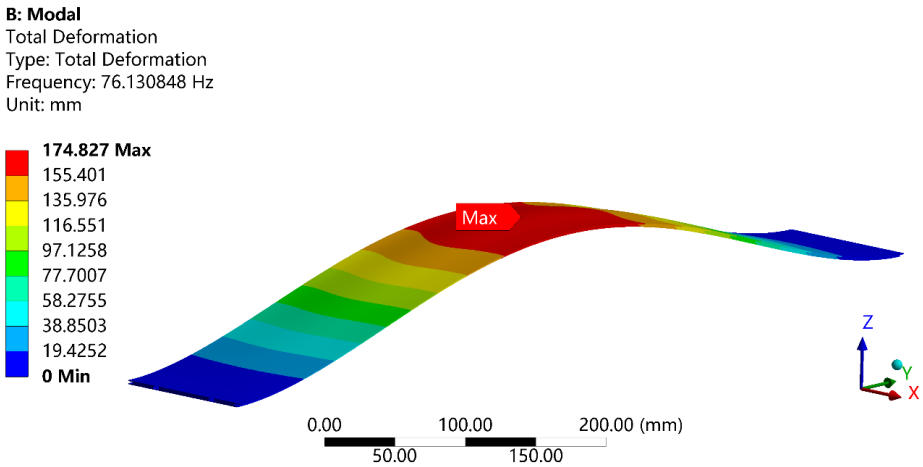


Figure 5.96: The first-order mode and the corresponding natural frequency of OTK ladder

5.4.4.1.3 Thermal characterisation According to the specifications for the OTK sensor, the cooling design must meet the following requirements:

- The overall sensor operating temperature should not exceed 30°C.
- The temperature uniformity across a single sensor should be maintained within 5°C.

Based on numerical simulations for different pipe diameters, and considering cooling system simplification, a pipe with an inner diameter (ID) of 5 mm using water cooling was selected as the baseline for the OTK cooling.

A water cooling fluid structure coupled finite element model was established to study the temperature distribution along the entire longitudinal length of the stave, considering a specific water cooling flow rate. The following configurations were used in the model:

- The heat generated by the sensors was uniformly distributed, with a magnitude of 300 mW/cm^2 (sensor heat flux).
- Cooling water entered the stave with a flow velocity of 2 m/s and a temperature of 5°C.
- Natural convection and radioactive heat transfer were not considered.

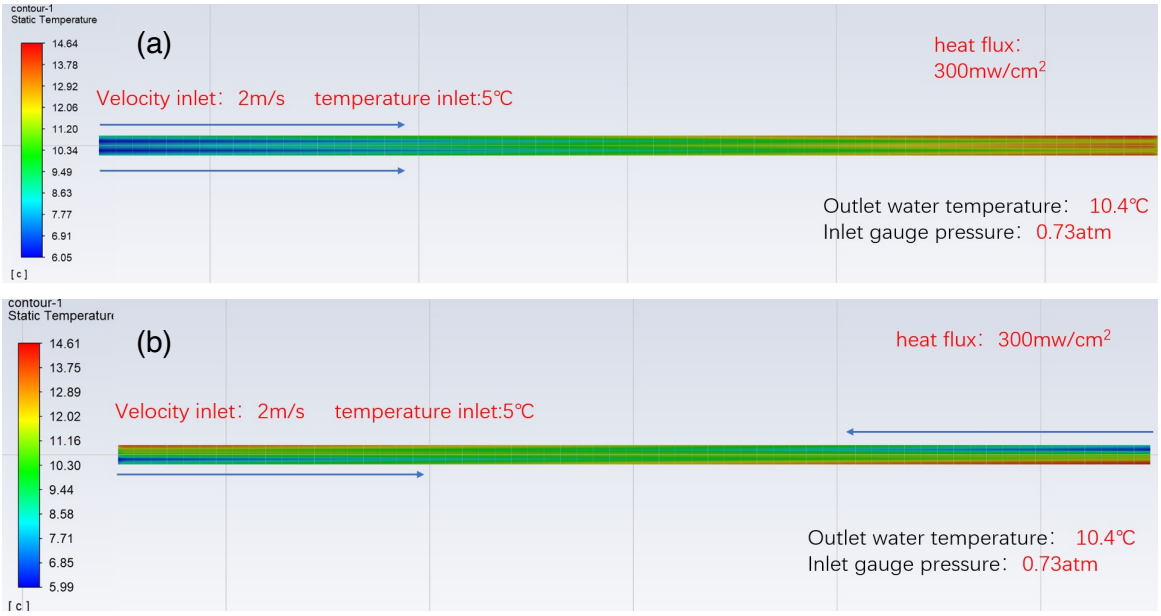


Figure 5.97: Simulation results of water cooling with a flow velocity of 2 m/s and an inlet temperature of 5°C, for (a) inlets on the same side and (b) inlets on both sides.

With the inlets of the two pipes on the same side, the simulation results are shown in Fig. 5.97 (a). As seen, the temperature gradient along the 5,680 mm length of the stave can be controlled within 10°C. When the inlets are set on

both sides, the maximum temperature on the stave shows no significant change, as shown in Fig. 5.97 (b).

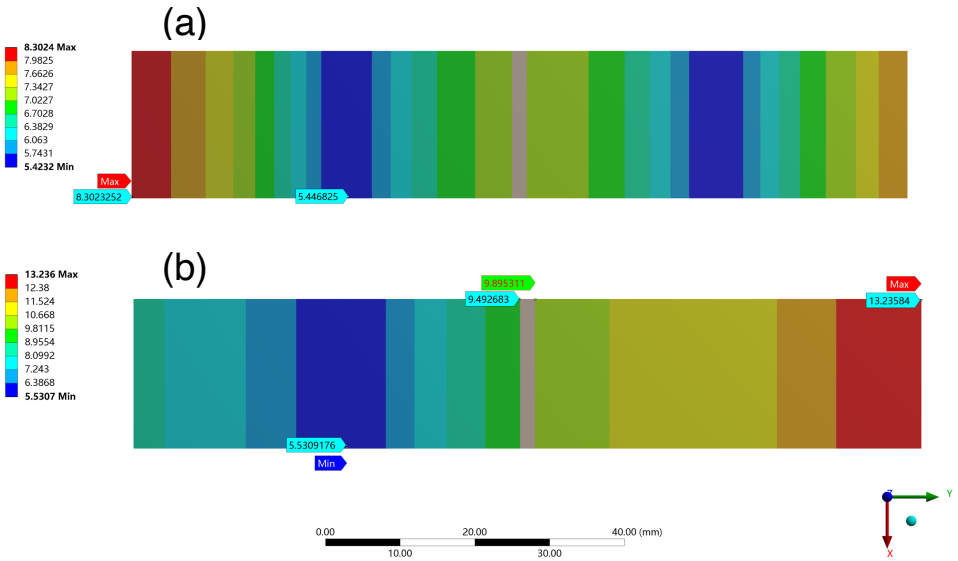


Figure 5.98: Thermal simulation of the temperature gradient aross two sensors in transverse direction, for (a) the inlet on the same side and (b) the inlet on both sides.

The temperature gradient across a single sensor is another key parameter for evaluating the cooling performance. Figure 5.98 (a) shows the temperature field distribution of two sensors near the inlet end, with the inlet on the same side, while Figure 5.98 (b) shows the temperature field distribution of two sensors near one end, with the inlet on both sides.

These results show that water cooling can meet the thermal requirements of the OTK, utilizing two 5 mm ID pipes for a stave and a water flow velocity of 2 m/s. The temperature field along the entire length of the stave can be maintained within 10°C, and the temperature difference across a single sensor can be kept within 5°C.

5.4.4.2 Endcap support

Figure 5.99 illustrates the breakdown of the OTK endcap, comprising a layer of sensor modules, a layer of cooling plates, conection rods, an inner structural ring, and an outer structural ring. To simplify both the assembly and testing processes, the endcap is segmented into 16 sectors, each with its own dedicated detection, mechanical, and cooling structures.

A detailed view of one OTK sector is shown in Fig. 5.100, which is composed of:

- Sensor Modules: The sensors glued with low-mass PCBs equipped with radiation-tolerant DC-DC converters, readout ASICs, and other components.
- Cooling Plate:
  - The cooling plate consists of two layers of high stiffness carbon fiber facesheets sandwiching a low-mass, high thermal conductivity foam core embedded serpentine cooling loops. The composite pyrolytic graphite foam is the same as the one used in the OTK barrel stave.
  - The edges of the sector are enclosed by side closeouts, which interface with inlets and outlets of cooling loops. These closeouts, made of carbon fiber, serve as critical mechanical interfaces to the overall support structures, enhancing the sector's stiffness.
  - The sensors in the modules are attached to the cooling plate (more accurately, the carbon fiber facesheet) using thermal adhesive.

16 composite rods are installed along the edges to join adjacent sectors, forming the complete OTK endcap disk. Figure 5.101 illustrates the mechanical interface between neighboring sectors, where each composite rod extends from the inner to outer ring, connecting adjacent cooling plates. To reinforce the structural integrity of the assembly, inner and outer mounting rings are secured to the disk's perimeter, enhancing the connections between neighboring sectors.

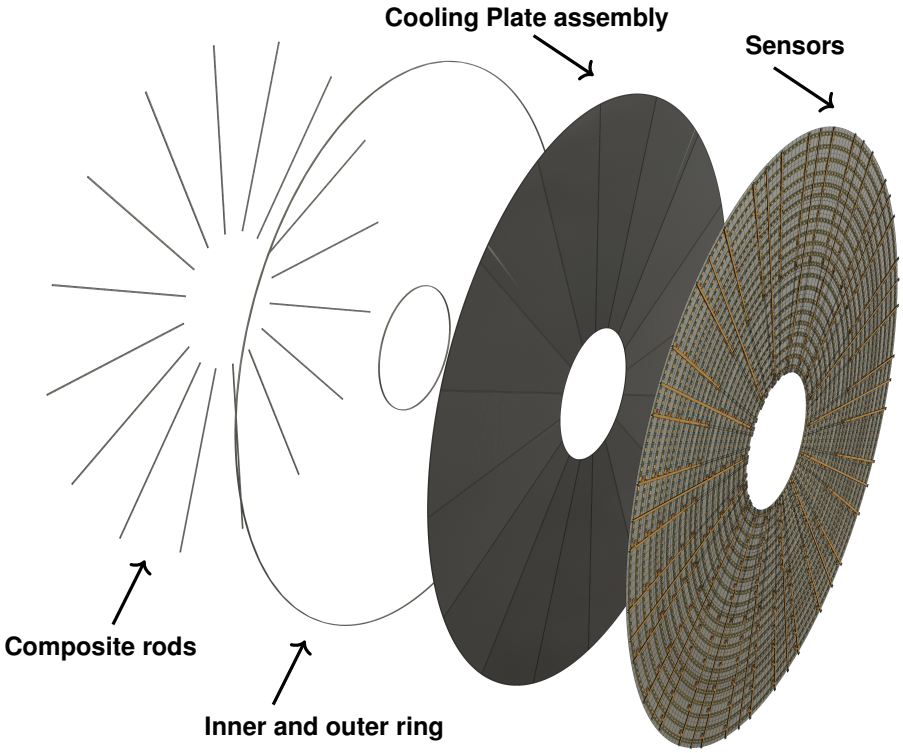


Figure 5.99: OTK endcap mechanics and cooling

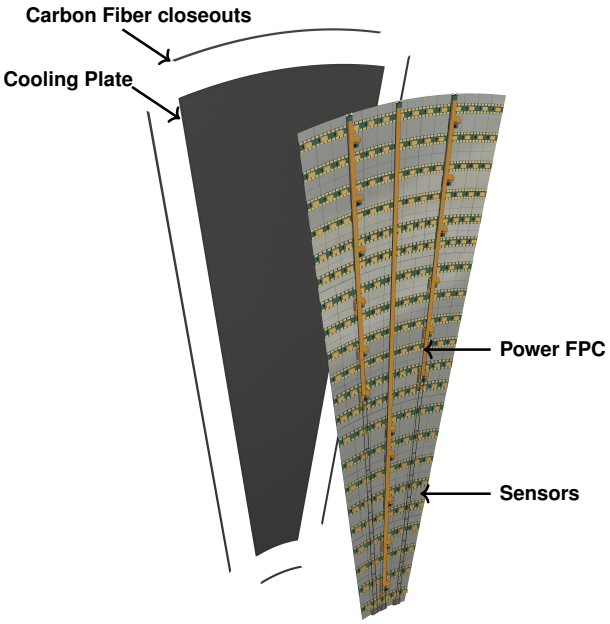


Figure 5.100: OTK 1/16 sector mechanics and cooling

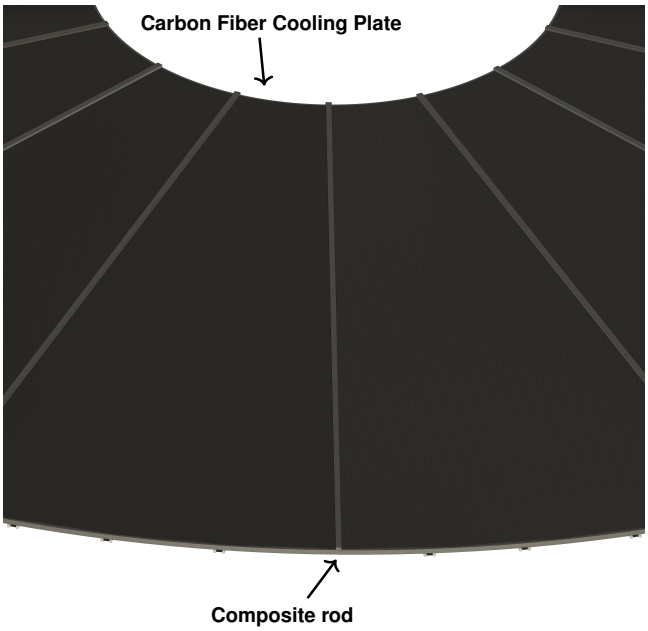


Figure 5.101: Mechanical connection between sectors

Together with the rods, these rings enhance the overall stiffness of the endcap and absorb induced stress. Additionally, the outer ring also serves as a routing structure for the cooling lines from the cooling plate.

5.4.4.2.1 Materials The two facesheets of the cooling plate for each 1/16 sector are constructed from layers of high-modulus unidirectional carbon fiber material combined with cyanate ester resins. The interface between the cooling tubes and the facesheets is formed using thermally conductive carbon foam, such as Allcomp K9. Water circulating through cooling loops of the cooling plate has been chosen as the baseline cooling medium for the OTK endcap.

The rods, inner ring, and outer ring, which connects sectors to a endcap disk, must be made from stiff materials. The rods are constructed from carbon fiber. For the inner ring and the outer ring, the primary candidate materials are the high-performance PEEK polymer and Torlon polyamide-imide technology.

Table 5.16 lists the estimated contributions of the OTK endcap to the material budget. The overall estimated material budget is 1.584% X_0.

Estimation of OTK endcap material contributions					
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	PCB metal layers	Cu		1.436	0.200
	PCB Insulating layers	Polyimide		28.41	0.070
	Sensor	Silicon	300	9.369	0.320
	Glue		100	44.37	0.023
	Other electronics				0.100
Structure	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Cooling tube wall	Titanium		3.560	0.169
	Cooling fluid	Water		35.76	0.105
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	6000	186	0.322
	Carbon fiber facesheet	Carbon fiber	300	26.08	0.115
	Glue	Cyanate ester resin	200	44.37	0.045
Total					1.584

Table 5.16: Estimation of OTK endcap material contributions

5.4.4.2.2 Structural characterisation

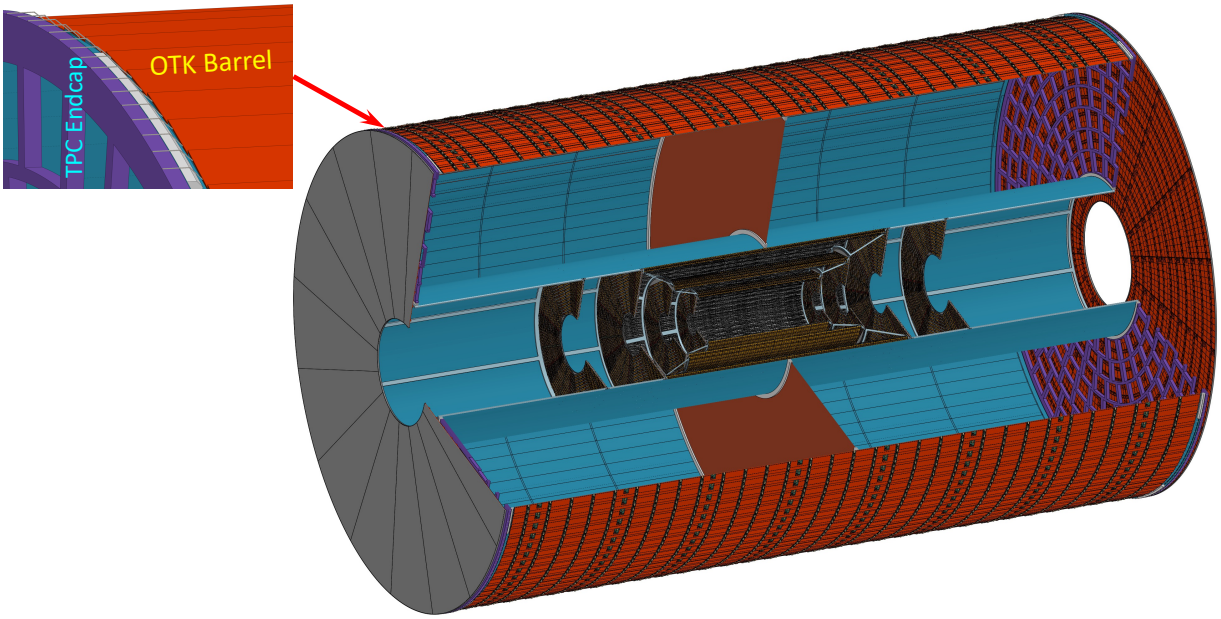


Figure 5.102: OTK Mechanics and Installation

5.4.4.2.3 Thermal characterisation

5.4.5 Prospects and plan

Responsible person: Qi YAN, Mei ZHAO, Xiongbo YAN

zhaomei:

AC-LGAD can provide 4D information including timing and spatial, which can serve as tracker layer for particle identify and time-of-light layer for future colliders, but researches still need to be done about the performance of long strip AC-LGAD. From sensor part, researches will be done to clarify the strip AC-LGAD performance, including simulation, sensor fabrication and testing. By using TCAD tools, Model of AC-LGAD with different strip length and process parameters will be built to study how the strip length affect the sensors signal and how to change the process parameters to optimize the sensors spatial and timing performance. Based on the simulation results, prototype of AC-LGAD with long strips will be fabricated and test(strip length: 4cm, 2cm, 1cm). The testing will include I-V, C-V, spatial resolution and timing performance, while radiation testing and beam test will also be done after the basic test. Strip length and pitch size may be changed to keep the performance after some submission for sensor fabrication and testing. AC-LGAD with 2cm strip length is considered as backup plan. while reducing the strip length from 4cm to 2cm, increasing the strip pitch from 100um to 200um, the readout channel number and power consumption will be similar to the 4cm design. Considering the strip length affect to timing performance and yield, after demostration of the performance of strip AC-LGAD with different length, the decision of the AC strip length and sensor size will be made. The readout scheme will base on a careful study to the signal of LGAD strip. The crital parts like preamplifier, discriminator, and TDC modules will be verified in the first submission. Performance testing of the ASIC will be carried out after 3 months, then will undergo radiation hardness testing. In the second submission, the digital logic will be added in the integration of multi-channels,named V0. The chip will connect with the LGAD and do a careful test. The multi-channel design will be further refined, and the V1 version of the ASIC will be submitted for wafer production. Simultaneously, the prototype design of the LGAD readout frontend electronic system will be initiated. In 2027, a V2 version of the ASIC will be conducted, along with the system prototype with sensor and electronic. In the end of 2027, the prototype system will be finalized in preparation for the mass production of the chips. Moreover, sensors performance with ASIC will be test after sensor with ASIC module be built. The important thing here is to check if TOA and TOT can give enough information for timing and spatial resolution, and find ways to improve the ASIC and sensors to meet the requirement of OTK detector. Wire bonding is the way to connect sensors and ASIC now, which has no issues since the technology already be used in many experiment. While new method for sensor and ASIC package/connecting, like connecting sensor to inter board using balls and ASIC also to inter board, will also be studied to improve the detector design. Besides things mentioned above, assembly method and mechanics for arranging and supporting the modules will also be studies, including the support structure, support material, the cooling system and so on. For the cooling system, some trails using different cooling structure and material will be done. All the things mentioned above will be arranged in the 3-year plan.

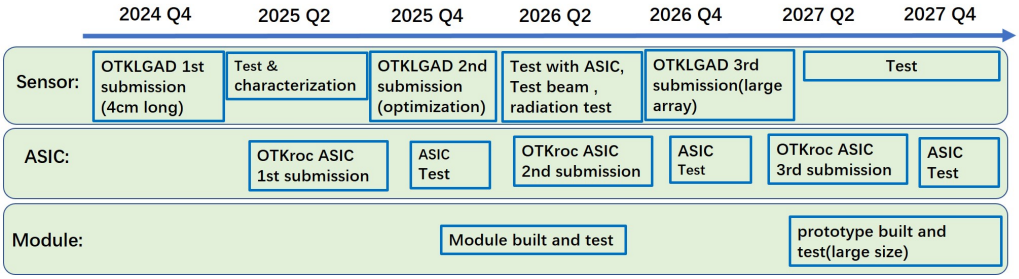


Figure 5.103: Timeline for OTK, including sensor, ASIC, mechanics and so on

5.5 Beam background estimation

Responsible person: Zhan LI, Xiaojie JIANG, Yiming LI, Qi YAN

The CEPC Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK) are designed to operate in the most demanding Z-pole mode. The readout data rate of the CEPC silicon tracker is predominantly influenced by the beam background.

Under Z-pole operation, the typical cross-section for $e^+e^- \to q\bar{q}$ is $\sim 3 \times 10^7\ \mathrm{fb}^{-1}$, corresponding to an event rate of ∼kHz. For most events, the track multiplicity is well below one hundred, resulting in a hit rate at the innermost part of the silicon tracker at the level of $10^3\ \mathrm{hits/cm^2/s}$. However, the beam background, as detailed in [MDI chapter reference], is estimated to be one to two orders of magnitude higher.

5.5.1 Beam background simulation

The primary sources of beam background are:

- pair production background
- single beam background.

5.5.1.1 Pair production background

Pair production background arises from beamstrahlung, a form of bremsstrahlung caused by the interaction of one beam's particles with the electromagnetic field of the opposite beam during collisions. This process produces photons, which can subsequently generate low-energy electron pairs, contributing to the pair production background.

This type of background is generated near the interaction point (IP). Shielding against this background is challenging. Most photons and electron pairs produced by beamstrahlung move forward and exit the detector region along the beam pipe. However, a fraction of particles with relatively higher momentum (generally < 0.3 GeV) can escape the beam pipe, enter the detector region, or generate secondary particles that impact the detector.

5.5.1.2 Single beam background

Single beam background includes the following four types:

- Beam Thermal Photon Scattering (BTH)
- Beam Gas Coulomb Scattering (BGC)
- Beam Gas Bremsstrahlung Scattering (BGB)
- Touschek Scattering (TSC)

5.5.1.2.1 Beam Thermal Photon Scattering (BTH) Certain components in the accelerator, such as the beam pipe, continuously emit large quantities of thermal photons. These photons undergo Compton scattering with the charged particles in the beam, causing energy loss. If the energy variation exceeds the accelerator's energy acceptance, the particles are lost and escape the beam pipe. The momentum range of background particles produced by this process is 0–beam momentum.

5.5.1.2.2 Beam Gas Coulomb Scattering (BGC) and Beam Gas Bremsstrahlung Scattering (BGB) Although the accelerator operates under high vacuum conditions, a small amount of residual gas remains. As particles pass through the beam pipe, they may scatter with these gas molecules, leading to:

- Elastic Scattering (Coulomb Scattering): Particles scatter off atomic nuclei of the gas molecules, changing their trajectory. If the angle change is too large, the particles escape the beam pipe.
- Inelastic Scattering (Bremsstrahlung): Particles emit photons and lose energy during scattering. If the energy loss exceeds the energy accelerator's energy acceptance, the particles escape the beam pipe.

For elastic scattering, the particle's momentum magnitude remains unchanged, with only the direction altered, resulting in an initial momentum equal to the beam momentum for background particles. For inelastic scattering, the initial momentum range of the background particles is 0–beam momentum.

5.5.1.2.3 Touschek Scattering (TSC) Within particle bunches in the accelerator, particles can undergo elastic scattering due to transverse oscillations. This scattering generates an energy spread among the beam particles. If this spread exceeds the accelerator's energy acceptance, beam loss occurs. The initial momentum of these background particles is equal to the beam momentum.

5.5.2 Hit rate estimation for beam background

The beam background is simulated using a dedicated program CEPC software (CEPCSW), incorporating all the sources of beam background discussed earlier. In the simulation, the beam background hit rates have been been estimated for Higgs mode, Low Lumi Z mode, and High Lumi Z mode, with the corresponding beam configurations for all 3 modes are summarized as follows:

- Low Lumi Z: A magnetic field of 3 T, a bunch spacing of 69 ns, ...
- Higgs: A magnetic field of 3 T, a bunch spacing of 346 ns, and a bunch spacing gap of 53%, meaning that only 47% of the beam ring has bunches simultaneously...
- High Limi Z:

Estimated Silicon Tracker Hit Rates [10^4 Hz/cm^2]						
	Low Lumi Z		Higgs		High Lumi Z	
	Average	Max	Average	Max	Average	Max
ITKB1	3.93	9.41	0.012	0.108		
ITKB2	2.04	5.26	0.019	0.202		
ITKB3	0.72	2.37	0.021	0.154		
OTKB	0.18	1.56	0.014	0.148		
ITKE1	10.63	58.70	0.151	1.052		
ITKE2	6.19	41.07	0.193	1.429		
ITKE3	2.45	24.80	0.166	1.427		
ITKE4	1.70	8.25	0.140	0.657		
OTKE	0.38	4.41	0.026	0.353		

Table 5.17: Estimated Silicon Tracker Hit Rates

The estimated average and maxinum hit rates for different layers of the tracking detector are summarized in Table 5.17. As an example, for the Low Lumi Z, the differential hit maps for individual tracker layers are shown in Figs. 5.104 and 5.105.

5.5.3 ITK tolerable hit rate

For the HV-CMOS pixel sensor used in the ITK, each fired pixel generates 42 bits of data, with an average of $\sim$1.5 pixels firing per hit. The data from all sensors in an ITK module (e.g., 14 sensors per barrel module) is transmitted to a data link chip (GBTx-like). This chip collects and aggregates data from each sensor via low-speed (640 Mbit/s or 320 Mbit/s) electrical links (e-links), serializes it, and encodes it for efficient high-speed transmission (10.24 Gbit/s) to an optical fiber link.

The supported data rate per sensor is up to 640 Mbit/s, corresponding to a maximum hit rate of 3.0×10^6 Hz/cm^2, considering the sensor's active area of 1.74 cm$\times$ 1.92 cm. This detector's tolerable hit rate is $\sim$32 times larger than the estimated maximum background hit rate for the first ITK barrel (ITKB1, 9.41×10^4 Hz/cm^2) and $\sim$5 times larger than that for the first ITK endcap at Low Lumi Z (ITKE1, 5.87×10^5 Hz/cm^2), as summarized in Table 5.17.

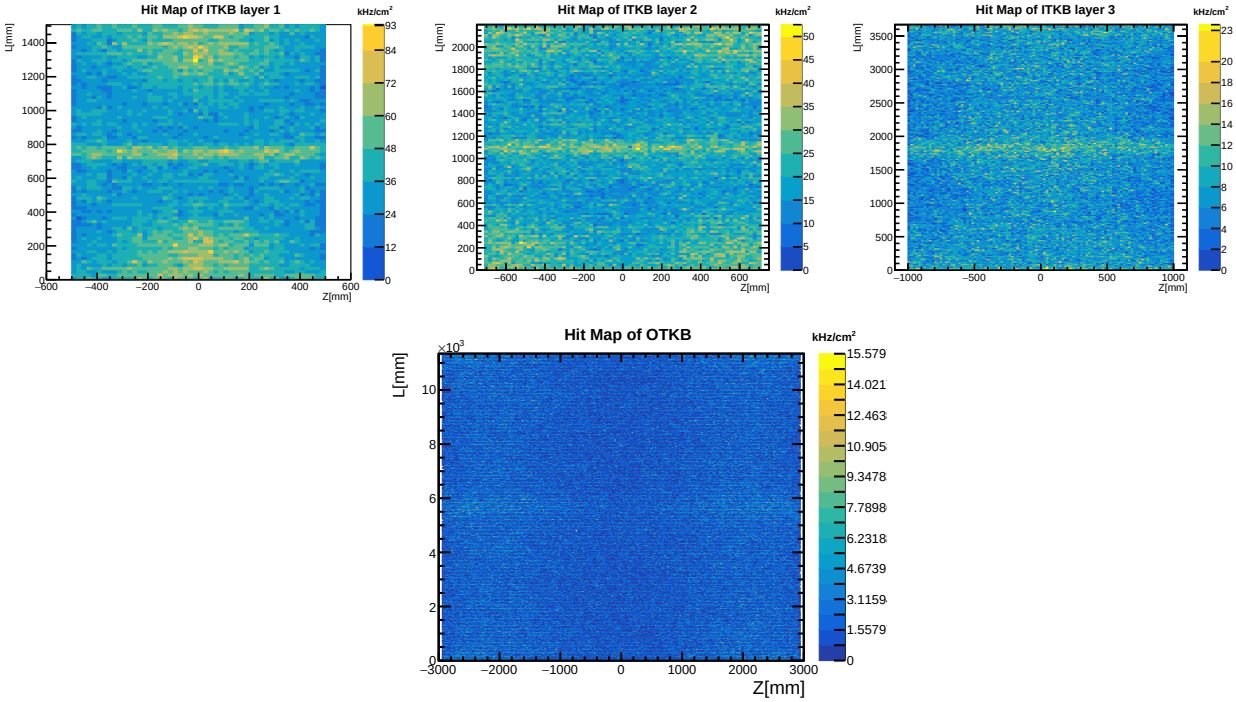


Figure 5.104: Background hit maps of the ITK and OTK barrels.

5.5.4 OTK tolerable hit rate

For the AC-LGAD strip sesnor used in the OTK, each fired strip generates 48 bits of data, with an average of $\sim$2 strips firing per hit. Data from 6 or 8 sensor readout ASICs (6 ASICs are used only in specific parts of the OTK endcap) is aggregated by the primary data aggregation chip. In the OTK barrel, 16 primary data aggregation chips (e-links) are connected to a common data link chip (GBTx-like) on the second aggregation board, with each primary data aggregation chip connecting via a 320 Mbit/s e-link. In the OTK endcap, 10 to 14 primary data aggregation chips (e-links) are connected to a common data link chip on the second aggregation board, with each primary data aggregation chip connecting via a 640 Mbit/s or 320 Mbit/s e-link.

The supported data rate per sensor readout ASIC is up to 40 Mbit/s for the barrel and up to 80 Mbit/s for the endcap, corresponding to a maximum hit rate of 7.4×10^4 Hz/cm^2 for the barrel (detector active area $\sim$1.28 cm $\times$ 4.4 cm per ASIC) and 2.0×10^5 Hz/cm^2 for the endcap (detector active area $\sim$1.28 cm $\times$ 3.3 cm per ASIC). This detector's tolerable hit rate is $\sim$5 times larger than the estimated maximum background hit rate for the OTK barrel (OTKB, 1.56×10^4 Hz/cm^2) and $\sim$5 times larger than that for the OTK endcap at Low Lumi Z (OTKE, 4.41×10^4 Hz/cm^2), as summarized in Table 5.17.

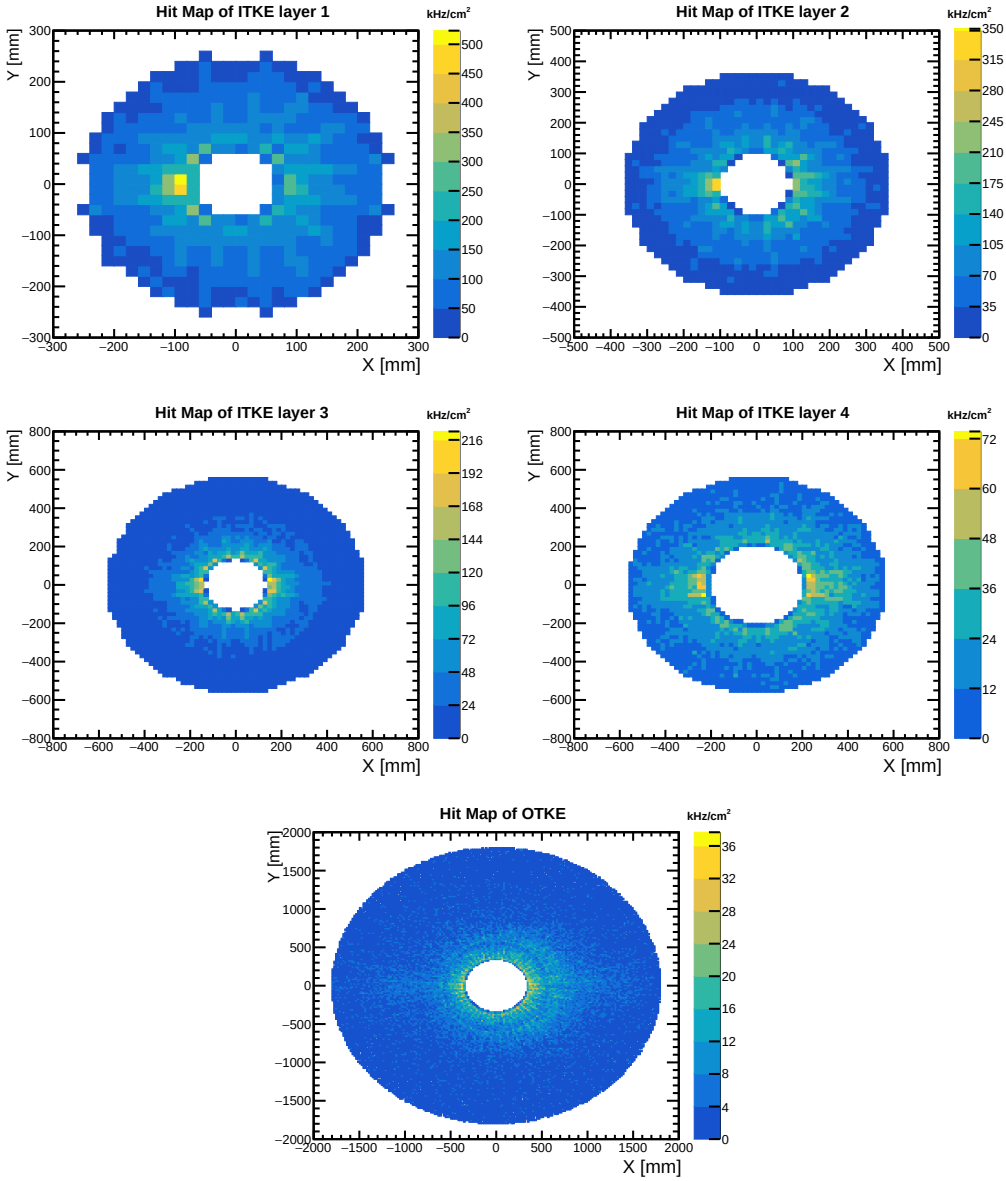


Figure 5.105: Background hit maps of the ITK and OTK endcaps.

5.6 Performance

Responsible person: Gang LI, Chengdong FU, Qi YAN

The complete CEPC tracking detector system, from the inside out, is divided into a silicon vertex detector, an inner silicon tracking detector, a time projection chamber, and an outer silicon tracking detector; on the other hand, it can also be divided into a barrel section and two end-cap sections.

According to the structure of CEPC tracking system, the performance of silicon tracker will be demonstrated in two ways. On one hand it will be shown as key component of a complete tracking system. On the other, the standalone performance of silicon tracker will be shown as well.

5.6.1 The performance of the barrel region

The CEPC tracking system is designed to encompass both electroweak physics (energetic leptons) and flavor physics (charged hadrons within a jet). This means that the tracker need achieve a resolution of several hundred MeV for Higgs mass and a few MeV for beauty and charm hadron masses, when all these particles decay to charged final states.The system aims to achieve a precision in transverse momentum measurement given by the formula:

$$\frac{\sigma_{P_t}}{P_t} = aP_t + \frac{b}{\sin^{\frac{1}{2}}\theta} ,$$

where $a = 2 \times 10^{-5}$ and $b = 0.001$. Figure 5.106 illustrates the anticipated momentum resolution for the CEPC tracking system within the barrel region. It is evident that both parameters a and b meet the specified requirements, achieved through the integration of the silicon tracker with the gaseous detector.

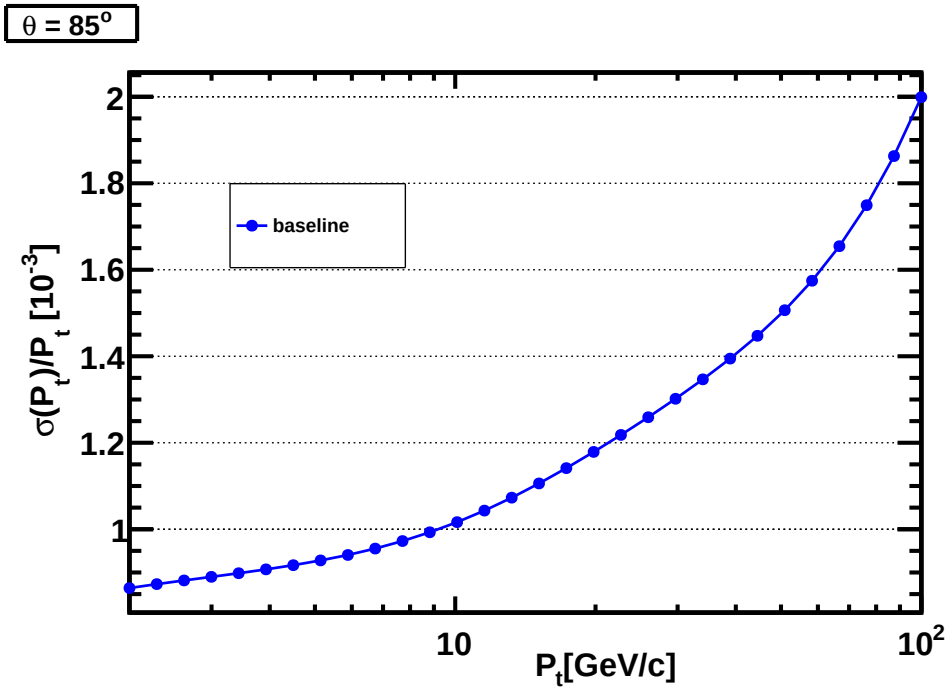


Figure 5.106: Transverse momentum resolution as a function of transverse momentum for the complete tracking system at a polar angle of $85°$.

5.6.1.0.1 Roles of gaseous and silicon trackers To effectively measure charged particle tracks across a wide range of high and low momenta, a combination of gaseous and silicon trackers is employed. This strategic approach enhances transverse momentum resolution by leveraging the unique strengths of each detector type. The silicon tracker provides the high spatial resolution necessary for precise measurements of high-momentum particles, while the gaseous detector's

low material budget is ideal for minimizing interactions with low-momentum particles, thus preserving their measurement integrity. By integrating these two systems, the performance of the detection process is optimized, ensuring accurate and reliable data across the entire momentum spectrum.

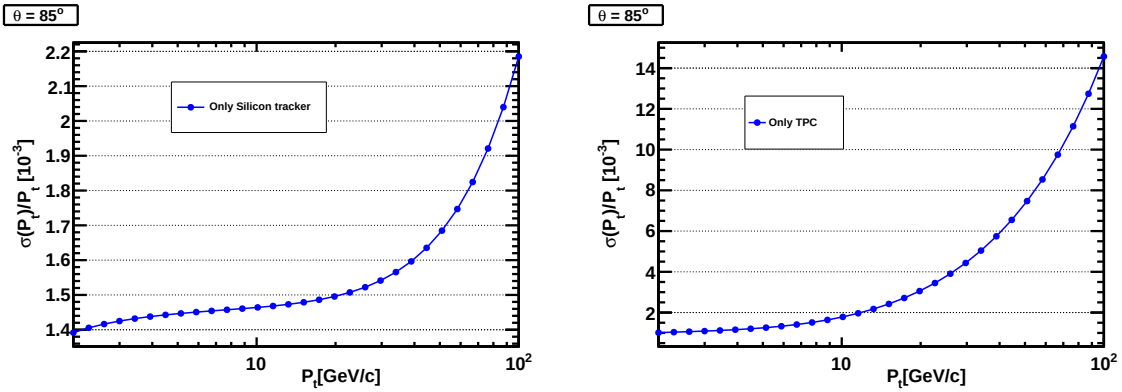


Figure 5.107: Transverse momentum resolution as a function of transverse momentum for the silicon tracker only (left panel), including vertex detector, and TPC only (right panel) at a polar angle of $85°$.

Silicon tracking detectors are renowned for their high precision in position measurement. This precision is a critical asset for particles with high momentum, as these particles exhibit minimal deflection within detectors. The fine measurement capabilities of silicon trackers are essential for accurately determining the momentum of these particles.

Conversely, gas detectors like TPCs possess a low material budget. This attribute significantly reduces the interaction between the detector material and the particles, thereby minimizing the disturbance to their momentum. This feature is particularly advantageous for particles with low momentum, as they are more susceptible to the effects of the material they pass through.

By integrating these two detector technologies, their complementary strengths are effectively harnessed. Silicon trackers are renowned for their precision in position measurement, which is crucial for high-momentum particles. Meanwhile, gas detectors, with their low material budget, are well-suited for low-momentum particles, ensuring minimal disruption to their trajectories.

Figure 5.107 presents the transverse momentum resolution as a function of transverse momentum for two distinct scenarios: the silicon tracker in isolation (left panel) and the TPC alone (right panel), both evaluated at a polar angle of $85°$. The left panel indicates that the silicon tracker exhibits a relatively good resolution. On the other hand, the right panel demonstrates that the TPC. In addition to its role in momentum measurement, TPC is capable of providing excellent dN/dx measurements, which are crucial for Particle Identification.

In summary, the collaborative effort of silicon tracking detectors and gas detectors offers a holistic solution for achieving exceptional transverse momentum resolution. This union not only exploits the high precision inherent to silicon trackers but also the low material budget characteristic of gas detectors, thus guaranteeing superior measurement accuracy across a broad range of particle momenta.

5.6.2 The performance of forward tracking (end-cap)

The forward region of the tracking system encompasses both the transition zone, where the TPC and silicon tracker work, and the very forward region, which is exclusively serviced by the silicon tracker. This area presents unique challenges for momentum resolution due to the scarcity of measurement points and the relatively short lever arm. Consequently, achieving precise momentum resolution in this region is particularly challenging.

However, the design of the tracking system, as evidenced by the extended length of the detectors, has managed to overcome these obstacles to a significant extent. Fig. 5.108 illustrates the transverse momentum resolution as a function of the polar angle in the forward region. The figure shows two distinct lines representing particles with momenta of 2 GeV (blue) and 100 GeV (red). It is observable that for both momentum regions, the resolution is still achieved at percent level or better in such challenging regions.

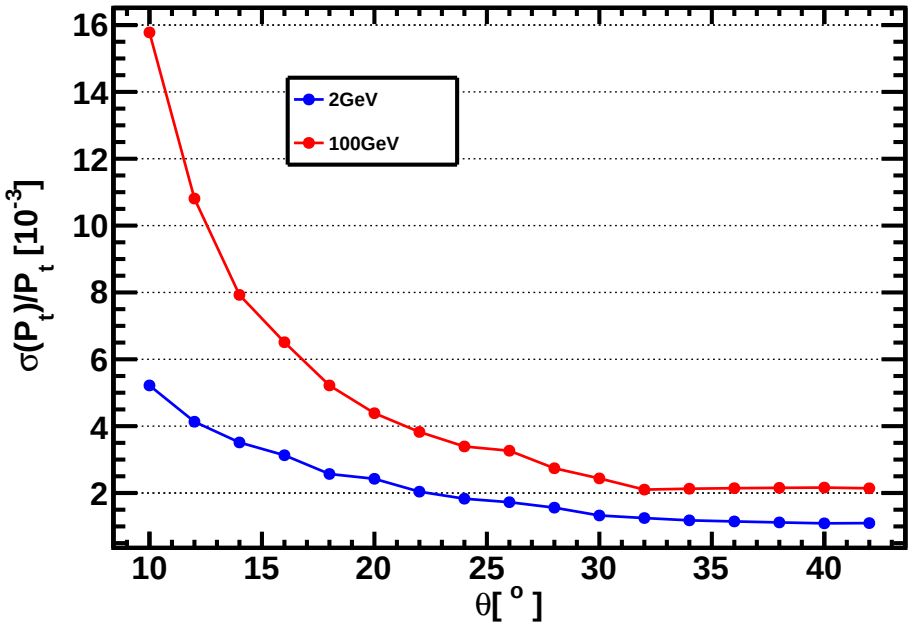


Figure 5.108: Transverse momentum resolution as a function of the polar angle in forward region.