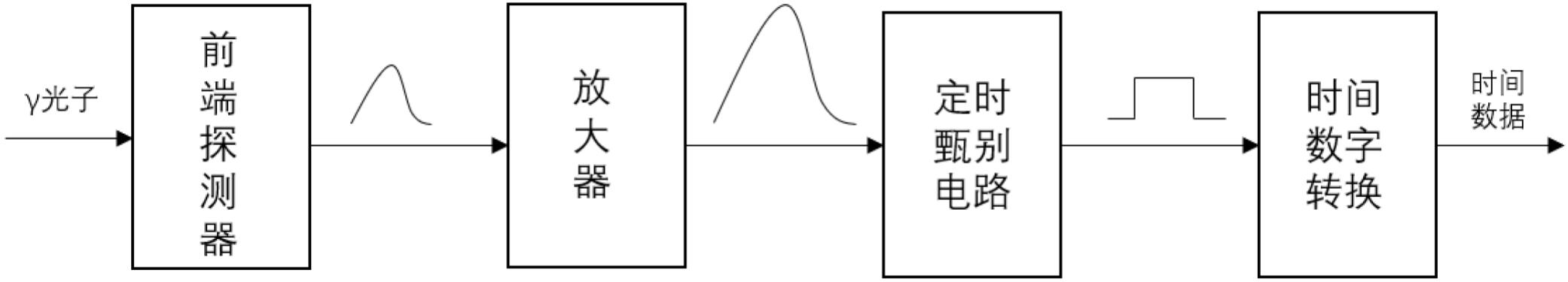
高精度时间时间测量

严雄波

1. 时间测量概述



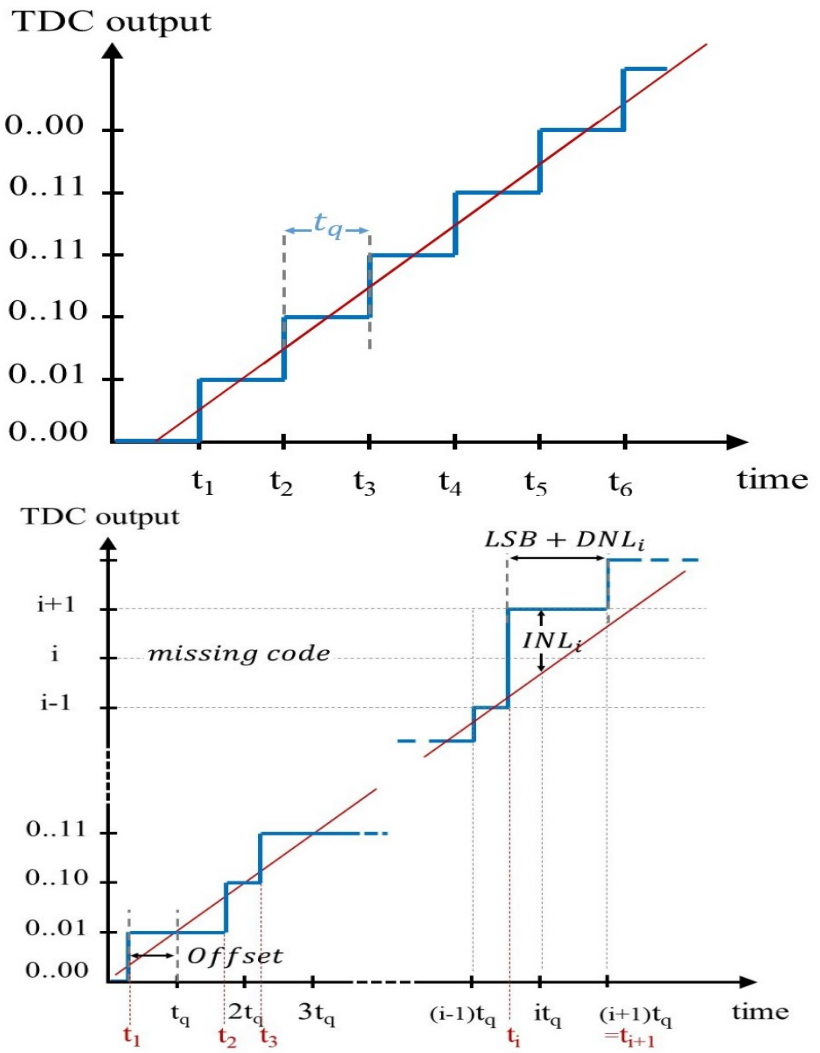
- 对于一个高能物理实验，通常探测器系统测量的一般两类信息：幅度信息和时间信息；
- 幅度信息通过ADC数字化，时间信息通过TDC数字化；
- 不同探测器由于其功能、要求的不同，对TDC的性能（主要是分辨率）的要求也有所区别。对于飞行时间测量（TOF）需要ps级时间分辨率。

1.1 性能指标

- 时间分辨率：TDC能够测量的最小时间间隔；
- 测量精度：理论上TDC对一个特定时间的测量，结果应该相同，但实际上存在一定的误差；
- 线性误差与非线性误差:线性误差主要是偏移误差和增益误差；非线性误差主要包括积分非线性与微分非线性；
- 动态范围：动态范围是TDC能够进行准确测量的时间范围；
- 转换时间：指从时间信息输入到得到可用测量结果之间的时间差；
- 功耗、面积等。

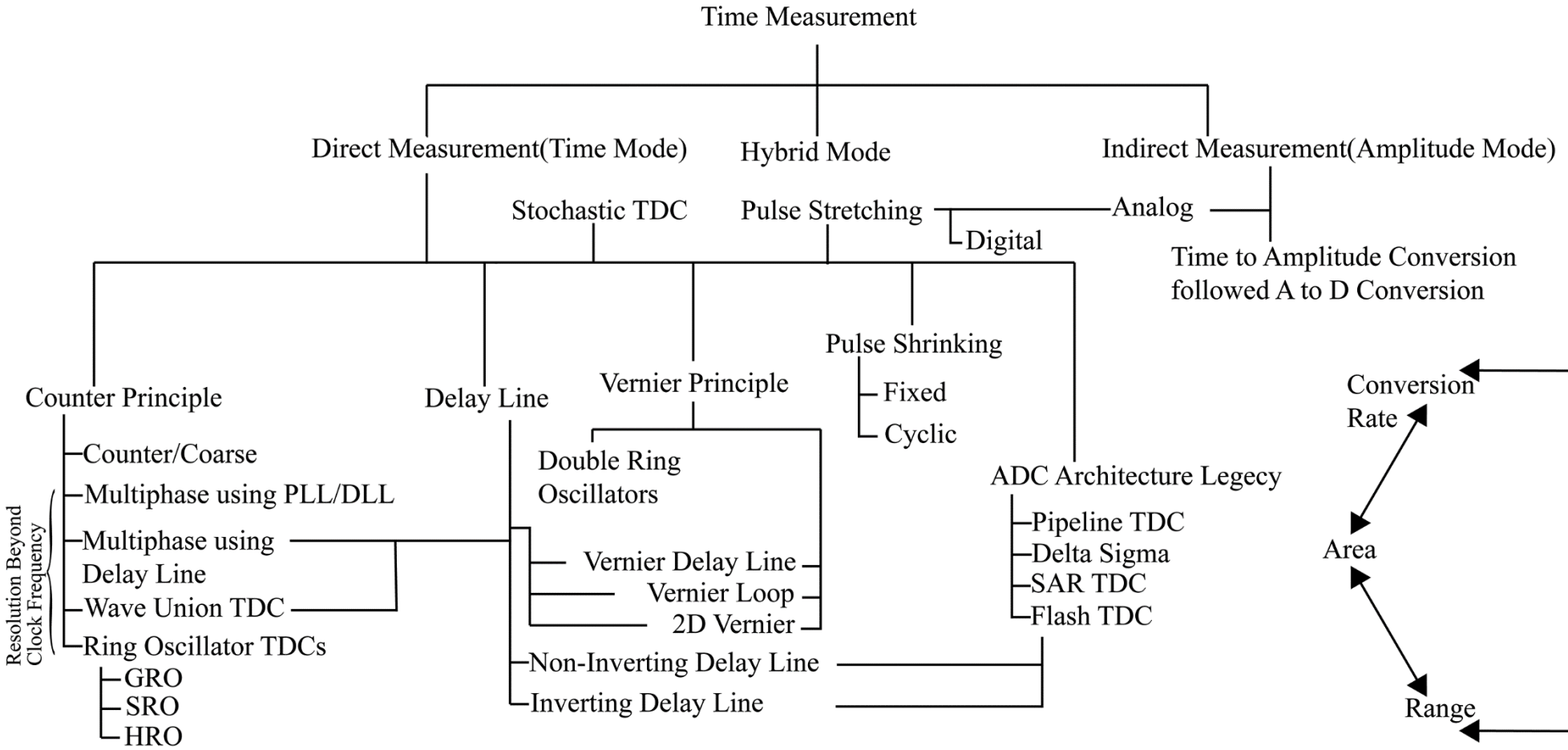
TDC的测量误差：

$$\sigma_{rms} = \sqrt{\sigma_q^2 + \sigma_{INL_{start}}^2 + \sigma_{INL_{stop}}^2 + \sigma_{CLK}^2 + \sigma_{TDC}^2}$$



1.2 TDC 分类

- 根据TDC的架构进行分类，可以分为三类：采样型TDC、噪声整形TDC以及随机TDC。

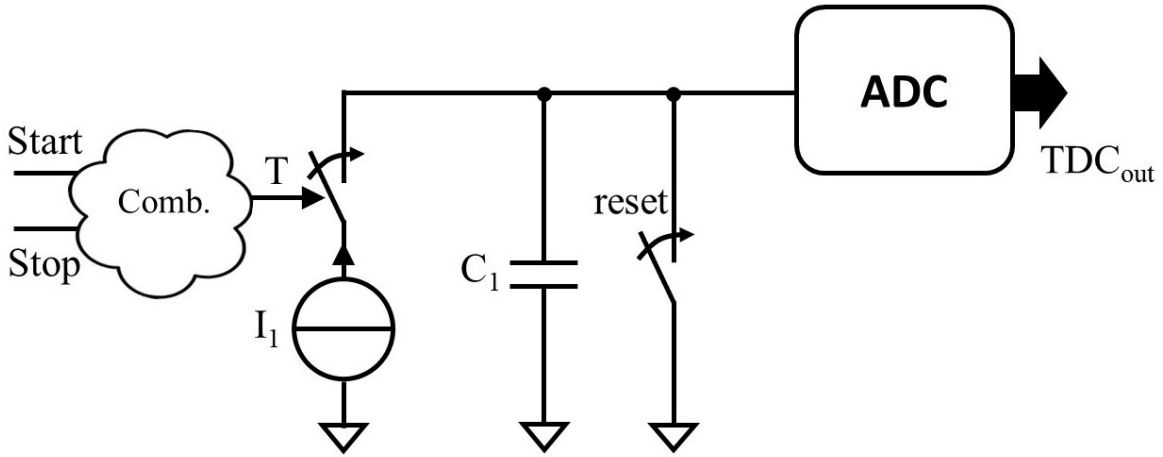


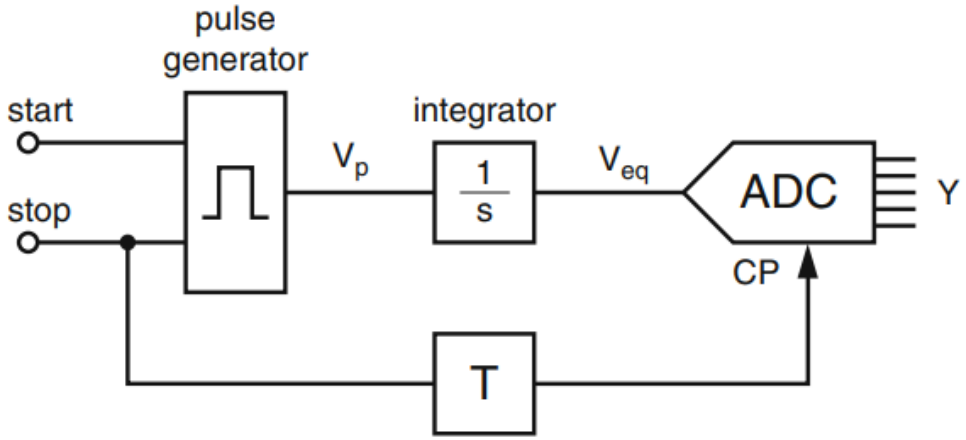
1.2 TDC分类

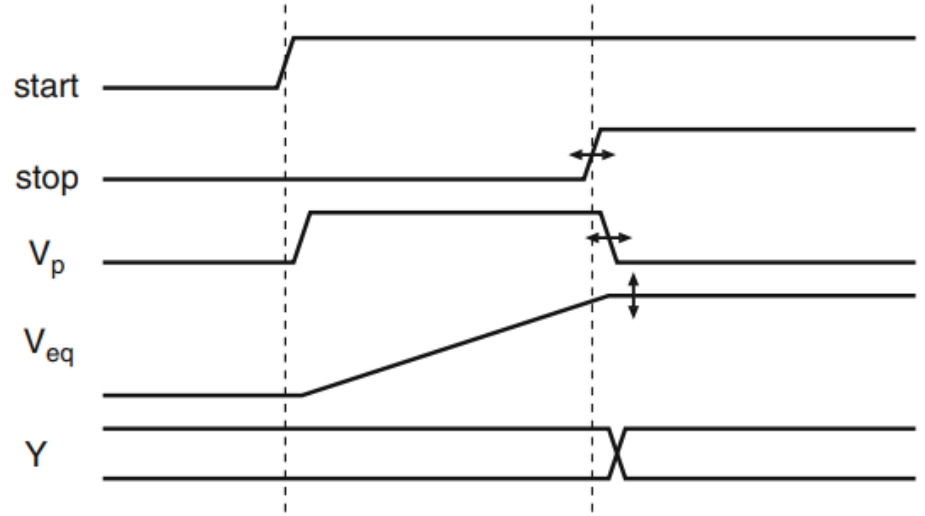
- 采样型TDC通过对时间信息进行采样进行转换
- 采样型 TDC 包括
  1. 基于模拟的 TDC
  2. 基于计数器的 TDC
  3. 延迟线 TDC
  4. 游标型TDC
  5. 逐次逼近型 TDC
  6. 脉冲收缩型 TDC

1.2.1 基于模拟的TDC

- 基于模拟的TDC使用间接测量的方式
- 主要思想：TAC+ADC
- 时间分辨率主要由ADC决定







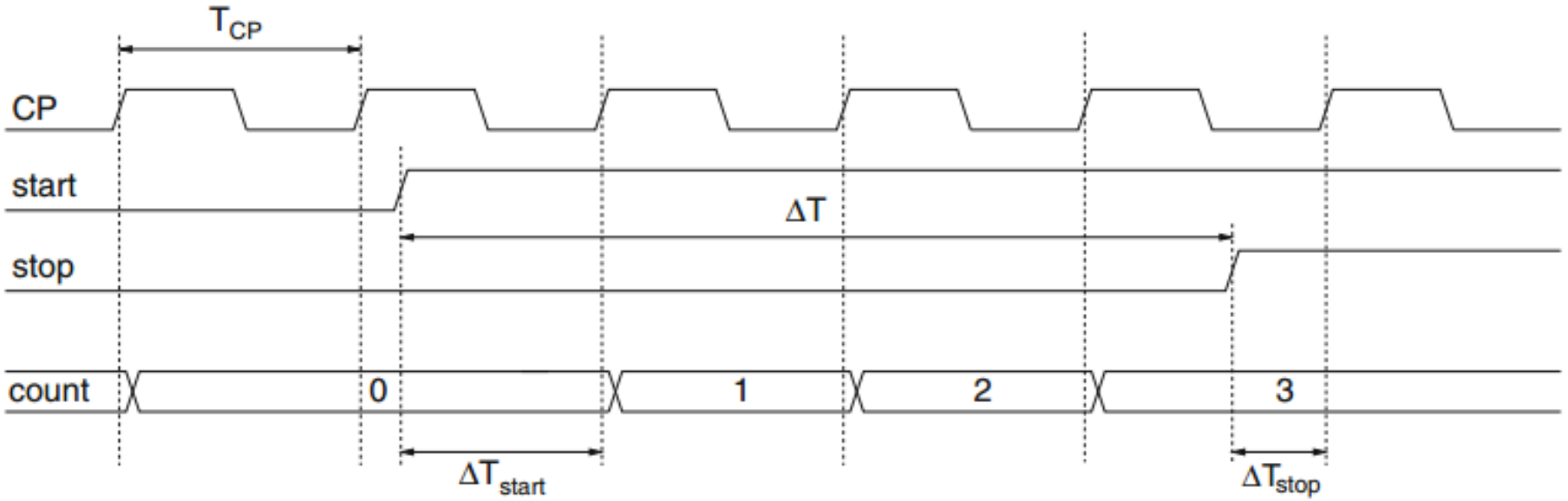
1.2.2 基于计数器的TDC

- 主要思想：对时钟进行计数；

$$\Delta T = N \cdot T_{CP} + (T_{CP} - \Delta T_{stop}) - (T_{CP} - \Delta T_{start}) = N \cdot T_{CP} + \epsilon_T$$

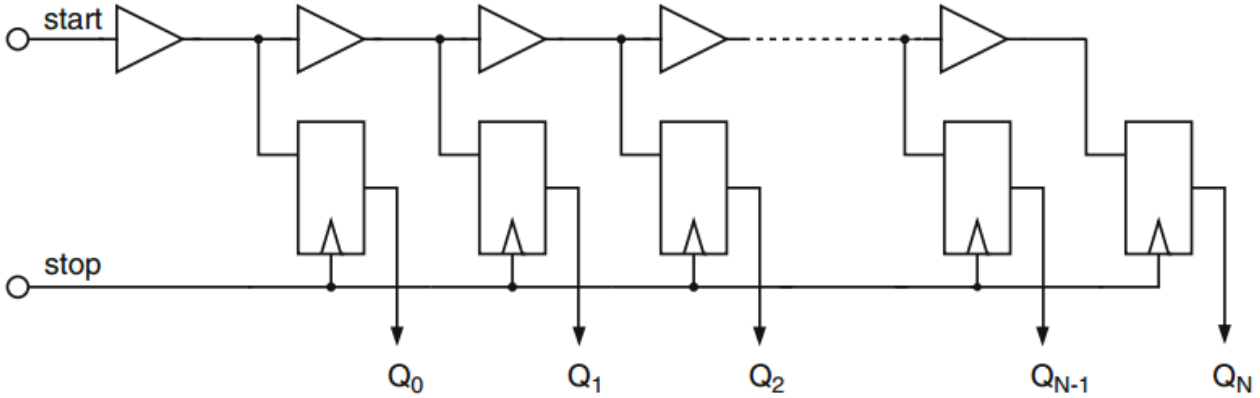
$$\epsilon_T = \Delta T_{start} - \Delta T_{stop} \in [-T_{CP}, T_{CP}]$$

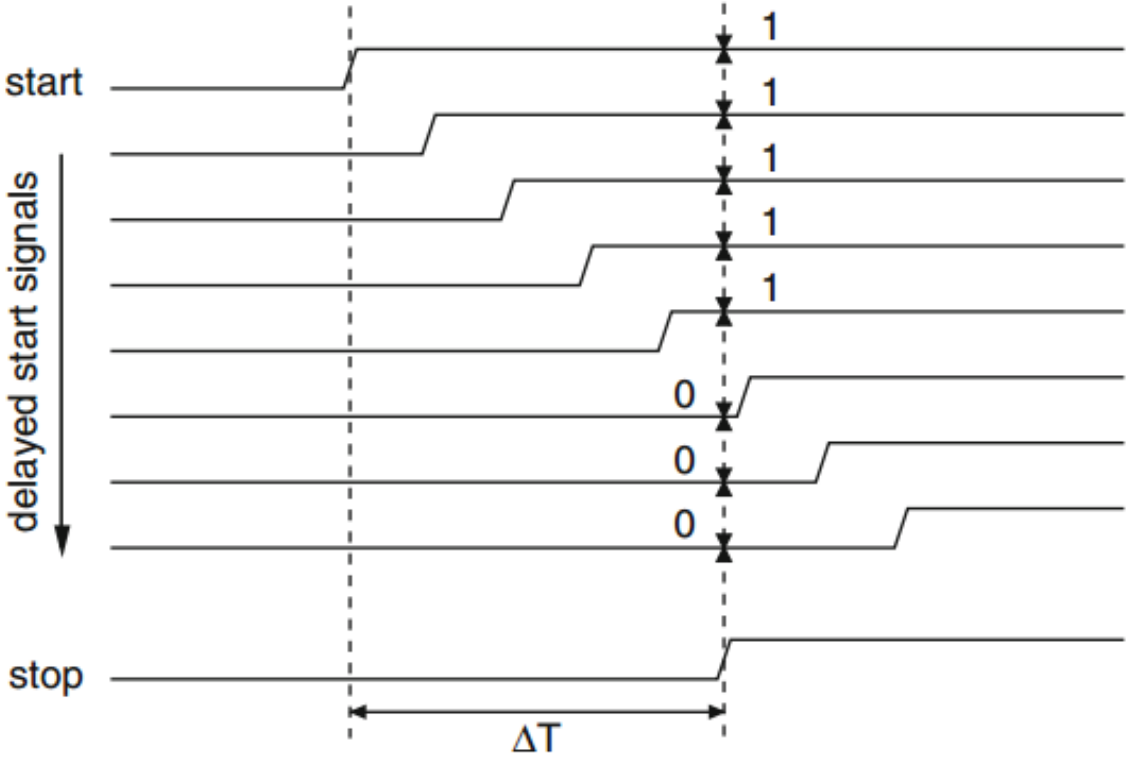
- 通过插值的方法可以实现百ps级时间分辨率



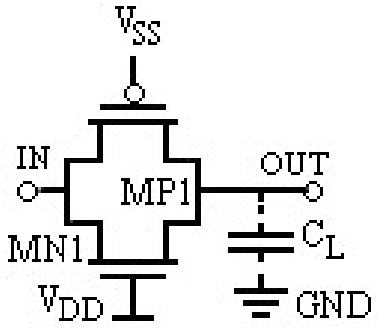
1.2.3 延迟线TDC

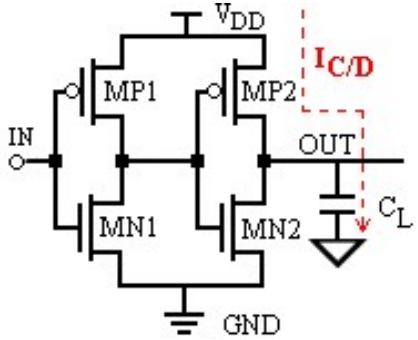
- 主要思想：起始信号被延迟，并每一次延迟后通过锁存器或寄存器进行采样，当停止信号到达时停止采样。延迟时间即为TDC的时间分辨率。
- 能够达到几十ps的时间分辨率。





- 延迟元件的选取：传输门、级联逆变器等。



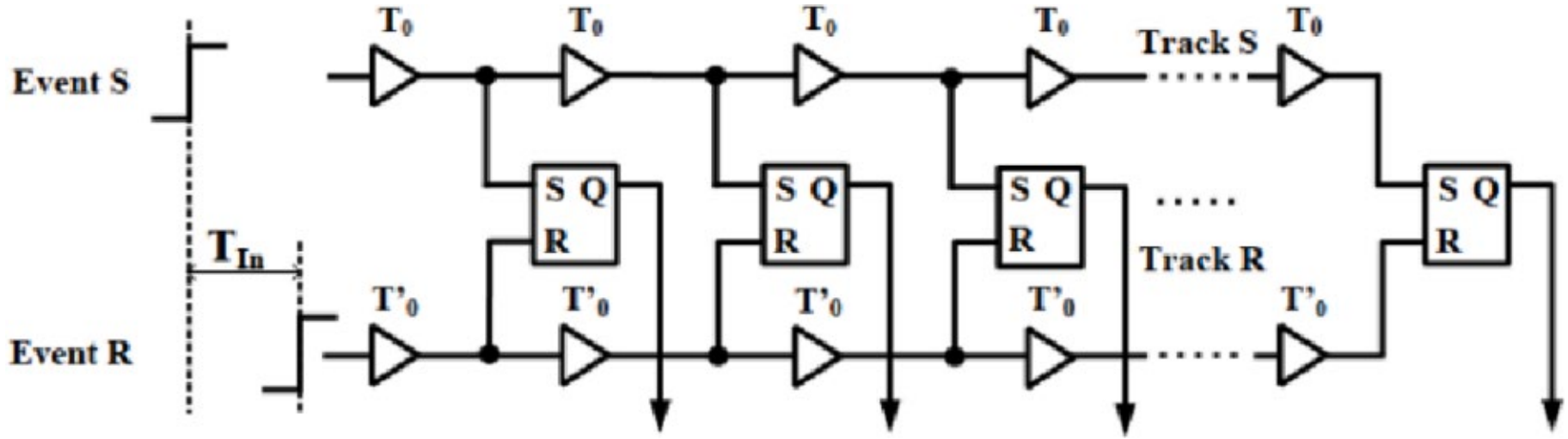


1.2.4 游标延迟线TDC

- 主要思想：使用两条延迟时间相差不大的延迟线分别对起始信号和延迟信号进行延迟，实现时间分辨率的提高。
- 时间分辨率为两延迟元件的延迟时间之差：

$$T_{LSB} = \Delta T = |T_0 - T_0'|$$

- 时间分辨率能够达到ps级。



1.3 各种TDC的优劣

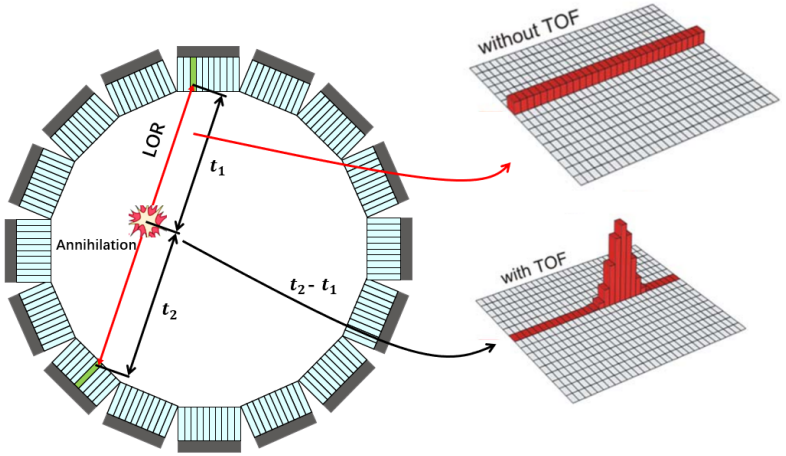
- 基于模拟的TDC可以通过时间放大提高对小时间间隔的测量精度，但时间放大会导致转换时间过长，且TDC的动态范围较小。
- 基于计数器的TDC结构简单易实现，但由于时钟周期的限制，分辨率难以提高。
- 延迟线TDC结构较为简单，且能够随着半导体工艺的提升提高时间分辨率（减小延迟单元延迟时间）。但受工艺的限制也是延迟线TDC的缺点之一。
- 游标延迟线TDC的时间分辨率能够做到比延迟线TDC更小，但是会增加转换时间，且动态范围较小，因此适合作为多级TDC的精测TDC。

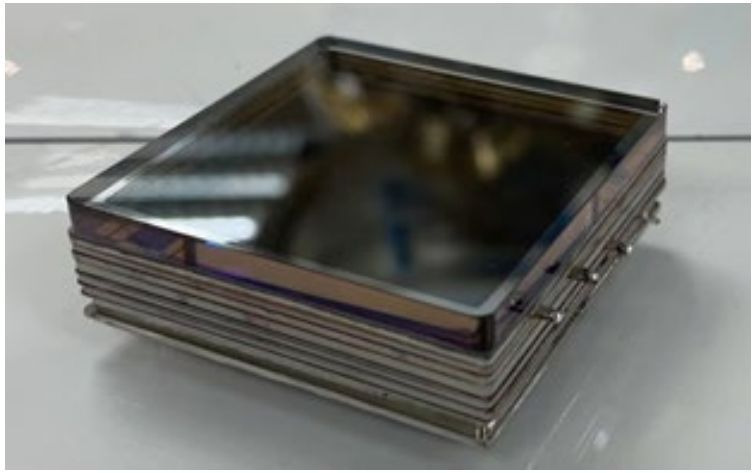
2.切伦科夫光成像TOF-PET高精度时间测量实现

Biograph Vision 600 （FWHM 230ps）

FPMT（Fast timing MCP-PMT）array is proposed for PET (Positron Emission Tomography) by detecting the Cerenkov light produced by gamma rays in the scintillator

Hoping coincident time resolution FWHM<100ps（FPMT TTS rms< 30ps，elec rms<10ps）

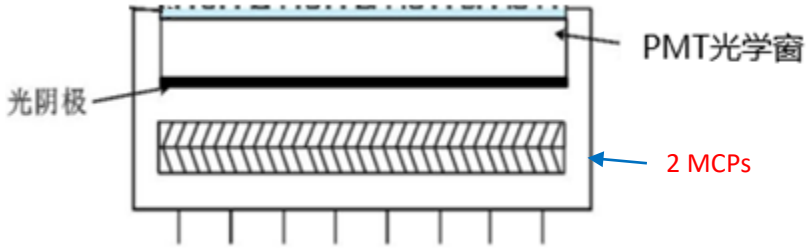




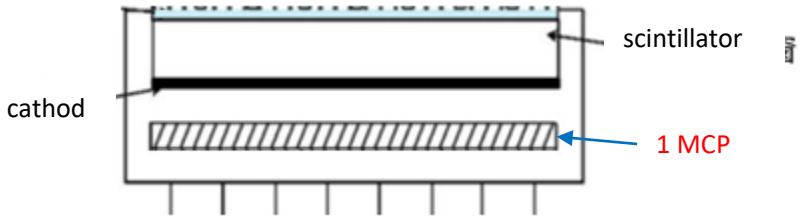
2.1 FPMT output characteristics

For FPMT with 2 MCPs：

- gain： ？ x10^6
- **leading： 0.2-0.5ns， mean： 300ps**
- **trailing： 0.3-0.7ns， mean： 500ps**
- **Pulse width@ middle： 0.6-0.8ns， mean： 0.7ns**
- Amplitude over 50 Ω： 30-90mV， mean： 60mV
- Cs for FPMT:4pF

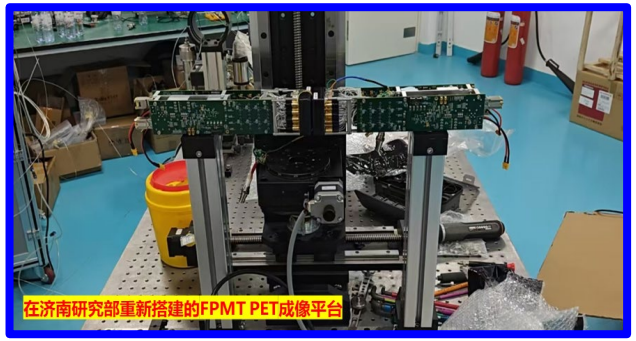


- **FPMT with Single MCP(in development)**
  - **Gain expected: <10^5**
  - **Faster leading edge**
  - **Smaller Cs**

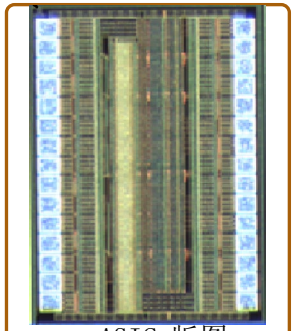


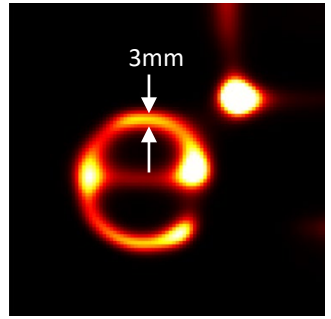
2.2 原型机方案验证

- 采用“甄别ASIC+ FPGA TDC”方案，完成128通道原理样机的可行性验证
  - 电子学系统**时间分辨σ<10ps, 整体系统分辨100ps（FWHM）**
    - 超快信号放大甄别ASIC研究，**前后沿<200ps**，时间分辨小于5ps
    - 通过FPGA实现高精度TDC，平均LSB<6ps
- 最终研究目标：FPMT电子学一体模块—iFPMT，整体系统分辨50ps




64通道FPMT PET电子学读出系统


ASIC 版图



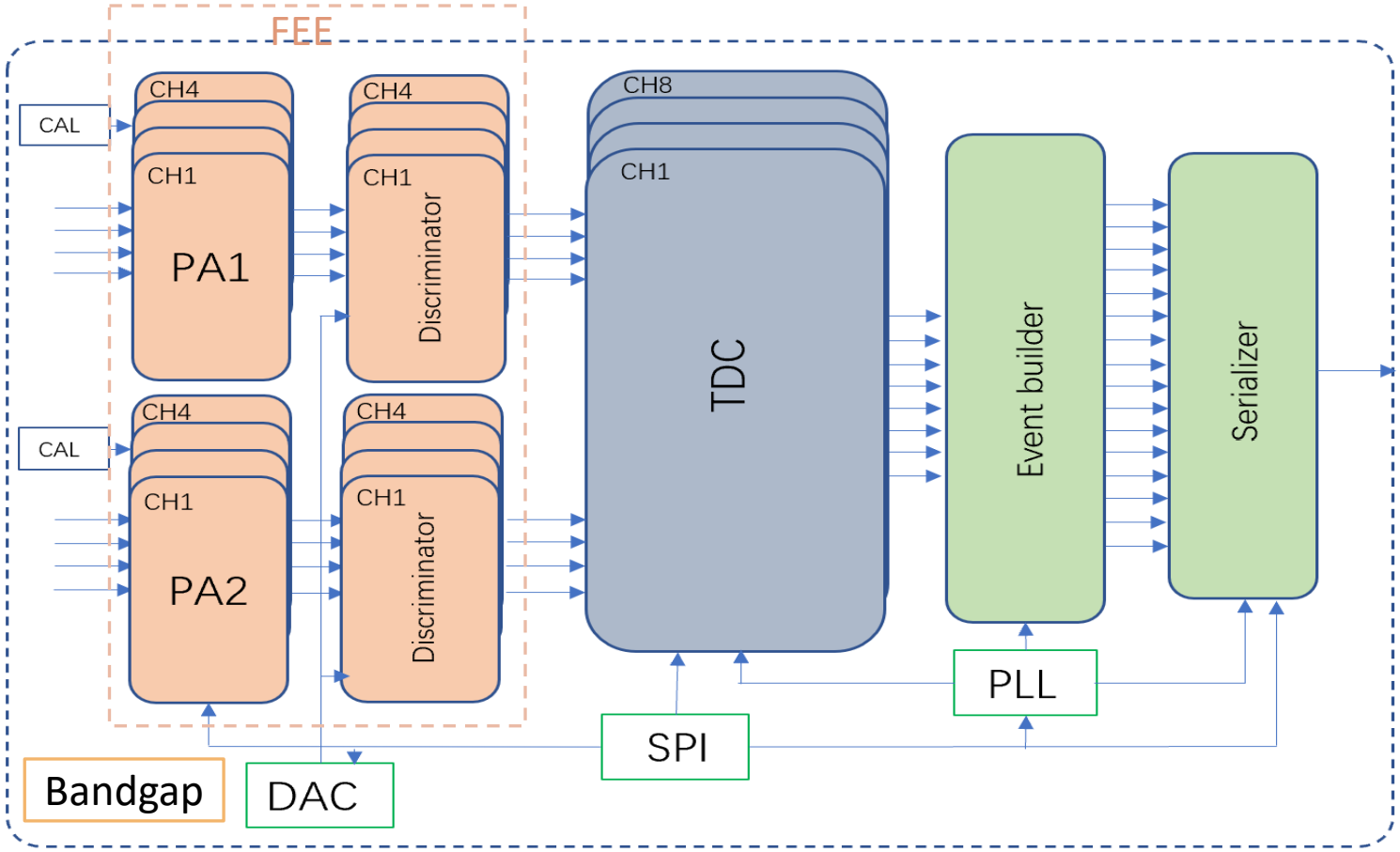
模体成像

* Biograph Vision 600 （FWHM 230ps）

Ref：Performance Characteristics of the Biograph Vision Quadra PET/CT System with a Long Axial Field of View Using the NEMA NU 2-2018 Standard，2022

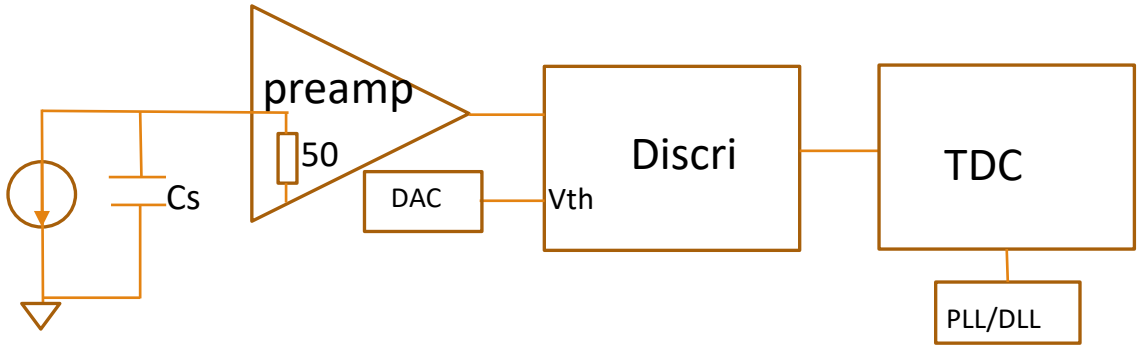
2.3 FPMROC架构

- Process： SMIC 55nm



- FEE： impedance matching, amplification, discrimination
- DAC: threshold and Q injection for test
- Bandgap: reference for DAC and preamp
- TDC： Time measurement， TOT for time walk correction
- PLL: clock for TDC and serializer
- Event builder： data coding, packing
- SPI： parameters configuration

Jitter distribution expected



➢ FEE：
--Dynamic range： 16fC-160fC
--Jitter： <6ps
--input impedance: ~50 Ω

➢ DAC
--DAC for Vth: Global +local,
10-12 bit, 0.5-1.0V, rms noise<50uV
--DAC for Q injection： 13bit, 0.1-0.6V,

➢ PLL,DLL:
--Frequency： 5.12GHz
--RMS jitter<1ps

➢TDC： precision<8ps

--TOA resolution（LSB）： 10 ps

--TOA precision： <8ps

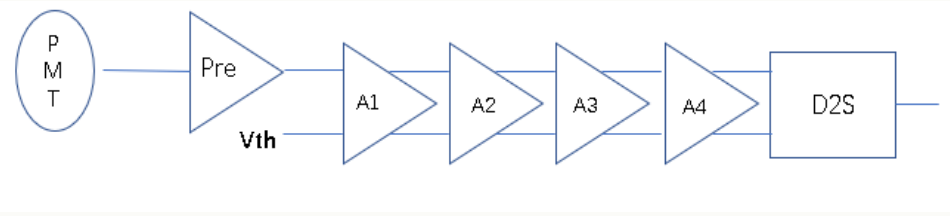
--Dead time： 25ns

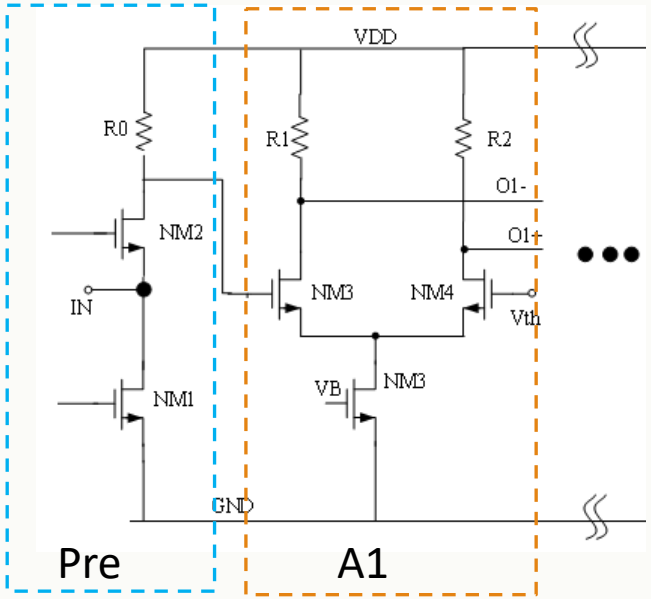
Spec

Parameter	Value
Process	SMIC 55 nm
TOA resolution	< 10 ps (LSB)
TOA range	0.5 ns~24.5 ns
TOT resolution	< 10 ps
TOT range	0.3~2 ns
TOA INL/DNL	< 1 LSB
TOT INL/DNL	< 1 LSB
Dead time	25 ns
TOA/TOT precision	<8 ps
Power consumption	30 mW/ch
Output data width	32-bit

FEE scheme

Scheme 1

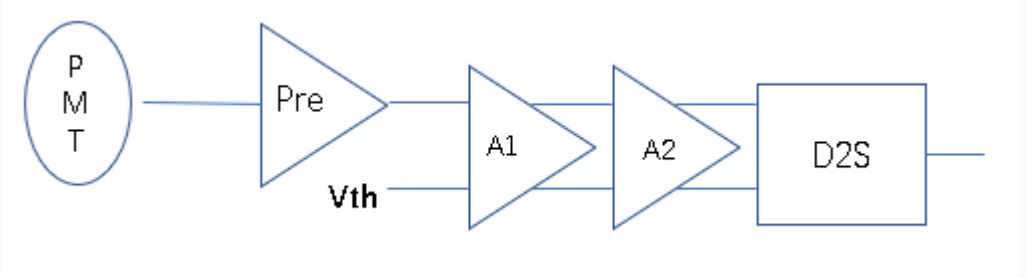




-higher BW

-flat 50Ω

Scheme 2



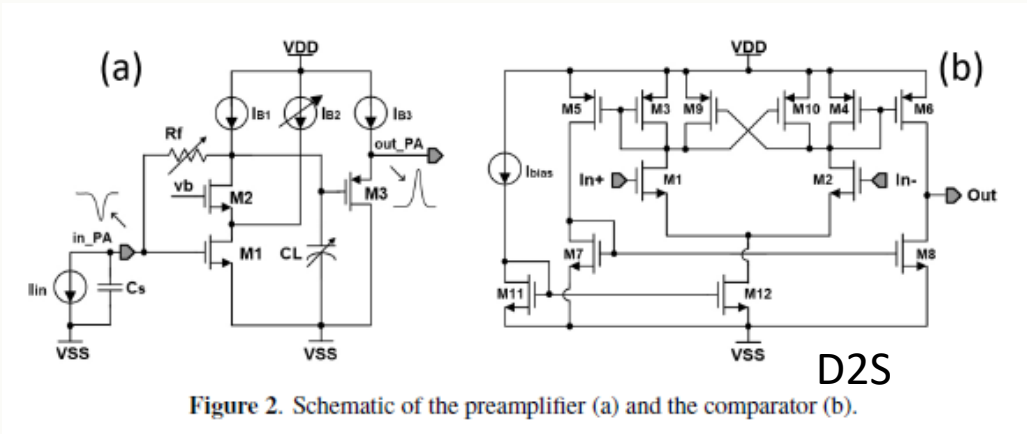
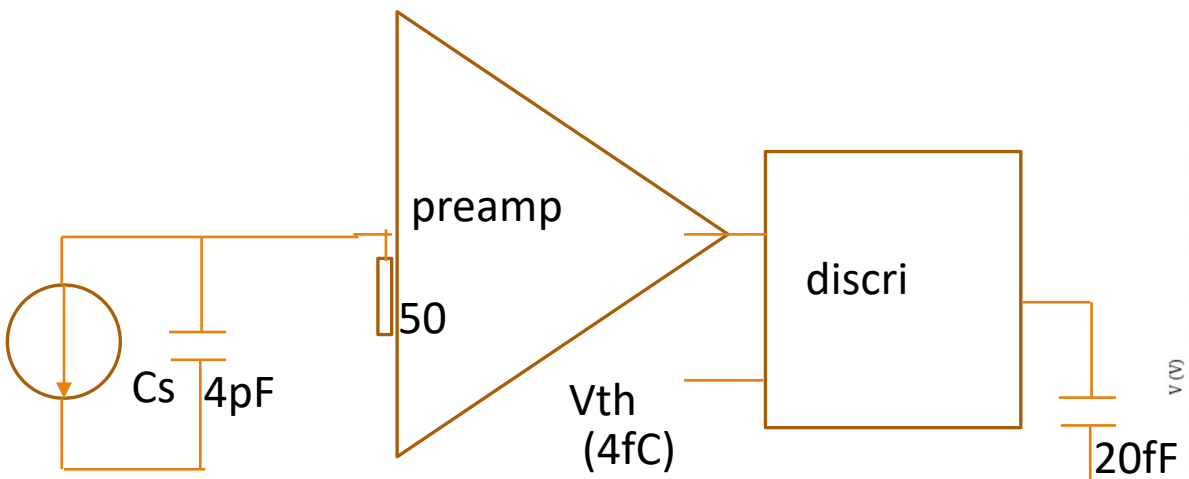
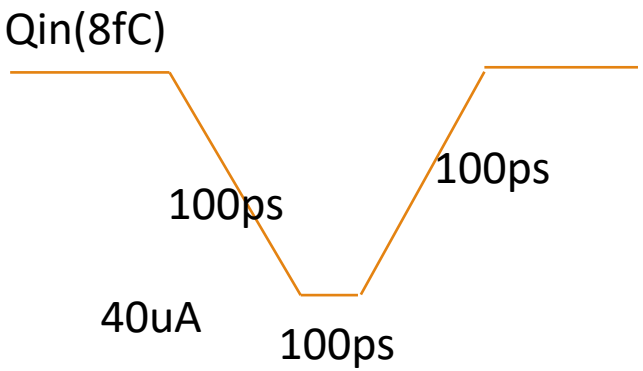


Figure 2. Schematic of the preamplifier (a) and the comparator (b).

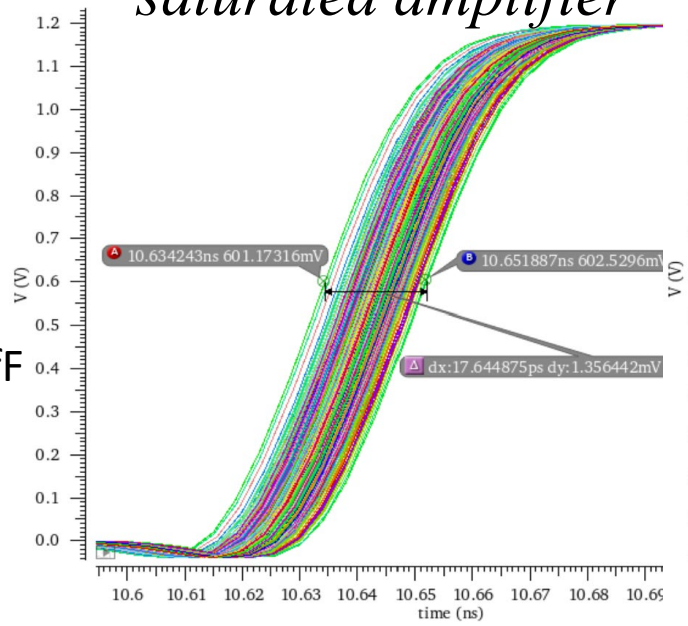
-higher gain

Trans noise simulation for FEE

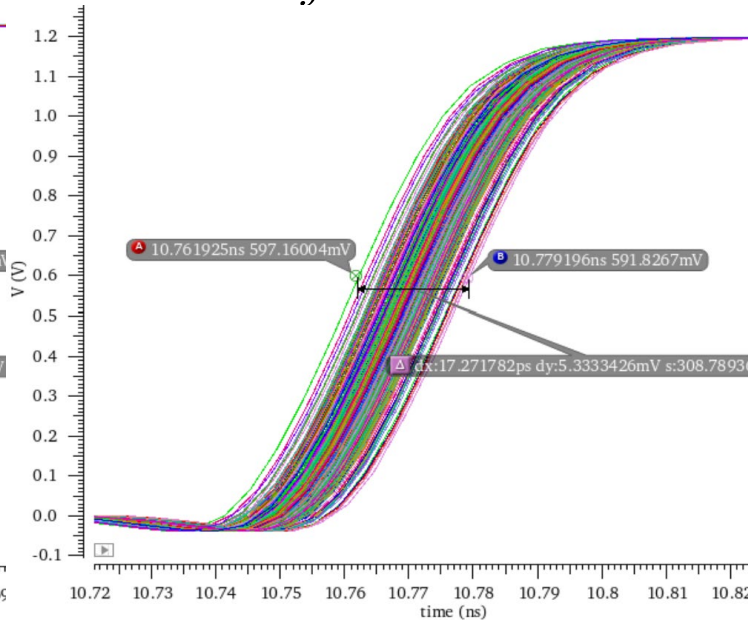




noise simulation for saturated amplifier



noise simulation for TIA

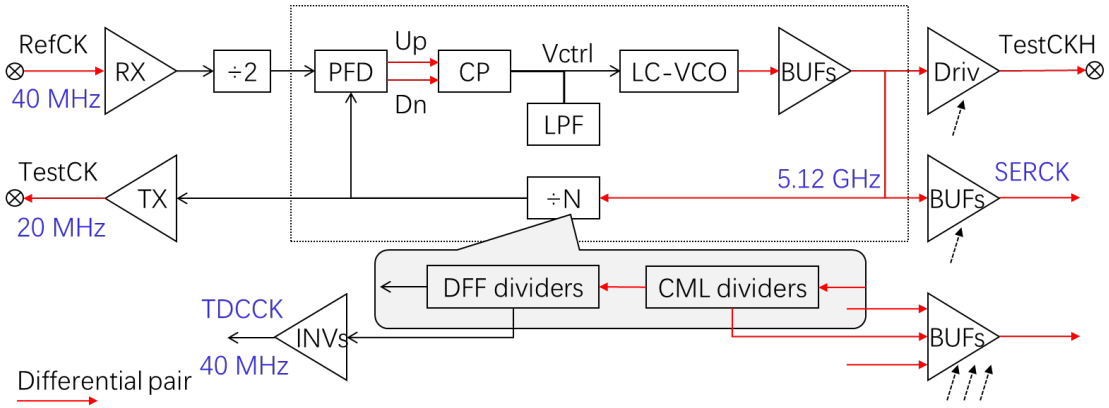


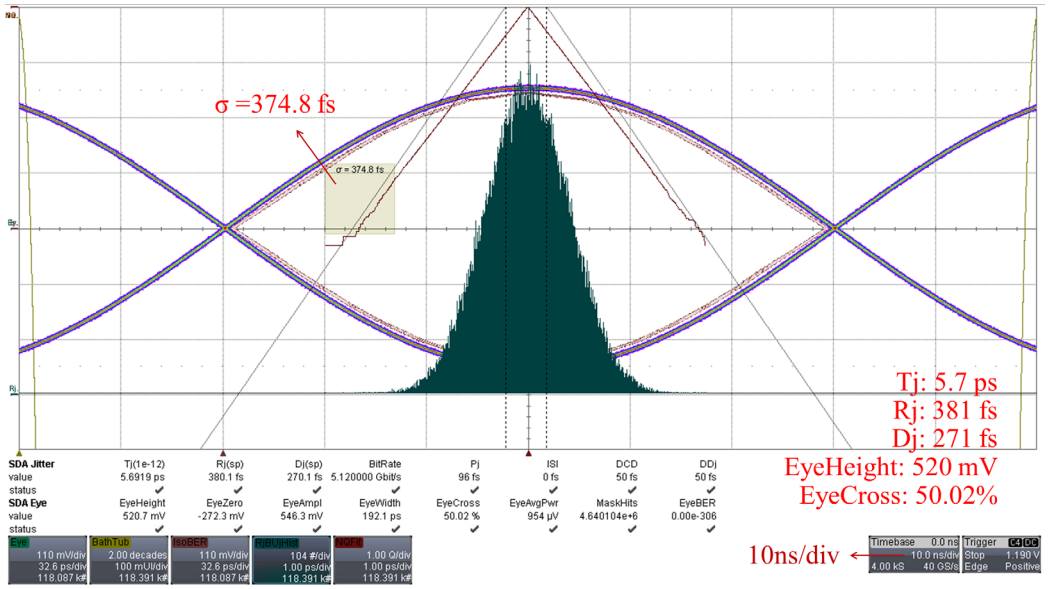
➢*400 runs of transient noise are simulated for both front end schemes. The total jitter of discriminators of both scheme are less than 18 ps. For the preamplifier of first scheme, the RMS noise is 158 uV with a slope of 67V/us, while the RMS noise is 508 uV with a slope of 145V/us for the other one.*

PLL

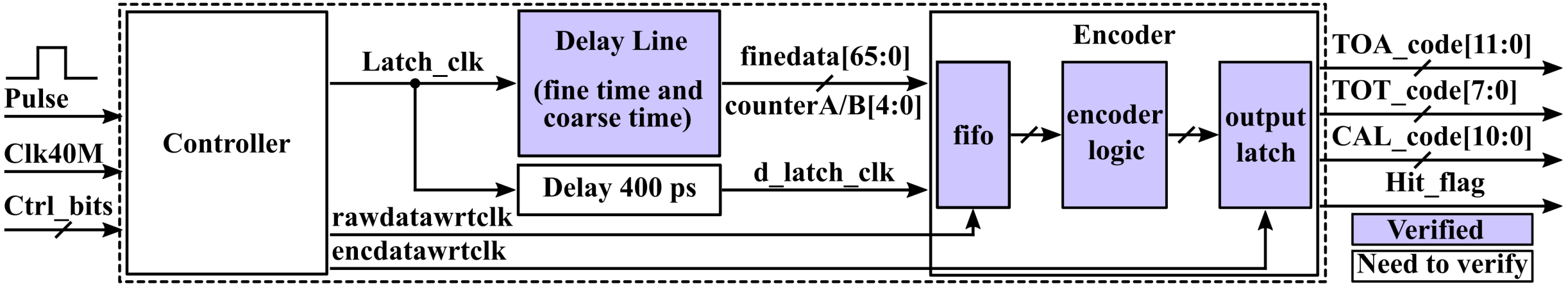
PLL performance

- *The PLL core has previously undergone submission, with a measured frequency range of 4.74~5.92 GHz, and RMS jitter of less than 460 fs. More details can be found in the paper: https://doi.org/10.1007/s41365-022-01074-2.*



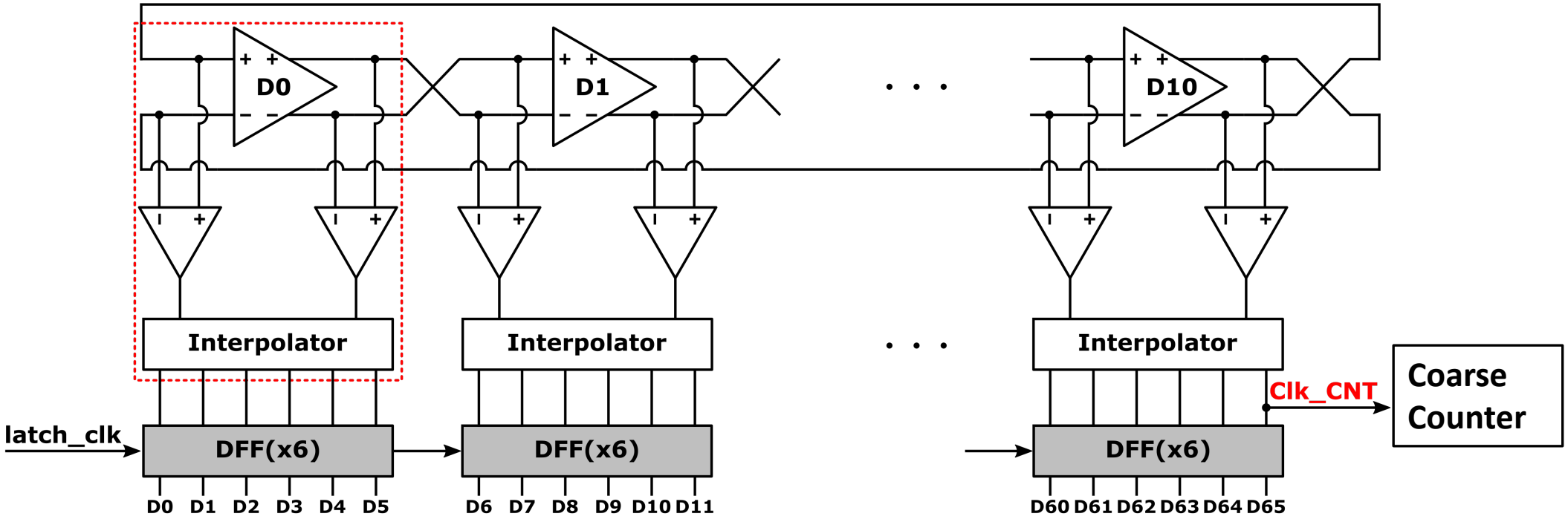


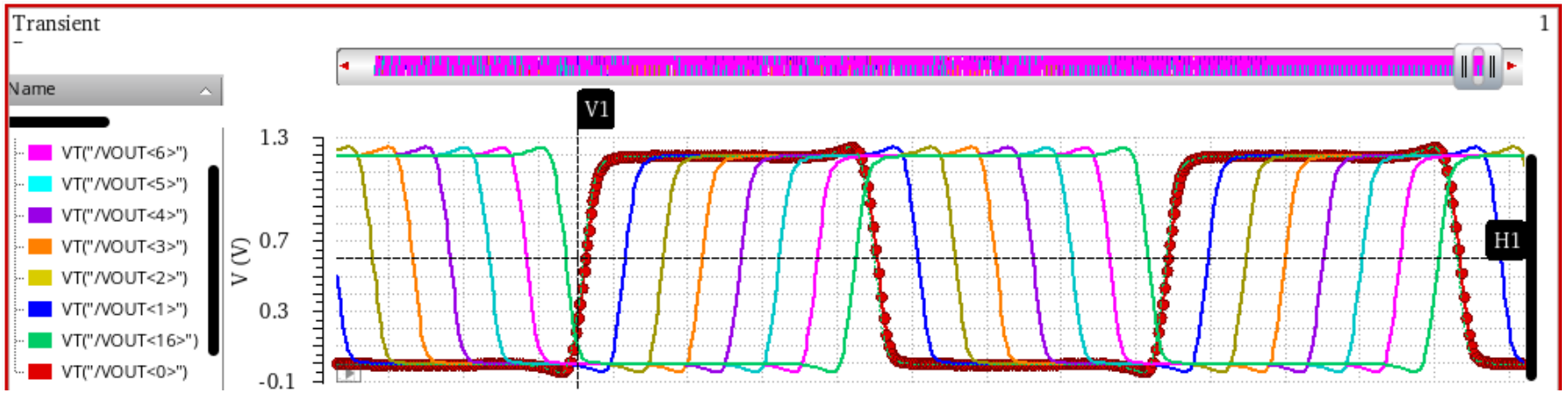
TDC Core Structure



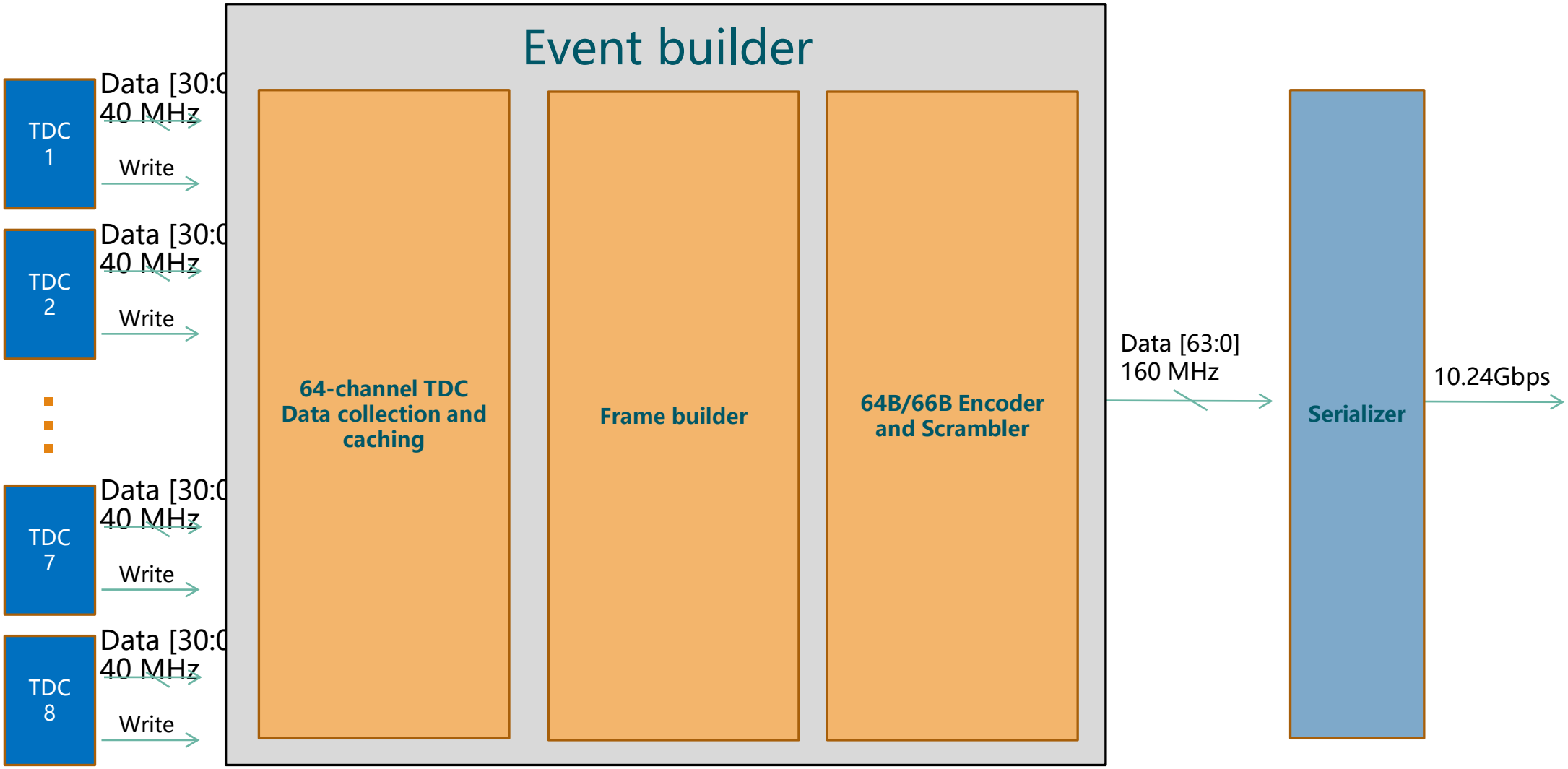
- The FPMROC TDC consists of Controller, Delay Line and Encoder. The Delay Line and encoder logic have already verified.
- The Controller receives Pulse that comes from the discriminator and 40 MHz clock (CLK40M) then generates latch clock to drive the Delay Line and the Encoder.
- The Delay Line is made up of fine time part and coarse time part. The fine time part is composed by 11 differential delay cells and the coarse time part consists of two ripple counters.
- The Encoder converts the Delay Line raw data (fine time and coarse time) into binary code.

Block diagram of the Delay Line





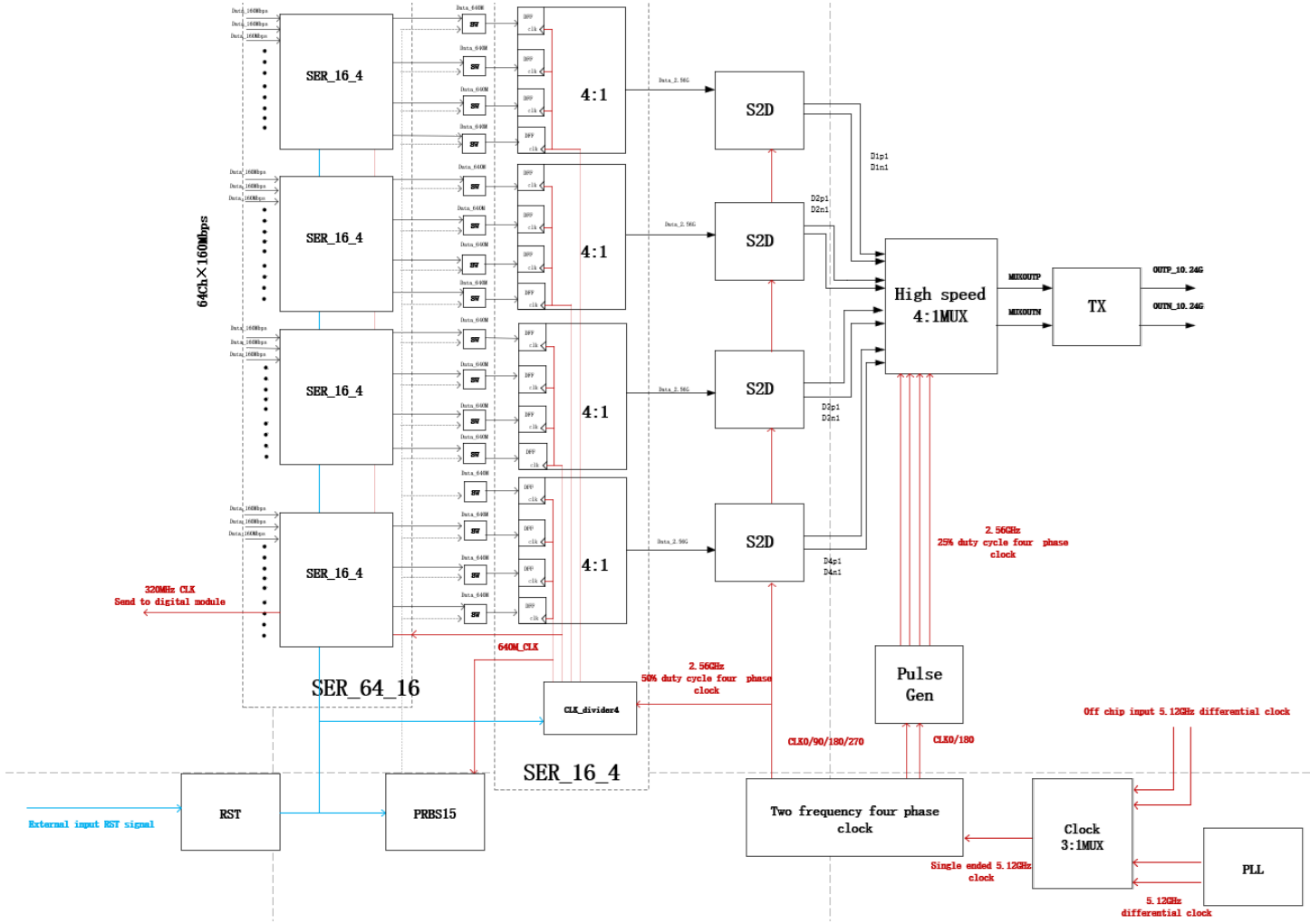
Event builder



Serializer

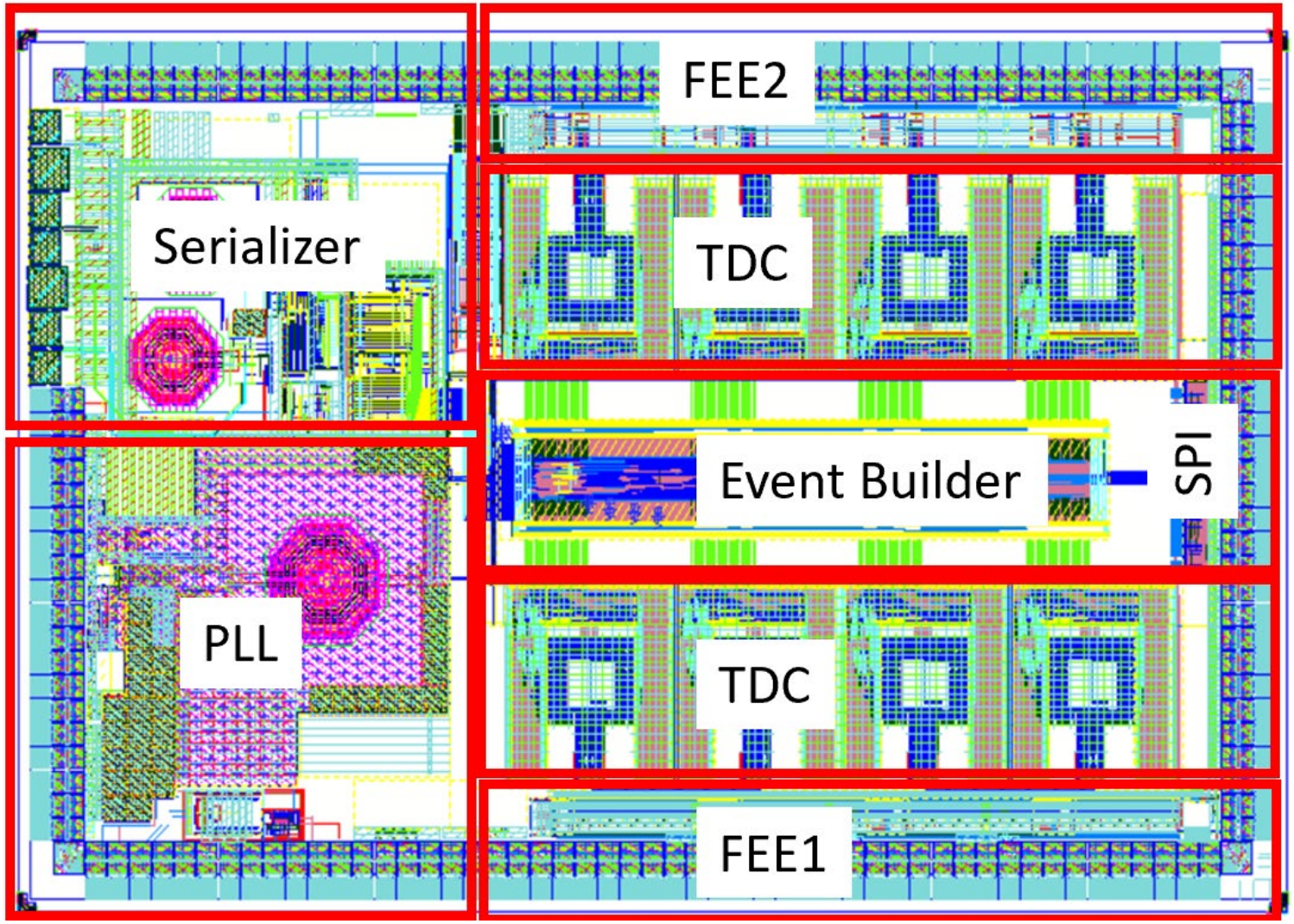
设计及参数

- 64: 1 最高串行速率10.24 Gbps 并串转换模块 Serializer
- 低速64:16 （2.56 Gbps）采用CMOS逻辑门电路
- 高速4:1 （10.24 Gbps）采用差分CML逻辑门电路



64:1 10 Gbps Serializer模块框图

Layout



针对OTK需要做的优化：

- TDC 核心的实现方式：事例驱动型
- 单通道电路的尺寸和布局