Radiation-Hardened Electronics Designs for a CMOS Image Sensor

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Introduction

CMOS Image Sensors(CIS) are extensively utilized in cameras, microphones, and monitoring systems. However, in nuclear applications such as space exploration, reactor monitoring, and High Energy Physics (HEP) experiments, images can deteriorate due to radiation effects. One of the most significant effects is the Total Ionizing Dose(TID). It occurs when energy is deposited in SiO_2, leading to the accumulation of positive charges and the creation of interface states, which can severely impact both photodiodes and circuits. Under irradiation, a rapid increase in dark current can diminish light signals. Additionally, threshold voltage shifts and increased power consumption are common issues in integrated circuits. Radiation-Hardened By Design(RHBD) techniques can be employed to mitigate the TID effects. Intuitively, keeping photodiodes away from SiO_2 is advantageous. Enclosed Layout Transistors (ELT) have proven to be beneficial for radiation-hardened designs. Based on the principles, two generations of chips have been fabricated. In the tests, the basic functionality of the photodiode was achieved with a TID of 100 Mrad(SiO_2). Up to 10 Mrad(SiO_2), no significant performance degradation was observed in the radiation-hardened analog-to-digital converter(ADC) design.

1st Generation Design

This chip enables the separate study of the basic functionality and the Total Ionizing Dose (TID) effects on several different photodiodes and analog-to-digital converters.

- **Photodiodes**
  - 8 different designs
  - 64x64 pixels per array
  - Enclosed Layout Transistor
  - Radiation-hardened digital cells
- **RHBD Methods**
  - Isolate lateral field oxide
  - Reduce trap density of upper oxide

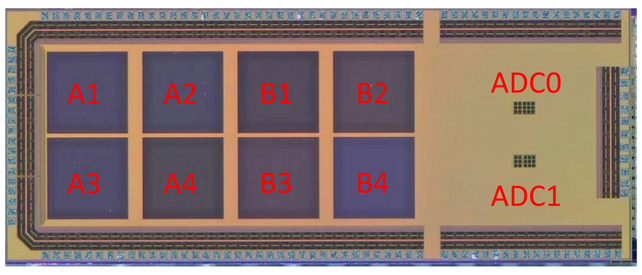

Figure 1. The microphotograph of CHIP Gen1.

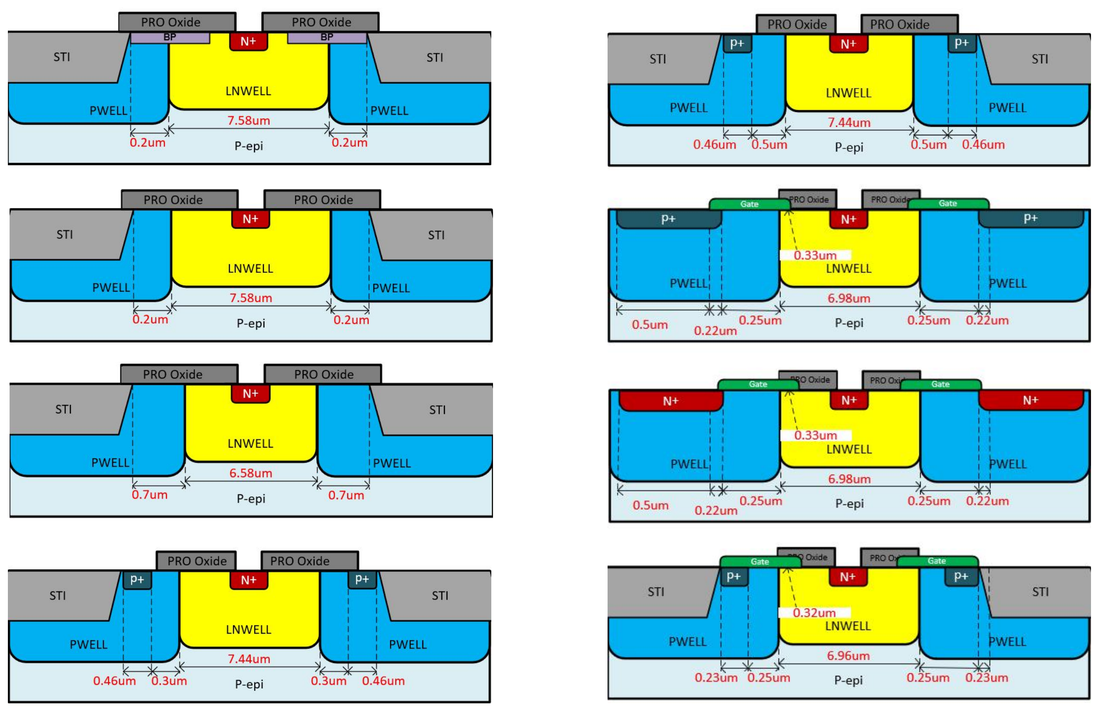

Figure 2. Cross section views of 8 studied photodiode layouts. (a) Photodiode designs of A1-A4. (b) Photodiode designs of B1-B4.

- **Ramp ADC**
  - 0 - 1.8V input range
  - Standard/RH-ADC in comparison
  - two working phase — Charge/Reset
- **RHBD Methods**
  - Annular Gate Layout Transistor
  - Externally controlled ramp

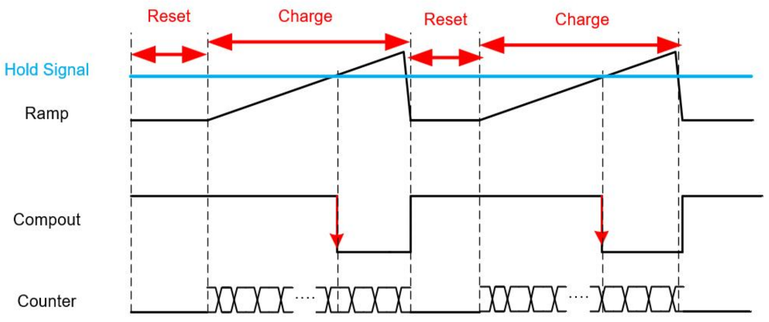

Figure 3. The principle of A/D conversion

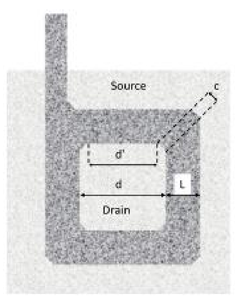

Figure 4. Enclosed layout transistor

2nd Generation Design

The second design was fabricated into a fully functional chip, integrating pixel photodiodes and a column-level readout chain. As a crucial component of signal conversion, the column ADCs have been meticulously optimized to achieve high ramp linearity, thereby enhancing conversion performance. Additionally, four different transistor layouts were employed to explore the limits of radiation hardness.

- **Column level ADC**
  - 64 columns in total
  - 4 different radiation-hardened designs
  - High ramp linearity
  - 0 - 0.8V input range
- **RHBD Methods**
  - Radiation-hardened layouts
  - Careful layout placement

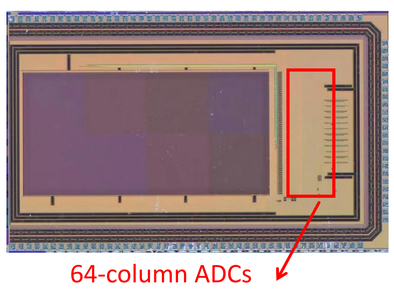

Figure 5. The microphotograph of CHIP Gen2.

It is currently under test！

Chips Display

Please closely observe the chips!

Test Results

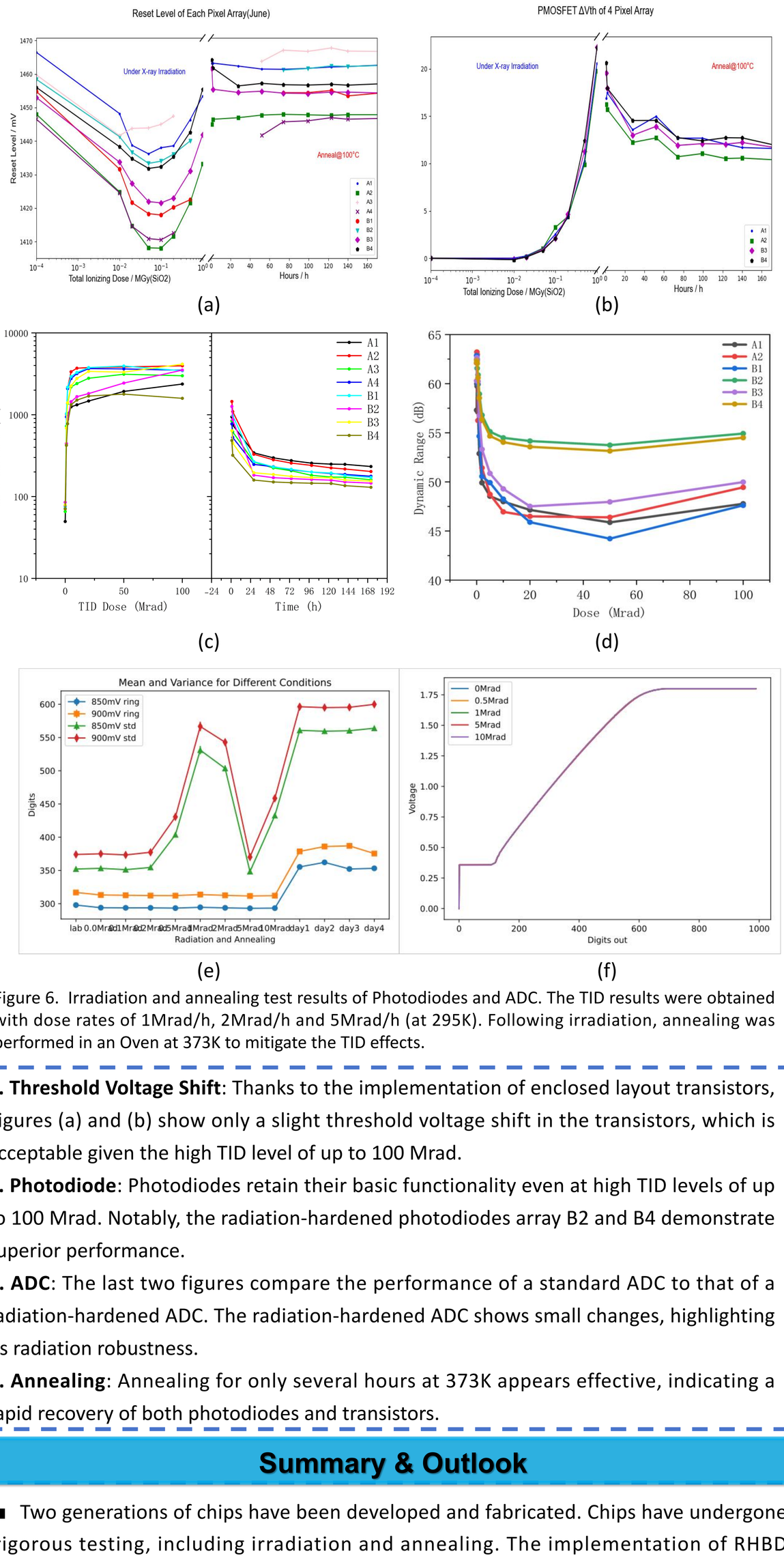

Figure 6. Irradiation and annealing test results of Photodiodes and ADC. The TID results were obtained with dose rates of 1Mrad/h, 2Mrad/h and 5Mrad/h (at 295K). Following irradiation, annealing was performed in an Oven at 373K to mitigate the TID effects.

1. Threshold Voltage Shift: Thanks to the implementation of enclosed layout transistors, Figures (a) and (b) show only a slight threshold voltage shift in the transistors, which is acceptable given the high TID level of up to 100 Mrad.

2. Photodiode: Photodiodes retain their basic functionality even at high TID levels of up to 100 Mrad. Notably, the radiation-hardened photodiodes array B2 and B4 demonstrate superior performance.

3. ADC: The last two figures compare the performance of a standard ADC to that of a radiation-hardened ADC. The radiation-hardened ADC shows small changes, highlighting its radiation robustness.

4. Annealing: Annealing for only several hours at 373K appears effective, indicating a rapid recovery of both photodiodes and transistors.

Summary & Outlook

■ Two generations of chips have been developed and fabricated. Chips have undergone rigorous testing, including irradiation and annealing. The implementation of RHBD techniques has contributed to the radiation robustness and reliability of these chips.

■ Based on the designs and test results, a new generation design will be submitted in February 2025. We are continuing to refine and optimize the radiation hardended designs, with the goal of deploying them in practical applications.