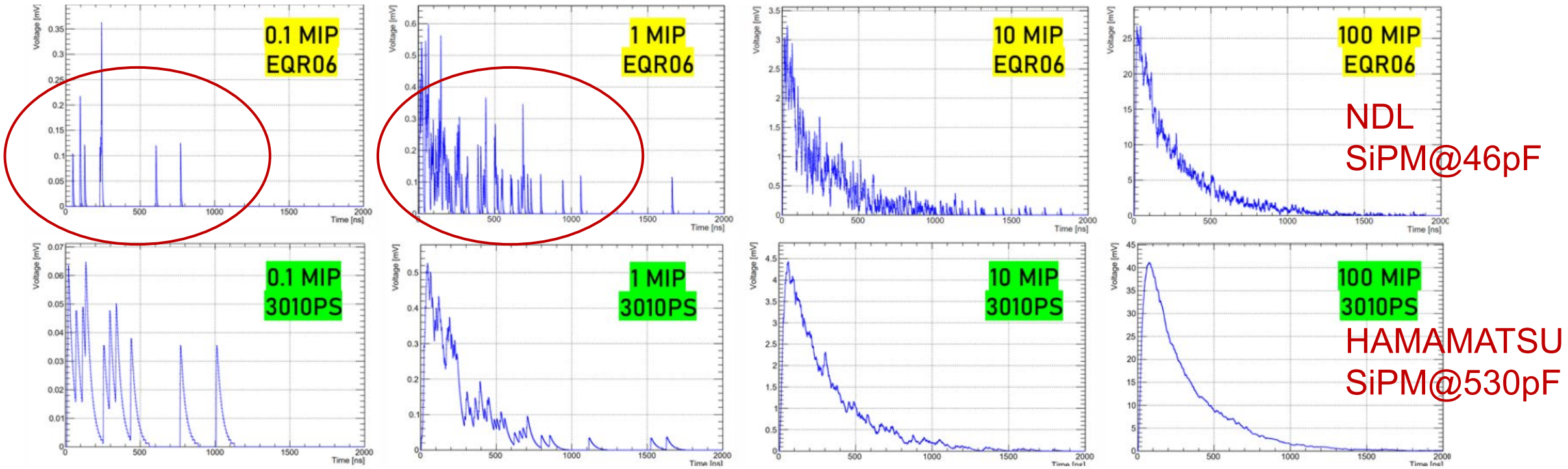
Discussion on ChoMin ASIC design for ECAL/HCAL/Muon



- **A simulation waveform provided for both NDL & Hamamatsu SiPM**
- **NDL signals disperse into multiple single photons due to the small capacitance & long response time of BGO for ECAL**
  - **Big impact on amplitude threshold, esp for dispersing small signals**
  - **Difficulties for picking up signals from background event by conventional charge integration**
  - **Large jitter on small signal timing**

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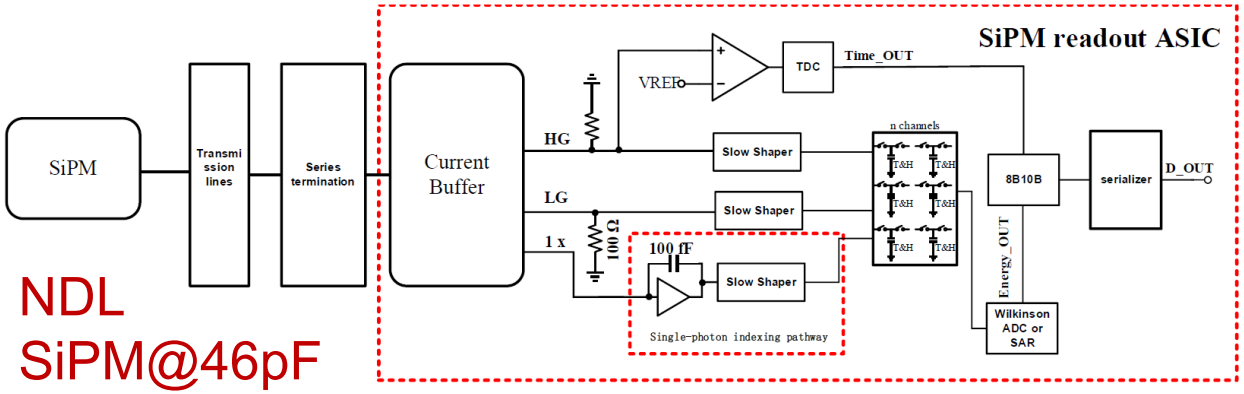
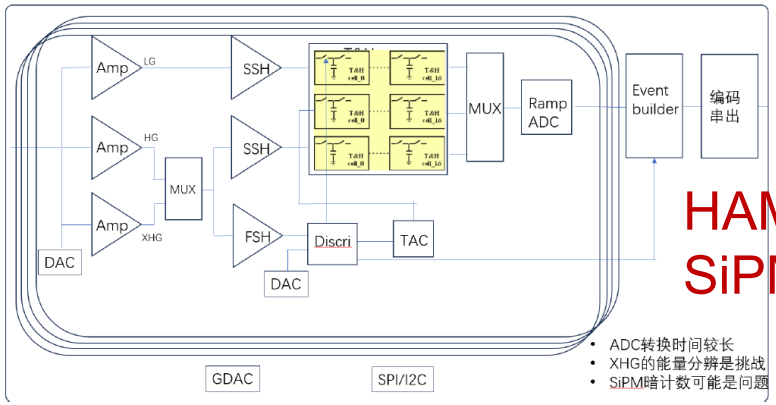


NDL
SiPM@46pF



HAMAMATSU
SiPM@530pF

By Huaishen LI,
Xiongbo YAN et al.

- **Discussions in the past weeks with our colleagues**
- **Dedicated ASIC schemes designed for each case (NDL vs Hamamatsu)**
- **Came to a first common view:**
  - **NDL SiPM has to be the final choice for CEPC, due to the cost limit**
  - **Small signal dispersion may be the real case**
- **Further things to do**
  - **To get the real waveform of NDL**
  - **Add background signals together with small event for a global view**
  - **Define the ASIC specification excluding the unknown factors of NDL SiPM, esp timing & threshold**

Key ASICs design initiated

- The first tapeout in April for several ASICs
  - Data Link chip set
    - ChiTu:
      - Main protocol defined: focusing on FEC12, omit FEC5 in lpGBT
      - Fixed on “10.24Gbps” output rate, omit “5.12Gbps” in lpGBT
      - Key blocks design tasks allocated to the charge person/team
    - TaoTie, KinWoo: specification defined
  - Basha module
    - More rad-test on commercial LDO & DC-DC, some can even survive at CEPC’s rad-level
    - DC-DC controller to be tapeout in April
    - Will have a discussion on module design team soon
  - ChoMin
    - To be tapeout in April
- Scheduled to have a collective review in Feb 10~14, mainly on overall scheme