

CEPC Silicon Tracker Progress Report (17)

Qi Yan on behalf of the Silicon Tracker Group

Jan 6, 2025, IHEP

Progress on Silicon Tracker Ref-TDR

The Silicon Tracker group is dedicated to finalizing the drafting of the Silicon Tracker chapter of the Ref-TDR as soon as possible:

- ~90% of the content has been completed, with the full chapter nearing 100 pages.
The following topics will continue to be added:
 - Overview of ITK and OTK
 - Mechanical and thermal analysis of the endcap
- Our group has undergone two rounds of weekly global internal reading, discussion, and revision of the Silicon Tracker Ref-TDR. We will continue this paper reading until the chapter reaches certain quality level.
- I am full-time working on drafting and systematically revising of the entire chapter of the Silicon Tracker Ref-TDR during the last few months.

Main Contributors and Sections of Silicon Tracker Ref-TRD

(Blue indicated the parts after my pre-revision)

Chapter 5 Silicon Trackers		1
5.1	Requirements	1
5.1.1	Physics requirements	1
5.1.2	Specific requirements on Silicon Tracker	2
5.2	Overview of ITK and OTK	3
5.2.1	Technology Options and Boundary Conditions	3
5.2.2	Optimization Tools	4
5.2.3	Layout Optimization	4
5.2.3.1	The tracker length	4
5.2.3.2	Barrel Region	4
5.2.3.3	End-cap Region	4
5.2.4	Summary and discussion on tracker system layout	5
5.3	Inner silicon tracker (ITK)	5
5.3.1	CMOS chip R&D	6
5.3.1.1	HV-CMOS pixel R&D	6
5.3.1.1.1	Technology survey for silicon pixel detectors	6
5.3.1.1.2	Development of HVCMOS pixel sensor for CEPC	6
5.3.1.1.3	COFFEE1	7
5.3.1.1.4	COFFEE2	9
5.3.1.2	CMOS strip R&D	13
5.3.2	ITK design	20
5.3.2.1	ITK barrel design	20
5.3.2.2	ITK endcap design	21
5.3.2.3	Alternative design for the ITK	25
5.3.3	Readout electronics	30
5.3.4	Mechanical and cooling design	31
5.3.4.1	Barrel local support	31
5.3.4.1.1	Materials	31
5.3.4.1.2	Structural characterisation	32
5.3.4.1.3	Thermal characterisation	33
5.3.4.2	Endcap local support for CMOS strip detector	34
5.3.4.2.1	Materials	35
5.3.4.2.2	Structural characterisation	35
5.3.4.2.3	Thermal characterisation	35
5.3.5	Prospects and plan	37
5.3.5.1	Development of the CMOS pixel sensor	37
5.3.5.2	Development of the CMOS strip sensor	38
5.3.5.3	Module and system level development	39
5.4	Outer silicon tracker (OTK) with TOF	40
5.4.1	AC-LGAD sensor and ASIC R&D	40
5.4.1.1	AC-LGAD Sensor R&D	40
5.4.1.1.1	AC-LGAD simulation	41
5.4.1.1.2	Testing setup	42
5.4.1.1.3	Pixelated AC-LGAD prototypes	44
5.4.1.1.4	Strip AC-LGAD prototype and properties	46
5.4.1.2	AC-LGAD ASIC R&D	51
5.4.1.2.1	General requirements	51
5.4.1.2.2	Data transmission bandwidth requirements	51
5.4.1.2.3	ASIC architecture	52
5.4.1.2.4	Single-channel readout electronics	52
5.4.1.2.5	Prototype	56
5.4.1.2.6	Power distribution and grounding	59
5.4.1.2.7	Radiation tolerance	59
5.4.1.2.8	Monitoring	60
5.4.1.2.9	Development plan and schedule	60
5.4.2	OTK design	61
5.4.2.1	OTK barrel design	61
5.4.2.2	OTK endcap design	63
5.4.3	Readout electronics	68
5.4.3.1	Front-end board	68
5.4.3.2	Concentrator card and power distribution	68
5.4.3.3	Slow control and monitoring	69
5.4.3.4	Clock distribution	69
5.4.4	Mechanical and cooling design	70
5.4.4.1	Barrel support	70
5.4.4.1.1	Materials	71
5.4.4.1.2	Structural characterisation	72
5.4.4.1.3	Thermal characterisation	73
5.4.4.2	Endcap support	74
5.4.4.2.1	Materials	76
5.4.4.2.2	Structural characterisation	76
5.4.4.2.3	Thermal characterisation	77
5.4.5	Prospects and plan	78
5.5	Beam background estimation	79
5.5.1	Beam background simulation	79
5.5.1.1	Pair production background	79
5.5.1.2	Single beam background	79
5.5.1.2.1	Beam Thermal Photon Scattering (BTH)	79
5.5.1.2.2	Beam Gas Coulomb Scattering (BGC) and Beam Gas Bremsstrahlung Scattering (BGB)	79
5.5.1.2.3	Touschek Scattering (TSC)	80
5.5.2	Hit rate estimation for beam background	80
5.5.3	ITK tolerable hit rate	80
5.5.4	OTK tolerable hit rate	81
5.6	Performance	83
5.6.1	The performance of the barrel region	83
5.6.1.0.1	Roles of gaseous and silicon trackers	83
5.6.2	The performance of forward tracking (end-cap)	84

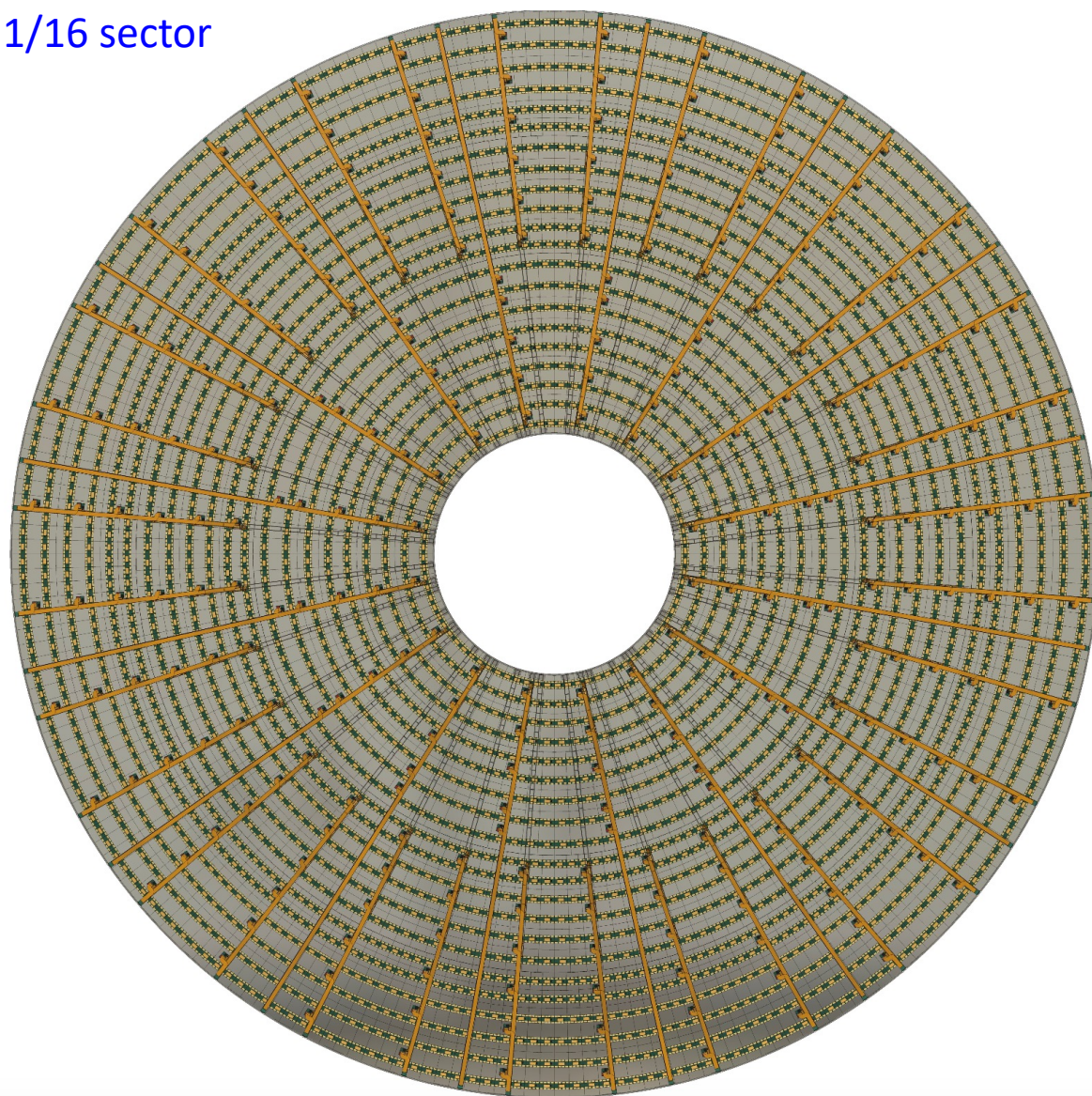
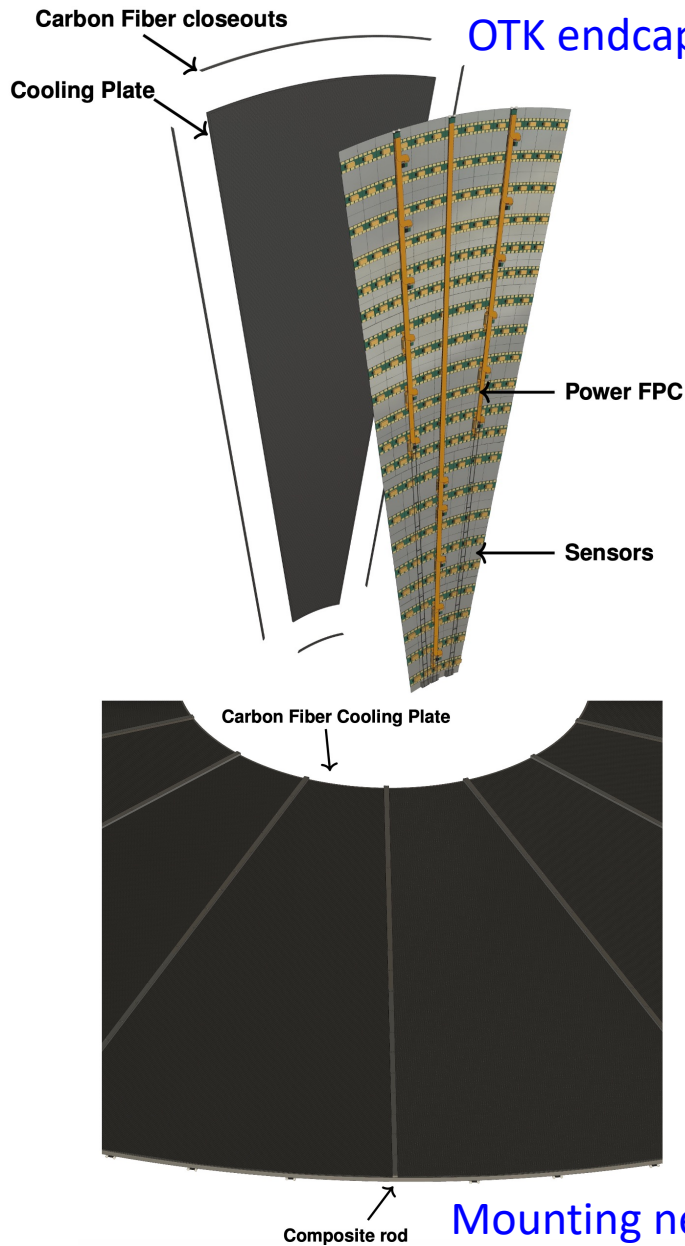
Main Contributors and Sections of Silicon Tracker Ref-TRD

(Blue indicated the parts after my pre-revision)

Chapter 5 Silicon Trackers		1
5.1	Requirements	1
5.1.1	Physics requirements	1
5.1.2	Specific requirements on Silicon Tracker	2
5.2	Overview of ITK and OTK	3
5.2.1	Technology Options and Boundary Conditions	3
5.2.2	Optimization Tools	4
5.2.3	Layout Optimization	4
5.2.3.1	The tracker length	4
5.2.3.2	Barrel Region	4
5.2.3.3	End-cap Region	4
5.2.4	Summary and discussion on tracker system layout	5
5.3	Inner silicon tracker (ITK)	5
5.3.1	CMOS chip R&D	6
5.3.1.1	HV-CMOS pixel R&D	6
5.3.1.1.1	Technology survey for silicon pixel detectors	6
5.3.1.1.2	Development of HVCMOS pixel sensor for CEPC	6
5.3.1.1.3	COFFEE1	7
5.3.1.1.4	COFFEE2	9
5.3.1.2	CMOS strip R&D	13
5.3.2	ITK design	20
5.3.2.1	ITK barrel design	20
5.3.2.2	ITK endcap design	20
5.3.2.3	Alternative design for the ITK	20
5.3.3	Readout electronics	30
5.3.4	Mechanical and cooling design	31
5.3.4.1	Barrel local support	31
5.3.4.1.1	Materials	31
5.3.4.1.2	Structural characterisation	32
5.3.4.1.3	Thermal characterisation	33
5.3.4.2	Endcap local support for CMOS strip detector	34
5.3.4.2.1	Materials	35
5.3.4.2.2	Structural characterisation	35
5.3.4.2.3	Thermal characterisation	35
5.3.5	Prospects and plan	37
5.3.5.1	Development of the CMOS pixel sensor	37
5.3.5.2	Development of the CMOS strip sensor	38
5.3.5.3	Module and system level development	39
5.4	Outer silicon tracker (OTK) with TOF	40
5.4.1	AC-LGAD sensor and ASIC R&D	40
5.4.1.1	AC-LGAD Sensor R&D	40
5.4.1.1.1	AC-LGAD simulation	41
5.4.1.1.2	Testing setup	42
5.4.1.1.3	Pixelated AC-LGAD prototypes	44
5.4.1.1.4	Strip AC-LGAD prototype and properties	46
5.4.1.2	AC-LGAD ASIC R&D	51
5.4.1.2.1	General requirements	51
5.4.1.2.2	Data transmission bandwidth requirements	51
5.4.1.2.3	ASIC architecture	52
5.4.1.2.4	Single-channel readout electronics	52
5.4.1.2.5	Prototype	56
5.4.1.2.6	Power distribution and grounding	59
5.4.1.2.7	Radiation tolerance	59
5.4.1.2.8	Monitoring	60
5.4.1.2.9	Development plan and schedule	60
5.4.2	OTK design	61
5.4.2.1	OTK barrel design	61
5.4.2.2	OTK endcap design	63
5.4.3	Readout electronics	68
5.4.3.1	Front-end board	68
5.4.3.2	Concentrator card and power distribution	68
5.4.3.3	Stop control and monitoring	69
5.4.3.4	Clock distribution	69
5.4.4	Mechanical and cooling design	70
5.4.4.1	Barrel support	70
5.4.4.1.1	Materials	71
5.4.4.1.2	Structural characterisation	72
5.4.4.1.3	Thermal characterisation	73
5.4.4.2	Endcap support	74
5.4.4.2.1	Materials	76
5.4.4.2.2	Structural characterisation	76
5.4.4.2.3	Thermal characterisation	77
5.4.5	Prospects and plan	78
5.5	Beam background estimation	79
5.5.1	Beam background simulation	79
5.5.1.1	Pair production background	79
5.5.1.2	Single beam background	79
5.5.1.2.1	Beam Thermal Photon Scattering (BTH)	79
5.5.1.2.2	Beam Gas Coulomb Scattering (BGC) and Beam Gas Bremsstrahlung Scattering (BGB)	79
5.5.1.2.3	Touschek Scattering (TSC)	80
5.5.2	Hit rate estimation for beam background	80
5.5.3	ITK tolerable hit rate	80
5.5.4	OTK tolerable hit rate	81
5.6	Performance	83
5.6.1	The performance of the barrel region	83
5.6.1.0.1	Roles of gaseous and silicon trackers	83
5.6.2	The performance of forward tracking (end-cap)	84

Thanks to all the contributors

Ref-TDR Continuously Incorporates Latest Elaborate Design



Weekly Highlight Invited Talk in Silicon Tracker Group

- We hold weekly invited highlight talk within the Silicon Tracker group, covering topics such as the progress on detector developments, electronics, mechanics (cooling), and software, with all staff and students in the group involved to present. The focus is on sharing, communication, and encouragement, and the content can include current work, future plan, or work outside of CEPC.
- Good work will be selected for CEPC Day to have sufficient recognition. Exceptional work will also be recommended to represent the group at conference presentations.

高精度时间时间测量

严雄波

2025. 1. 3

