CEPC Silicon Tracker

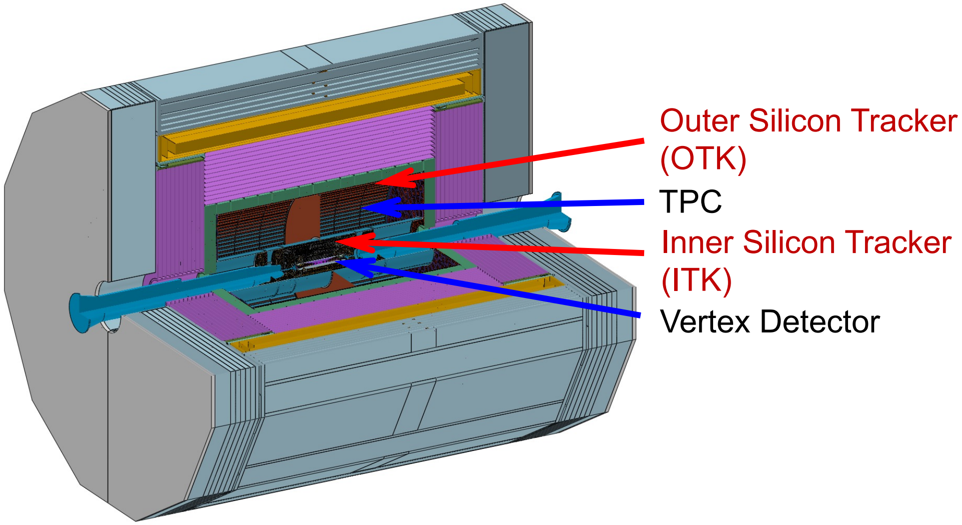
Qi Yan *on behalf of the Silicon Tracker Group*

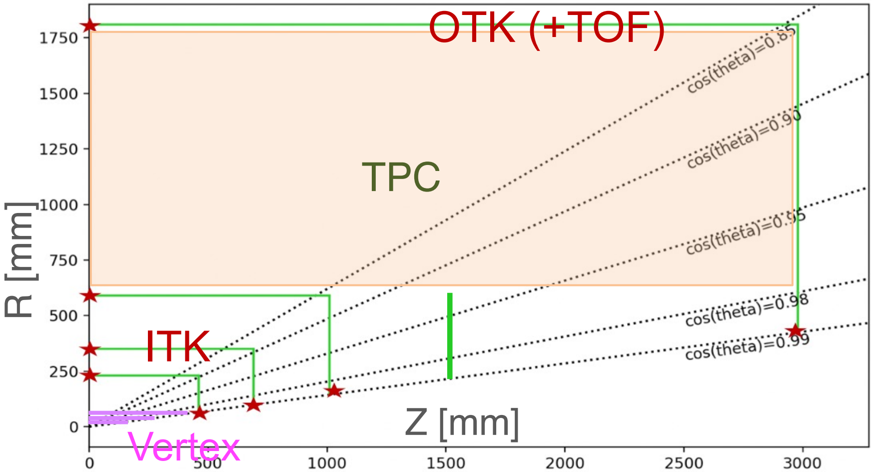
CEPC Day, Jan 24, 2025, IHEP

Overview of CEPC Silicon Tracker

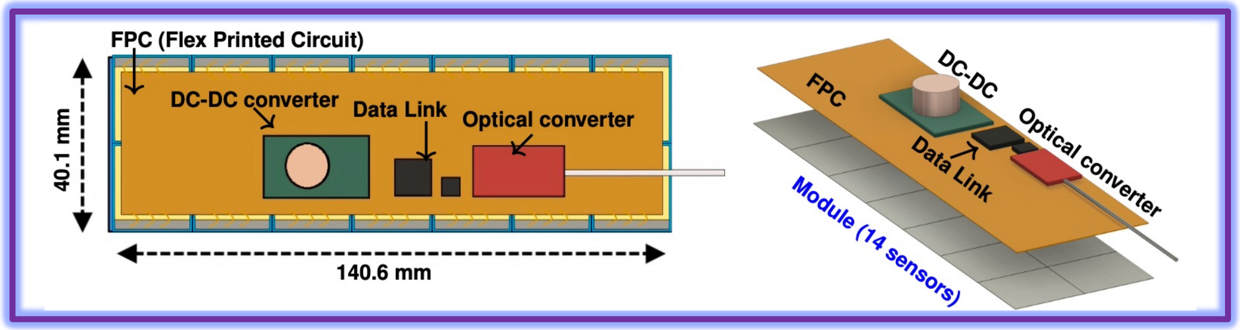
We have developed a comprehensive design for the CEPC Silicon Tracker, incorporating many unique design features compared to existing experiments.

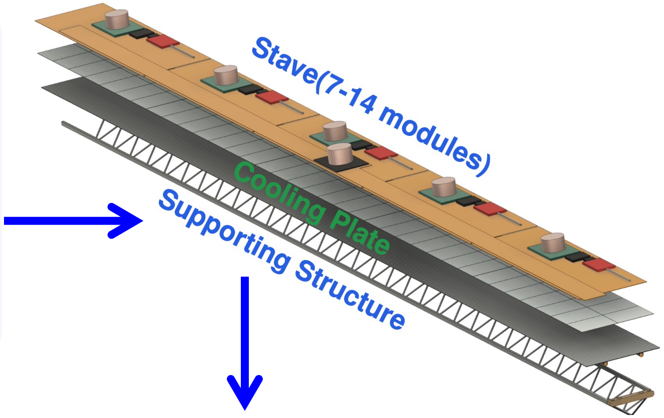
In this presentation, I will give a complete overview of the CEPC Silicon Tracker.

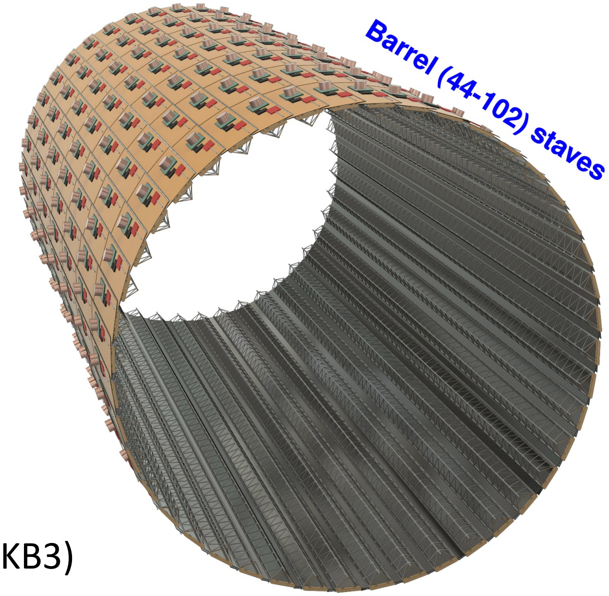




CEPC ITK Design: Barrels with HVCMOS Pixels







HVCMOS pixel sensor:

- Sensor size: 20 mm × 20 mm (active area of 17.4 mm × 19.2 mm)
- Array size: 512 rows × 128 columns
- Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
- Time resolution: 3-5 ns
- Power consumption: ~200 mW/cm^2

Module:

- 14 sensors (2 rows × 7 columns)
- Sensor gap: 100 μm
- Module dimensions: 140.6 mm × 40.1 mm

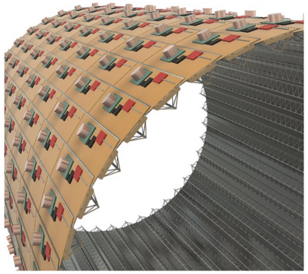
Stave:

- Module gap: 300 μm
- Length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)

Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

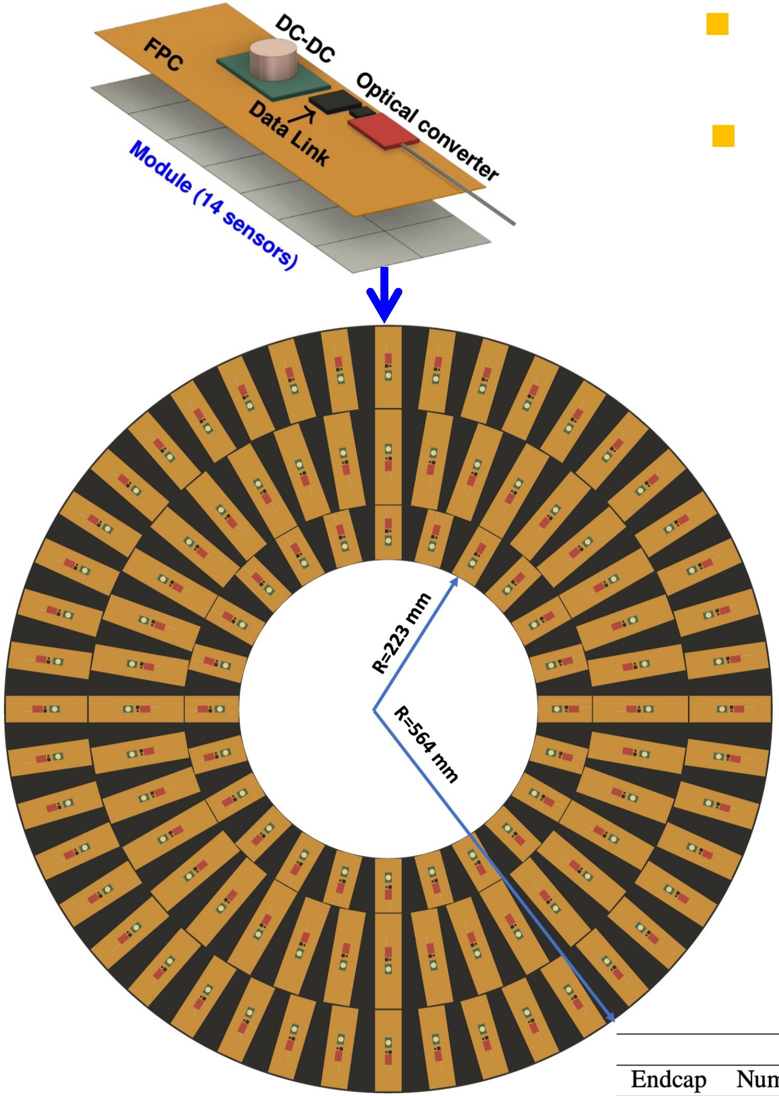
Information about staves, modules, and sensors used for 3 ITK barrels construction

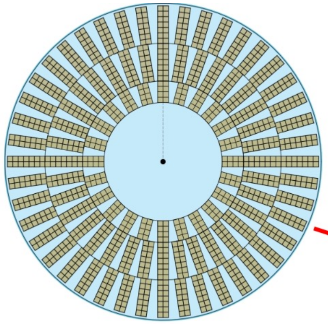
Barrel	Number of staves	Modules per stave	Sensors per module	Total number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4312	1.72
ITKB2	64	10	14	8960	3.58
ITKB3	102	14	14	19992	8.00
Total	210			33264	13.31



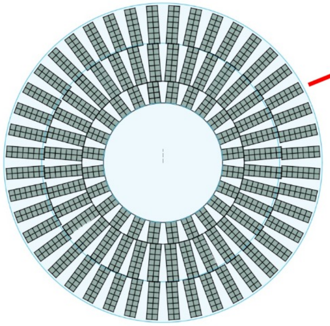
CEPC ITK Design: Endcaps with HVCMOS Pixels

- Module:
  - 3 types of modules：8, 12, and 14 sensors for all 4 ITK endcaps
- Endcap active area radii:
  - 81.5 mm<r<242.5 mm(ITKE1), 110.5 mm<r<352.3 mm (ITKE2), 163 mm <r<564 mm (ITKE3), and 223 mm<r<564 mm (ITKE4)

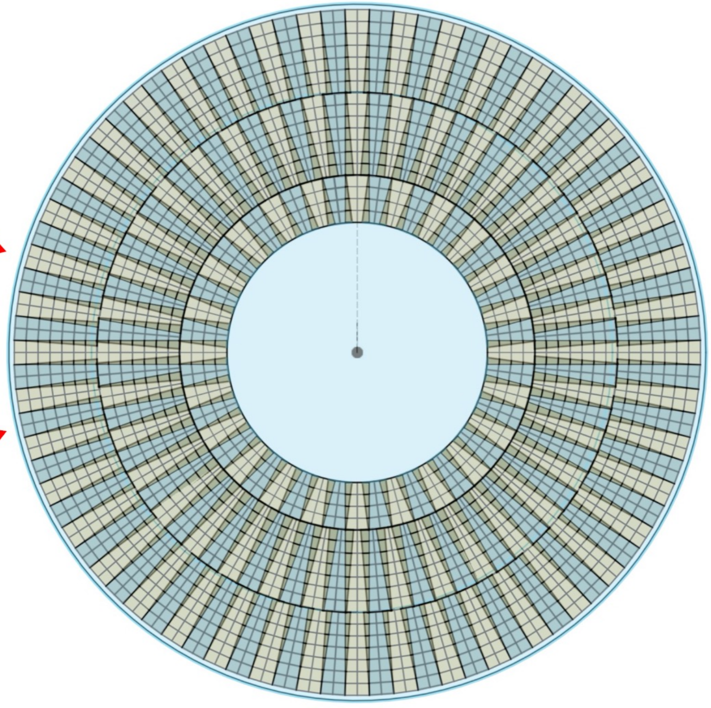




Front view of endcap



Back view of endcap

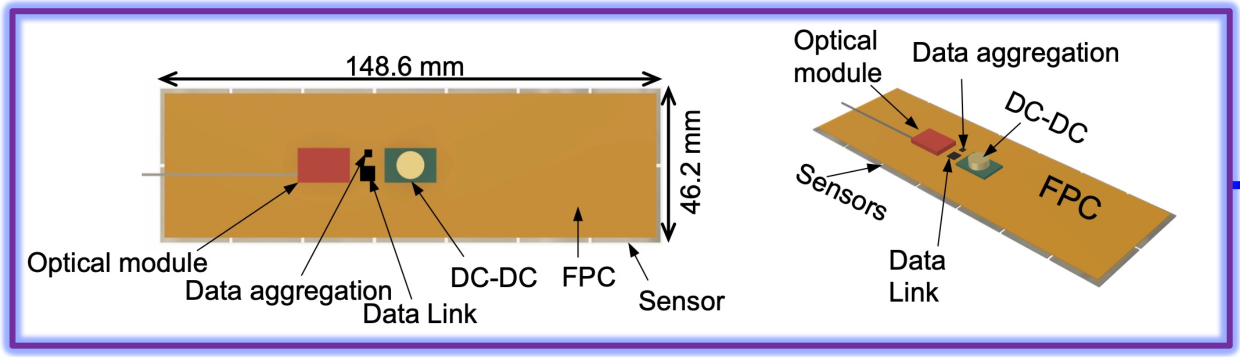


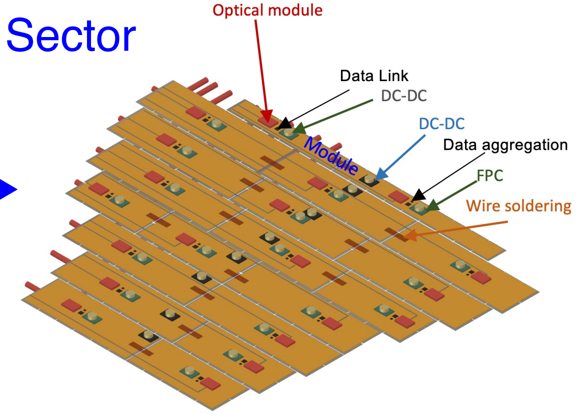
Perspective view of full endcap

The Module and Sensor Layout of a Single Face of Each ITK Endcap

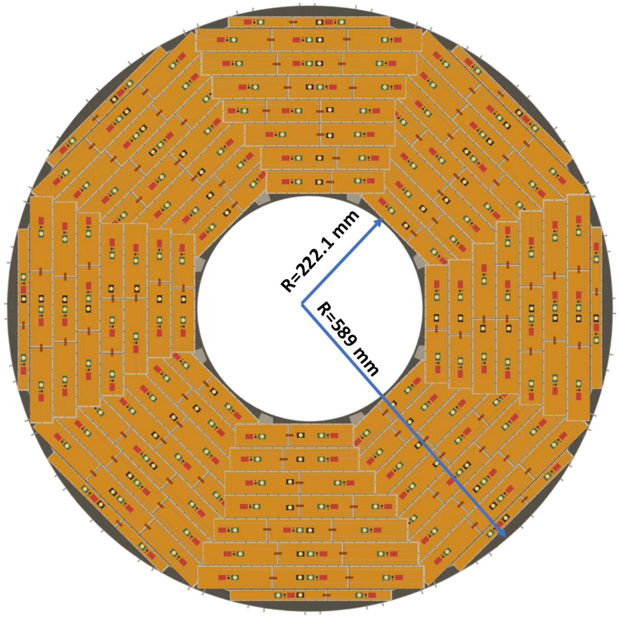
Endcap	Number of module rings	Number of modules per module ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	264
ITKE2	2	16,24,28	8,8,8	544
ITKE3	3	24,36,44	12,14,14	1408
ITKE4	3	24,36,44	8,12,14	1312
Total				3528

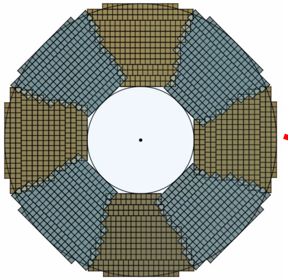
CEPC ITK Design: Endcaps with CMOS Strips (Alternative)



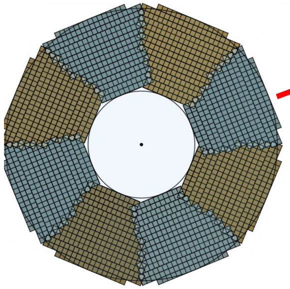


- CMOS Strip Chip/Sensor (CSC) for CEPC:
  - Chip size: 21 mm × 23 mm
  - Strip number per chip: 1024
  - Strip pitch size: 20 μm (spatial resolution 5 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~80 mW/cm



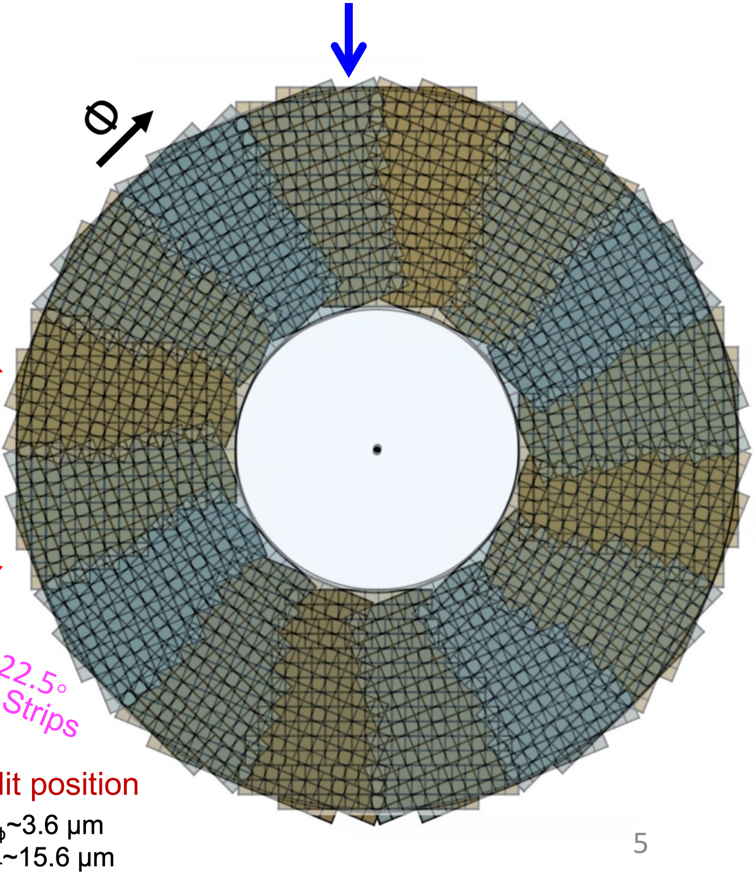


Normal half endcap



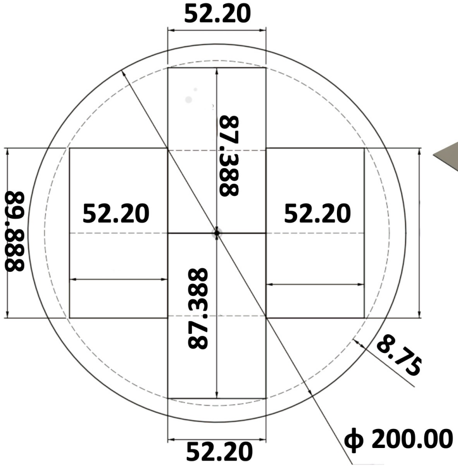
22.5◦ half endcap

$\sigma_\phi \sim 3.6$ μm
$\sigma_r \sim 15.6$ μm

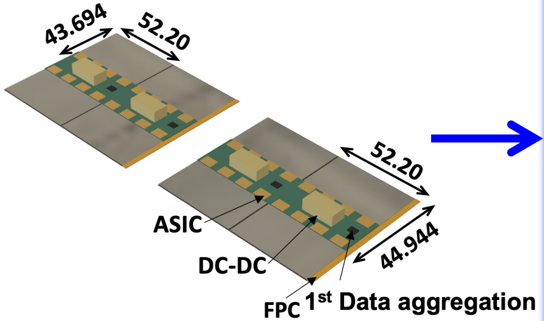


CEPC OTK Barrel Design with AC-LGAD Strips

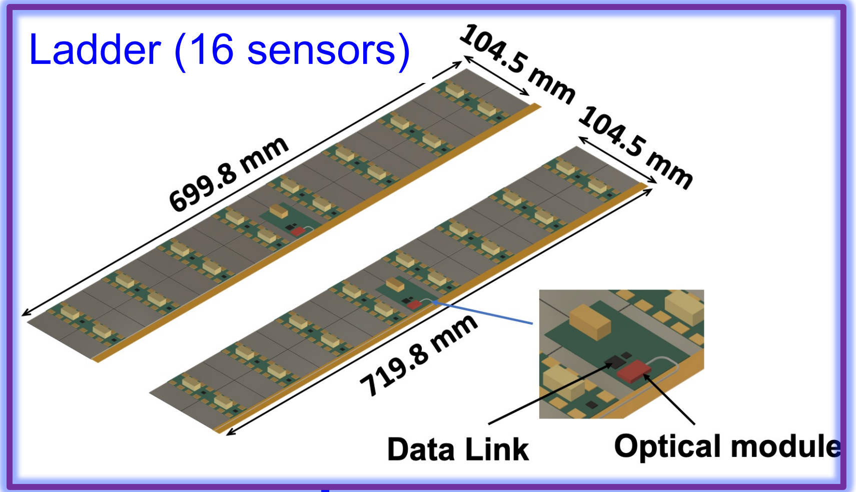
8'' wafer



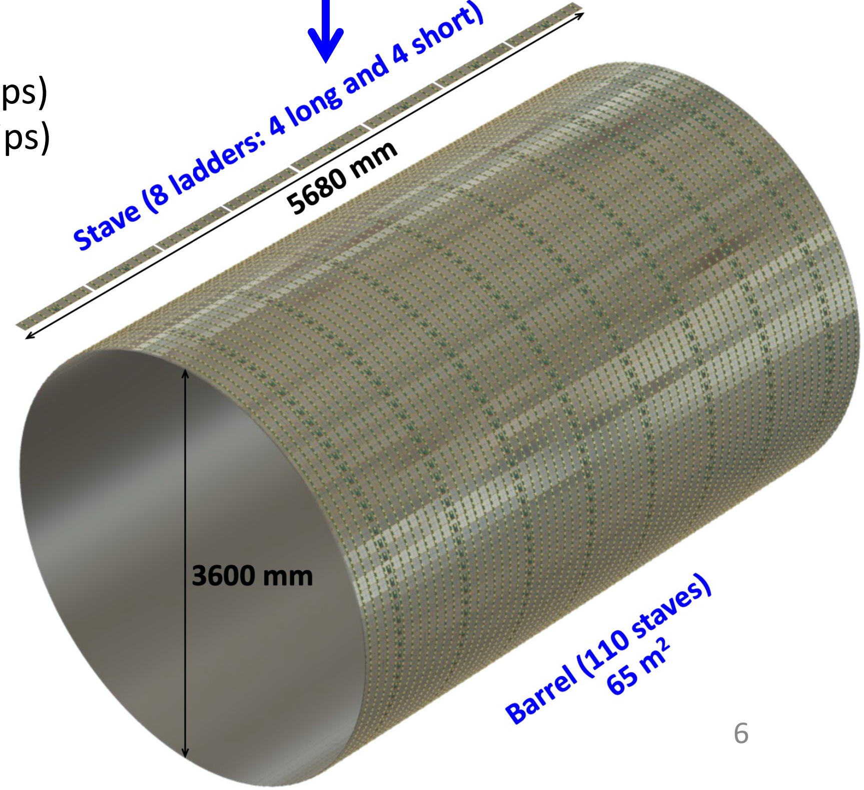
Module (2 sensors)



Ladder (16 sensors)

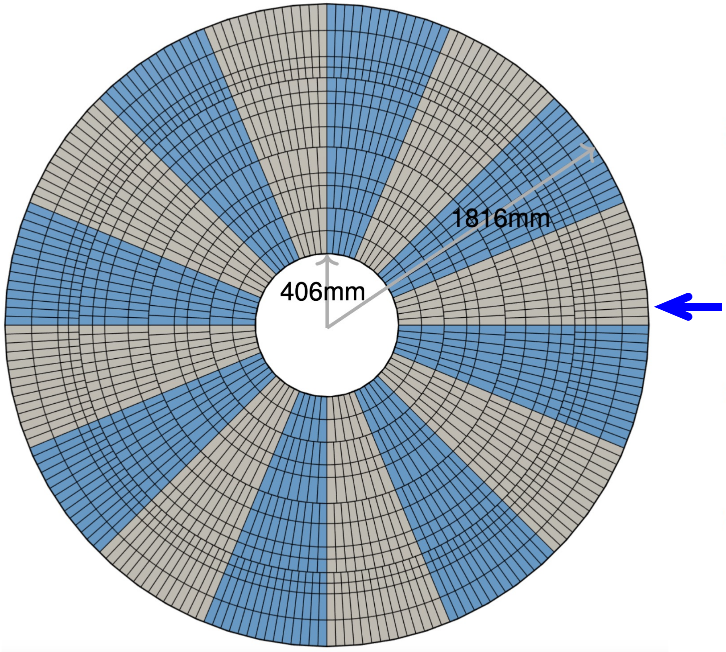


- AC-LGAD sensor:
  - Sensor size: 87.388 mm × 52.20 mm (2 sets of strips)
    89.888 mm × 52.20 mm (2 sets of strips)
  - Strip length: 43.644 mm or 44.894 mm
  - Strip number: 512 ×2
  - Strip pitch: 100 µm
  - Time resolution: 50 ps
  - Power consumption: 300 mW/cm^2
- Module: 2 sensors (16 readout ASICs with 128-channels)
- Ladder:
  - 8 modules (16 sensors)
  - Length: 699.8 mm or 719.8 mm
- Stave: 8 ladders (4 short+4 long)

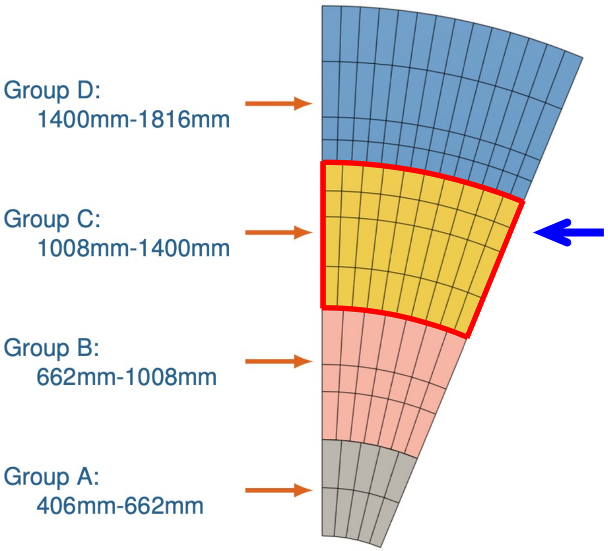


CEPC OTK Endcap Design with AC-LGAD Strips

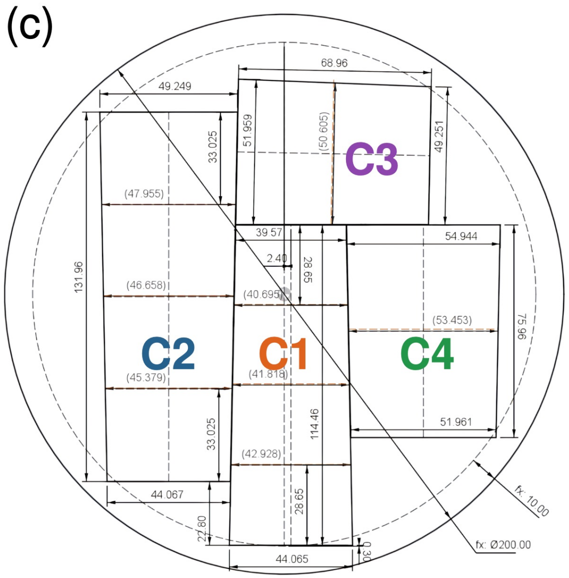
Endcap (16 sectors, 10 m^2)



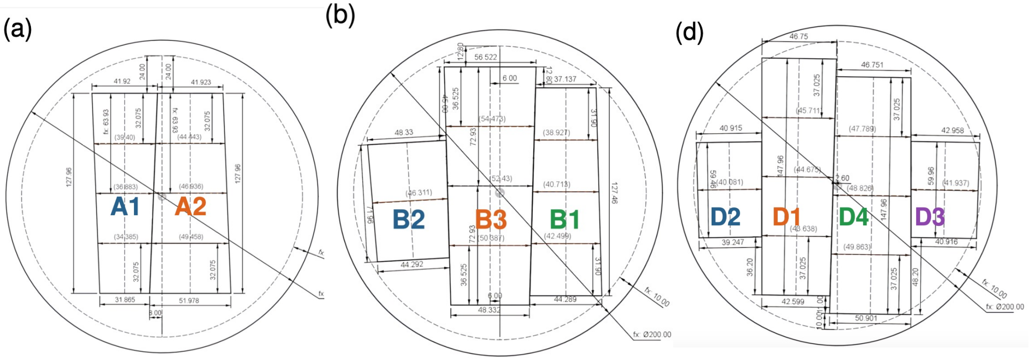
1/16 Sector



Sensor: 8’’ wafer (group C sensors)



- OTK endcap consists of 13 rings, arranged into 4 groups.
- Each group contains 2-4 types of trapezoid sensors, dicing from one 8’’ silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
- The long sensor contains 4 sets of short strips while short sensor contains 2 sets of short strips.
  - Strip pitch : 80.7-113.8 μm
  - Strip length : 28.38-37.61 mm

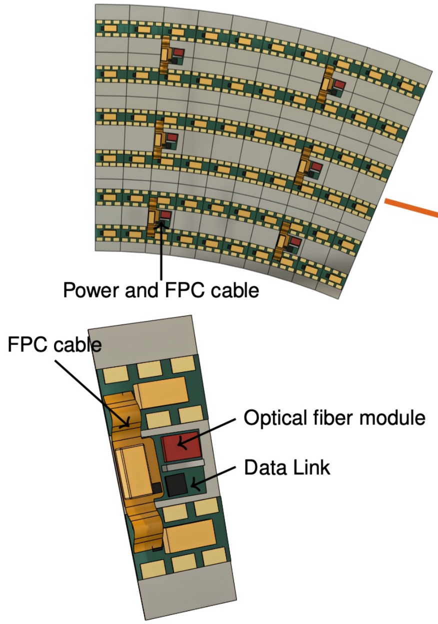


8’’ wafer (group A, B, D sensors)

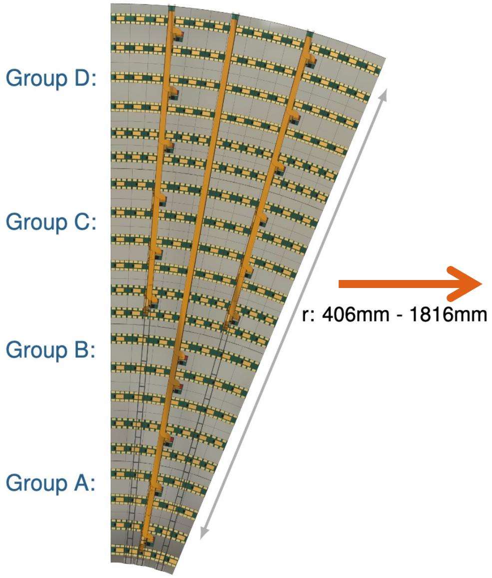
Maximize the use of silicon wafers and facilitate detector assembly.

CEPC OTK Endcap Design with AC-LGAD Strips (2)

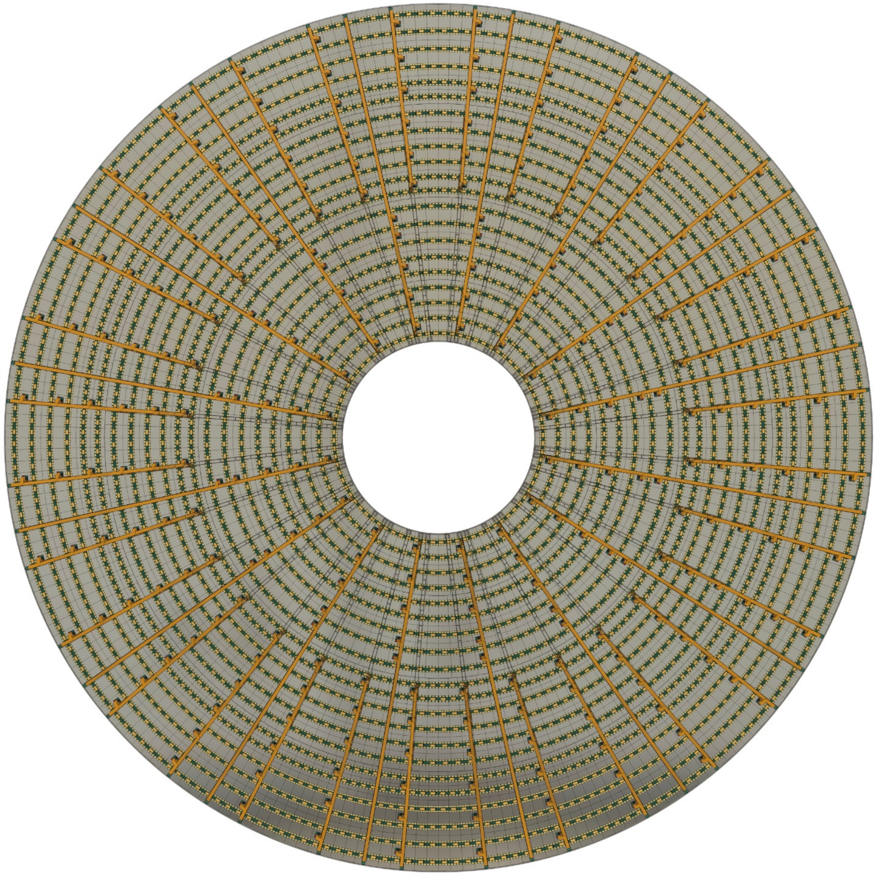
Group C sensors:



1/16 Sector



Endcap (16 sectors)



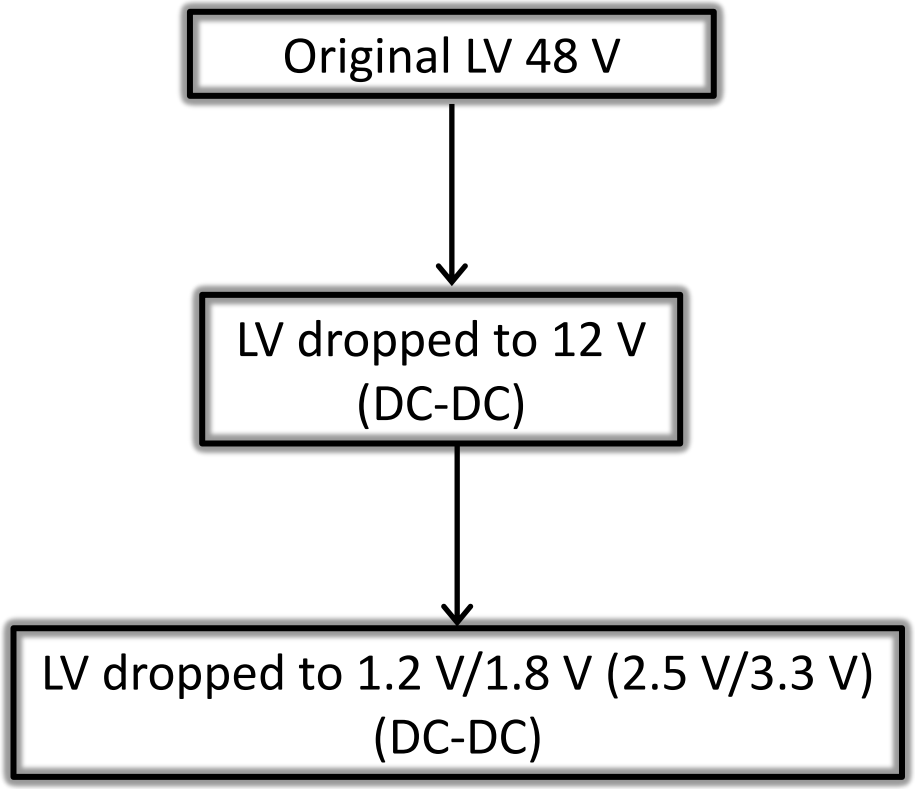
OTK Endcap Trapezoidal Sensor Strip Parameters

Sensor type	Number of strip sets	Number of strips per set	Strip pitch [μm]	Strip length [mm]
A1	4	384	81.5-107.6	31.755
A2	4	512	80.7-100.3	31.755
B1	4	384	95.1-113.8	31.630
B2	2	512	85.3-93.2	35.610
B3	4	512	93.2-109.2	36.255
C1	4	384	101.5-113.2	28.380
C2	4	512	84.9-95.0	32.755
C3	2	512	95.0-100.3	34.110
C4	2	512	100.3-106.1	37.610
D1	2	384	100.6-105.0	29.360
D2	2	384	105.0-109.4	29.610
D3	4	512	82.0-90.1	36.755
D4	4	512	90.1-98.2	36.755

Sensors and Silicon Wafers Usage per OTK Endcap

Mask	A		B			C				D			
Sensor type	A1	A2	B1	B2	B3	C1	C2	C3	C4	D1	D2	D3	D4
Number of sensors	80	80	112	112	112	160	160	160	160	224	224	224	224
Number of wafers	80		112			160				224			

Silicon Tracker Power Cabling Scheme



Original LV 48 V

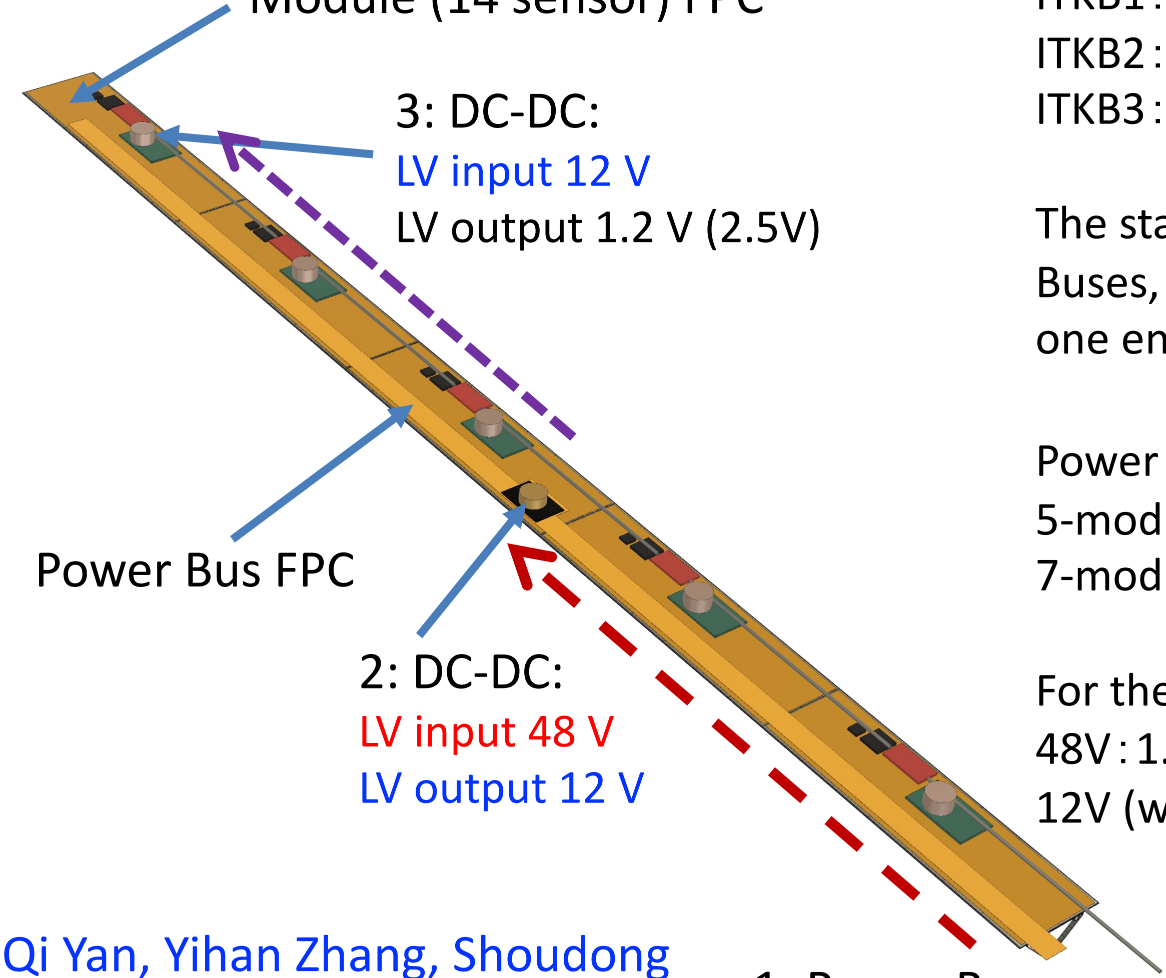
↓

LV dropped to 12 V
(DC-DC)

↓

LV dropped to 1.2 V/1.8 V (2.5 V/3.3 V)
(DC-DC)

Power Rail for ITK Barrel Stave



Module (14 sensor) FPC

3: DC-DC:
LV input 12 V
LV output 1.2 V (2.5V)

Power Bus FPC

2: DC-DC:
LV input 48 V
LV output 12 V

1: Power Bus:
HV input 150 V
LV input 48 V

ITKB1 : 7 modules per stave (986.6 mm)
ITKB2 : 10 modules per stave (1,409.6 mm)
ITKB3 : 14 modules per stave (1,973.2 mm)

The staves of ITKB2 and ITKB3 use 2 Power Buses, each serving 5 or 7 modules from one end.

Power requirement per Power Bus:
5-module: ~60 W
7-module: ~84 W

For the 7 modules, the currents are:
48V : 1.75 A
12V (with 2 lanes): 3.5 A

Qi Yan, Yihan Zhang, Shoudong Luo, Xiongbo Yan

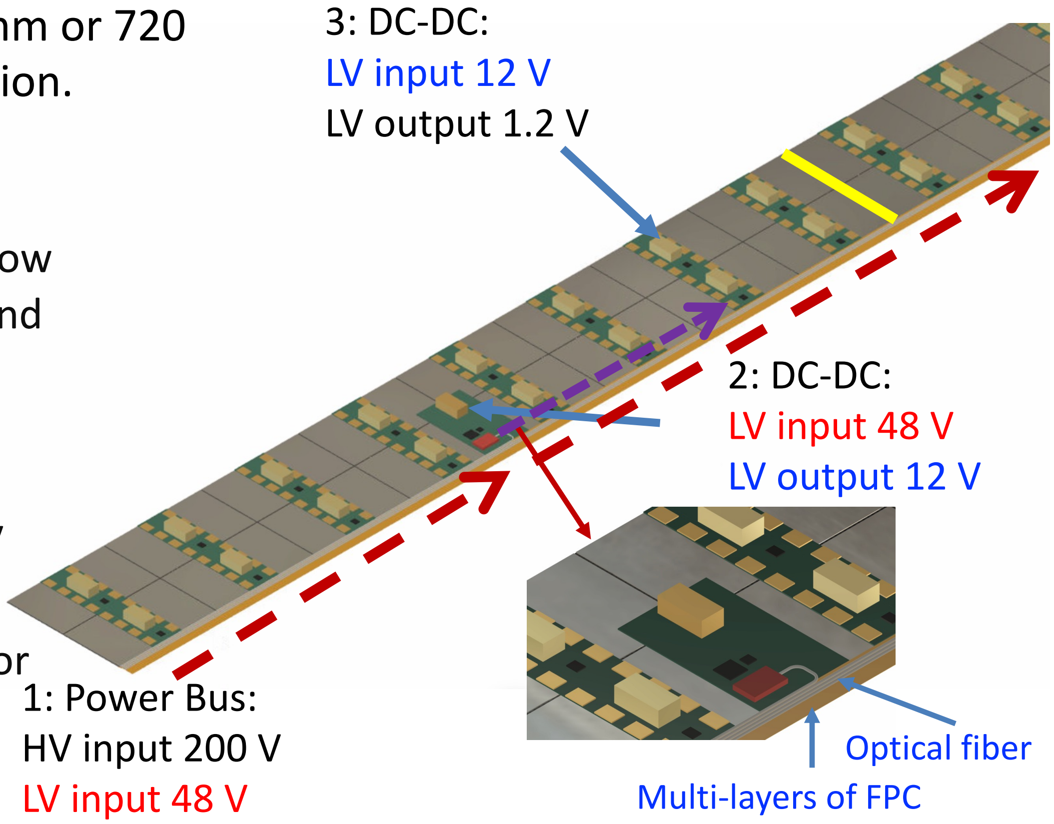
Power Rail for OTK Barrel Stave

Qi Yan, Yihan Zhang, Shoudong Luo, Xiongbo Yan

One OTK stave consists of 8 ladders (700 mm or 720 mm), with 4 ladders read out in one direction.

OTK Voltage Transmission

- The high voltage (HV, 200 V) and original low voltage (LV, 48 V) are transmitted to the 2nd data aggregation boards through the long power bus FPC (Stave FPC).
- The DC-DC converters in the 2nd data aggregation boards step down the 48 V LV input to 12 V.
- The 12 V LV, along with 200 V HV for sensor biasing, is distributed to all modules via shorter ladder FPC.



3: DC-DC:
LV input 12 V
LV output 1.2 V

2: DC-DC:
LV input 48 V
LV output 12 V

1: Power Bus:
HV input 200 V
LV input 48 V

Data Link:

- Data output, clock and commands inputs are transmitted between sensor modules and optical module on the secondary data aggregation board through the ladder FPC.

Power Rail for OTK Endcap (1/16 Sector)

Total power requirement:
1840 W per sector ($300\ \mathrm{mW/cm^2}$)

Upper Area: 🟥 670 W each
Lower Area: 🟦 500 W

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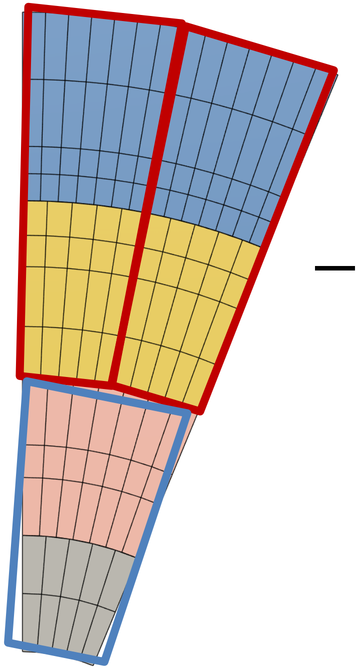
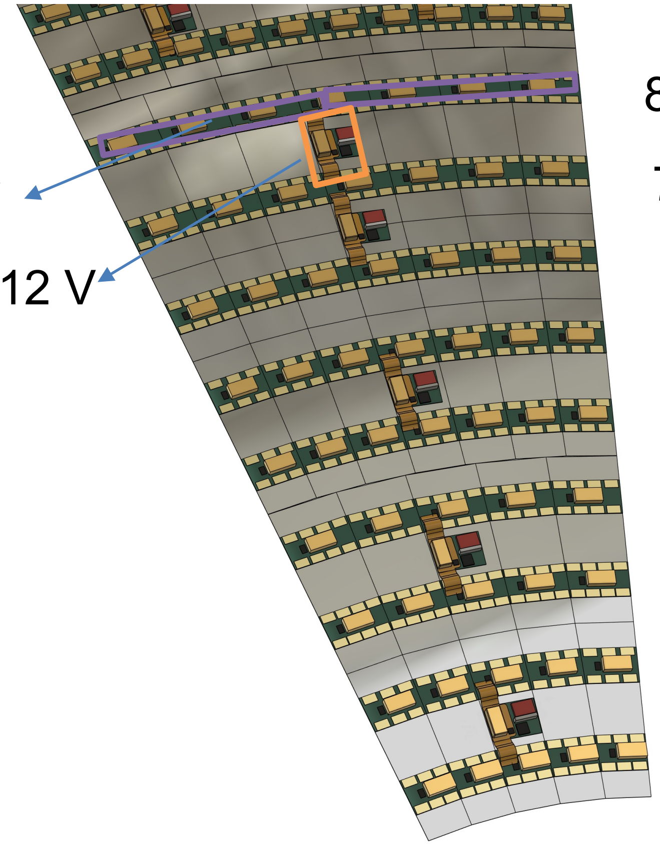
Shoudong Luo, Xiongbo Yan



一级:12 V -> 1.2 V

二级:48 V -> 12 V



83.6 W ~7A (12 V)

77.2 W

70.1 W

60.8 W

48.3 W

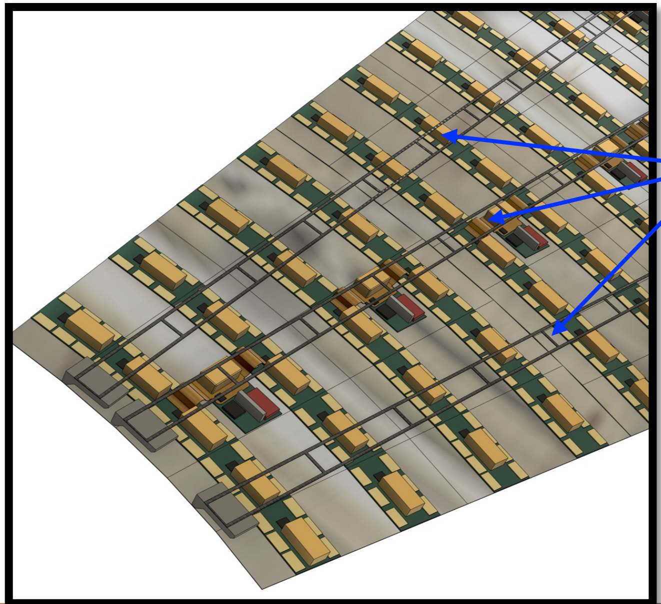
46.8 W

42.2 W

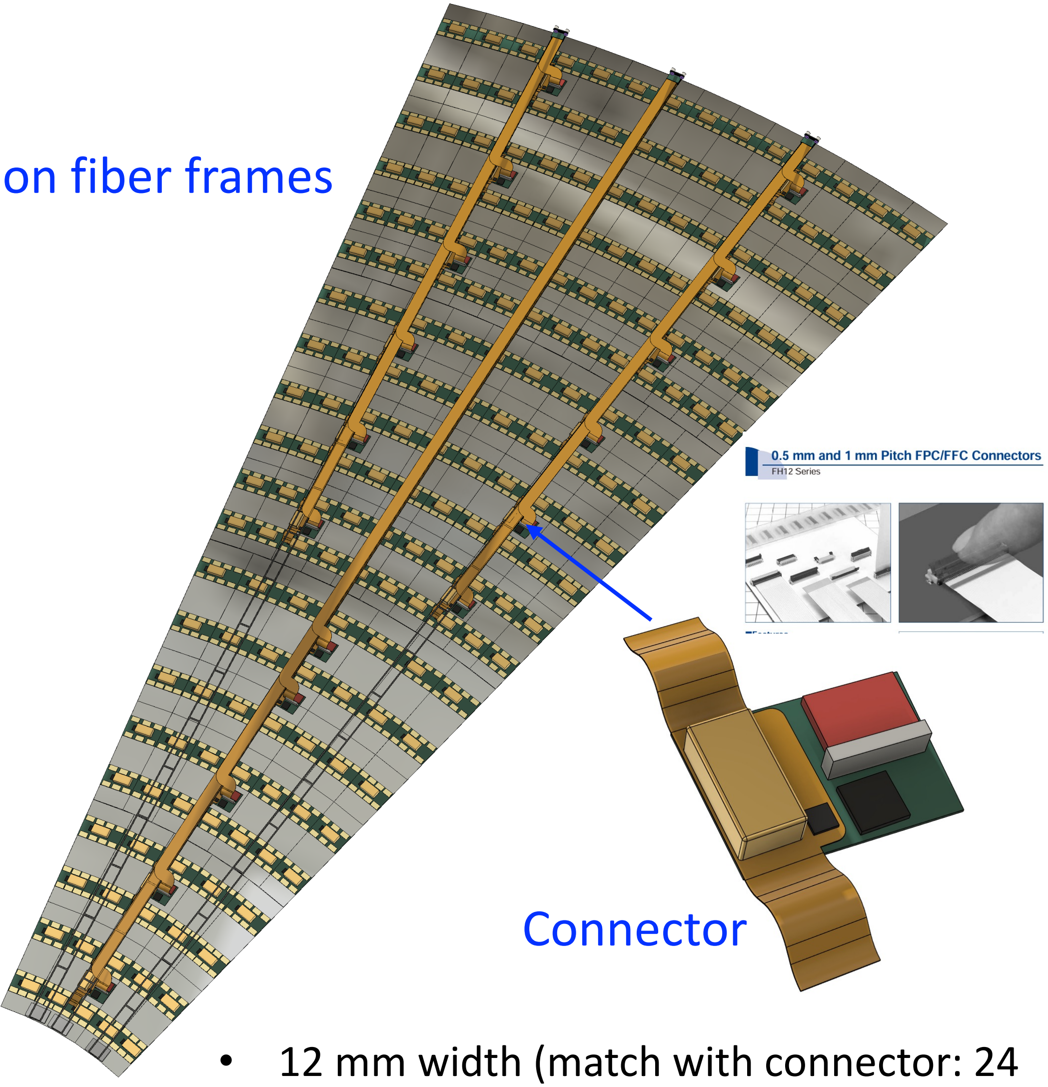
38.9 W

32.1 W

OTK Endcap Power Rail: Power Buses on 3 Frames

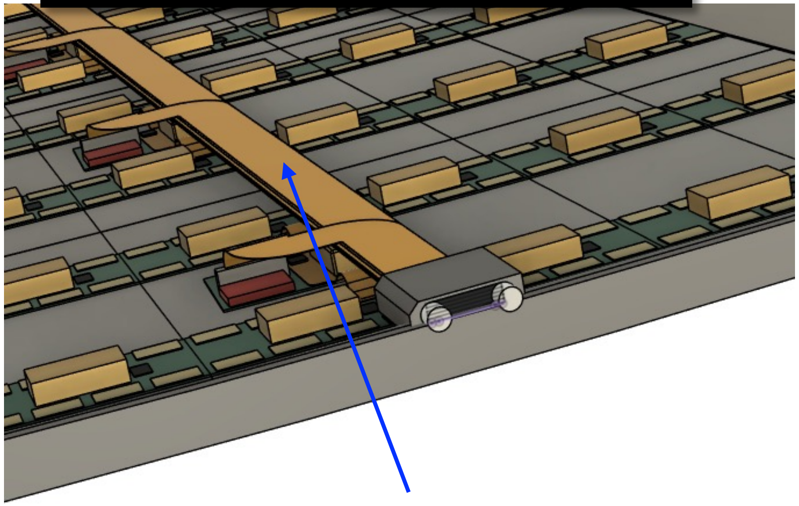


Carbon fiber frames



0.5 mm and 1 mm Pitch FPC/FFC Connectors
FH12 Series

Connector



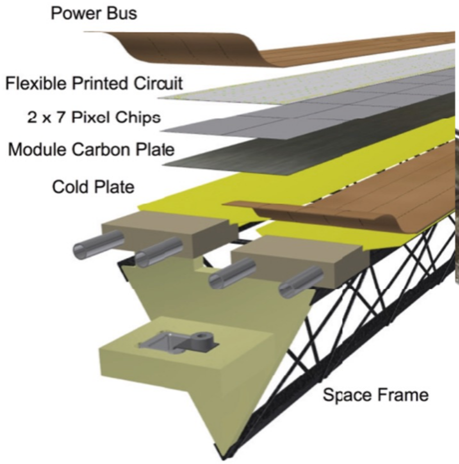
Power Bus transmits: HV (200 V) and LV (48 V)

- 180 µm thick (with metal layer of 25 µm copper or aluminum) is more than sufficient

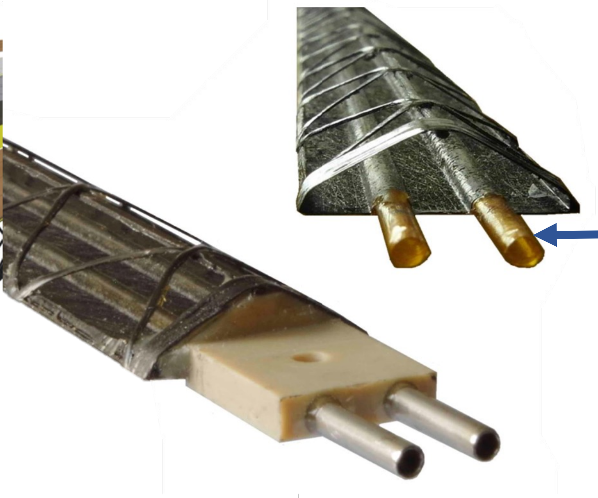
- 12 mm width (match with connector: 24 pins x 0.5 mm pitch)
- Max length: 1,330 mm
- Max power transmission: 4.8 A, 230 W

Improvement of the ITK Stave Support and Cooling Design

ITS2 Outer barrel stave

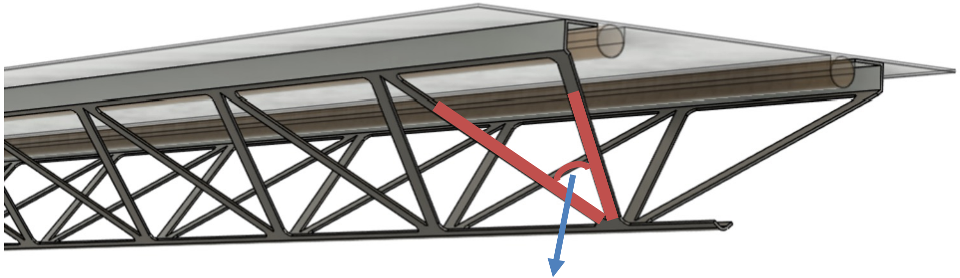


ITS2 Inner barrel stave



Polyimide pipe

Qi Yan, Yihan Zhang, Yujie Li, and Quan Ji



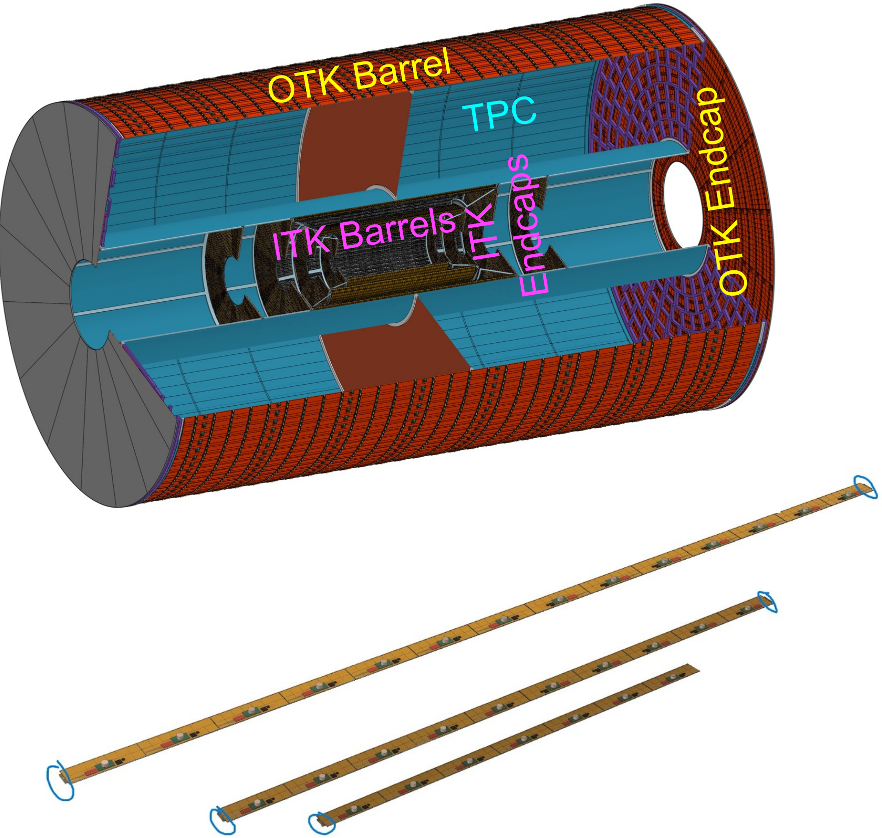
CEPC ITK Barrel stave

58 – 62 deg

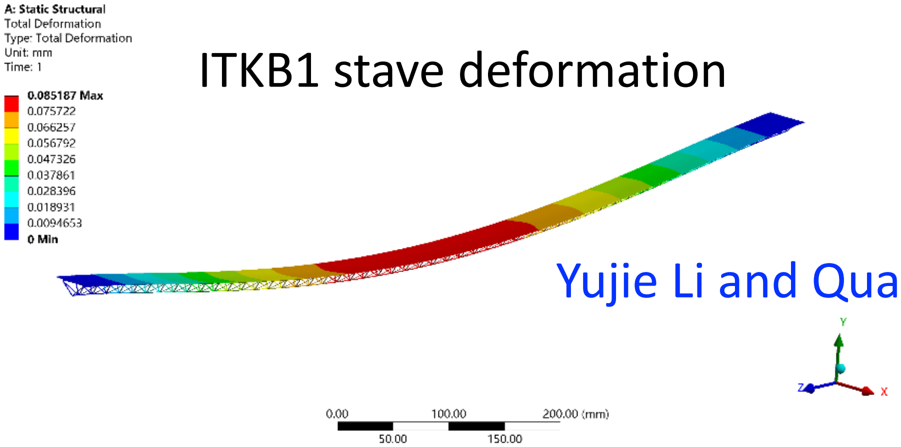
CEPC ITK barrel truss

Water with polyimide cooling pipe was used as baseline cooling fluid for the ITK. Polyimide possesses outstanding properties such as low mass, high temperature resistance, corrosion resistance, radiation resistance, and high strength.

ITK Stave Deformation and First Natural Frequency



ITKB1 stave deformation



Yujie Li and Quan Ji

First order mode and first natural frequency

ITK Stave	ITKB1	ITKB2	ITKB3
Stave length [mm]	987	1410	1974
Maximum sag [µm]	85	289	896
First natural frequency [Hz]	126	69	34

The first natural frequency indicates the frequency at which an external impulse can induce resonance phenomena in the structure, resulting in oscillations of the sensor positions.

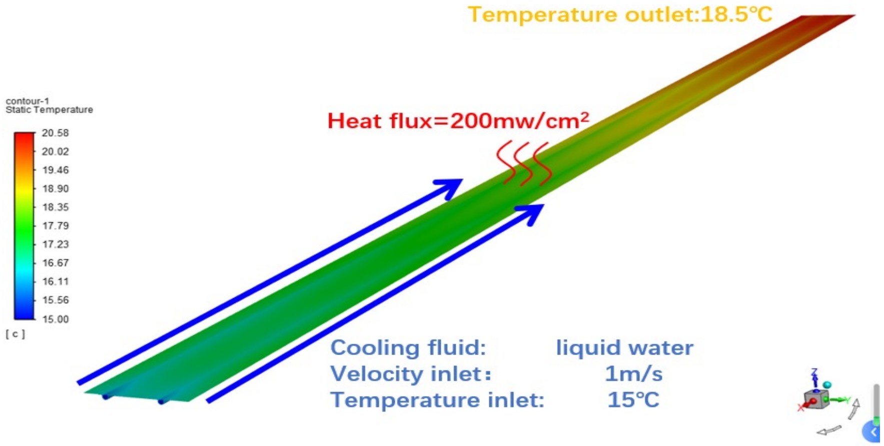
ITK Barrel Stave Thermal Characterisation

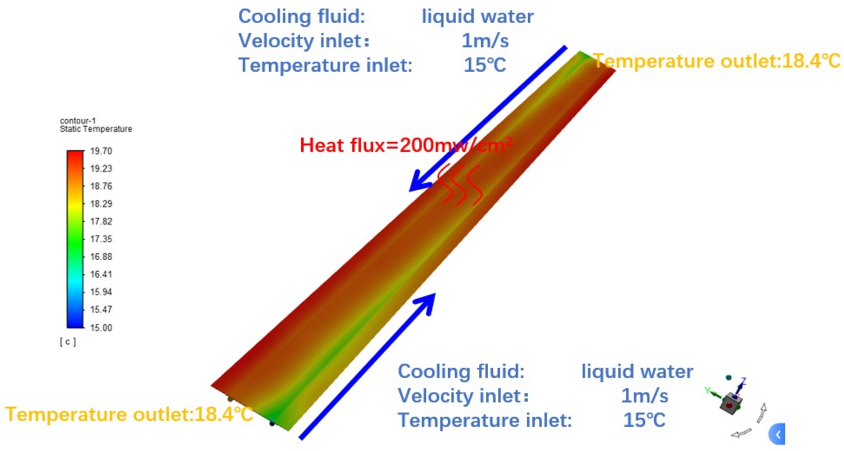
The heat generated by ITK sensors with a magnitude of 200 mW/cm^2. The cooling design should achieve the following:

- The overall sensor operating temperature <30 °C.
- The temperature uniformity across a single sensor <5°C.

Yujie Li and Quan Ji

A water cooling fluid structure coupled finite element model was established to study the temperature distribution:





The temperature gradient along the 987 mm length of the stave can be controlled within 5°C. The water cooling meets the detector's requirements.

ITK Mechanical and Cooling Structure Design

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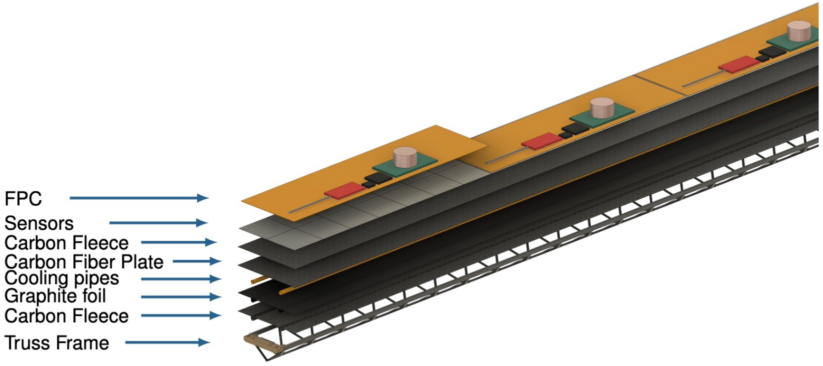
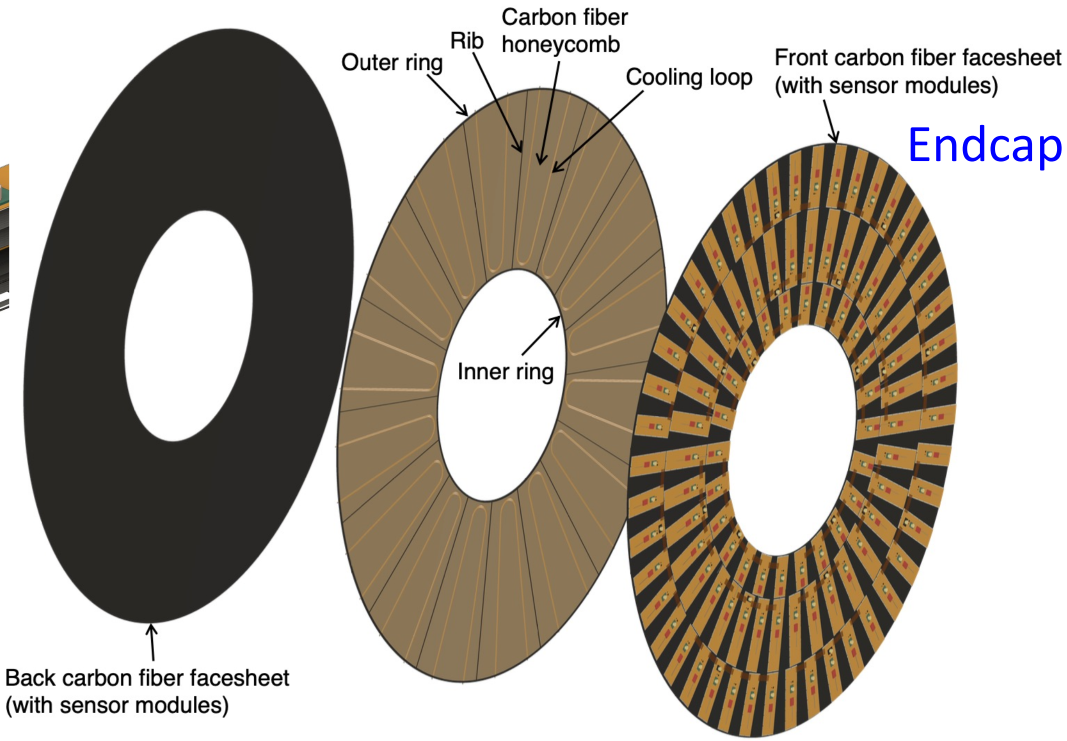
Barrel



Endcap



Estimation of ITK stave material contributions

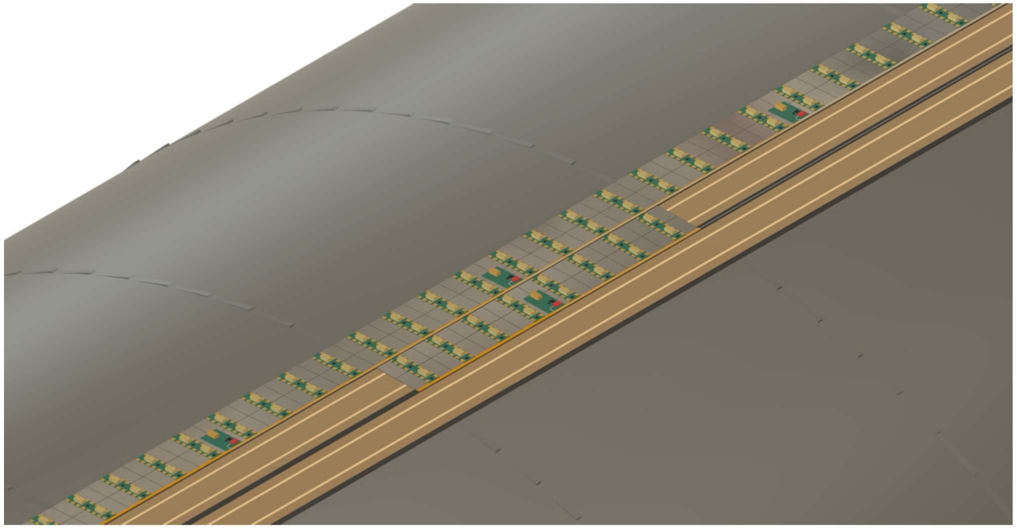
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64	28.41	0.013
	Cooling fluid	Water		35.76	0.105
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Total					0.673

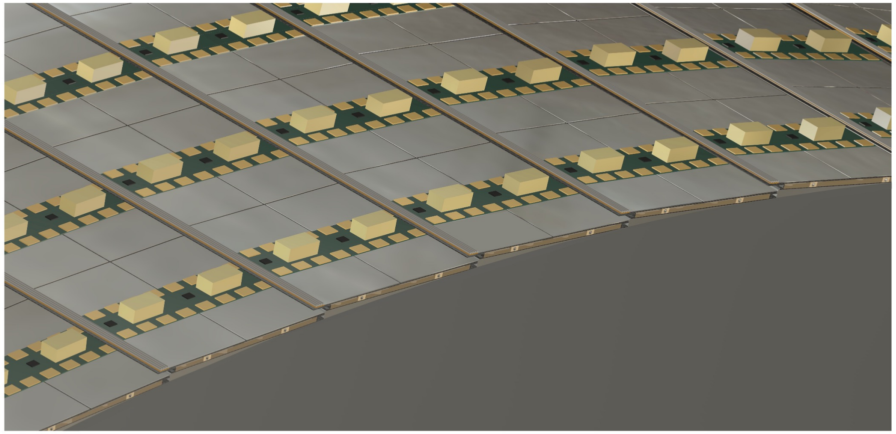
Estimation of ITK HV-CMOS pixel endcap material contributions

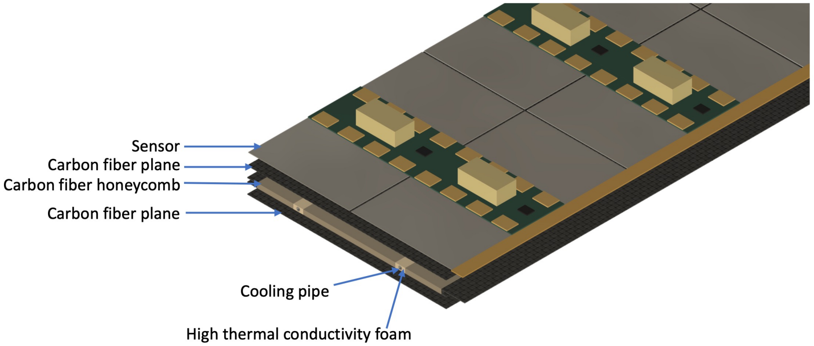
Functional unit	Component	Material	Thickness [μm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Structure	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Titanium		3.560	XXX
	Cooling fluid	Water		35.76	XXX
	Graphite foam+Honeycomb	Allcomp+Carbon fiber	2000	186	0.108
	Carbon fiber facesheet	Carbon fiber	150	26.08	0.057
	Glue	Cyanate ester resin	200	44.37	0.045
Total					0.591+XXX

Mechanical and Cooling Structure Design for the OTK Barrel

Qi Yan, Shoudong Luo, Quan Ji

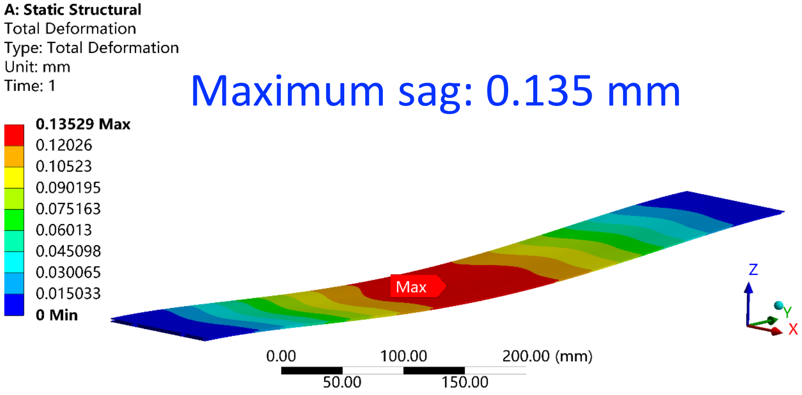




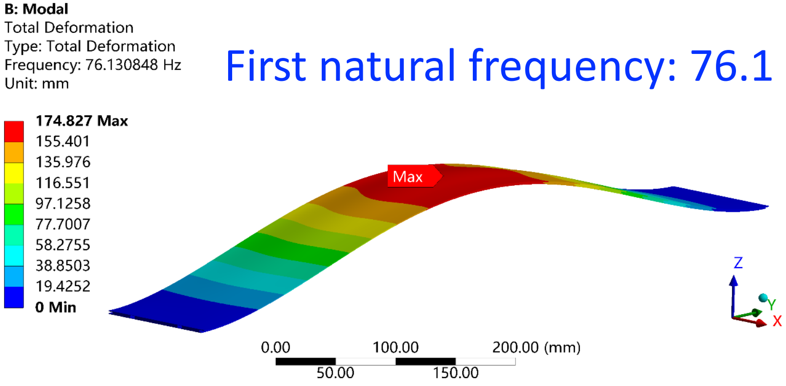


1) The TPC outer barrel is made of a carbon fiber cylinder with stepped ramp rings.
2) The lower support carbon fiber facesheet, with a carbon fiber honeycomb glued on top, was mounted onto the stepped ramp rings.
3) Two cooling pipes (~6 m in length), were then inserted into the gaps of the carbon fiber honeycomb, sealed with high conductivity foam surrounding them.
4) 8 ladders were glued on top one by one to enclose stave honeycomb and complete the construction of one stave. Each OTK ladder (~0.7 meters) has its own support, consisting of 16 sensors, electronic components, and a carbon fiber facesheet.

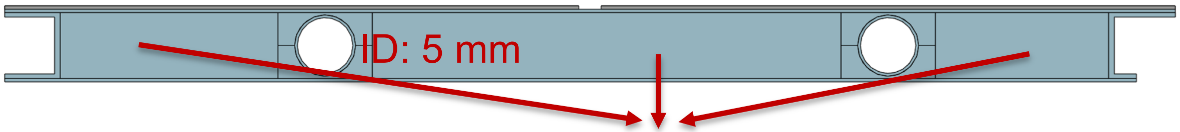
OTK Barrel Structural and Thermal Characterisation



Maximum sag: 0.135 mm

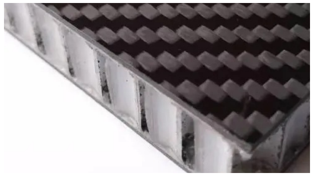


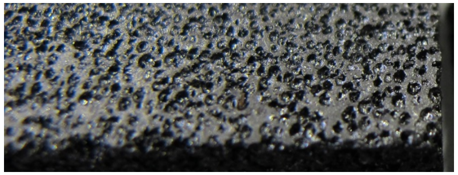
First natural frequency: 76.1 Hz

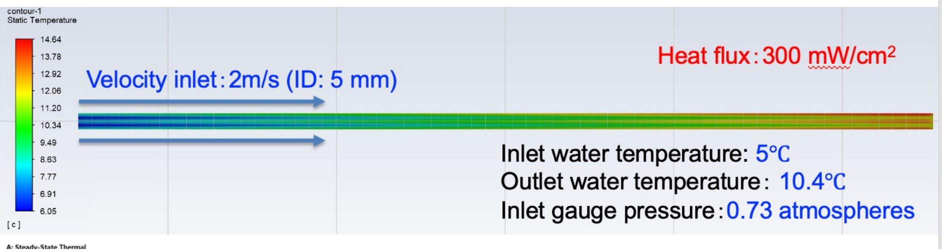


Yujie LI and Quan JI

Honeycomb filled with poco foam to increase thermal conductivity



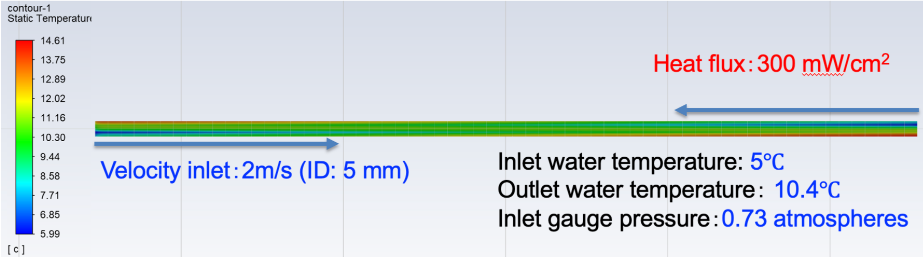




Heat flux: 300 mW/cm²

Velocity inlet: 2m/s (ID: 5 mm)

Inlet water temperature: 5℃
Outlet water temperature: 10.4℃
Inlet gauge pressure: 0.73 atmospheres



Heat flux: 300 mW/cm²

Velocity inlet: 2m/s (ID: 5 mm)

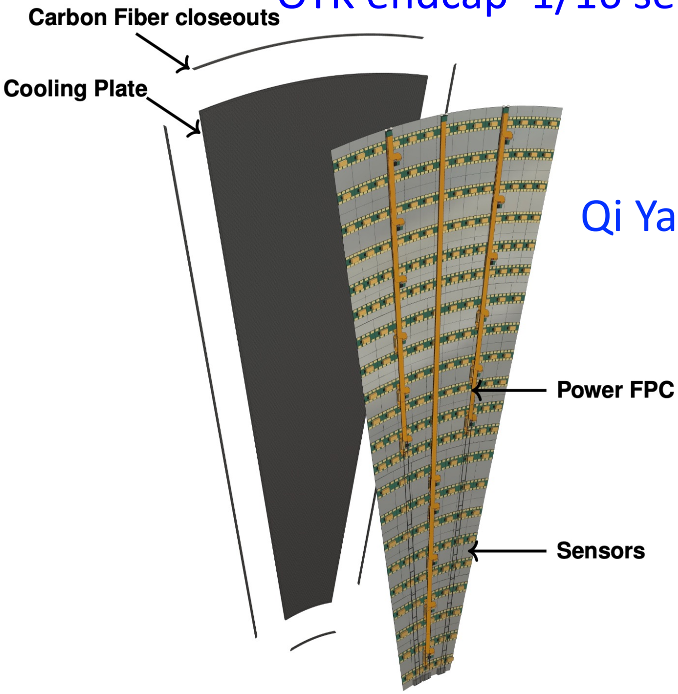
Inlet water temperature: 5℃
Outlet water temperature: 10.4℃
Inlet gauge pressure: 0.73 atmospheres

Using a 5 °C and 2 m/s water inlet (ID: 5 mm), the maximum temperature difference across one sensor is <2.9 °C for inlet from one end and <4 °C for inlet from two ends.

Water cooling can meet the thermal requirements for the OTK over ~6 m stave length.

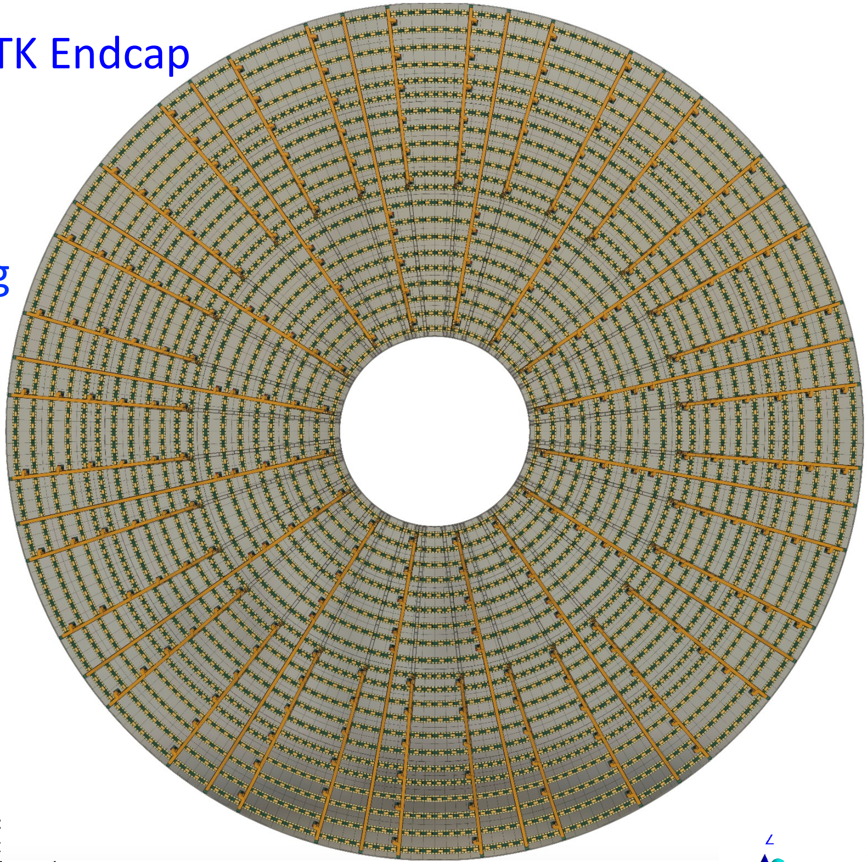
Mechanical and Cooling Design for the OTK Endcap

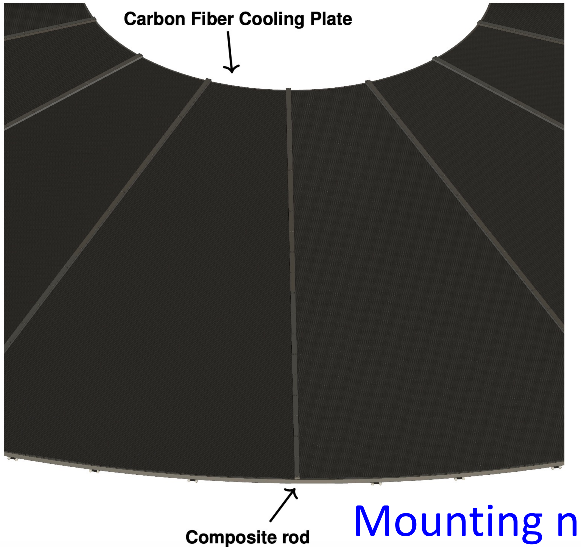
OTK endcap 1/16 sector



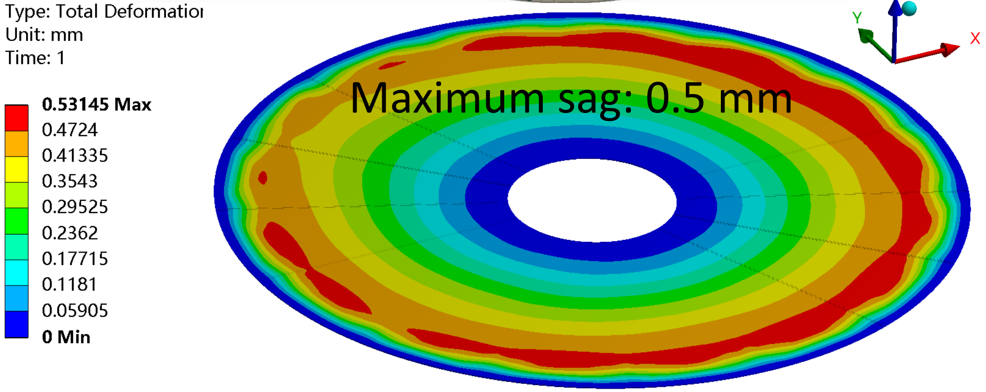
Qi Yan *and* Yihan Zhang

OTK Endcap





Mounting neighboring 1/16 sectors



Maximum sag: 0.5 mm

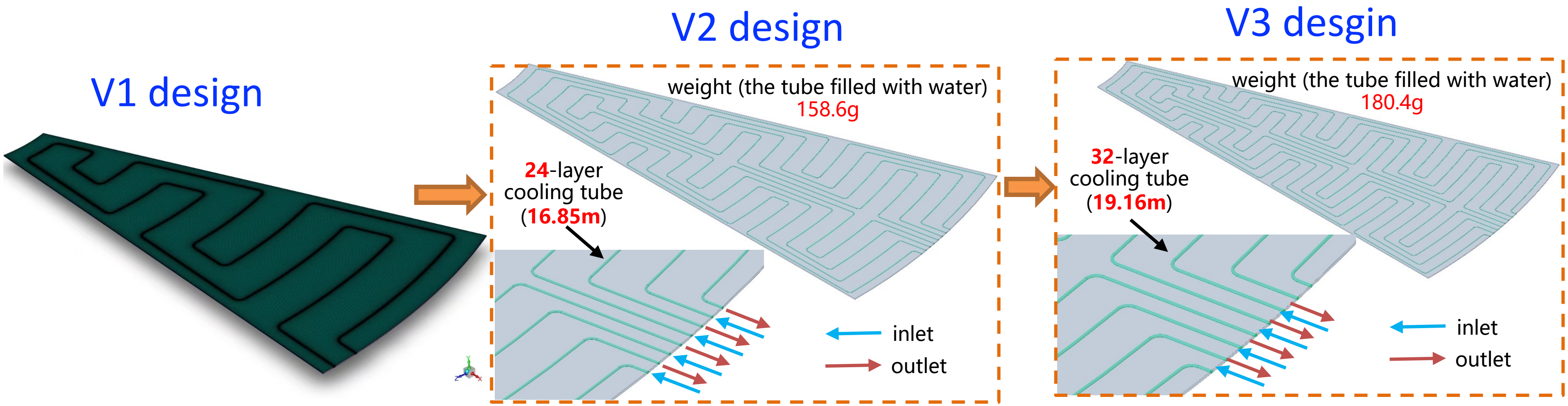
Yujie LI *and* Quan JI

Cooling Loop Design for the OTK Endcap

A few months ago, Quan Ji, Gang Li, and I visited Zhengzhou University of Light Industry, to explore ways to strengthen CEPC’s R&D capabilities in mechanical and thermal systems.

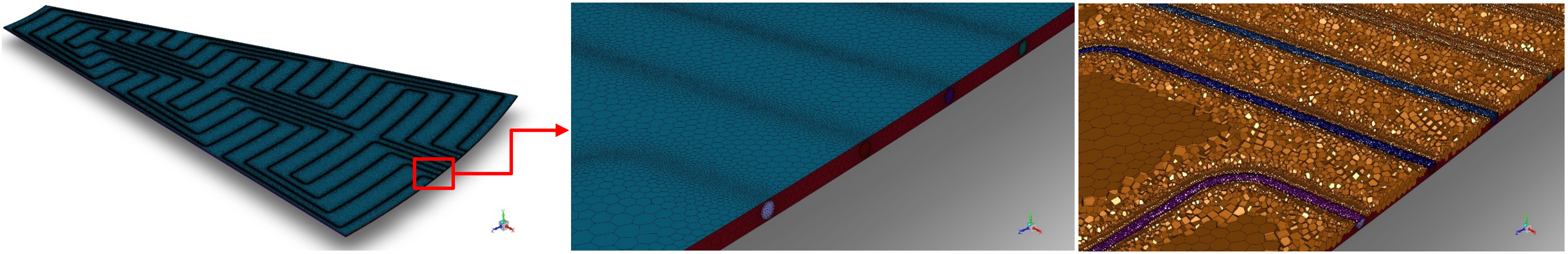
The School of Energy and Power Engineering at Zhengzhou University of Light Industry has extensive experience and a strong focus on thermal system development, including CO_2 cooling. During our visit, we were highly impressed by their expertise in both thermal and mechanical engineering.

On Jan 10, the Dean of the School of Energy and Power Engineering, Professor Xuehong Wu, and his team, visited IHEP in return. They are now actively contributing to the design and analysis of the CEPC thermal system.

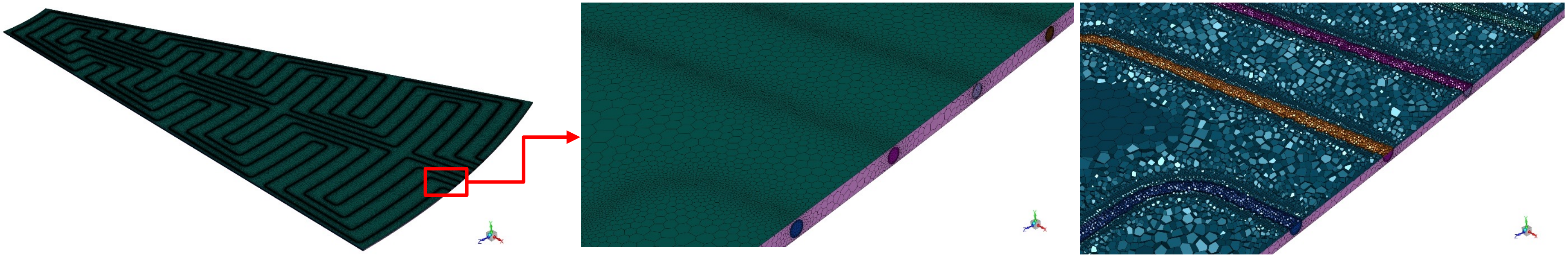


Cooling loops design and thermal analysis for the OTK endcap performed by Zhengzhou University of Light Industry（郑州轻工业大学）.

OTK Endcap Thermal Mesh Generation



24-layer cooling tube(16.85m, cell count 9356670，Orthogonal Quality≥0.5)



32-layer cooling tube(19.16m, cell count 10645946，Orthogonal Quality≥0.5)

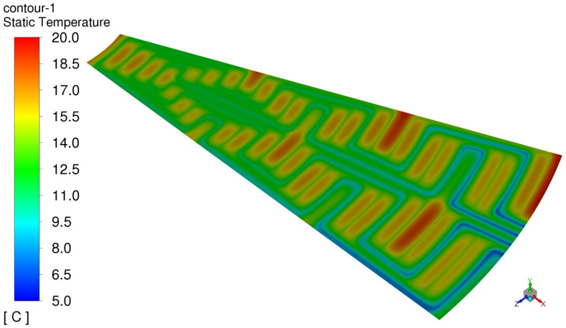
✓ The mesh generation is performed for two different cooling tube arrangements, and numerical solutions are obtained using the finite volume method.

✓ The cooling performance of both arrangements is analyzed and compared.

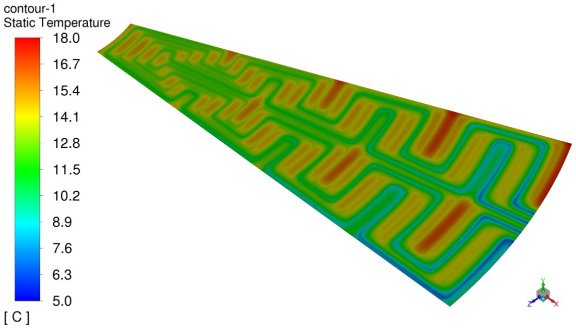
- Cooling tube diameter: 2.6 mm
- Water inlet velocity: 2.5m/s

Continuous optimization is ongoing!

Xuedong Wu, Yong Liu, …
(郑州轻工业大学)



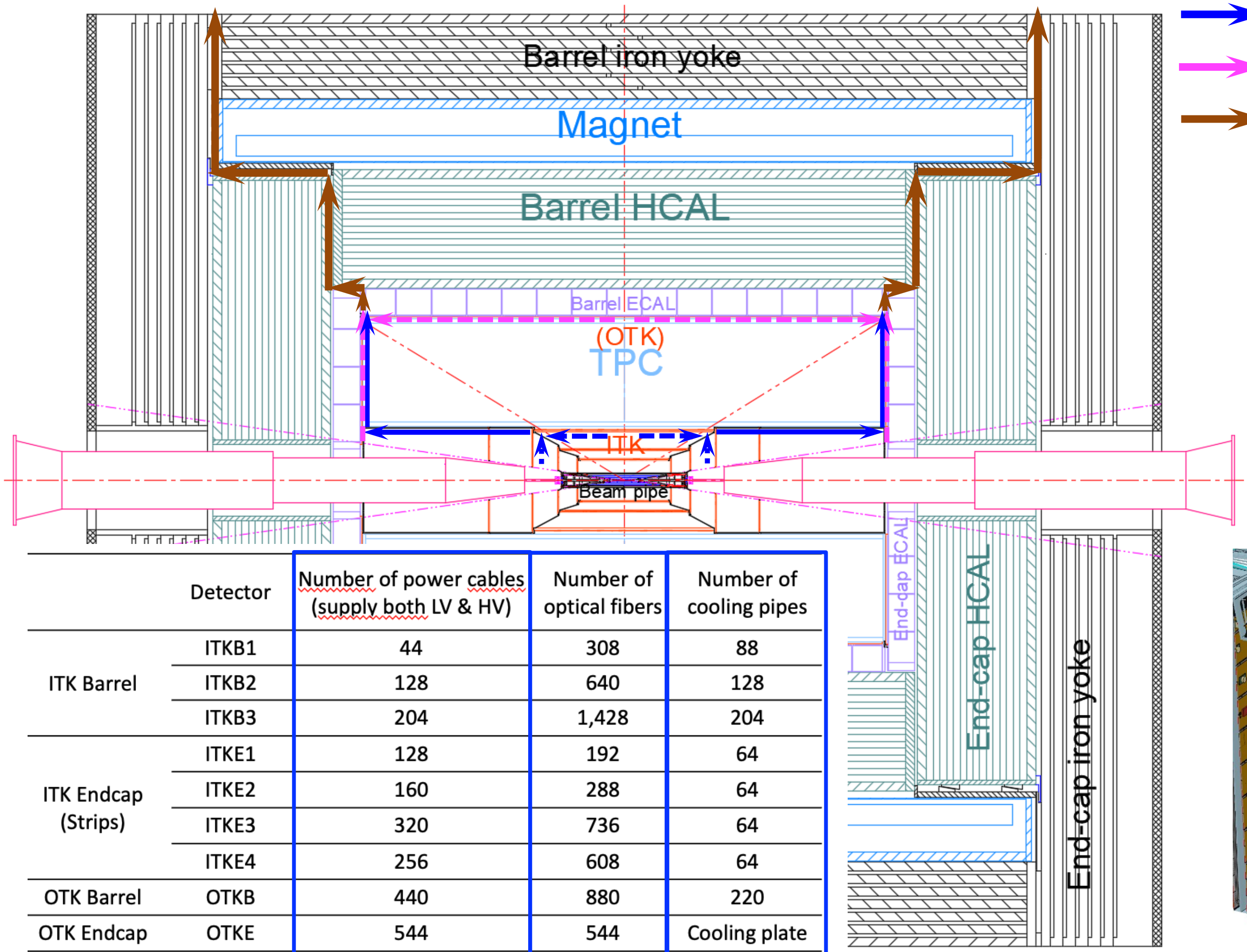
24-layer cooling tube



32-layer cooling tube

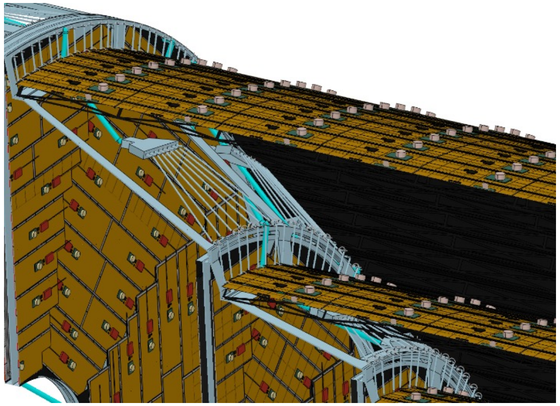
Silicon Tracker Power and Cooling Rail Routing Outward

Qi Yan, Quan Ji, Xiongbo Yan

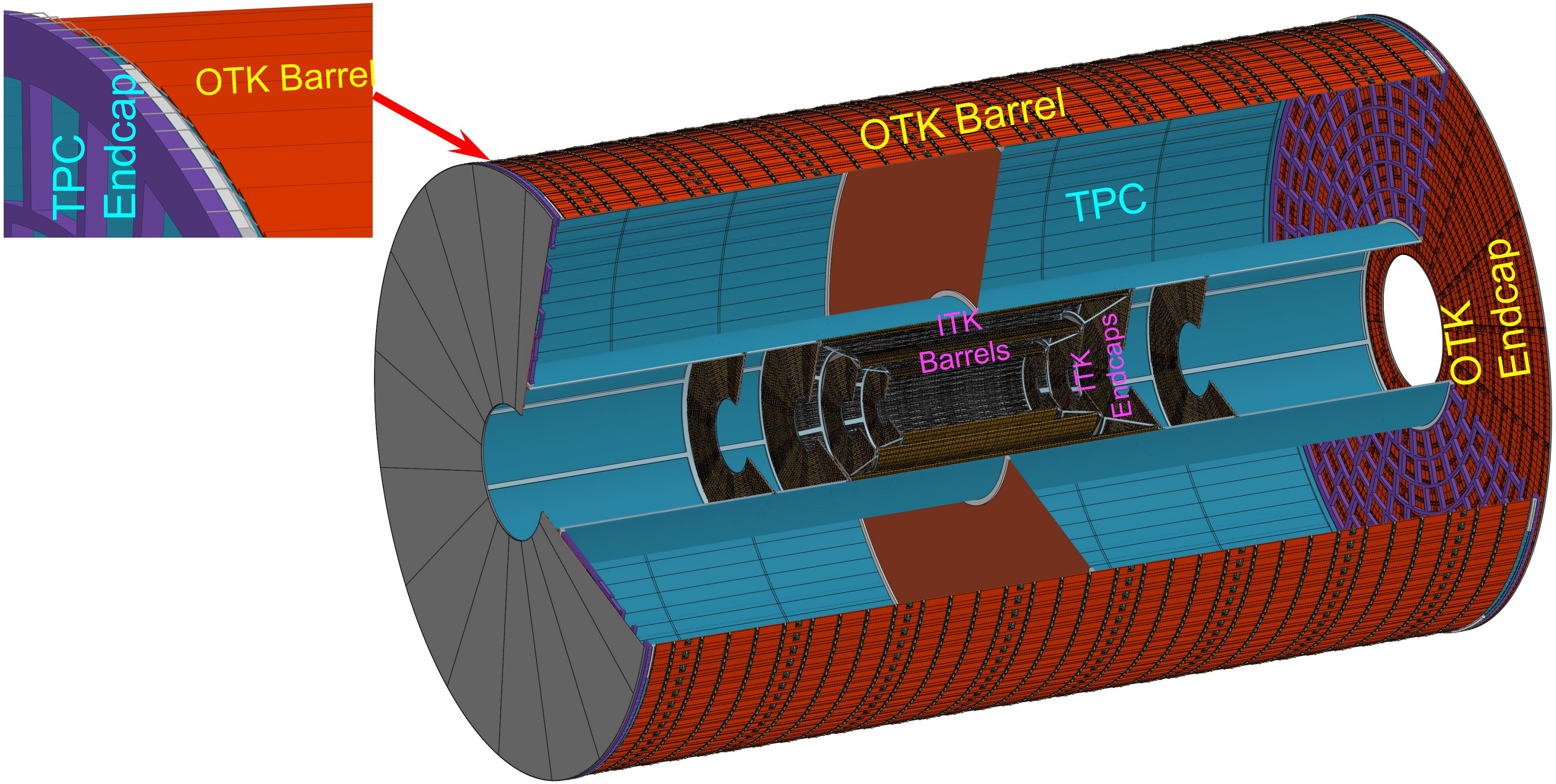


- → ITK cable and pipe
- → OTK cable and pipe
- → ITK & OTK cable and pipe

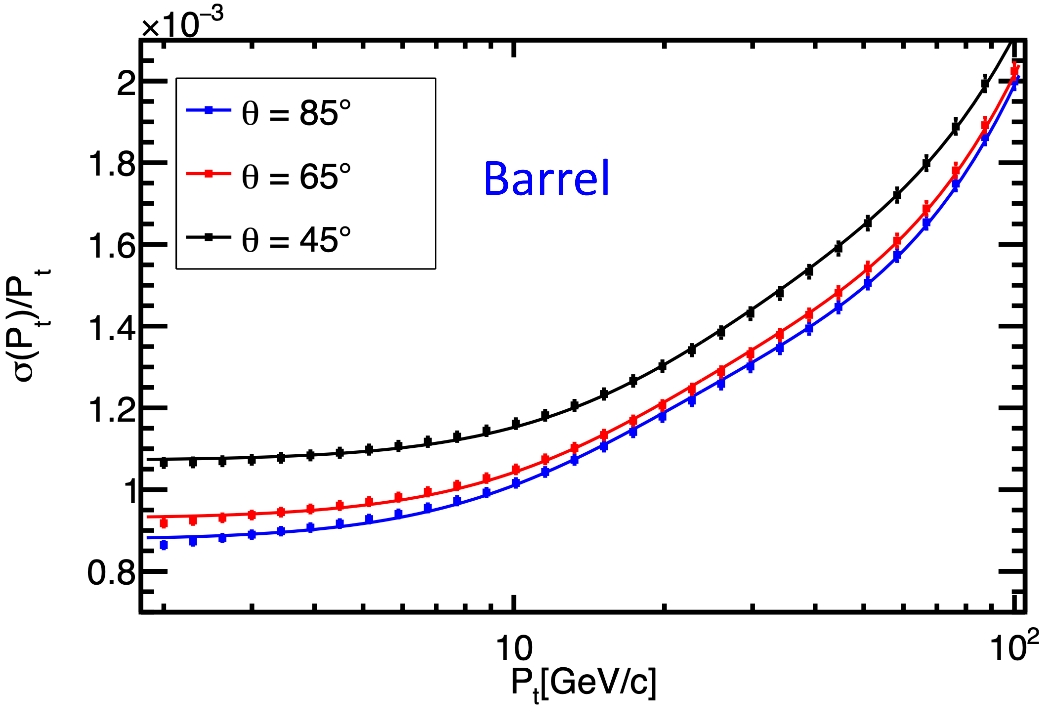
	Detector	Number of power cables (supply both LV & HV)	Number of optical fibers	Number of cooling pipes
ITK Barrel	ITKB1	44	308	88
	ITKB2	128	640	128
	ITKB3	204	1,428	204
ITK Endcap (Strips)	ITKE1	128	192	64
	ITKE2	160	288	64
	ITKE3	320	736	64
	ITKE4	256	608	64
OTK Barrel	OTKB	440	880	220
OTK Endcap	OTKE	544	544	Cooling plate
Total		2,224	5,624	



CEPC Silicon Tracker



Parameterization of CEPC Tracking Performance



Qi YAN and Gang LI’s formulae

Momentum resolution in the barrel region:

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}} = ap_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}} = as_1p_t \oplus \frac{bs_2}{\beta\sqrt{\sin\theta}}$$

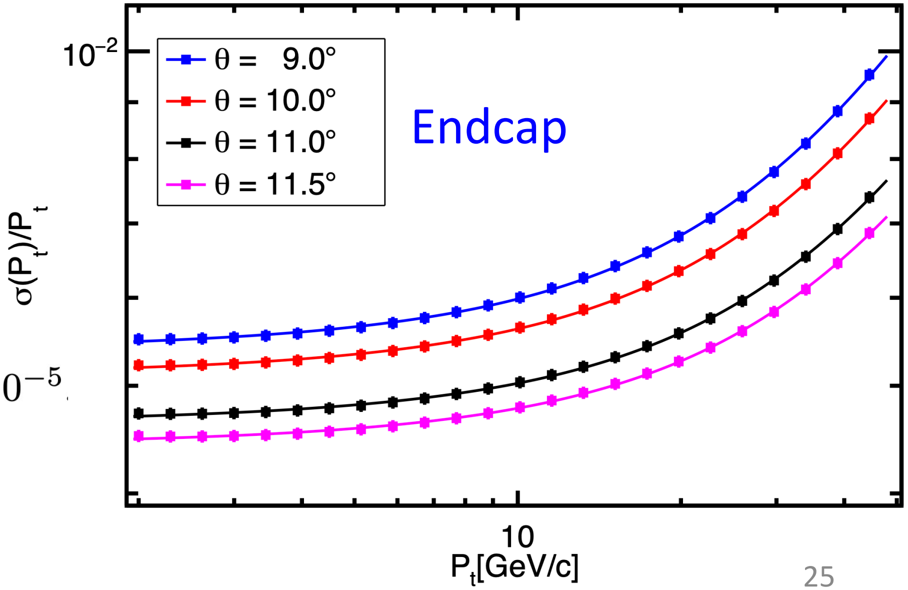
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{Si}}^{-2} + \left(\frac{\sigma_{p_t}}{p_t}\right)_{\mathrm{TPC}}^{-2}}}$$

where $a = 1.5 \times 10^{-5}$, $b = 1.4 \times 10^{-3}$, $s_1 \approx 6$, and $s_2 \approx 0.8$.

Momentum resolution in the endcap region:

$$\frac{\sigma_{p_t}}{p_t} = \frac{a'p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

where $a' \approx 0.4 \times 10^{-5}$, $b' \approx 0.9 \times 10^{-3}$, and $c' = 4.5 \times 10^{-5}$.



Progress on Silicon Tracker Ref-TRD

撰写负责人：李刚、严琪

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撰写负责人：李一鸣、周扬

撰写负责人：史欣

撰写负责人：严琪

撰写负责人：严雄波

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撰写负责人：赵梅、严雄波、严琪

撰写负责人：严琪、李一鸣

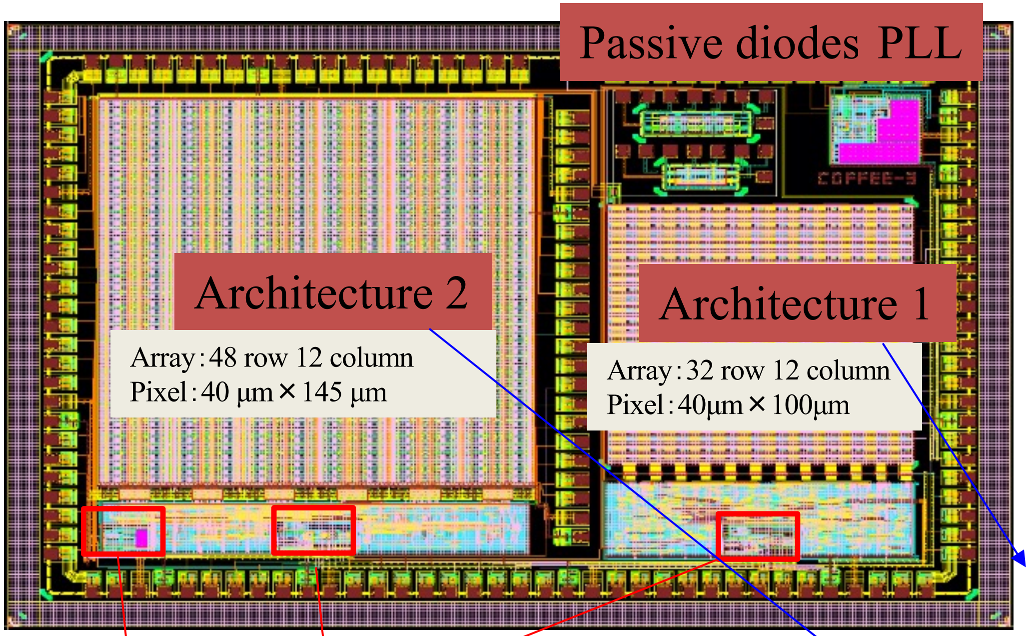
撰写负责人：李刚、严琪

>90% of the content has been completed, with the full chapter nearing 100 pages.

Progress on COFFEE3 Development and Submission

Submitted 2025.1/ expected received 2025.5

Provided by Yang ZHOU



Passive diodes PLL

Architecture 2

Array: 48 row 12 column
Pixel: 40 µm × 145 µm

Architecture 1

Array: 32 row 12 column
Pixel: 40µm × 100µm

DLL

LVDS driver/receiver up to 1.28Gb/s

- In-pixel electronics;
- Pix matrix readout strategy;
- Periphery digital logics and functional IPs;
- Slow control & Fast control….
- Data/Power/CLK interfaces……

……

Two readout architectures:

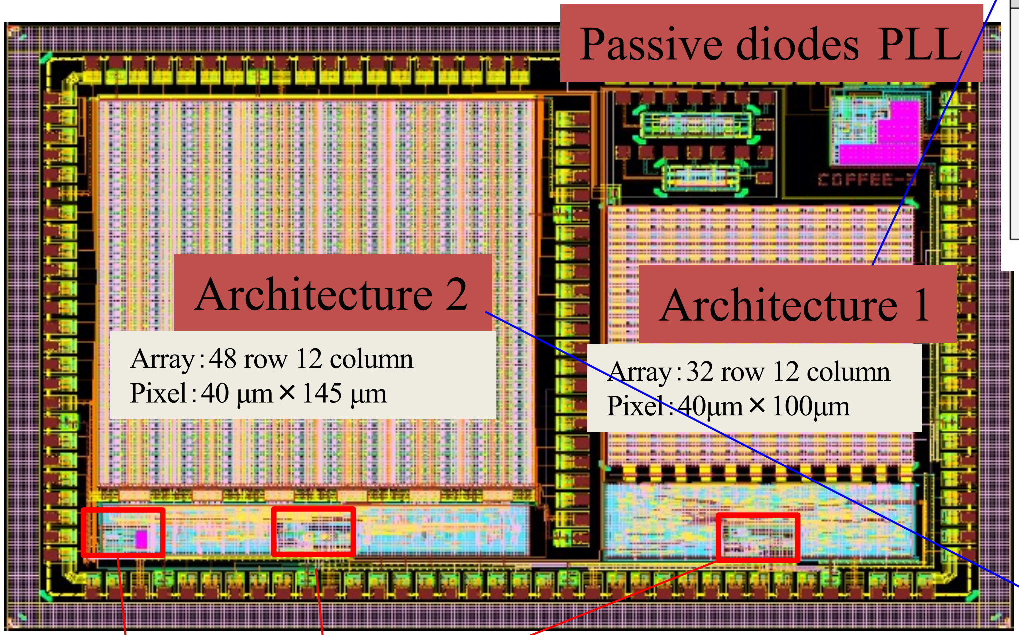
Both include nearly a complete ASIC readout framework, and the solution can be extended to a full-size chip.

Each pixel can independently adjust its threshold through SPI (4-bit in-pixel DAC) and configure the mask.

- **Architecture 1:** the optimized design framework based on current process conditions (Triple-well process);
- **Architecture 2:** an improved solution, while requires process modification. (Deep P-well required); fully utilize the advantages of the 55nm process node,.

Provided by Yang ZHOU

COFFEE3 architecture 2:



Passive diodes PLL

Architecture 2

Array: 48 row 12 column
Pixel: 40 µm × 145 µm

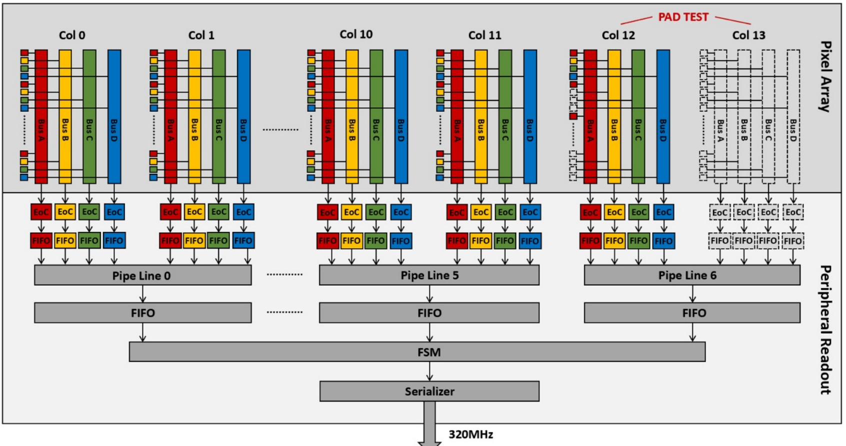
Architecture 1

Array: 32 row 12 column
Pixel: 40µm × 100µm

DLL

LVDS driver/receiver up to 1.28Gb/s

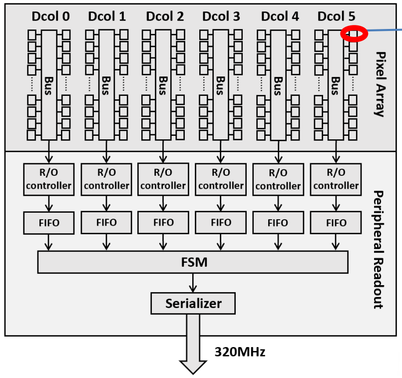
Architecture 1: NMOS Pixel Array Schematic Diagram

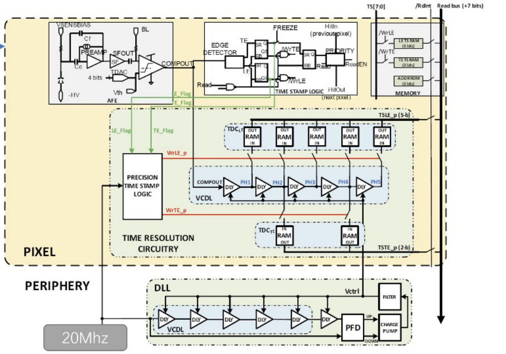


LVDS driver/receiver up to 1.28Gb/s

- In-pixel NMOS based comparator, in-pixel 4-bit DAC for threshold tuning;
- Time information（TOA, TOT…）and data formation in the end of each column;
- Improved capability to manage high incident conditions;

Architecture 2: an improved solution, fully utilize the advantages of the 55 nm process node





LVDS driver/receiver up to 1.28Gb/s

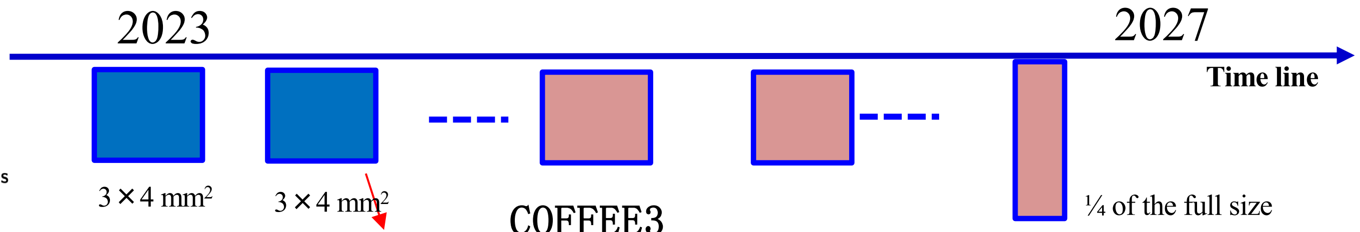
- In-pixel Coarse-fine TDC and 4-bit threshold tuning;
- ToA and ToT information are saved in each pixel;
- Data-driven readout;

Prototypes in 55 nm HV-CMOS Process

Several MPWs to reach the full-size full-function sensor

COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS



2023

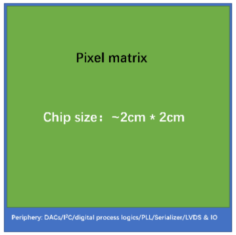
2027

Time line

3×4 mm²

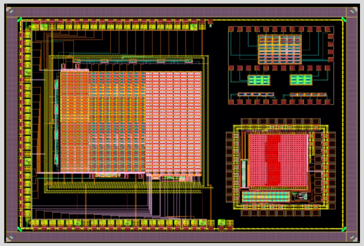
3×4 mm²

¼ of the full size

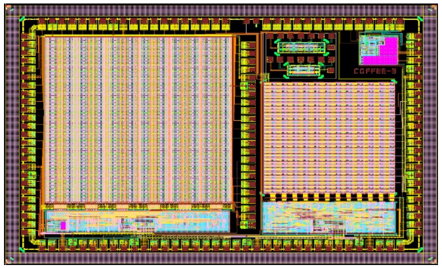


HV process

COFFEE2



COFFEE3



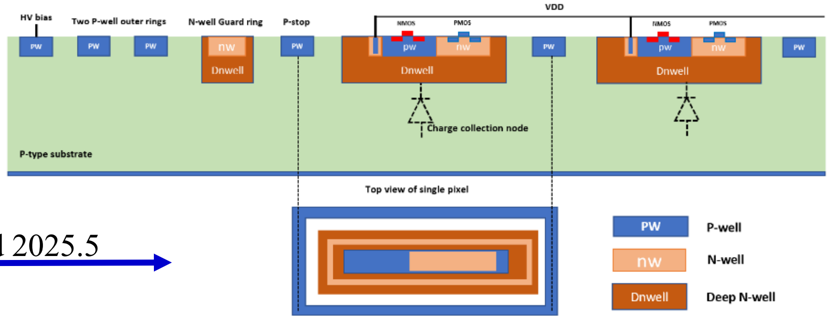
Submitted 2023.8/received 2023.12

Submitted 2025.1/ expected received 2025.5

Process characteristics & Technology validation

- In-pixel electronics;
- Pix matrix readout strategy;
- Periphery digital logics and functional IPs;
- Slow control & Fast control….
- Data/Power/CLK interfaces……

……



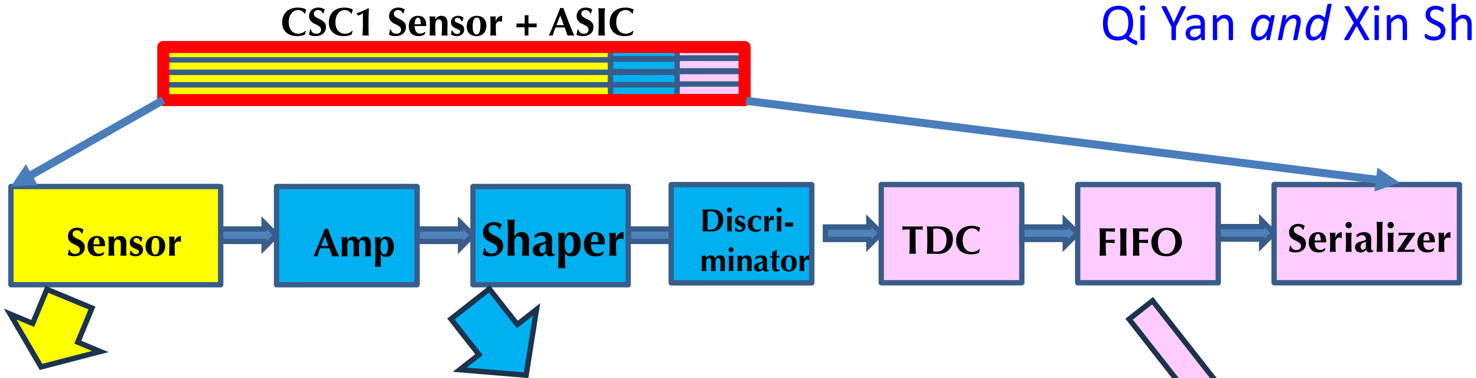
HV-CMOS process cross-section diagram showing the guard ring and pixel structure.

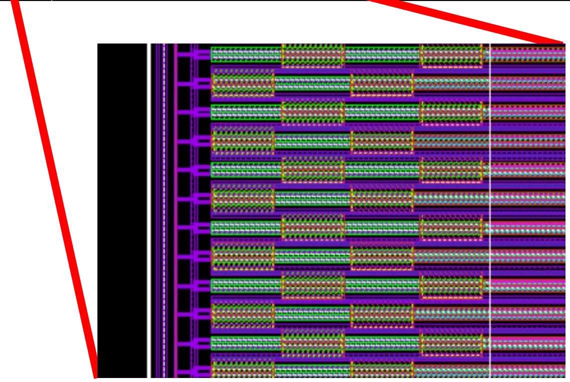
COFFEE3芯片设计团队：15 designers

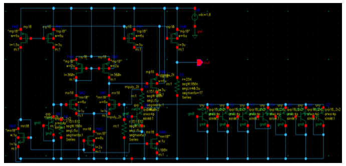
- **高能所：**李乐怡（山东大学/高能所）、张晓旭（南京大学/高能所）、赵梅、陆卫国、周扬；
- **西北工业大学：**吴慧敏、赵泽煊、赵宇、魏政、魏晓敏；
- **浙江大学：**邓建鹏、李鹏戌；
- **大连民族大学：**陈洋、王雨颉、施展；

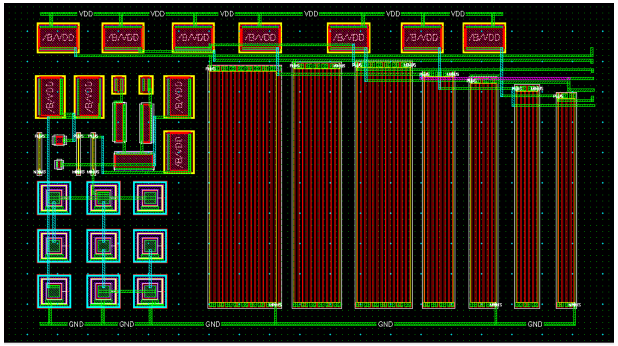
Progress on CMOS Strip Chip (CSC1) Development

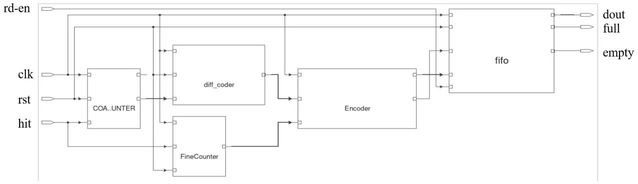
Qi Yan *and* Xin Shi

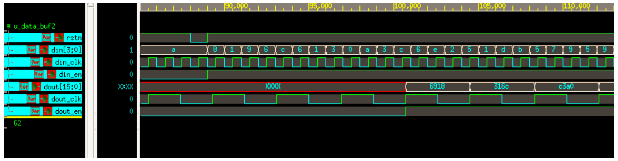






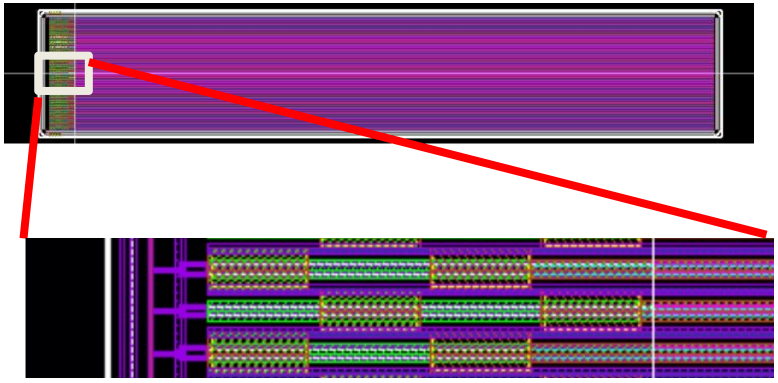


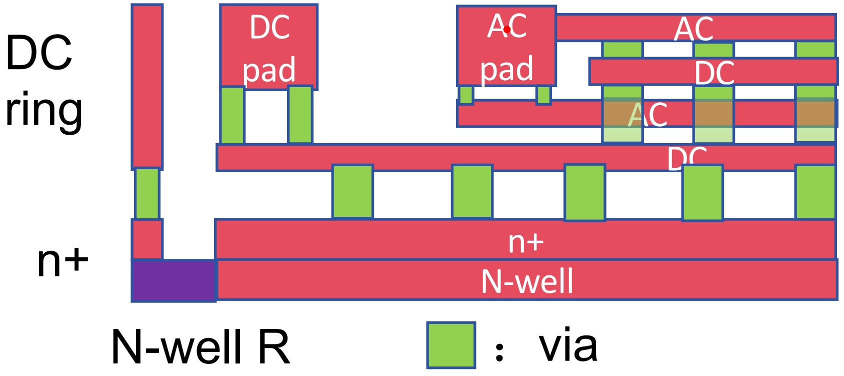


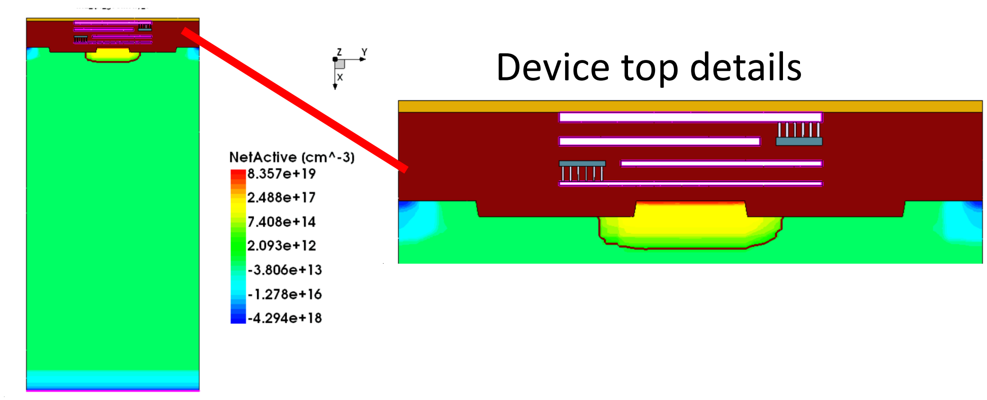


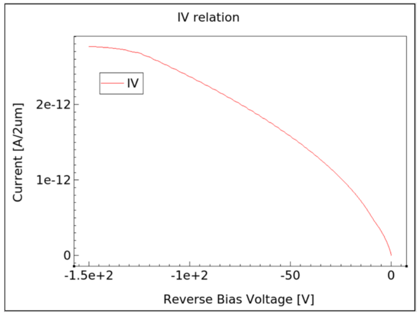
CMOS Strip Sensor Design and Simulation

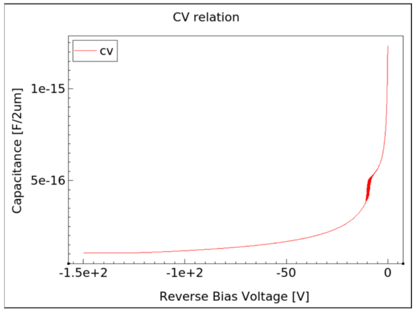
- Foundry: CSMC CMOS (1P4M)
- Sensor Size: 20.000 mm × 3.486 mm
- Strip length: 19.716 mm, pitch 75.5 µm
  - n-well:18 µm, n+: 15 µm
  - p-well: 4 µm, p+: 2 µm
- pad area: 75 µm × 180 µm
- Number of channels: 40
- n-well to bias ring via well-resister
- Two n+ guard rings
- Doping concentration









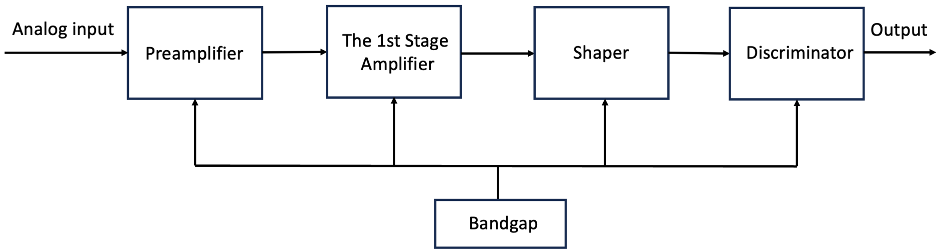


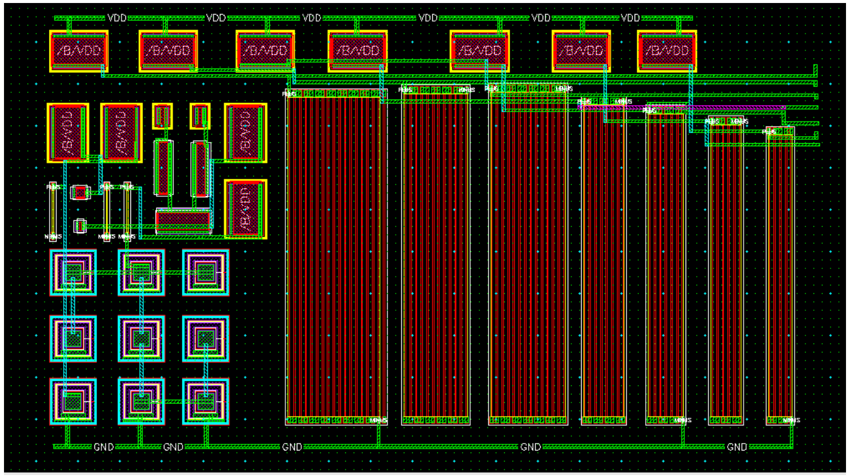
IV/CV results consistent with existing data*

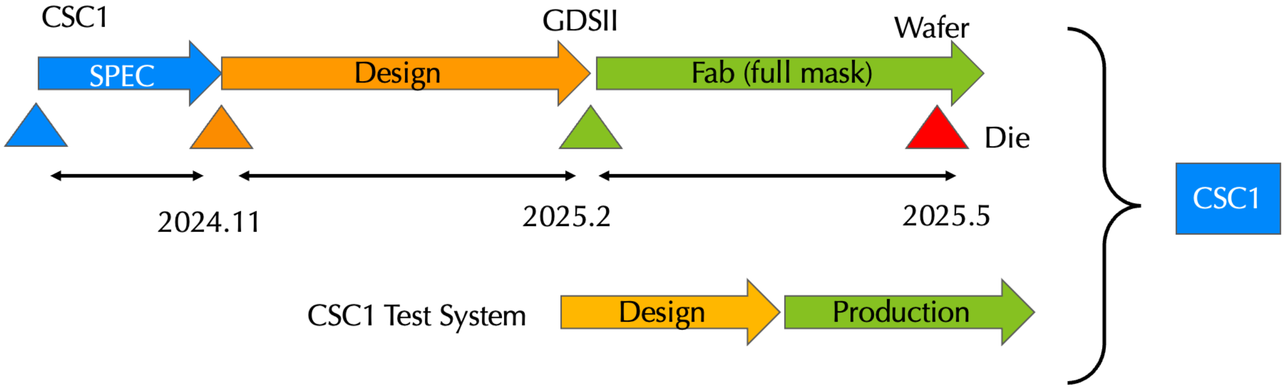
* Diehl et. al, Characterization of passive CMOS strip sensors, NIMA 1033 (2022) 166671

Analog Frontend Design Status and CSC1 Submission

- Completed the design of Analog Frontend (AFE): Preamplifier, the 1st stage amplifier, shaper, discriminator, and bandgap.
  - Circuit design, layout design, pre-simulation, and post-simulation
- Completed the overall Design Rule Checking (DRC), Layout Versus Schematics (LVS) checks.







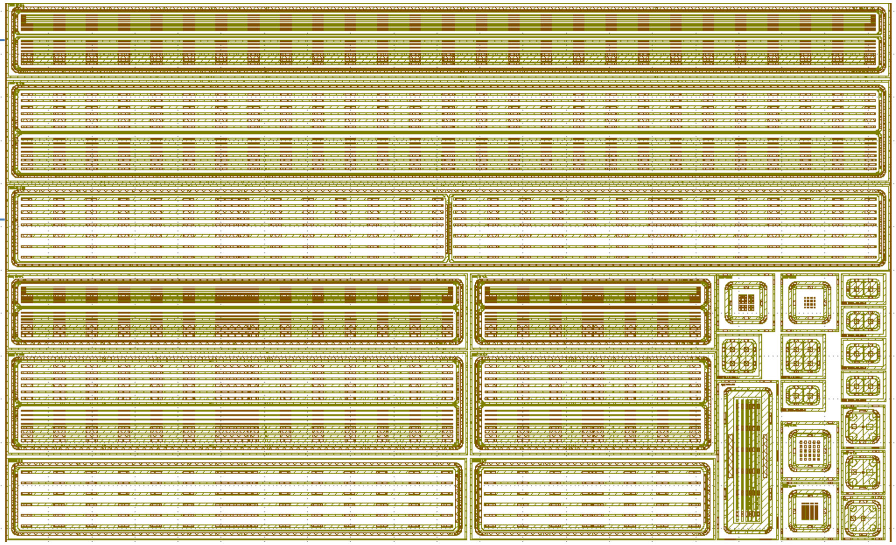
- Working on the TDC
- Target for submission by February

AC-LGAD Strip Sensor New R&D Design

New layout and design was done based on simulation. IHEP new AC-LGAD strip sensor prototype design for the CEPC OTK&TOF:

- Strip length： 1 cm, 2 cm, and 4 cm
- Strip pitch size: 100 µm, 200 µm, and 500 µm
- Optimized isolated structure design to reduce sensor capacitance
- Process design optimized for better spatial resolution (n+ layer dose)

Designed by Mei Zhao

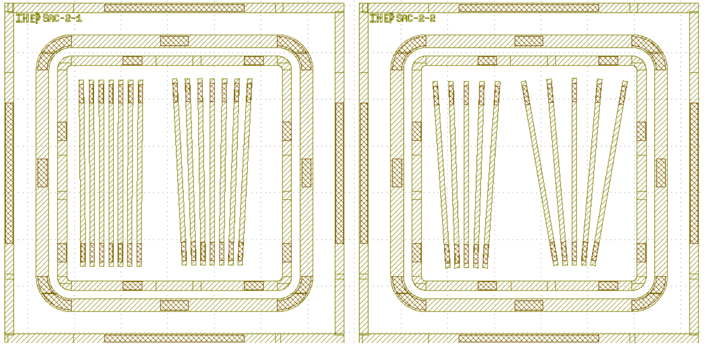


4cm AC-LGAD

2cm AC-LGAD

1cm AC-LGAD

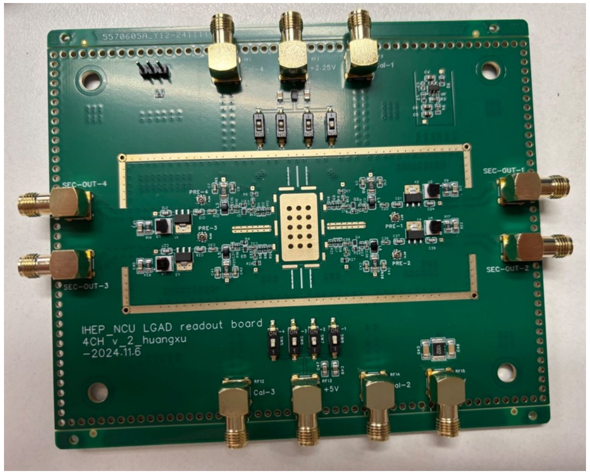
Sector shape AC-LGAD for endcap



AC-LGAD Sensor Readout Board Preparation

Mei Zhao

- 4-channels readout boards has been fabricated for AC-LGAD testing
- 2-stage amplifiers, Gain~70
- Signal shape has significantly improved, showing no oscillations.



Measure	P1:min(C2)	P2:max(C2)	P3:median(C2)	P4:ovsh+(C2)
value	-105.6 mV	21.9 mV	1.10 mV	—
mean	-102.218 mV	20.967 mV	1.3267 mV	—
min	-110.5 mV	14.3 mV	682 µV	—
max	-96.6 mV	26.1 mV	1.91 mV	—
sdev	1.690 mV	1.499 mV	161.5 µV	—
num	2.385e+3	2.385e+3	2.385e+3	0
status	✓	✓	✓	✗

AC-LGAD Strip Sensor Development Plan

Short term plan: 2024.12-2025.2

Simulation: ongoing

- Simulation of Strip length and its effect (signal shape)
- Simulation to reduce capacitance (isolation structure)
- Simulation of process parameters to optimize spatial resolution (AC coupling capacitor, n+ dose)

Testing:

- Multi-channel readout board with low noise design and fabrication (2 stages of amplifier) **done**
- Testing of short strip connected, radiation testing(TID) **ongoing**

Submission 1: 2025.2 (layout design is done, process simulation ongoing)

Strip AC-LGAD with different length and pad-pitch size: [1 cm, 2 cm, 4 cm] [100um, 200 um, 500 um]

- Strip AC-LGAD with different process parameters: n+ dose, dielectric material and thickness, …
- Strip AC-LGAD with different isolation structure →Capacitance
- Sensors with EPI layer of different thickness (50 um, 65 um, 80 um, 300 um)

Sensor Testing:

- clarify the sensors performance and requirement (include test beam and radiation test)
- Find out how to optimize the sensor performance (structure and process)

Submission 2: 2025.10

- Based on the results from first version and more simulation
- Sensors with strip length ~4cm

Sensor Testing: basic properties and test together with ASIC and BEE

Submission 3: 2026.6

- large area sensor design and fabrication

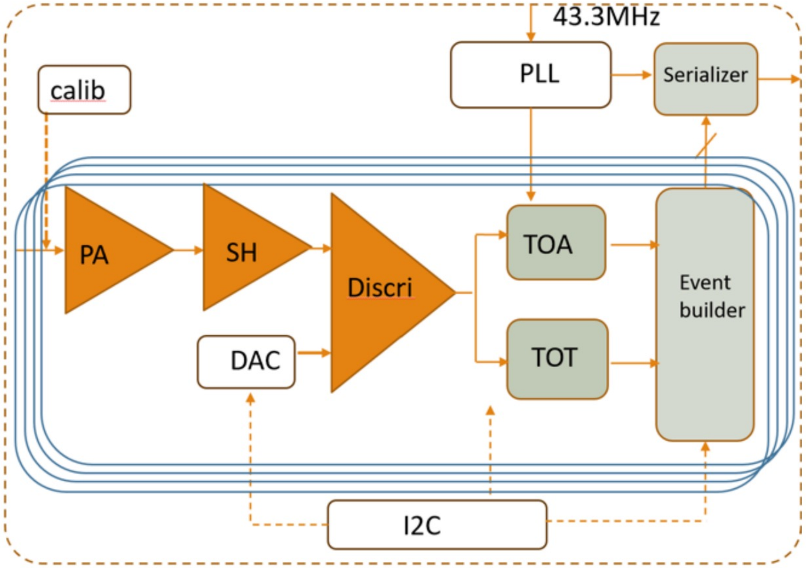
Submission 4 if needed: 2027.2

- module: built sensor + ASIC module and test

OTK AC-LGAD Readout ASIC (JuLoong, 烛龙)

Xiongbo YAN

- Functions:
  - TOA (Time of arrival) for precise time and TOT (Time over threshold) for time walk correction and accurate position determination.
  - Each channel includes preamplifier, discriminator, and Time-to-Digital Converter (TDC).
- Requirements:
  - 128 channels, channel pitch less than 100 µm.
  - Single channel power consumption less than 20 mW.
  - Time resolution for TOA better than 30 ps.



JuLoong diagram

OTK AC-LGAD ASIC Development Progress

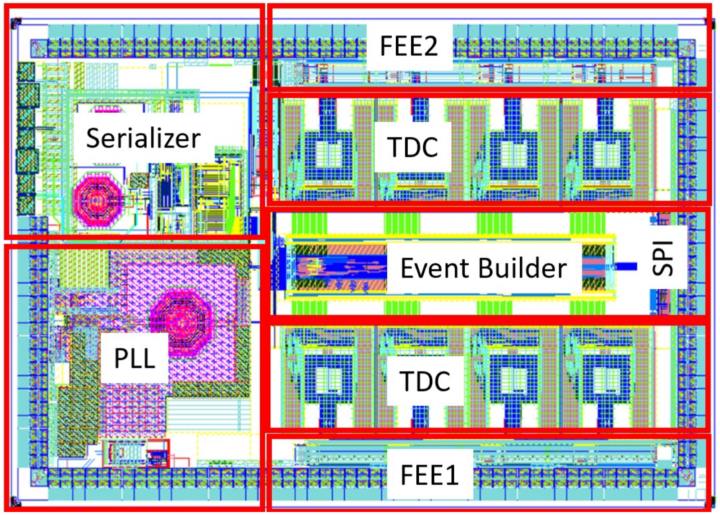
Xiongbo YAN

Several key cells are designed or verified:

- FPMROC (10 ps) chip
  - FEE: Preamplifier+Discriminator

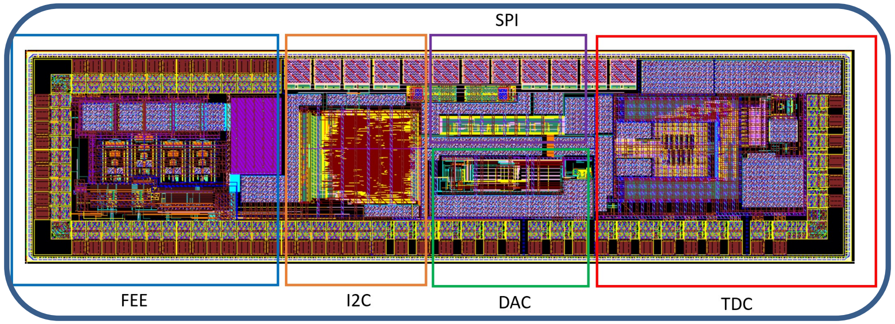
    jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF

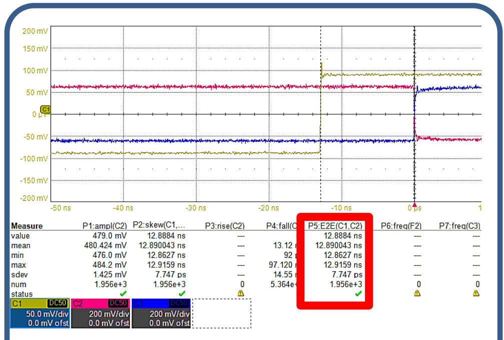
    (need to be test with real LGAD sensor)
  - TDC core needs a new design
  - PLL, Serializer, SPI is verified but need to be simplified



FPMROC

- I2C Slave: ASIC parameter configuration
- 12-bit DAC: threshold and calibration

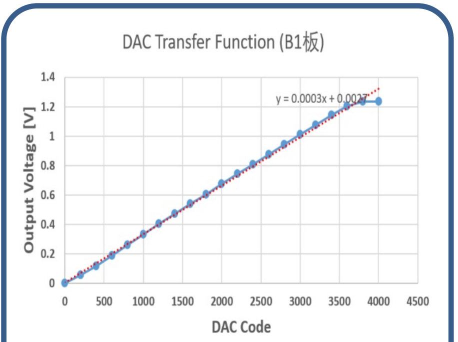




Measure	P1:ampl(C2)	P2:skew(C1,...	P3:rise(C2)	P4:fall(C	P5:E2E(C1,C2)	P6:freq(F2)	P7:freq(C3)
value	479.0 mV	12.8884 ns	---		12.8884 ns	---	---
mean	480.424 mV	12.890043 ns	---	13.12	12.890043 ns	---	---
min	476.0 mV	12.8627 ns	---	92	12.8627 ns	---	---
max	484.2 mV	12.9159 ns	---	97.120	12.9159 ns	---	---
sdev	1.425 mV	7.747 ps	---	14.55	7.747 ps	---	---
num	1.956e+3	1.956e+3	0	5.364e+	1.956e+3	0	0
status	✓	✓	⚠		✓	⚠	⚠

C1 DC50 50.0 mV/div 0.0 mV ofst
C2 DC50 200 mV/div 0.0 mV ofst
C3 DC50 200 mV/div 0.0 mV ofst

FEE test result

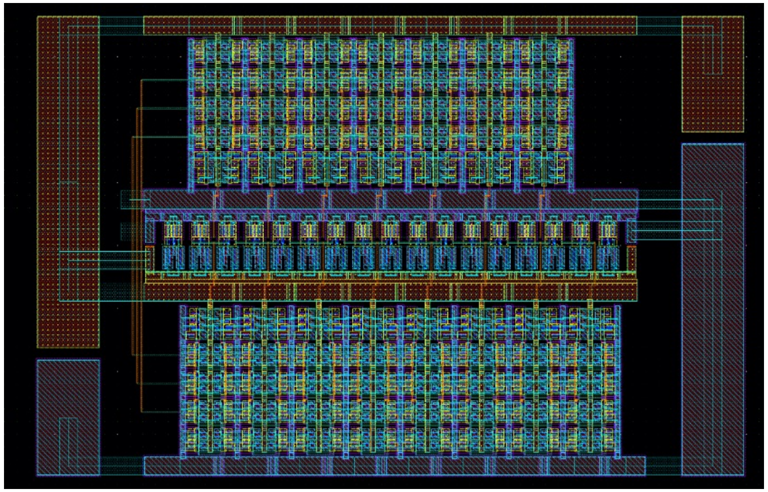


DAC test result

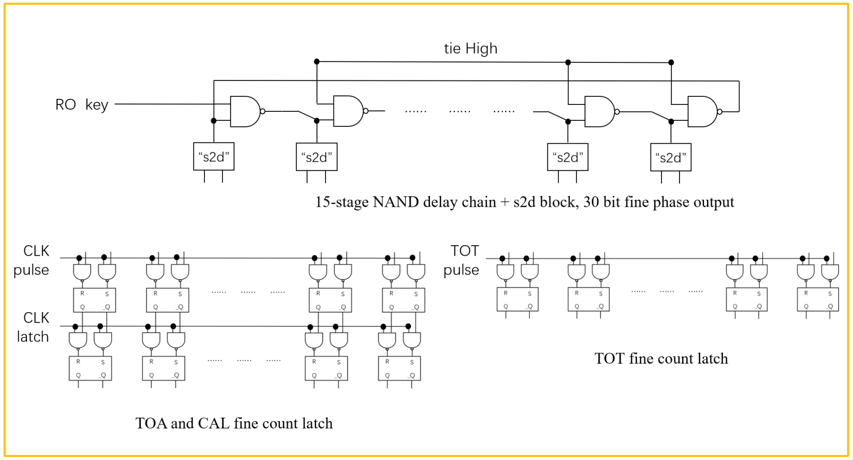
OTK AC-LGAD TDC Core Design

Xiongbo YAN

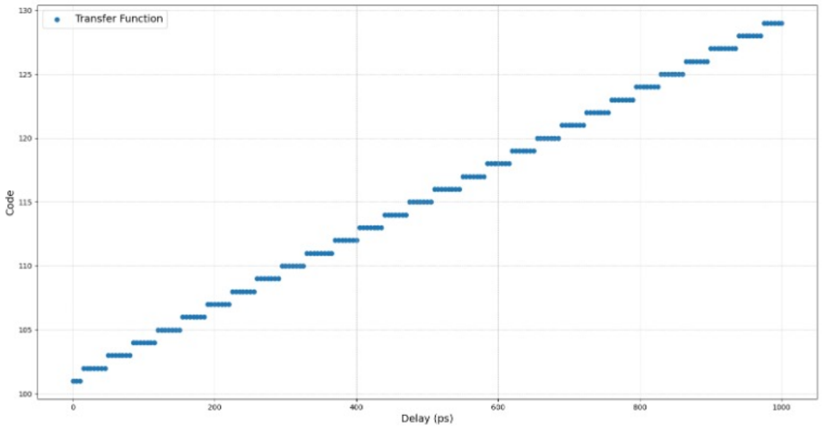
- Event driven delay line to reduce the power
- Real time Calibration for PVT (Process, Voltage, Temperature)
- LSB ~36 ps for preliminary layout post-simulation
- Power Consumption：
  - Average current for single event: 443 μA
  - Static current: < 5μA



Delay line layout



Single-Channel Delay Chain and Quantization Block Diagram



TOA transfer function curve (step=5 ps, TT27)

OTK AC-LGAD ASIC (JuLoong) Development Plan

- 2025.4: Design key components, including preamplifier, discriminator, and TDC, along with the design of the ASIC test system. Performance testing of the ASIC will be conducted by the end of the year, with radiation hardness testing for each component.
- 2025.7: Conduct components performance test.
- 2025.10: Refine components and complete the first version of multi-channel integration.
- 2026. 2: Performance test on the multi-channel ASIC, including radiation hardness testing.
- 2026. 6: Further refinement and integration of 128 channels.
- 2027.10: Performance testing of 128 channel ASIC will be conducted, integrated with LGAD sensor.
- 2027.12: Finalize the prototype and prepare for mass production of the chips.

Summary

- Our silicon tracker group is steadily progressing towards the Ref-TDR.
- We greatly appreciate the mechanical and thermal support from Xuedong Wu and his group at Zhengzhou University of Light Industry (郑州轻工业大学).
- After the Ref-TDR, we will focus on R&D efforts, including all sensor technologies and the supporting components, such as mechanical and thermal R&D.
- In parallel, I, along with the group members, will make significant efforts to strengthen our connections with research units and industries, including semiconductor foundries, to advance the R&D work.

5.4.5.4 Summary

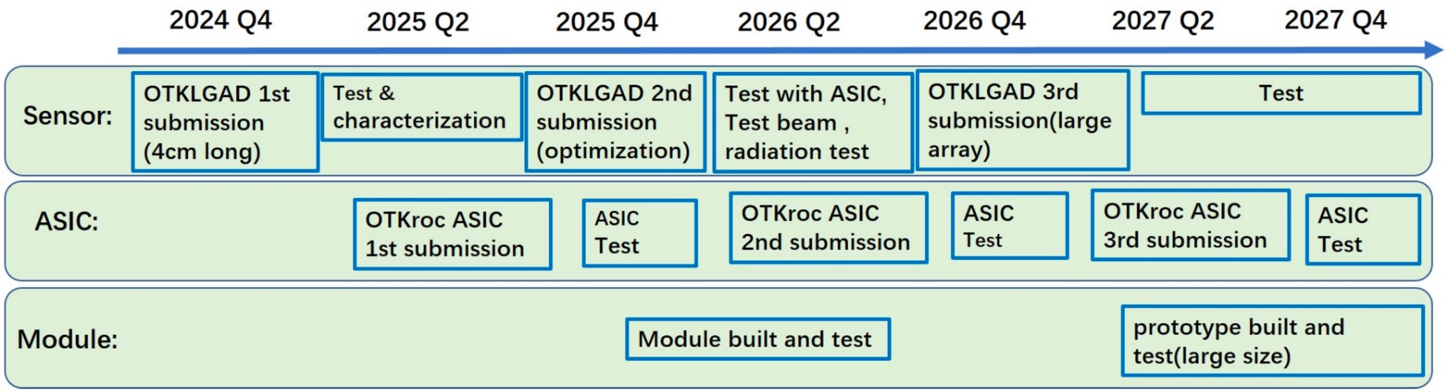


Figure 5.106: Timeline for OTK, including sensor, ASIC, mechanics and so on

All the R&D mentioned above is part of a 3-year plan, as detailed in Fig. 5.106. Considering the project timeline of more than 5 years from construction, the CEPC project is flexible enough to adjust its technical approach and has sufficient backup plans for the engineering phase. For example, if the performance of the AC-LGAD strip sensor degrades significantly for large-dimension strip sensor, we may consider using conventional large-dimension sensor, with or without an external time-of-flight detector, or opt for bump bonding or monolithic AC-LGAD technology if it becomes mature.

For the OTK system, including sensor, readout ASIC, and mechanical and cooling components, we are open to both domestic collaborations with research units and industry as well as international partnerships. In light of all these factors, we are confident in delivering a high performance OTK system that meets the physics requirements in a timely manner.