

The DarkSide-20k Dark Matter Detector: Physics Goals and Data Acquisition

Marek Walczak

21-10-2025



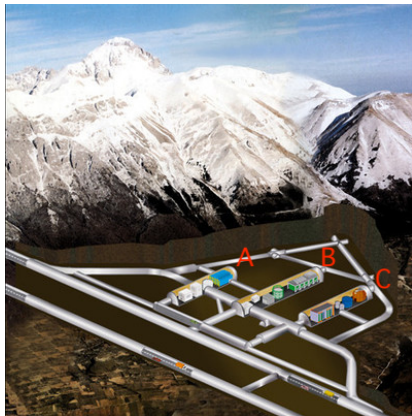
Laboratori Nazionali del Gran Sasso (LNGS)



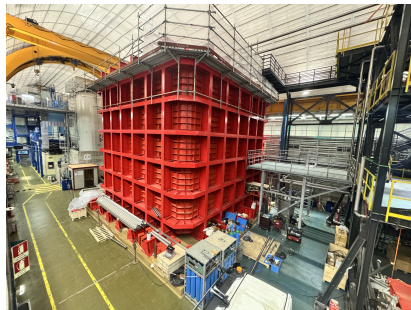
- founded in 1987
- covered by 1400 m of rock (3800 mwe shielding)
- can be accessed by car
- one of largest underground research centers (there are around 16 deep underground labs in the world)



- Abruzzo region in central Italy, 120 km from Rome
- below Gran Sasso mountain in Italy

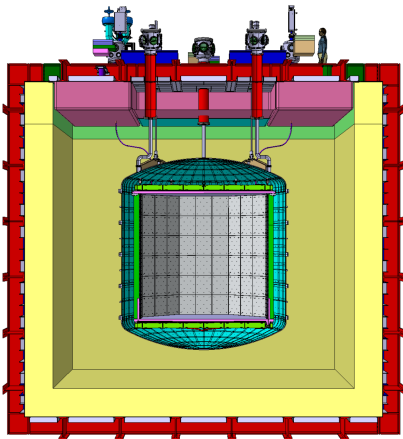


- DarkSide-20k will be installed in LNGS in Hall-C



- construction: 2022 - 2028
- nominal duration of operation: 10 years

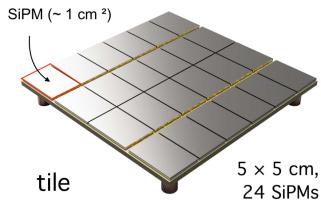
DarkSide-20k overview



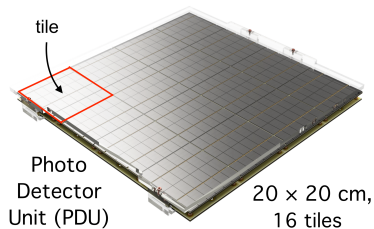
more details in Ako's talk!

- Time Projection Chamber (TPC) filled with 50 t of underground Ar (UAr) (20 t fiducial)
- Inner Veto (IV): 36 t of UAr between the TPC and the vessel (neutron tagging)
- Outer Veto (OV) filled with 650 t of atmospheric Ar (AAr) (muons and their shower products)
- WLS: TPB coating in TPC, PolyEthylene Naphthalate (PEN) foils in the veto

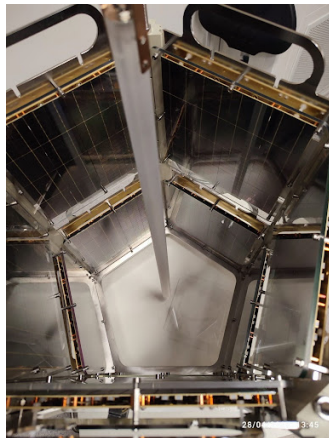
Light detection



one channel: 4 tiles



more details in Dmitrii's and Devidutta's talks!



10 veto PDUs prepared for cryogenic test

Custom silicon photomultipliers (SiPM)

- Low noise at **88 K**
- Tuned sensitivity vs light spectrum
- **SNR** for single tile **> 13**
- Photon detection efficiency: 45%
 - scintillation signal is mostly single photoelectron
- Timing resolution: 10 ns
 - important for bkg rejection (**see Ako's talk**)
- **Dark-count rate**: few-tens mHz/mm²
 - may spoil **PSD** / contribute to DAQ dead time
- 26 m² overall

Readout channels:

	PDUs	channels
TPC	528	2112
IV	120	480
OV	30	120
total	678	2712

Expected event rate in the Inner Detector (ID: TPC and IV): **200 evnt. / sec** (100 evnt. / sec in the TPC)

To reduce possible sources of bias, the DAQ:

- continuously acquires signals from the TPC and vetos (**triggerless operation**),
 - system doesn't wait for the trigger decision,
- the waveforms are digitized and transferred for further processing,
- analysis of the signals for physics searches delegated to a computing farm.
- DAQ system is also **capable of running in trigger mode** if there is a need.

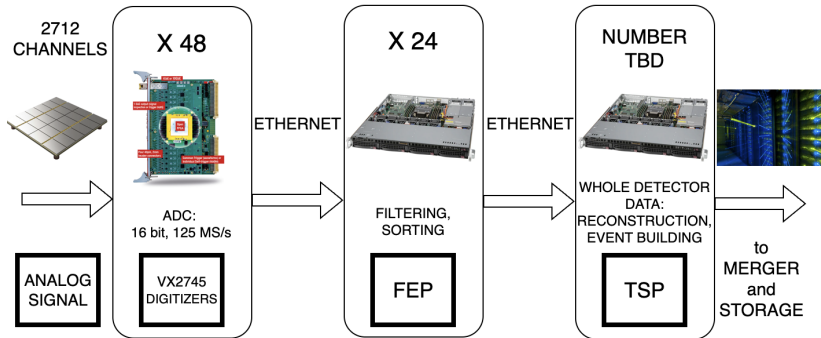
4 **identical racks**, each having:

- 12 **waveform digitizers** receive analog data from PDUs
 - (48 in total)

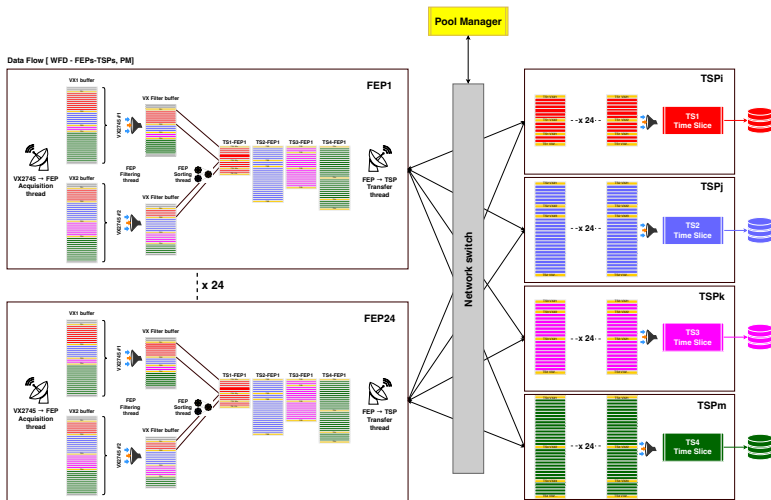
Additional racks in IT room:

- 24 **Fron End Processors (FEPs) machines**
 - (1 per 2 digitizers)
 - readout, filtering, sorting
- **Time Slice Processors (TSPs) machines**
 - number under discussion
 - receive sorted data from FEPs
 - analysis, sending data for storage

Data Flow (simplified)

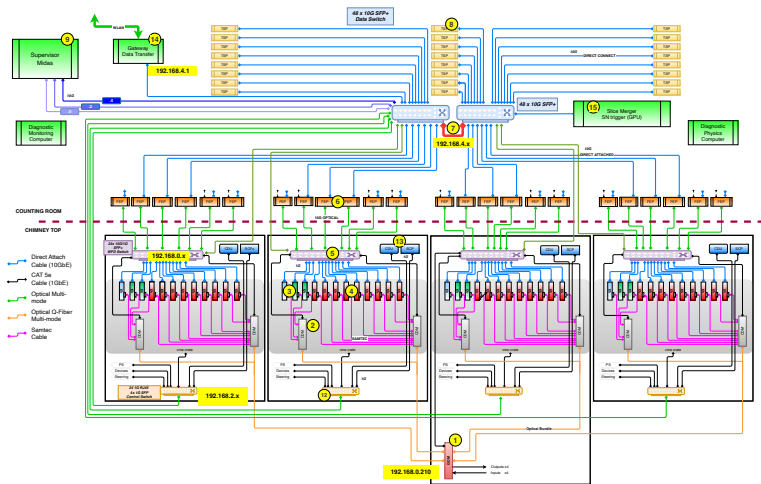


Data Flow



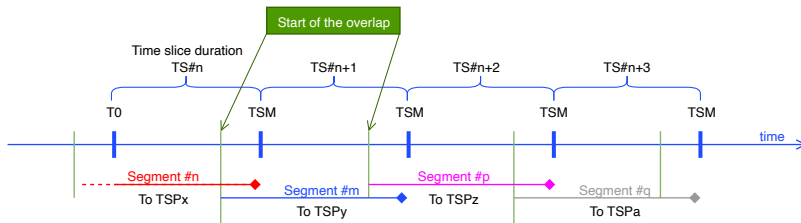
Digitized data is read by **FEPs**, sorted, processed and transferred to the **TSPs** for further processing -> storage

DS-20k DAQ architecture

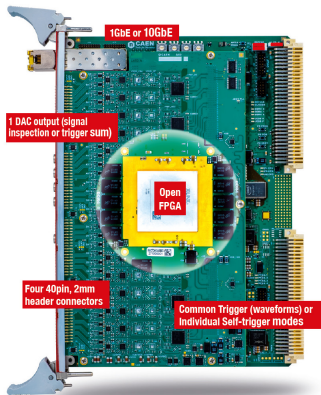


Global / Crate Data Manager (G/CDM, 1, 2), Digitizers (3, 4), network switches (5, 7,12), FEPs (6), TSPs (8), Midas Supervisor (9), Slow Control processors (SCP, 13), Getaway (14) and Merger (15)

Time Slice concept

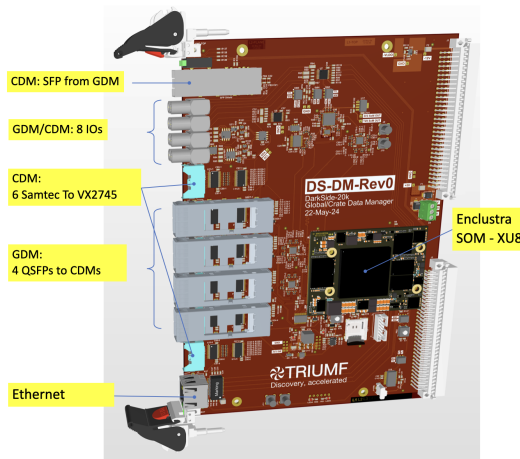


- data written to disk after the signals from the whole detector are gathered as a Time Slice (TS)
- each TS is assigned to a dedicated TSP
- part of TS is duplicated to include boundary events

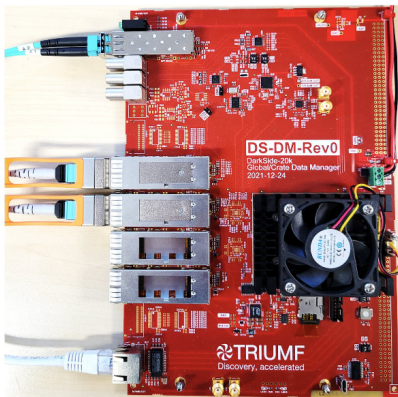


- 16 bit @ 125 MS/s ADC
- 64 analog inputs, differential
- programmable gain, $4 V_{pp} \div 0.04 V_{pp}$
- Open FPGA - allows custom firmware implementation:
- FW: identify segments containing at least one "peak"
- uses Finite Impulse Response (FIR) filter

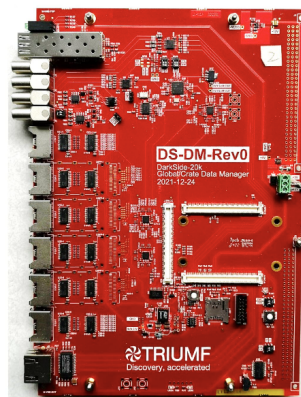
Global / Crate Data Manager board



Data Manager boards ensure clock distribution and segment assembly



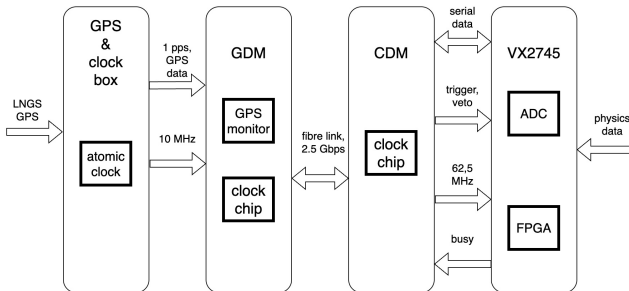
Global Data Manager
(GDM)



Crate Data Manager
(CDM)

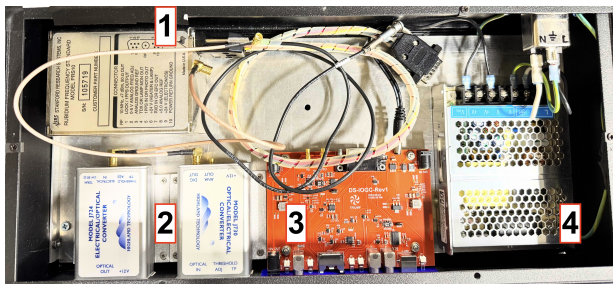
I/Os	Specification	Purpose
1 RJ45 port	1Gbit Ethernet	Configuration
4 QSFP+	2.5Gb/s communication to CDM	Clock Trigger
4 NIM inputs	IRIG-B, 10MHz Ref clock, Ext TrgIN-1, Ext TrgIN-II	GPS, Triggers
4 NIM outputs	1PPS, Ext TrgOUT-1	GPS, Trigger

GPS signal decoded in GDM

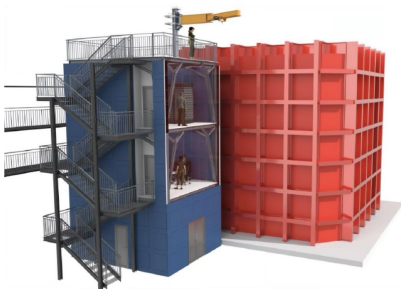


- atomic clock runs from GPS receiver 1 pps signal
 - provides 10MHz ext. clock to GDM.
- GPS irig-b datestamp is decoded in GDM

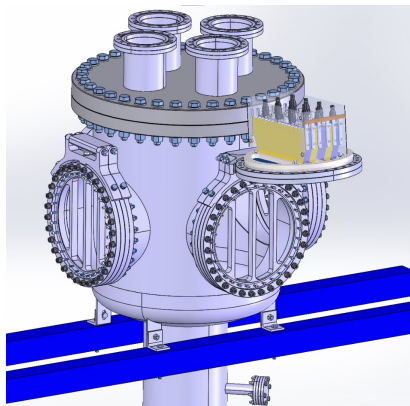
Atomic clock



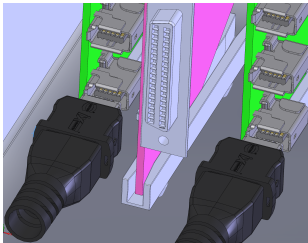
- Stanford Research Sytem PRS10 Rubidium clock (1),
- optical/electrical and electrical/optical converters (2),
- custom input-output GPS Clock board (IOGC, 3) developed in TRIUMF,
- power supply (4)



- IT rooms in Hall-C
- 8 chimneys on the rooftop of the cryostat:
 - 4 for ID, 4 for OV



- ID chimney: 4 flanges
 - steering, PDU ID, LV, HV, signal
- 640 channels per ID chimney

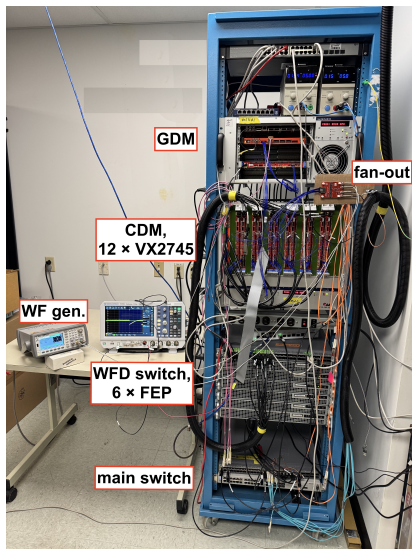


Ethernet IX Industrial Connector



Tests: Vacuum, Lightproof, Cross talk

Quadrant setup in TRIUMF, Canada



Quadrant setup:

- one of four identical racks of the final system
- 12 waveform digitizers (WFDs)
- 6 FrontEnd Processors (FEPs)
- 2 network switches
- Time Slice Processors (TSPs) (located in a separate rack in next room)

synchronization test - waveform generator signal

12 ch. connected to single digitizer

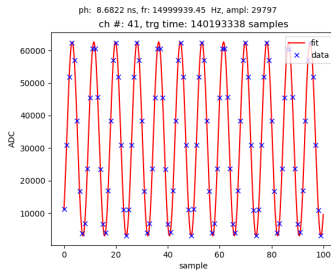
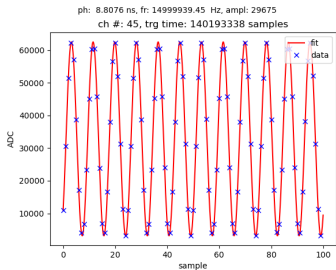
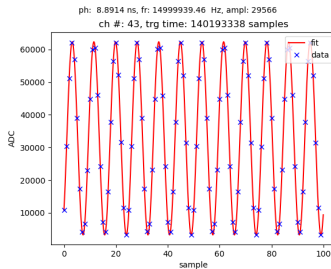
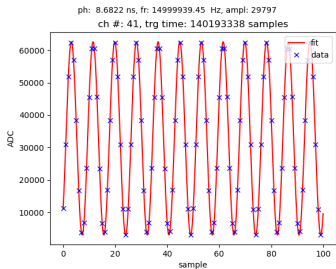


one channel per VX

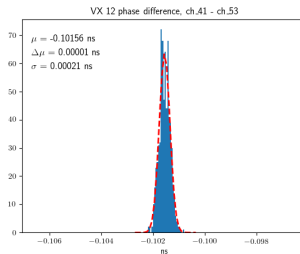
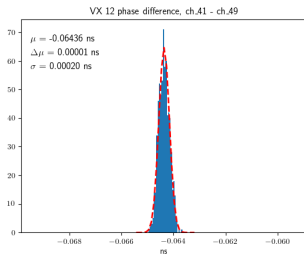
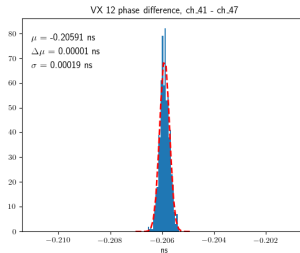
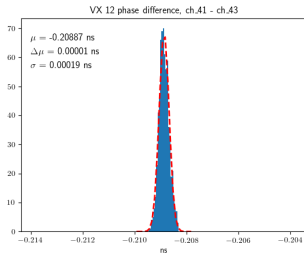


- WG: sine,
- 15 MHz,
- 150 mVpp
- CDM trigger: 50 Hz
- DAQ: 16k samples, 8k events (WFs)

only 100 first samples shown here



phase difference (single digitizer shown here)



result: phase shift between channels is **below 500 ps**

data rate & stability tests of the Quadrant system

Data: simultaneous trigger on all 768 channels (i.e. the worst case scenario)

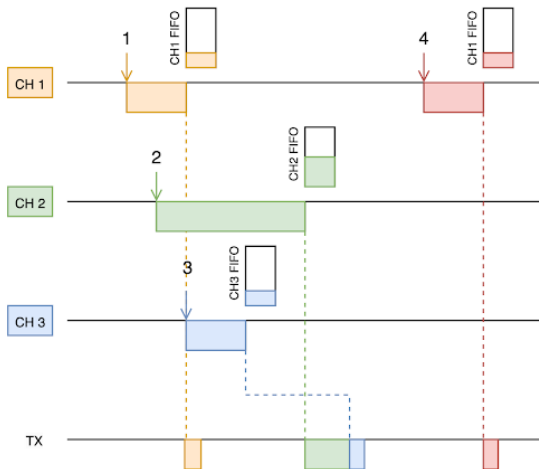
- Data rate 250 MB/s per board (VX -> FEP)
- FEP -> TSP rates are 8 MB/s per FEP
- Hardware is stable, can run for days - 1 week run completed

Run Status				
Run 1609	Start: Tue May 27 15:40:55 2025		Running time: 0h05m19s	
Running (Stop: /break)	Alarm(s):	Restart: Off	Data dir: /data/vision	
174838936 15:45:16.934 2025/05/27 [FEP_004,00A0K] [log_slave.coc:763]acquiredata_event_fepv_board,00A0K] Possible data loss! Board 0 now regular data with timestamp 257.002143s, but most recent slice (257) should have range 256.001650s to 257.001650s! Creating 1 file time-slice-marker.				
Equipment				
Equipment +	Status	Events	Events(/s)	Data[MB/s]
GMN	CC-0k OFF-0k V0-0k	95816	280.0	0.016
COM00	CC-0k OFF-0k V0-0k	95825	280.0	0.018
COM01	CC-0k OFF-0k V0-0k	0	0.0	0.000
VMEP001	Main ch. Output Off	0	0.0	0.000
VMEP002	Off	0	0.0	0.000
FEP_001	Sent slice 305, last slice size 6.094MB	0	0.0	0.000
FEP_002	Sent slice 304, last slice size 5.624MB	0	0.0	0.000
FEP_003	Sent slice 304, last slice size 5.644MB	0	0.0	0.000
FEP_004	Sent slice 304, last slice size 5.704MB	0	0.0	0.000
FEP_005	Sent slice 303, last slice size 5.834MB	0	0.0	0.000
FEP_006	Sent slice 304, last slice size 5.634MB	0	0.0	0.000
PostTrigger	Mbr: 3, receiving: 2, analyzing: 0	0	0.0	0.000
TSP_000	last slice: 352, to: 14.38 - 20.78 MHz, rate: 6.028 - 0.087 x	0	0.0	0.000
TSP_001	TSP_001(data01)	0	0.0	0.000
TSP_002	TSP_002(data02)	0	0.0	0.000
TSP_003	TSP_003(data03)	0	0.0	0.000
TSP_004	TSP_004(data04)	0	0.0	0.000
TSP_005	TSP_005(data05)	0	0.0	0.000

Acquisition sequences are managed by Maximum Integrated Data Acquisition System (MIDAS)

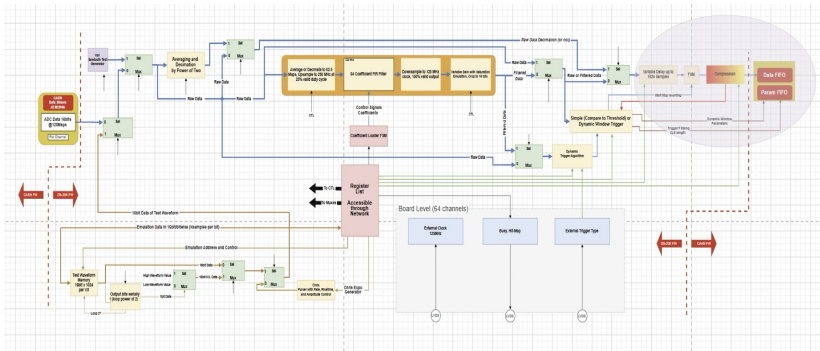
Possible challenge: VX2745 BUSY logic

- readout: 16 bits per 8 ns
- transmission to the sorting buffer is 8 times faster
- Busy->Pause Run->Resume run cycle when the buffer is full

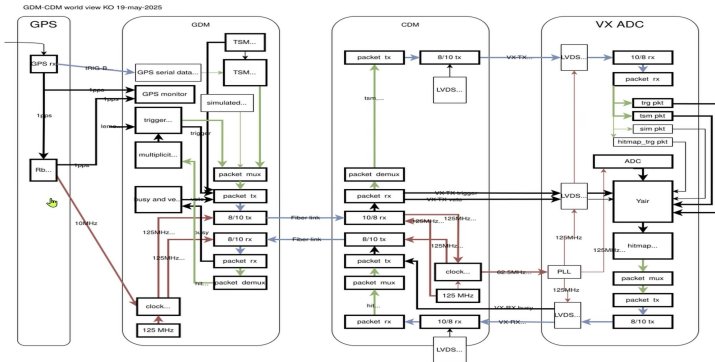


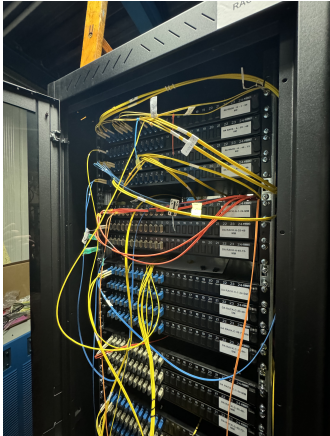
- Compression in the digitizer helps with the potential busy issue
- Lossless compression implemented in VHDL by Warsaw Tech. Uni.
 - compression factor 2.1 - 2.6
 - software implementation of compression and decompression tested on the FEP
 - 230 MB/s decompression data rate / core
 - ongoing: implementation in VX and FEP
- Quadrant setup will be shipped to LNGS this year
- Remaining HW (additional 3 racks) is beeing ordered

- DarkSide-20k experiment under construction in LNGS
- Developed DAQ system allows continuous acquisition from 2712 channels
- DAQ based on commercially available CAEN's VX2745 digitizers
- Multi-board synchronization of 48 modules provided by custom Data Manager boards
- Biggest direct Dark Matter experiment, commissioning expected in 2028

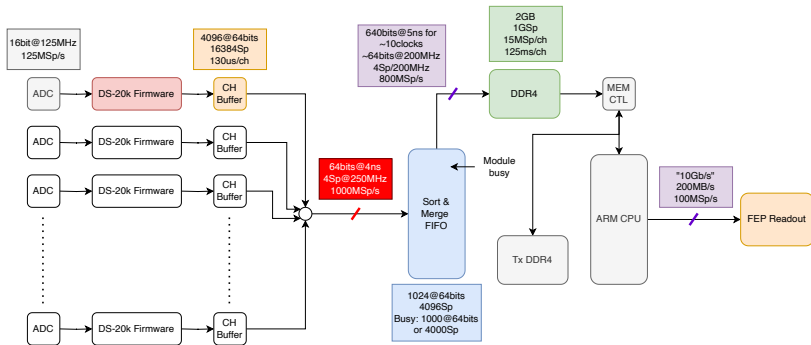


Backup

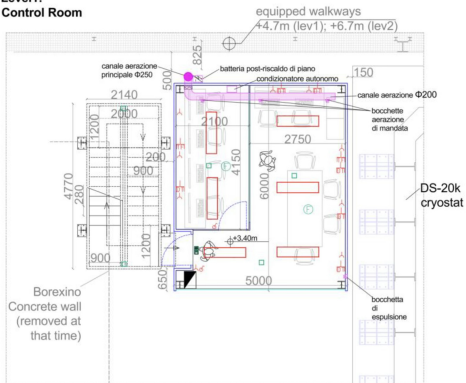




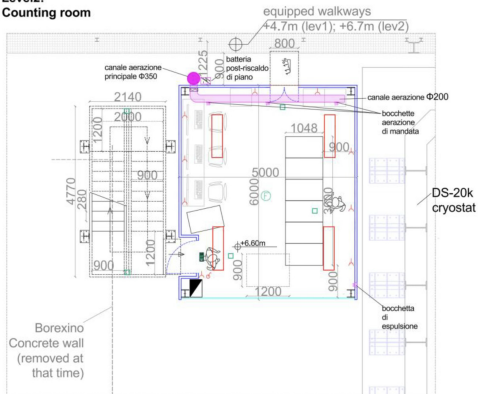
- signal measured it in GS1 LOC. TD. TEL room
- about 100 m from Hall C



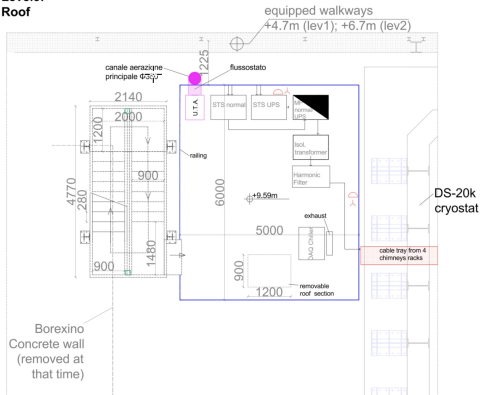
Level1: Control Room



Level2: Counting room



Level3: Roof



DarkSide Wiki page

- system description
- instructions

Configuration

The table below shows the total number of active channels for the overall detector: 2112 channels for the two detection planes, 480 channels for the Inner Veto within the LAr volume, and 128 Outer Veto in the Atmospheric Liquid Argon (ALA) surrounding vessel volume. Each Photo-Detector Unit (PDU) handles 4 detection channels, also called Photo-Detector Module or PDM, each corresponding to the analogism of the signals from 4 individual SPW lines, each composed of 2x1x1 and 5SPW sensors.

Parameter	Count
Total number of channels	2720
Number of TPC channels	2112
Number of Inner Veto channels	480
Number of Outer Veto channels	128
Total number of PDUs	680
Number of TPC PDUs	528
Number of Inner Veto PDUs	120
Number of Outer Veto PDUs	32

The channel count is distributed in four distinct locations on the top of the detector (Chimney). The channel composition at the chimney is shown as follows:

	Channels	#PDU (4 channels per PDU)	#POU TPC+Veto per DS-20k	#POU TPC+Veto per Chimney (4)	#POU TPC+Veto per Flange (4)	#POU TPC+Veto per interface (2)
TPC	2112	528	648	162	41	14
Channels						
Inner Veto	480	120				
Channels						
Outer Veto	128	32				
Total	2720	680				

2112 + 480 + 128 = 2720 channels

$12_{VX} * 64ch * 4 chimneys = 3072 channels$

$12_{VX} * 4 chimneys = 48_{VX} (1uV + 2uV + 9TPC)$

- additional information will be accessible from MIDAS page

Overall status: all good

After power up of DM boards, if the PDS completion - do in order: for GDM, CDM1, CDM2, ... press "reset mg" of each board, then press "armreset mg".

GDM commands

GDM mg enable trigger disable trigger reset mg armreset mg G.G FORCE_HOLD on G.G FORCE_HOLD off G.G INT

CDM commands

CDM100 GDM mg enable trigger disable trigger reset mg armreset mg G.G FORCE_HOLD on G.G FORCE_HOLD off G.G INT
 CDM101 GDM mg enable trigger disable trigger reset mg armreset mg G.G FORCE_HOLD on G.G FORCE_HOLD off G.G INT

Triggers generated

Host	TRG	Busy	HITMAP_TRG	heavy TSM
GDM	7413540	381258	156870	3355 5224
CDM0	0	0	0	0
CDM1	0	0	0	0

Triggers passed to VX

Host	Packet TRG	Packet HITMAP_TRG	TSM LVDS	TRG LVDS	TSM LVDS veto
GDM	0	0	0	7432048	5224 0
CDM0	7435844	156677	5224	5	0 753185
CDM1	7435844	156677	5224	5	0 753185

Clock status

Host G.G good Clock chip status

Host	TRG	L05_W0	00F_W0	IN1	IN_SEL	RGSTRL	IN_SEL_1	20W
GDM	7413540	381258	156870	3355 5224	0	0	0	0
CDM0	7435844	156677	5224	5	0	0	0	0
CDM1	7435844	156677	5224	5	0	0	0	0

QSPF link status

Host	OK	Badlink ports	QSPF link status	QSPF link status
GDM	7413540	381258	156870	3355 5224
CDM0	7435844	156677	5224	5
CDM1	7435844	156677	5224	5