Development of Silicon Interposer

(An Ultra-Low-Radioactivity Solution for the SiPM Photo-detector)

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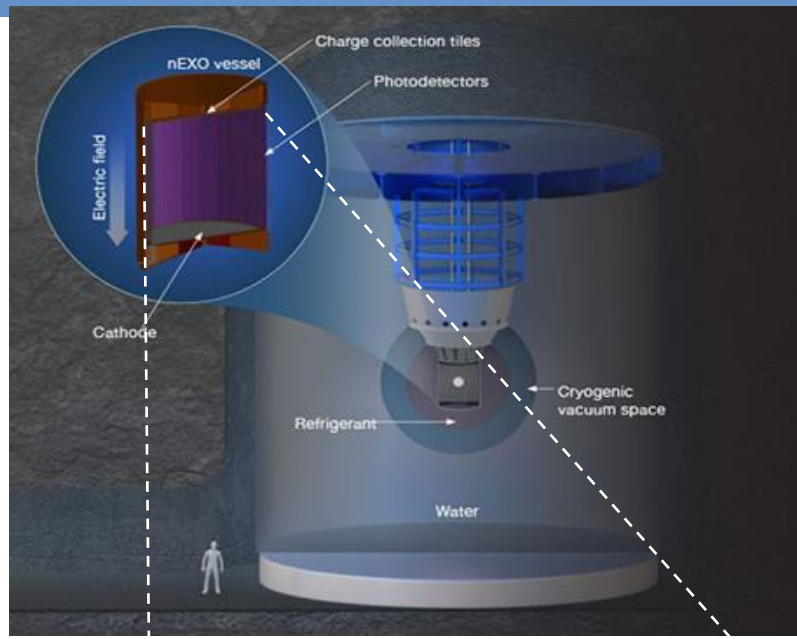
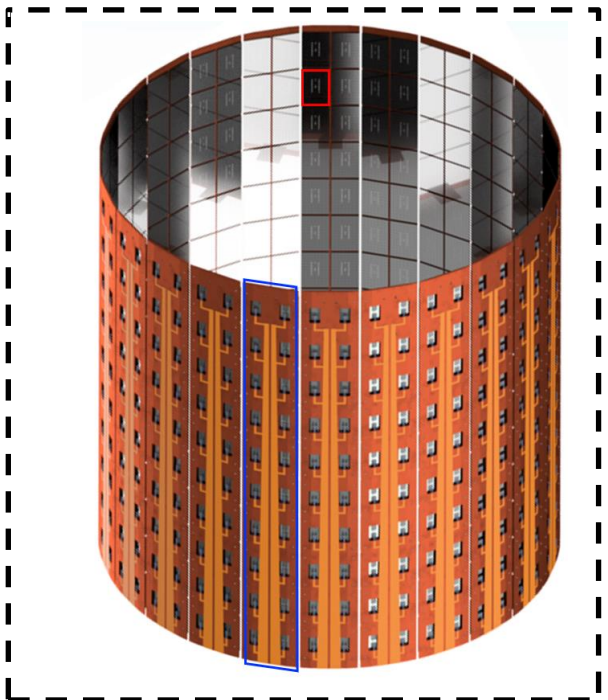
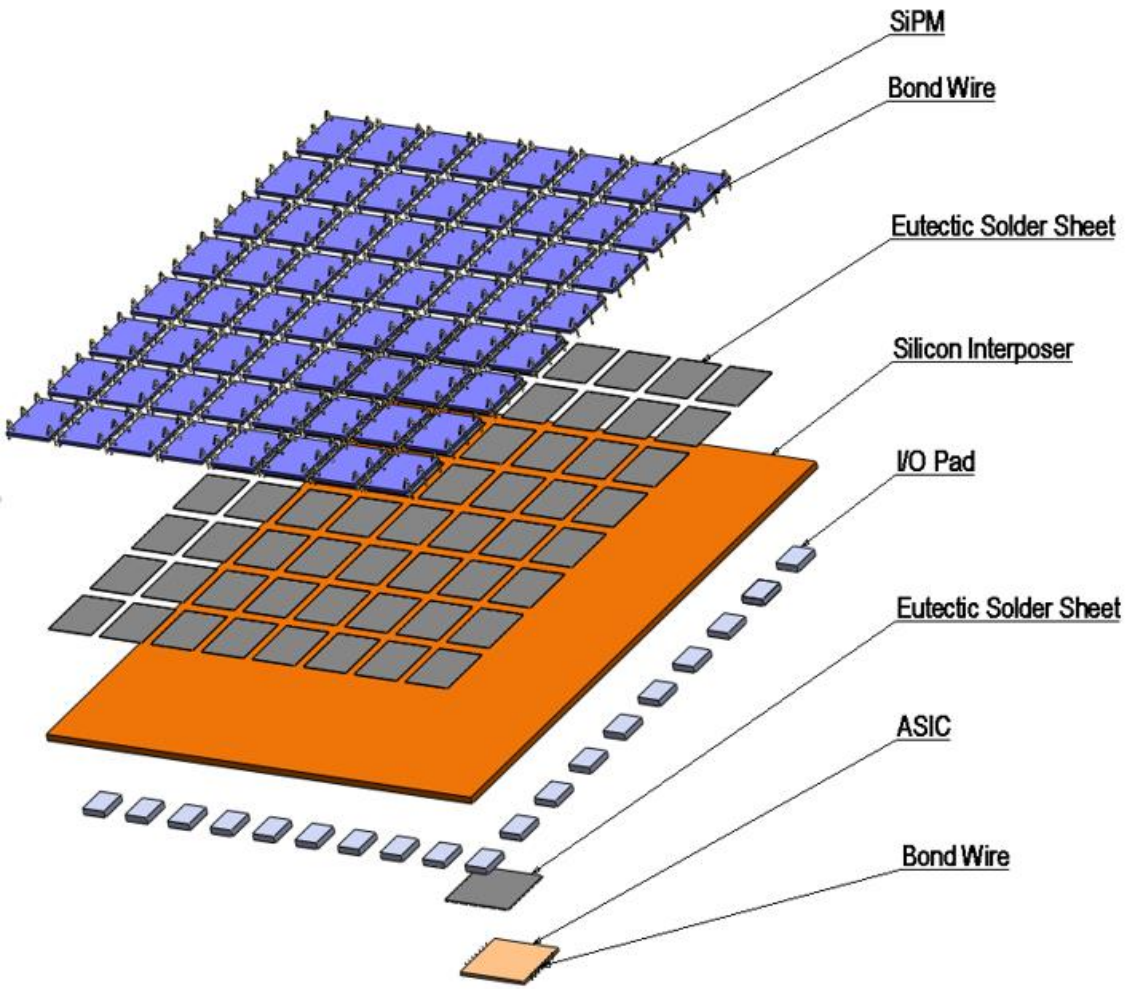
Motivation

- The noble liquid detector is quite powerful for dark matter and 0νββ searches
- It is a must to build a detector with ultra-low radioactivity background
- Interposer development is driven by the requirements of the nEXO experiment
  - Building an ultra-low radioactivity background photodetector with ~4.6 m^2 VUV sensitive SiPMs
- Two technical approaches
  - Silicon-based interposer (IHEP/IME, Sherbrooke-TRIUMF-IZM)
  - Quartz-based interposer (BNL)





A concept of low-background photodetector



- ❄ **Using SiPMs as photosensor**
  - ➢ **Low background SiPMs available**
- ❄ **Using ASIC chips for readout**
  - ➢ **high level of integration**
  - ➢ **Low background achievable**
- ❄ **Interposer with good purity (challenging)**
  - ➢ **Supporting SiPMs → enough mechanical strength (thickness)**
  - ➢ **Connecting SiPMs and ASIC → multiple RDLs with vias**
  - ➢ **Low temperature → good CTE matching with SiPMs**

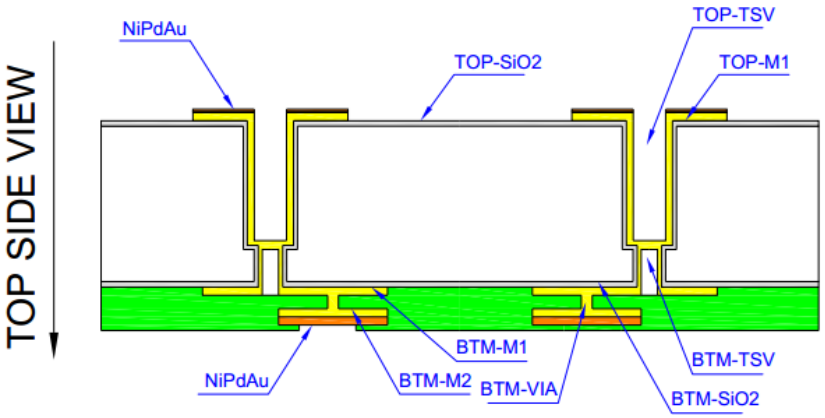
Typical Requirements of Interposer

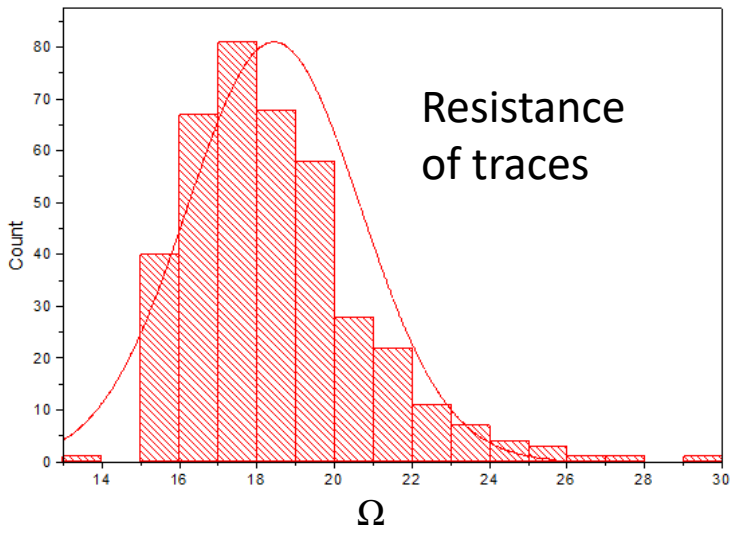
- **Requirements from nEXO**
  - **Resistance (traces + TSVs) < 2 Ω → reduce input impedance**
  - **Insulation among channels > 1 TΩ → good SPE resolution**
  - **Thickness > 300 um → enough mechanical strength**
  - **Size: 10 cm × 10 cm → easier assembly and less material**
  - **Number of RDLs ≥ 3 → good shielding**

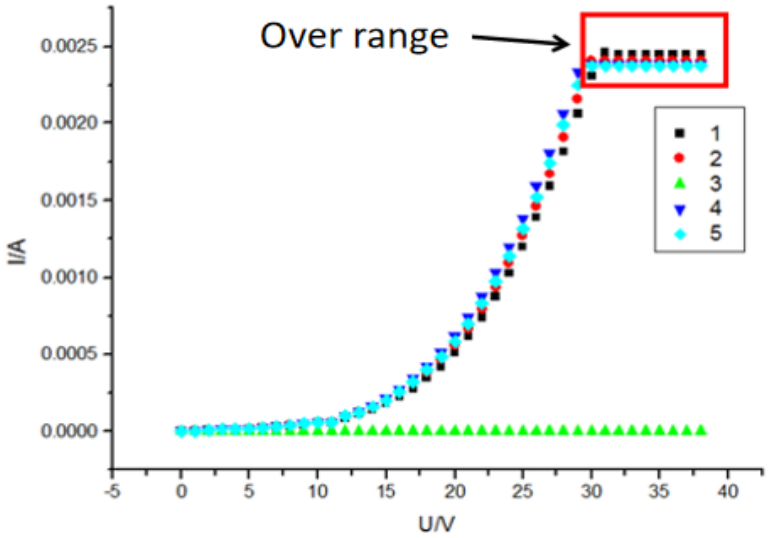
- **It is quite challenging to make large silicon interposer with TSVs**
  - **2017, IHEP/IME starts to develop silicon interposer**
  - **2018, Sherbrooke + IZM starts to work on silicon interposer**
  - **A few years later, BNL focuses on quartz-based interposer**

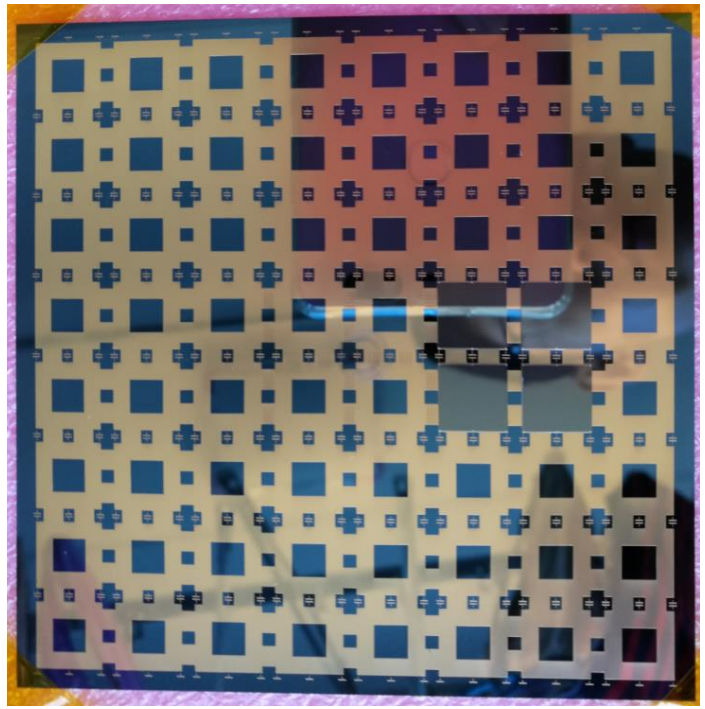
Silicon Interposer prototype in 2018

- The 1st silicon interposer was made in 2018
  - Size: 10 cm x 10 cm, thickness: 320 um
  - 3 RDLs connected with TSVs
  - Number of channels: 64
- Two major issues:
  - Large trace resistance: 14~30 Ω
  - Poor insulation: tens of MΩ



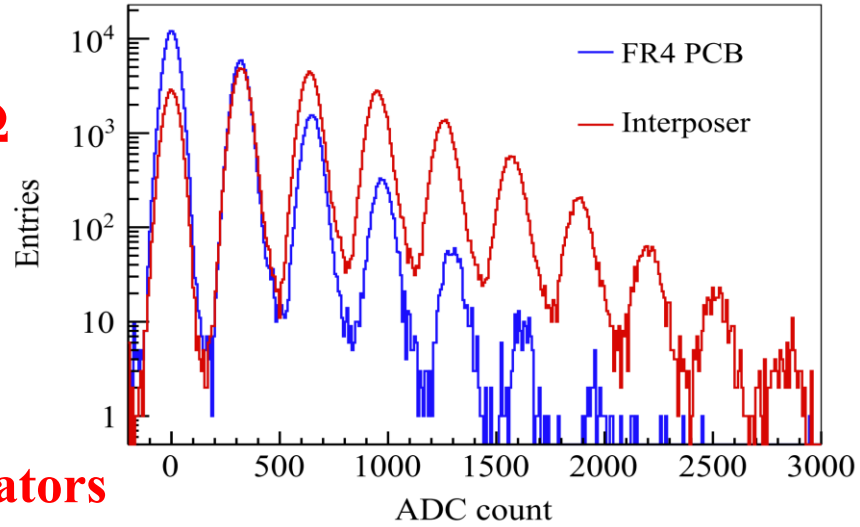






Silicon Interposer in 2021 (Run-I)

- The same size with the prototype
- Trace design was optimized, which reduces the resistance < 2 Ω
- Better insulation performance due to improved manufacturing technique
  - Tens of MΩ → better than 100 G Ω
- Very promising radiopurity!!!
  - < 1-2 ppt (both 238U and 232Th) measured by our PNNL collaborators
- The first SPE signals from SiPMs mounted on one selected channel



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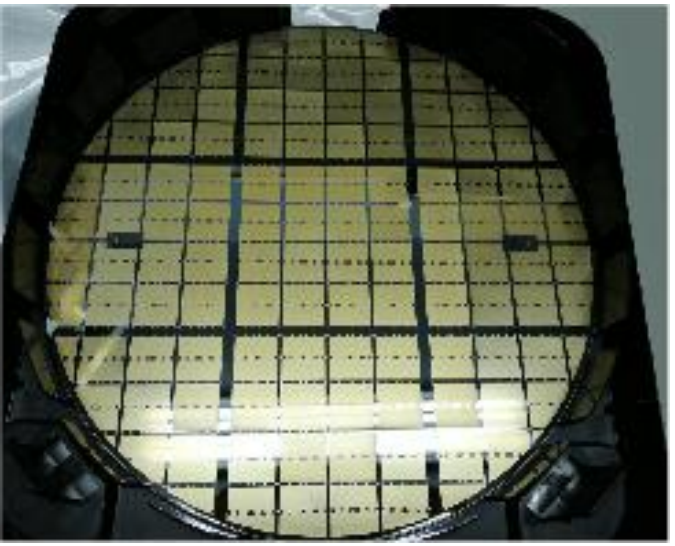


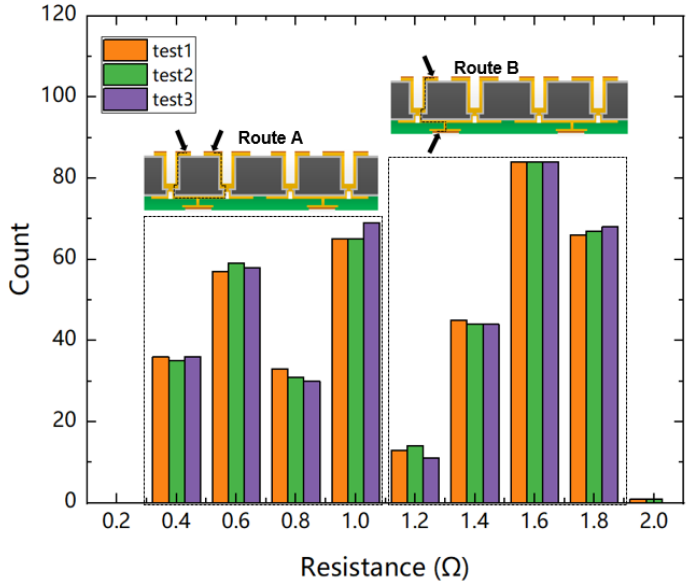
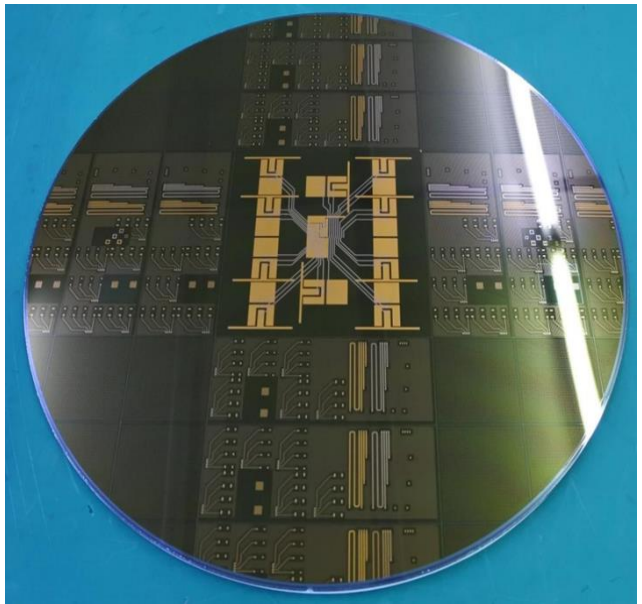


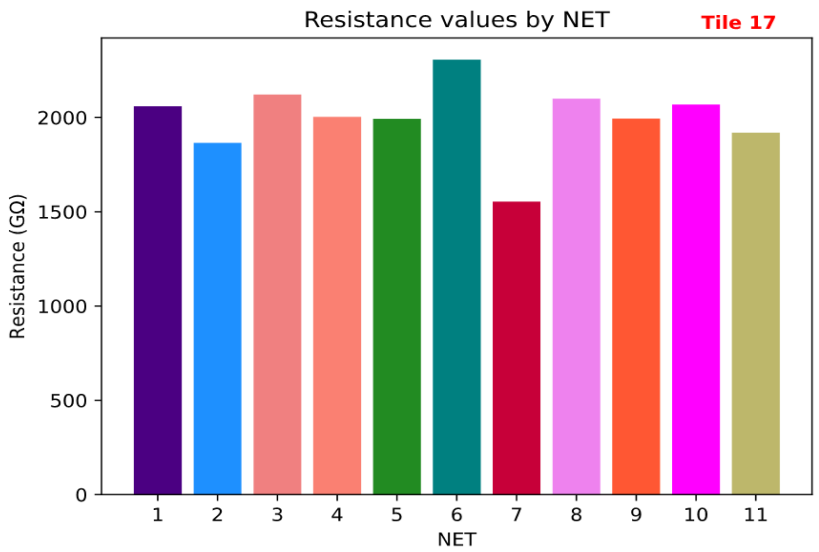
TABLE II
INSULATION RESISTANCES OF DIFFERENT BLOCKS ON THE INTERPOSER.

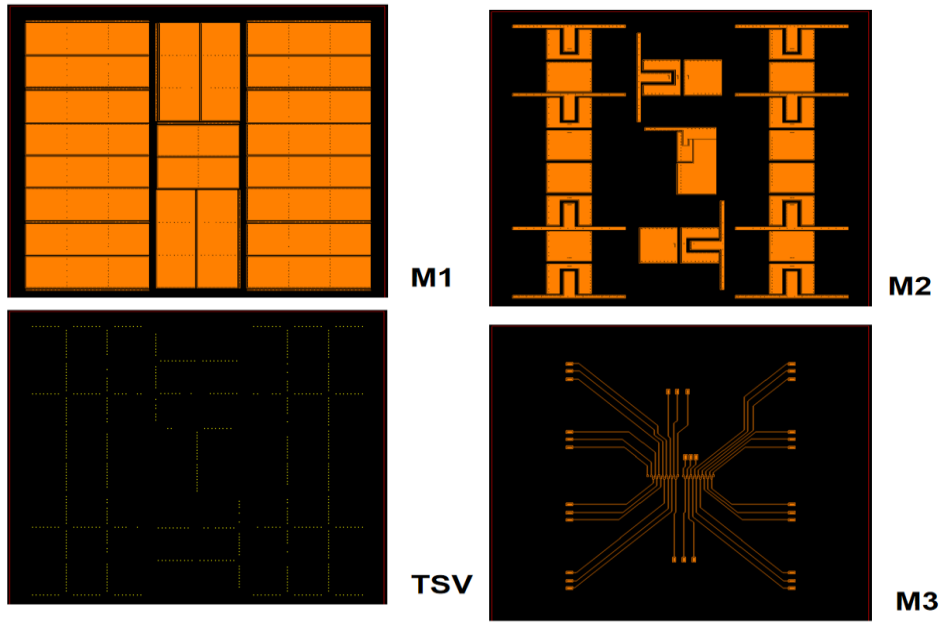
Block ID	R (GΩ)	Block ID	R (GΩ)
1	861	9	2500
2	125	10	475
3	644	11	1670
4	965	12	2260
5	161	13	482
6	924	14	647
7	26500	15	35900
8	537	16	548

Silicon Interposer in 2023 (Run-II)

- It was designed to mount SiPMs manufactured by FBK
  - 11 channels with 3p2s SiPM configuration
- The trace design keeps same with that in Run-I, trace R < 2 Ω
- > 1 TΩ insulation performance achieved on the overall interposer
- FBK SiPMs fully assembled on the interposer
  - No mechanical issues during a few temperature cycling (up to 0.4 ℃/min)

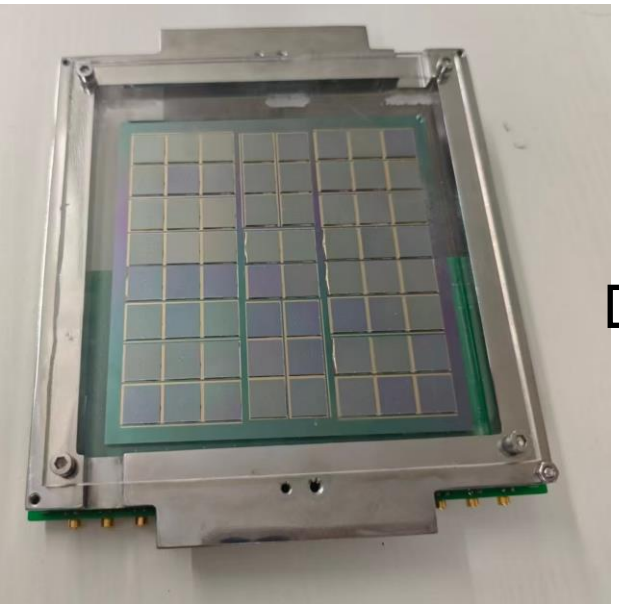


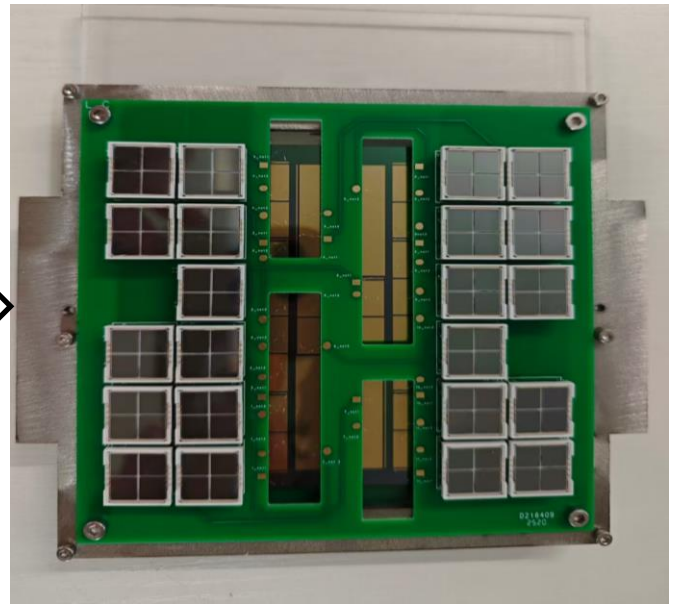


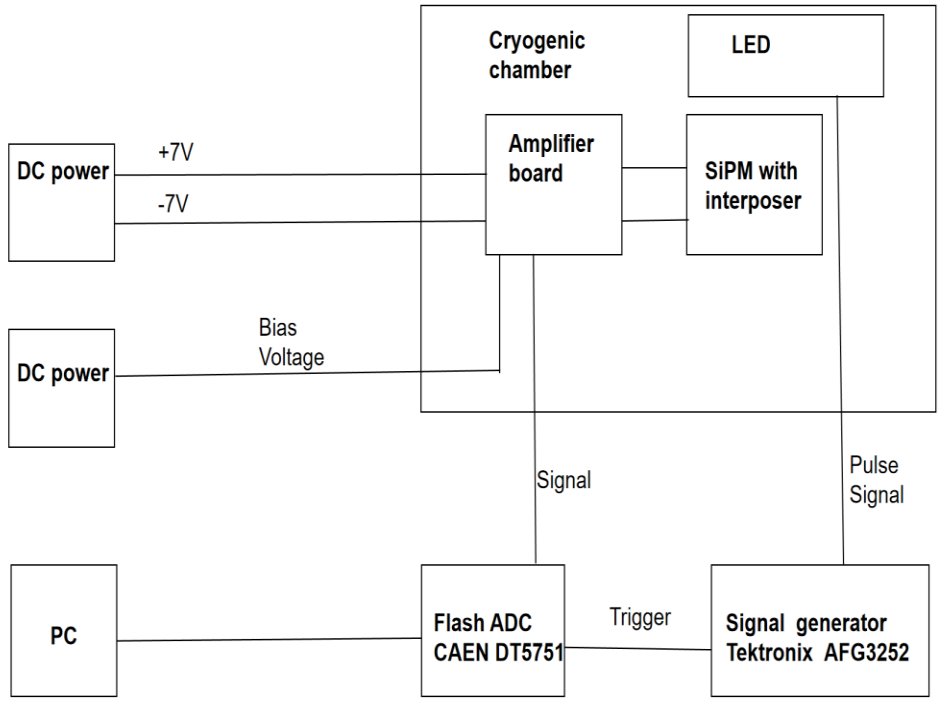


Performance of Integrated Interposer

- All channels work well at room temperature, but hard to see SPE signals at low temperatures
  - The working voltage range is significantly reduced for FBK SiPMs
- Mouting HPK SiPMs on the interposer through an adapter board
  - VUV4 SiPMs, two arrays in one channel
- A custom made pre-amplifier board used to readout SiPMs and digitized by DT5751 from CAEN
- All tests were performed in a cryogenic chamber which can control the temperature from room temperature to LXe temperature

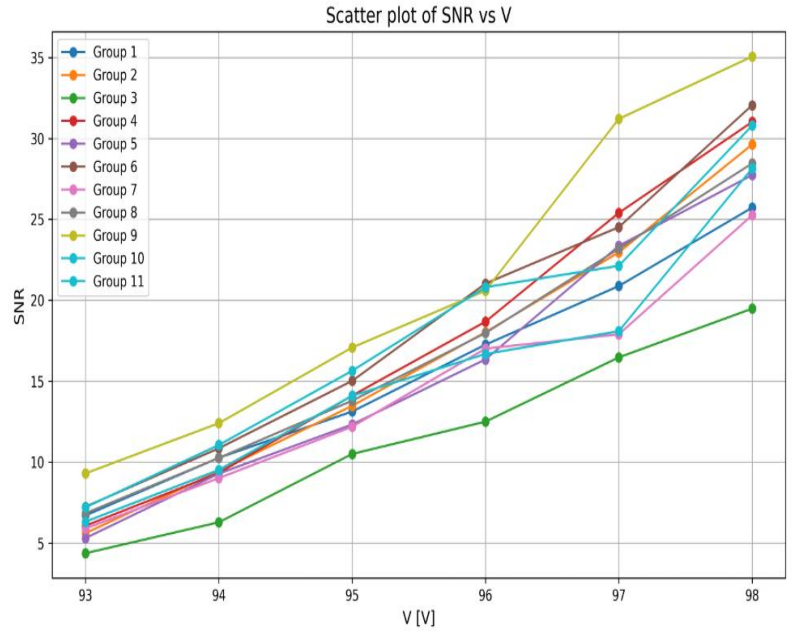


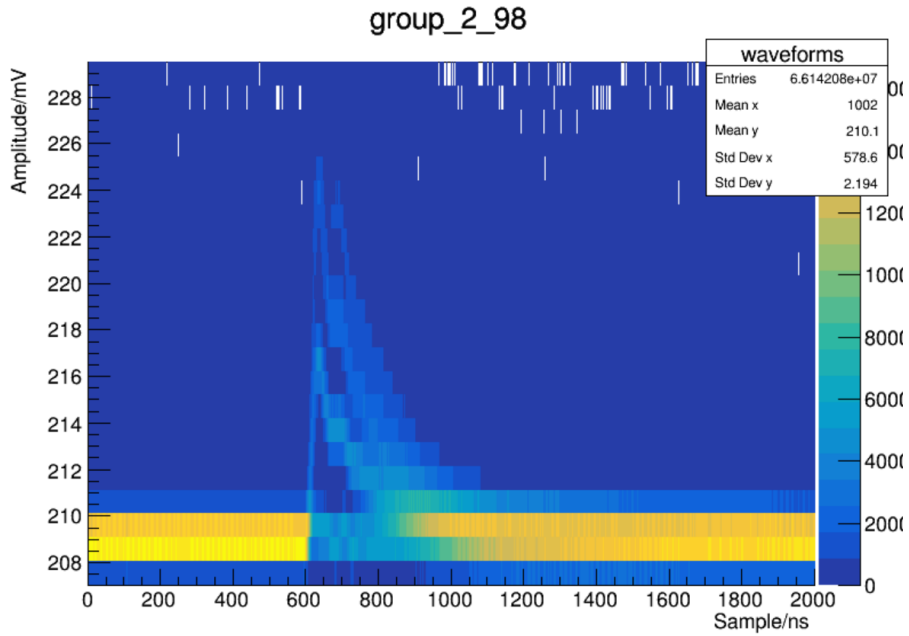


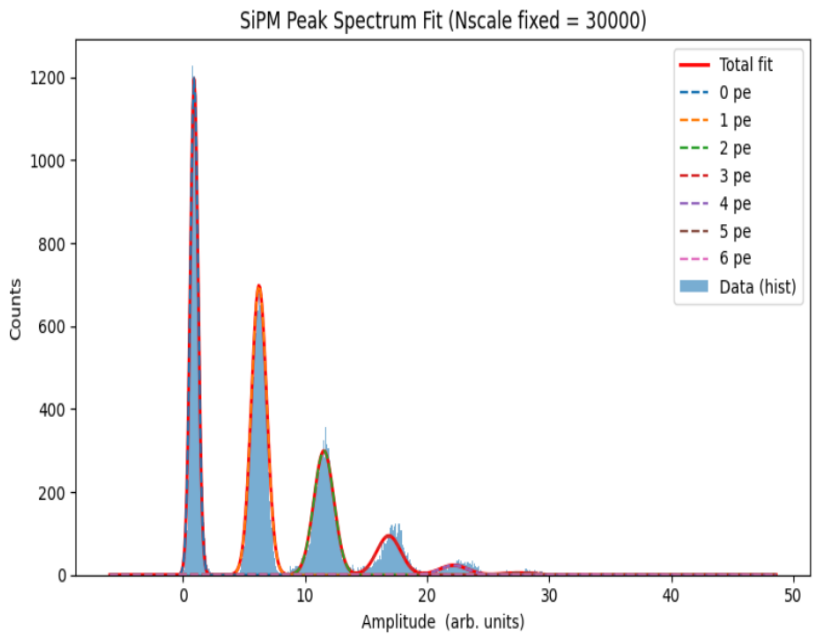


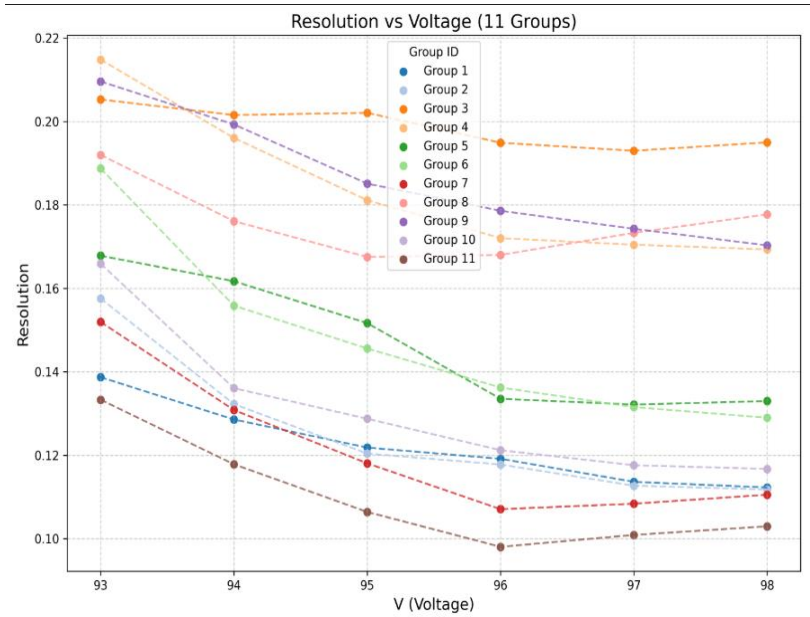
Results from Run-II Interposer

- ❄ **All channels work normally at 4 different temperatures**
  - ➢ **-20 ℃, -60 ℃, -100 ℃ and -120 ℃**
- ❄ **The clear SPE signals can be observed for all channels at low temperatures**
- ❄ **The SNR and SPE resolution are presented as a function of the bias voltage**
- ❄ **A fully successful demonstration of a silicon interposer-based photodetector module was achieved!**



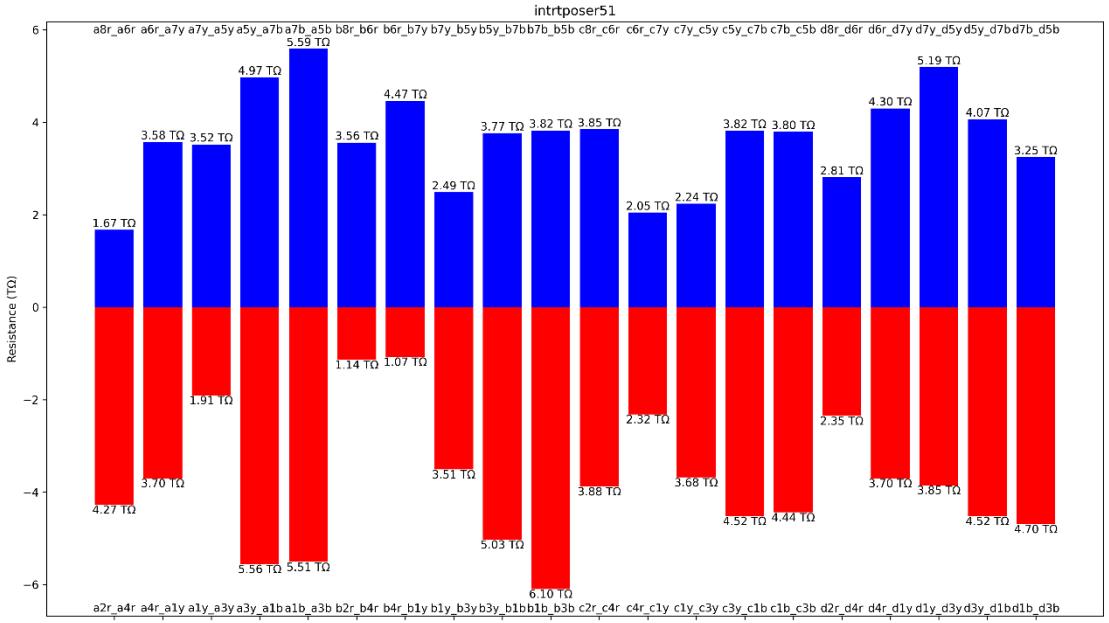


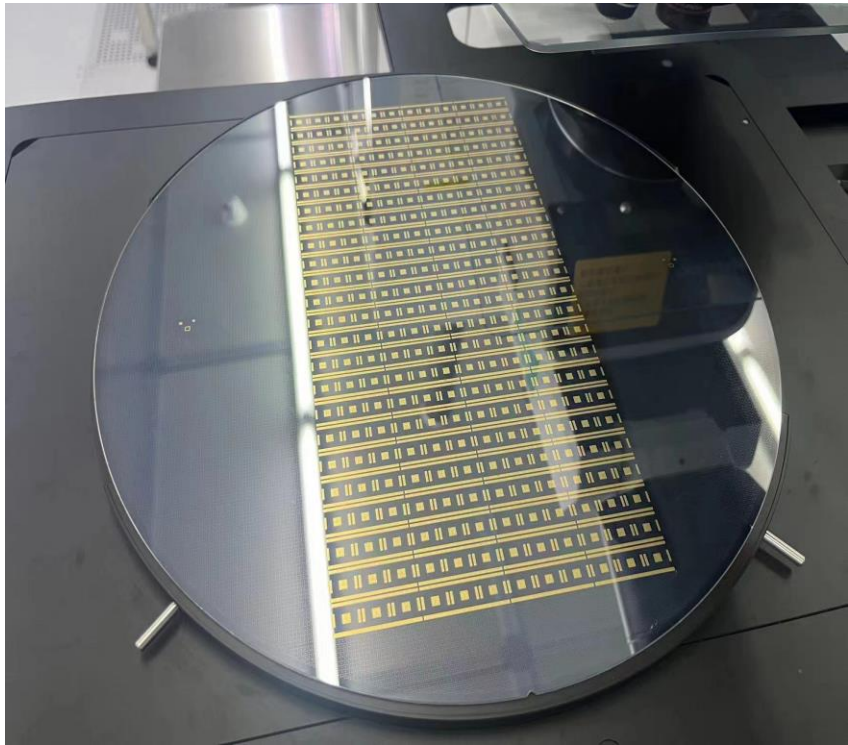




Silicon Interposer from Run-III in 2023

- ❄ The size was adjusted to nEXO's final design, 123.8 mm × 82.6 mm
- ❄ Designed for mounting HPK SiPMs
- ❄ The same manufacture process with Run-II
- ❄ Good insulation performance (> 1 TΩ) and low trace resistance (< 2 Ω)
- ❄ Waiting for mounting HPK SiPMs and testing
- ❄ This will be the last run of interposer manufacture during the R&D phase





Summary

- **Building an ultra-low background photodetector is a must for many rare events search projects**
  - **Developing interposer is a key and quite challenging**
- **The manufacture process and technique have been established for making a large size silicon-based interposer with ultra-low background**
- **The performance of the silicon interposer integrated with SiPMs looks quite promising**
- **We hope this technique can be used in the coming low background projects soon**
- **Welcome for discussions**